TXB0106-Q1 6-Bit Bidirectional Voltage-Level Translator With Auto-Direction Sensing and ±10kV ESD Protection

1 Features

- Qualified for Automotive Applications
- 1.2V to 3.6V on A Port and 1.65 to 5.5V on B Port ($V_{CCA} \leq V_{CCB}$)
- V_{CC} Isolation Feature – If Either V_{CC} Input Is at GND, All Outputs Are in the High-Impedance State
- OE Input Circuit Referenced to V_{CCA}
- I_{off} Supports Partial-Power-Down Mode Operation
- ESD Protection Exceeds AEC-Q100
  - A Port
    - 2000V Human-Body Model
    - 1500V Charged-Device Model
  - B Port
    - ±10kV Human-Body Model
    - 1500V Charged-Device Model

2 Applications

- Heating and Cooling
- Telematics
- Radar

3 Description

This 6-bit noninverting translator uses two separate configurable power-supply rails. The A port is designed to track V_{CCA}. V_{CCA} accepts any supply voltage from 1.2V to 3.6V. The B port is designed to track V_{CCB}. V_{CCB} accepts any supply voltage from 1.65V to 5.5V. This allows for universal low-voltage bidirectional translation between any of the 1.2V, 1.5V, 1.8V, 2.5V, 3.3V, and 5V voltage nodes. V_{CCA} should not exceed V_{CCB}.

When the output-enable (OE) input is low, all outputs are placed in the high-impedance state.

The TXB0106-Q1 device is designed so that the OE input circuit is supplied by V_{CCA}.

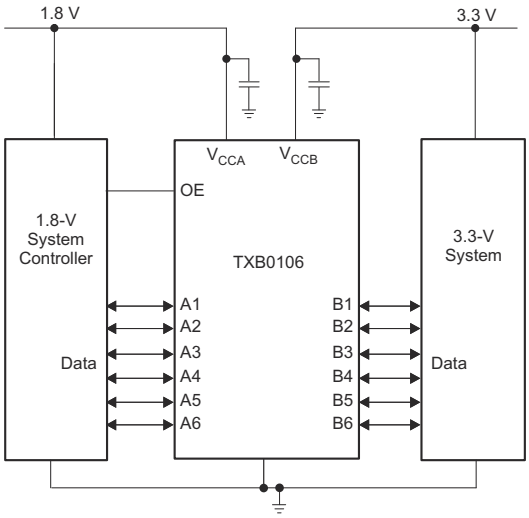
This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

Package Information

PART NUMBER	PACKAGE (1)	BODY SIZE (NOM)
TXB0106-Q1	TSSOP (16)	5.00mm × 4.40mm
TXB0106-Q1	WQFN (16)	3.50mm x 2.50mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Typical Operating Circuit

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4 Pin Configuration and Functions

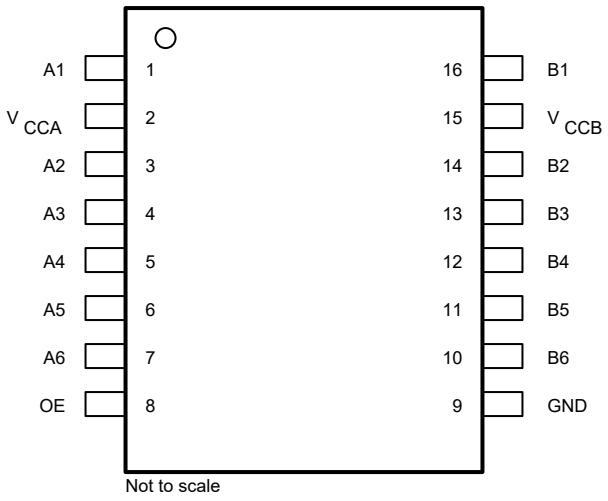


Figure 4-1. PW Package 16-Pin TSSOP Top View

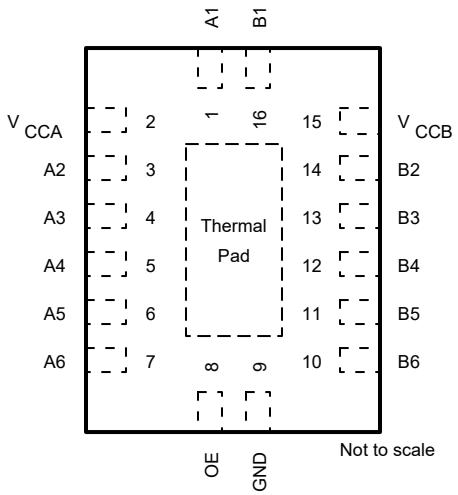


Figure 4-2. BQB Package 16-Pin WCSP Top View

Pin Functions

NAME	NO.	I/O	DESCRIPTION
A1	1	I/O	Input/output 1. Referenced to V_{CCA}.
A2	3	I/O	Input/output 2. Referenced to V_{CCA}.
A3	4	I/O	Input/output 3. Referenced to V_{CCA}.
A4	5	I/O	Input/output 4. Referenced to V_{CCA}.
A5	6	I/O	Input/output 5. Referenced to V_{CCA}.
A6	7	I/O	Input/output 6. Referenced to V_{CCA}.
B1	16	I/O	Input/output 1. Referenced to V_{CCB}.
B2	14	I/O	Input/output 2. Referenced to V_{CCB}.
B3	13	I/O	Input/output 3. Referenced to V_{CCB}.
B4	12	I/O	Input/output 4. Referenced to V_{CCB}.
B5	11	I/O	Input/output 5. Referenced to V_{CCB}.
B6	10	I/O	Input/output 6. Referenced to V_{CCB}.
GND	9	—	Ground
OE	8	I	Output enable. Pull OE low to place all outputs in the high-impedance state. Referenced to V_{CCA}.
V_{CCA}	2	I	A-port supply voltage. $1.2V \le V_{CCA} \le 3.6V$, $V_{CCA} \le V_{CCB}$.
V_{CCB}	15	I	B-port supply voltage. $1.65V \le V_{CCB} \le 5.5V$.

5 Specifications

5.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CCA}	Supply voltage range		–0.5	4.6	V
V_{CCB}	Supply voltage range		–0.5	6.5	V
V_I	Input voltage range (1)		–0.5	6.5	V
V_O	Voltage range applied to any output in the high-impedance or power-off state(1)		–0.5	6.5	V
	Voltage range applied to any output in the high or low state(1) (2)	A inputs	–0.5	V_{CCA} + 0.5	V
		B inputs	–0.5	V_{CCB} + 0.5	
I_{IK}	Input clamp current	V_I < 0		–50	mA
I_{OK}	Output clamp current	V_O < 0		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CCA}, V_{CCB}, or GND			±100	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature range		–65	150	°C

(1) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(2) The values of V_{CCA} and V_{CCB} are provided in the *Recommended Operating Conditions* table.

5.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)		±2000	V
		Charged-device model (CDM), per AEC Q100-011	All pins	±1500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

			V_{CCA}	V_{CCB}	MIN	MAX	UNIT
V_{CCA}	Supply voltage				1.2	3.6	V
V_{CCB}					1.65	5.5	
V_{IH}	High-level input voltage	Data inputs	1.2V to 3.6V	1.65V to 5.5V	V_{CCI}× 0.65(1)	V_{CCI}	V
		OE			V_{CCA}× 0.65	5.5	
V_{IL}	Low-level input voltage	Data inputs	1.2V to 5.5V	1.65V to 5.5V	0	V_{CCI}× 0.35(1)	V
		OE	1.2V to 3.6V		0	V_{CCA}× 0.35	
Δt/Δv	Input transition rise or fall rate	A-port inputs	1.2V to 3.6V	1.65V to 5.5V		40	ns/V
		B-port inputs	1.2V to 3.6V	1.65V to 3.6V		40	
				4.5V to 5.5V		30	
T_A	Operating ambient temperature (TXB0106I)				–40	85	°C
	Operating ambient temperature (TXB0106)				-40	125	°C

(1) V_{CCI} is the supply voltage associated with the input port.

5.4 Thermal Information

THERMAL METRIC (1)		TXB0106-Q1		UNIT
		PW (TSSOP)	BQB (WQFN)	
		16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	107.5	63.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	42.3	64.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	52.6	33.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	4.2	2.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	52	33.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	-	16.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application note.

5.5 Electrical Characteristics (TXB0106I)

over recommended operating ambient temperature range (unless otherwise noted)(1) (2)

PARAMETER			TEST CONDITIONS	V_{CCA}	V_{CCB}	T_A = 25°C			–40°C to 85°C		UNIT
						MIN	TYP	MAX	MIN	MAX	
V_{OHA}		Output high voltage, A port	I_{OH} = –20µA	1.2V			1.1				V
				1.4V to 3.6V					V_{CCA} – 0.4		
V_{OLA}		Output low voltage, A port	I_{OL} = 20µA	1.2V			0.9				V
				1.4V to 3.6V						0.4	
V_{OHB}		Output high voltage, B port	I_{OH} = –20µA		1.65V to 5.5V				V_{CCB} – 0.4		V
V_{OLB}		Output low voltage, B port	I_{OL} = 20µA		1.65V to 5.5V					0.4	V
$I_{lkg(I)}$	OE	Input leakage current		1.2V to 3.6V	1.65V to 5.5V			±1		±2	µA
$I_{lkg(off)}$	A port	Off-state leakage current		0V	0V to 5.5V			±1		±2	µA
	B port			0V to 3.6V	0V			±1		±2	
I_{OZ}	A or B port	High-impedance output current	OE = GND	1.2V to 3.6V	1.65V to 5.5V			±1		±2	µA
I_{CCA}		V_{CCA} supply current	V_I = V_{CCI} or GND, I_O = 0	1.2V	1.65V to 5.5V		0.06				µA
				1.4V to 3.6V						9	
				3.6V	0V					2	
				0V	5.5V					2	
I_{CCB}		V_{CCB} supply current	V_I = V_{CCI} or GND, I_O = 0	1.2V	1.65V to 5.5V		3.4				µA
				1.4V to 3.6V						9	
				3.6V	0V					–2	
				0V	5.5V					2	
I_{CCA} + I_{CCB}		Combined supply current	V_I = V_{CCI} or GND, I_O = 0	1.2V	1.65V to 5.5V		3.5				µA
				1.4V to 3.6V						18	
I_{CCZA}		High-impedance V_{CCA} supply current	V_I = V_{CCI} or GND, I_O = 0, OE = GND	1.2V	1.65V to 5.5V		0.05				µA
				1.4V to 3.6V						5	
I_{CCZB}		High-impedance V_{CCB} supply current	V_I = V_{CCI} or GND, I_O = 0, OE = GND	1.2V	1.65V to 5.5V		3.3				µA
				1.4V to 3.6V						5	

over recommended operating ambient temperature range (unless otherwise noted)(1) (2)

PARAMETER			TEST CONDITIONS	V_{CCA}	V_{CCB}	T_A = 25°C			–40°C to 85°C		UNIT
						MIN	TYP	MAX	MIN	MAX	
C_I	OE	Input capacitance		1.2V to 3.6V	1.65V to 5.5V		5			5.5	pF
C_{io}	A port			1.2V to 3.6V	1.65V to 5.5V		5			6.5	pF
	B port						8			10	

(1) V_{CCI} is the supply voltage associated with the input port.
(2) V_{CCO} is the supply voltage associated with the output port.

5.6 Electrical Characteristics (TXB0106)

over recommended operating ambient temperature range (unless otherwise noted)(1) (2)

PARAMETER			TEST CONDITIONS	V_{CCA}	V_{CCB}	T_A = 25°C			–40°C to 125°C		UNIT
						MIN	TYP	MAX	MIN	MAX	
V_{OHA}		Output high voltage, A port	I_{OH} = –20µA	1.2V			1.1				V
				1.4V to 3.6V					V_{CCA} – 0.4		
V_{OLA}		Output low voltage, A port	I_{OL} = 20µA	1.2V			0.9				V
				1.4V to 3.6V						0.4	
V_{OHB}		Output high voltage, B port	I_{OH} = –20µA		1.65V to 5.5V				V_{CCB} – 0.4		V
V_{OLB}		Output low voltage, B port	I_{OL} = 20µA		1.65V to 5.5V					0.4	V
$I_{lkg(I)}$	OE	Input leakage current		1.2V to 3.6V	1.65V to 5.5V			±1		±2	µA
$I_{lkg(off)}$	A port	Off-state leakage current		0V	0V to 5.5V			±1		±2	µA
	B port			0V to 3.6V	0V			±1		±2	
I_{OZ}	A or B port	High-impedance output current	OE = GND	1.2V to 3.6V	1.65V to 5.5V			±1		±2	µA
I_{CCA}		V_{CCA} supply current	V_I = V_{CCI} or GND, I_O = 0	1.2V	1.65V to 5.5V		0.4				µA
				1.4V to 3.6V						10	
				3.6V	0V					7.5	
				0V	5.5V					-2	
I_{CCB}		V_{CCB} supply current	V_I = V_{CCI} or GND, I_O = 0	1.2V	1.65V to 5.5V		3.4				µA
				1.4V to 3.6V						31.5	
				3.6V	0V					–2	
				0V	5.5V					30.5	
I_{CCA} + I_{CCB}		Combined supply current	V_I = V_{CCI} or GND, I_O = 0	1.2V	1.65V to 5.5V		3.5				µA
				1.4V to 3.6V						38.5	
I_{CCZA}		High-impedance V_{CCA} supply current	V_I = V_{CCI} or GND, I_O = 0, OE = GND	1.2V	1.65V to 5.5V		0.4				µA
				1.4V to 3.6V						7	
I_{CCZB}		High-impedance V_{CCB} supply current	V_I = V_{CCI} or GND, I_O = 0, OE = GND	1.2V	1.65V to 5.5V		3.3				µA
				1.4V to 3.6V						31	
C_I	OE	Input capacitance		1.2V to 3.6V	1.65V to 5.5V		5			6.5	pF

over recommended operating ambient temperature range (unless otherwise noted)(1) (2)

PARAMETER			TEST CONDITIONS	V_{CCA}	V_{CCB}	T_A = 25°C			–40°C to 125°C		UNIT
						MIN	TYP	MAX	MIN	MAX	
C_{io}	A port			1.2V to 3.6V	1.65V to 5.5V		5			6.5	pF
	B port						8			13.5	

(1) V_{CCI} is the supply voltage associated with the input port.
(2) V_{CCO} is the supply voltage associated with the output port.

5.7 Timing Requirements – V_{CCA} = 1.2V, T_A = 25°C

			V_{CCB} = 1.8V	V_{CCB} = 2.5V	V_{CCB} = 3.3V	V_{CCB} = 5V	UNIT
			TYP	TYP	TYP	TYP	
	Data rate		20	20	20	20	Mbps
t_w	Pulse duration	Data inputs	50	50	50	50	ns

5.8 Timing Requirements – V_{CCA} = 1.5V ± 0.1V

over recommended operating ambient temperature range (unless otherwise noted)

			V_{CCB} = 1.8V ± 0.15V		V_{CCB} = 2.5V ± 0.2V		V_{CCB} = 3.3V ± 0.3V		V_{CCB} = 5V ± 0.5V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
	Data rate			50		50		50		50	Mbps
t_w	Pulse duration	Data inputs	20		20		20		20		ns

5.9 Timing Requirements – V_{CCA} = 1.8V ± 0.15V

over recommended operating ambient temperature range (unless otherwise noted)

			V_{CCB} = 1.8V ± 0.15V		V_{CCB} = 2.5V ± 0.2V		V_{CCB} = 3.3V ± 0.3V		V_{CCB} = 5V ± 0.5V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
	Data rate			52		60		60		60	Mbps
t_w	Pulse duration	Data inputs	19		17		17		17		ns

5.10 Timing Requirements – V_{CCA} = 2.5V ± 0.2V

over recommended operating ambient temperature range (unless otherwise noted)

			V_{CCB} = 2.5V ± 0.2V		V_{CCB} = 3.3V ± 0.3V		V_{CCB} = 5V ± 0.5V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
	Data rate			70		100		100	Mbps
t_w	Pulse duration	Data inputs	14		10		10		ns

5.11 Timing Requirements – V_{CCA} = 3.3V ± 0.3V

over recommended operating ambient temperature range (unless otherwise noted)

			V_{CCB} = 3.3V ± 0.3V		V_{CCB} = 5V ± 0.5V		UNIT
			MIN	MAX	MIN	MAX	
	Data rate			100		100	Mbps
t_w	Pulse duration	Data inputs	10		10		ns

5.12 Switching Characteristics –V_{CCA} = 1.2V, T_A = 25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.8V	V_{CCB} = 2.5V	V_{CCB} = 3.3V	V_{CCB} = 5V	UNIT
			TYP	TYP	TYP	TYP	
t_{pd}	A	B	9.5	7.9	7.6	8.5	ns
	B	A	9.2	8.8	8.4	8	
t_{en}	OE	A	1	1	1	1	µs
		B	1	1	1	1	
t_{dis} (1)	OE	A	20	17	17	18	ns
		B	20	16	15	15	
t_{rA}, t_{fA}	A-port rise and fall times		4.1	4.4	4.1	3.9	ns
t_{rB}, t_{fB}	B-port rise and fall times		5	5	5.1	5.1	ns
$t_{SK(O)}$	Channel-to-channel skew		2.4	1.7	1.9	7	ns
Max. data rate			20	20	20	20	Mbps

(1) Test procedure uses a 25MHz sine wave on the input.

5.13 Switching Characteristics – V_{CCA} = 1.5V ± 0.1V (TXB0106I)

over recommended operating ambient temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.8V ± 0.15V		V_{CCB} = 2.5V ± 0.2V		V_{CCB} = 3.3V ± 0.3V		V_{CCB} = 5V ± 0.5V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	B	1.4	13.5	1.2	10.5	1.1	10.5	0.8	10.1	ns
	B	A	0.9	15.2	0.7	13.8	0.4	13.8	0.3	13.7	
t_{en}	OE	A		1		1		1		1	µs
		B		1		1		1		1	
t_{dis} (1)	OE	A	6.6	33	6.4	25.3	6.1	23.1	5.9	24.6	ns
		B	6.6	35.6	5.8	25.6	5.5	22.1	5.6	20.6	
t_{rA}, t_{fA}	A-port rise and fall times		0.8	6.5	0.8	6.3	0.8	6.3	0.8	6.3	ns
t_{rB}, t_{fB}	B-port rise and fall times		1	7.3	0.7	4.9	0.7	4.6	0.6	4.6	ns
$t_{SK(O)}$	Channel-to-channel skew			2.6		1.9		1.6		1.3	ns
Max data rate			50		50		50		50		Mbps

5.14 Switching Characteristics – V_{CCA} = 1.5V ± 0.1V (TXB0106)

over recommended operating ambient temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.8V ± 0.15V		V_{CCB} = 2.5V ± 0.2V		V_{CCB} = 3.3V ± 0.3V		V_{CCB} = 5V ± 0.5V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	B	1.4	13.5	1.2	10.5	1.1	10.5	0.8	10.1	ns
	B	A	0.9	15.2	0.7	13.8	0.4	13.8	0.3	13.7	
t_{en}	OE	A		1		1		1		1	µs
		B		1		1		1		1	
t_{dis} (1)	OE	A	278	394	236	305	236	305	236	305	ns
		B	278	394	236	305	236	305	236	305	
t_{rA}, t_{fA}	A-port rise and fall times		0.8	6.5	0.8	6.3	0.8	6.3	0.8	6.3	ns
t_{rB}, t_{fB}	B-port rise and fall times		1	7.3	0.7	4.9	0.7	4.6	0.6	4.6	ns
$t_{SK(O)}$	Channel-to-channel skew			2.6		1.9		1.6		1.3	ns
Max data rate			50		50		50		50		Mbps

5.15 Switching Characteristics – V_{CCA} = 1.8V ± 0.15V (TXB0106I)

over recommended operating ambient temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.8V ± 0.15V		V_{CCB} = 2.5V ± 0.2V		V_{CCB} = 3.3V ± 0.3V		V_{CCB} = 5V ± 0.5V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	B	1.6	12	1.4	7.7	1.3	6.8	1.2	6.5	ns
	B	A	1.5	13.5	1.2	10	0.8	8.2	0.5	8	
t_{en}	OE	A		1		1		1		1	µs
		B		1		1		1		1	
t_{dis} (1)	OE	A	5.9	26.7	5.6	21.6	5.4	18.9	4.8	18.7	ns
		B	6.1	33.9	5.2	23.7	5	19.9	5	17.6	
t_{rA}, t_{fA}	A-port rise and fall times		0.7	5.1	0.7	5	1	5	0.7	5	ns
t_{rB}, t_{fB}	B-port rise and fall times		1	7.3	0.7	5	0.7	3.9	0.6	3.8	ns
$t_{SK(O)}$	Channel-to-channel skew			0.8		0.7		0.6		0.6	ns
Max data rate			52		60		60		60		Mbps

5.16 Switching Characteristics – V_{CCA} = 1.8V ± 0.15V (TXB0106)

over recommended operating ambient temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.8V ± 0.15V		V_{CCB} = 2.5V ± 0.2V		V_{CCB} = 3.3V ± 0.3V		V_{CCB} = 5V ± 0.5V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	B	1.6	12	1.4	7.7	1.3	6.8	1.2	6.5	ns
	B	A	1.5	13.5	1.2	10	0.8	8.2	0.5	8	
t_{en}	OE	A		1		1		1		1	µs
		B		1		1		1		1	
t_{dis} (1)	OE	A	278	393	191	256	190	248	189	248	ns
		B	278	393	191	256	190	248	189	248	
t_{rA}, t_{fA}	A-port rise and fall times		0.7	5.1	0.7	5	1	5	0.7	5	ns
t_{rB}, t_{fB}	B-port rise and fall times		1	7.3	0.7	5	0.7	3.9	0.6	3.8	ns
$t_{SK(O)}$	Channel-to-channel skew			0.8		0.7		0.6		0.6	ns
Max data rate			52		60		60		60		Mbps

5.17 Switching Characteristics – V_{CCA} = 2.5V ± 0.2V (TXB0106I)

over recommended operating ambient temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 2.5V ± 0.2V		V_{CCB} = 3.3V ± 0.3V		V_{CCB} = 5V ± 0.5V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	B	1.1	6.7	1	5.7	0.9	5	ns
	B	A	1	8.5	0.6	7	0.3	7	
t_{en}	OE	A		1		1		1	µs
		B		1		1		1	
t_{dis} (1)	OE	A	5	16.9	4.9	15	4.5	13.8	ns
		B	4.8	21.8	4.5	17.9	4.4	15.2	
t_{rA}, t_{fA}	A-port rise and fall times		0.8	3.6	0.6	3.6	0.5	3.5	ns
t_{rB}, t_{fB}	B-port rise and fall times		0.6	4.9	0.7	3.9	0.6	3.2	ns
$t_{SK(O)}$	Channel-to-channel skew			0.4		0.3		0.3	ns
Max data rate			70		100		100		Mbps

5.18 Switching Characteristics – V_{CCA} = 2.5V ± 0.2V (TXB0106)

over recommended operating ambient temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 2.5V ± 0.2V		V_{CCB} = 3.3V ± 0.3V		V_{CCB} = 5V ± 0.5V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	B	1.1	6.7	1	5.7	0.9	5	ns
	B	A	1	8.5	0.6	7	0.3	7	
t_{en}	OE	A		1		1		1	µs
		B		1		1		1	
t_{dis} (1)	OE	A	190	255	137	185	133	169	ns
		B	190	255	137	185	133	169	
t_{rA}, t_{fA}	A-port rise and fall times		0.8	3.6	0.6	3.6	0.5	3.5	ns
t_{rB}, t_{fB}	B-port rise and fall times		0.6	4.9	0.7	3.9	0.6	3.2	ns
$t_{SK(O)}$	Channel-to-channel skew			0.4		0.3		0.3	ns
Max data rate			70		100		100		Mbps

5.19 Switching Characteristics – V_{CCA} = 3.3V ± 0.3V (TXB0106I)

over recommended operating ambient temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 3.3V ± 0.3V		V_{CCB} = 5V ± 0.5V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}	A	B	0.9	5.5	0.8	4.5	ns
	B	A	0.5	6.5	0.2	6	
t_{en}	OE	A		1		1	µs
		B		1		1	
t_{dis} (1)	OE	A	4.5	13.9	4.1	12.4	ns
		B	4.1	17.3	4	14.4	
t_{rA}, t_{fA}	A-port rise and fall times		0.5	3	0.5	3	ns
t_{rB}, t_{fB}	B-port rise and fall times		0.7	3.9	0.6	3.2	ns
$t_{SK(O)}$	Channel-to-channel skew			0.4		0.3	ns
Max data rate			100		100		Mbps

5.20 Switching Characteristics – V_{CCA} = 3.3V ± 0.3V (TXB0106)

over recommended operating ambient temperature range (unless otherwise noted)

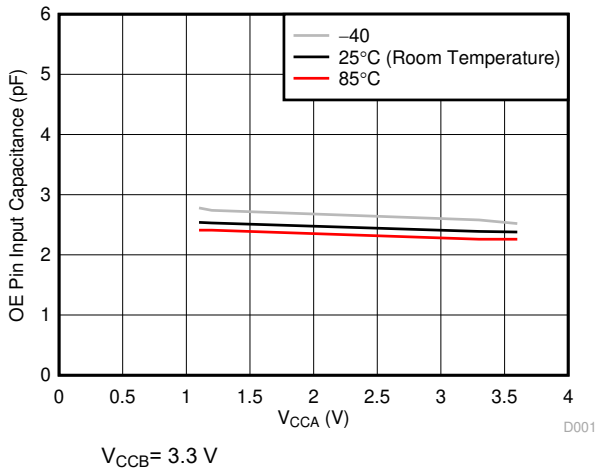
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 3.3V ± 0.3V		V_{CCB} = 5V ± 0.5V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}	A	B	0.9	5.5	0.8	4.5	ns
	B	A	0.5	6.5	0.2	6	
t_{en}	OE	A		1		1	µs
		B		1		1	
t_{dis} (1)	OE	A	137	185	97.6	127	ns
		B	137	185	97.6	127	
t_{rA}, t_{fA}	A-port rise and fall times		0.5	3	0.5	3	ns
t_{rB}, t_{fB}	B-port rise and fall times		0.7	3.9	0.6	3.2	ns
$t_{SK(O)}$	Channel-to-channel skew			0.4		0.3	ns
Max data rate			100		100		Mbps

5.21 Operating Characteristics

T_A = 25°C

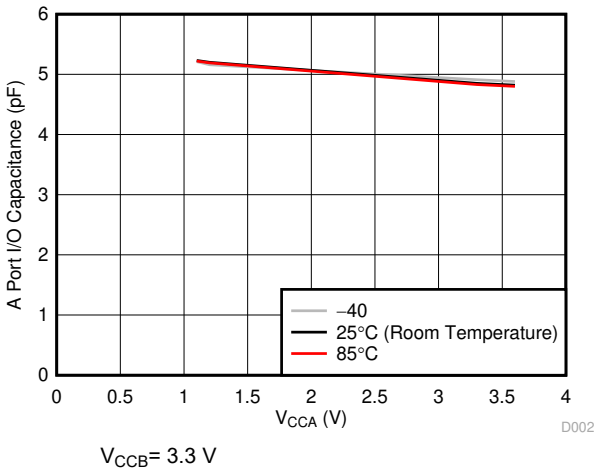
PARAMETER		TEST CONDITIONS	V_{CCA}							UNIT
			1.2V	1.2V	1.5V	1.8V	2.5V	2.5V	3.3V	
			V_{CCB}							
			5V	1.8V	1.8V	1.8V	2.5V	5V	3.3V to 5V	
			TYP	TYP	TYP	TYP	TYP	TYP	TYP	
C_{pdA}	A-port input, B-port output	C_L = 0, f = 10MHz, $t_r = t_f$ = 1ns, OE = V_{CCA} (outputs enabled)	9	8	7	7	7	7	8	pF
	B-port input, A-port output		12	11	11	11	11	11	11	
C_{pdB}	A-port input, B-port output		35	26	27	27	27	27	28	pF
	B-port input, A-port output		26	19	18	18	18	20	21	
C_{pdA}	A-port input, B-port output	C_L = 0, f = 10MHz, $t_r = t_f$ = 1ns, OE = GND (outputs disabled)	0.01	0.01	0.01	0.01	0.01	0.01	0.01	pF
	B-port input, A-port output		0.01	0.01	0.01	0.01	0.01	0.01	0.01	
C_{pdB}	A-port input, B-port output		0.01	0.01	0.01	0.01	0.01	0.01	0.03	pF
	B-port input, A-port output		0.01	0.01	0.01	0.01	0.01	0.01	0.03	

5.22 Typical Characteristics



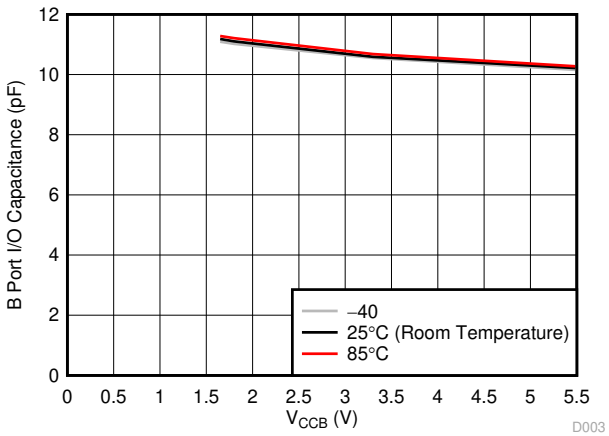
V_{CCB}= 3.3 V

Figure 5-1. Input capacitance for OE pin (C_I) vs Power Supply (V_{CCA})



V_{CCB}= 3.3 V

Figure 5-2. Capacitance for A port I/O pins (C_{iO}) vs Power Supply (V_{CCA})



V_{CCA}= 1.8 V

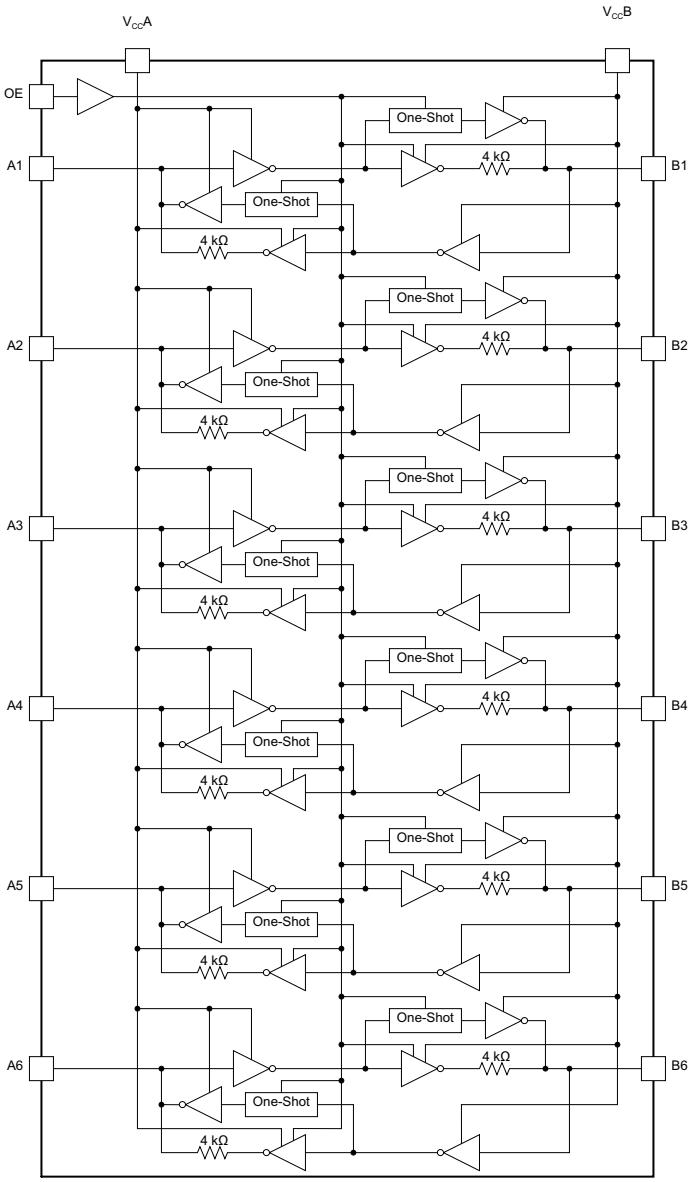
Figure 5-3. Capacitance for B port I/O pins (C_{iO}) vs Power Supply (V_{CCB})

6 Detailed Description

6.1 Overview

The TXB0106-Q1 device is a 6-bit, directionless voltage-level translator specifically designed for translating logic voltage levels. The A port is able to accept I/O voltages ranging from 1.2V to 3.6V, while the B port can accept I/O voltages from 1.65V to 5.5V. The device is a buffered architecture with edge-rate accelerators (one-shots) to improve the overall data rate. This device can only translate push-pull CMOS logic outputs. For open-drain signal translation, see TI's TXS family of products.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Architecture

The TXB0106-Q1 architecture (see Figure 6-1) does not require a direction-control signal to control the direction of data flow from A to B or from B to A. In a dc state, the output drivers of the TXB0106-Q1 device can maintain a high or low, but are designed to be weak, so that they can be overdriven by an external driver when data on the bus starts flowing in the opposite direction.

The output one-shots detect rising or falling edges on the A or B ports. During a rising edge, the one-shot turns on the PMOS transistors (T1, T3) for a short duration, which speeds up the low-to-high transition. Similarly, during a falling edge, the one-shot turns on the NMOS transistors (T2, T4) for a short duration, which speeds up the high-to-low transition. The typical output impedance during output transition is 70Ω at V_{CCO} = 1.2V to 1.8V, 50Ω at V_{CCO} = 1.8V to 3.3V, and 40Ω at V_{CCO} = 3.3V to 5V.

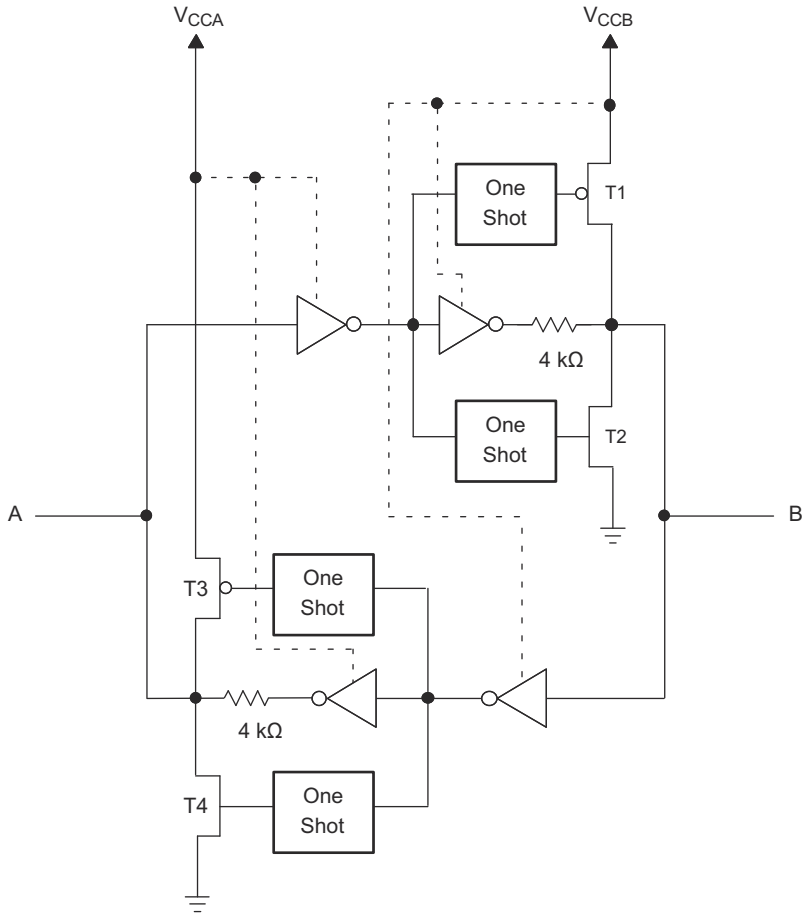
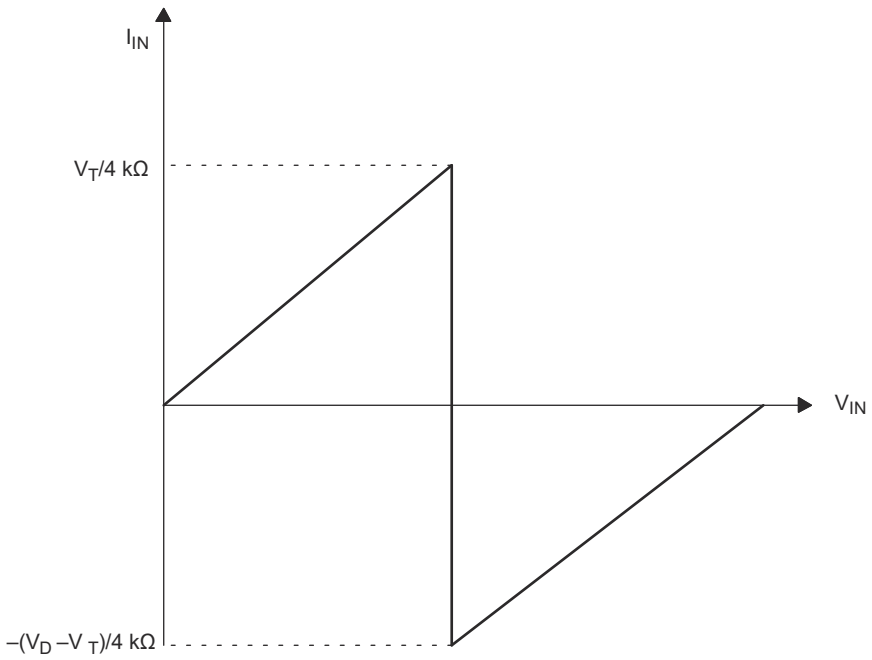


Figure 6-1. Architecture of the TXB0106-Q1 I/O Cell

6.3.2 Input Driver Requirements

Typical I_{IN} vs V_{IN} characteristics of the TXB0106-Q1 device are shown in Figure 6-2. For proper operation, the device driving the data I/Os of the TXB0106-Q1 device must have drive strength of at least ±2mA.



A. V_T is the input threshold voltage of the TXB0106-Q1 device (typically V_{CCI} / 2).
B. V_D is the supply voltage of the external driver.

Figure 6-2. Typical I_{IN} vs V_{IN} Curve

6.3.3 Power Up

During operation, ensure that $V_{CCA} \leq V_{CCB}$ at all times. During power-up sequencing, $V_{CCA} \geq V_{CCB}$ does not damage the device, so any power supply can be ramped up first. The TXB0106-Q1 device has circuitry that disables all output ports when either V_{CC} is switched off ($V_{CCA/B}$ = 0V).

6.3.4 Output Load Considerations

TI recommends careful PCB layout practices with short PCB trace lengths to avoid excessive capacitive loading and to ensure that proper one-shot (O.S.) triggering takes place. PCB signal trace-lengths should be kept short enough such that the round trip delay of any reflection is less than the O.S. duration. This improves signal integrity by ensuring that any reflection sees a low impedance at the driver. The O.S. circuits have been designed to stay on for approximately 10ns. The maximum capacitance of the lumped load that can be driven also depends directly on the O.S. duration. With very heavy capacitive loads, the O.S. can time out before the signal is driven fully to the positive rail. The O.S. duration has been set to best optimize trade-offs between dynamic I_{CC}, load driving capability, and maximum bit-rate considerations. Both PCB trace length and connectors add to the capacitance that the TXB0106-Q1 output sees, so it is recommended that this lumped-load capacitance be considered to avoid O.S. retriggering, bus contention, output signal oscillations, or other adverse system-level affects.

6.3.5 Enable and Disable

The TXB0106-Q1 device has an OE input that is used to disable the device by setting OE = low, which places all I/Os in the high-impedance (Hi-Z) state. The disable time (t_{dis}) indicates the delay between when OE goes low and when the outputs actually get disabled (Hi-Z). The enable time (t_{en}) indicates the amount of time the user must allow for the O.S. circuitry to become operational after OE is taken high.

6.3.6 Pullup or Pulldown Resistors on I/O Lines

The TXB0106-Q1 device is designed to drive capacitive loads of up to 70pF. The output drivers of the TXB0106-Q1 device have low dc drive strength. If pullup or pulldown resistors are connected externally to the data I/Os,

their values must be kept higher than 50kΩ to ensure that they do not contend with the output drivers of the TXB0106-Q1 device.

For the same reason, the TXB0106-Q1 device should not be used in applications such as I^2C or 1-Wire where an open-drain driver is connected on the bidirectional data I/O. For these applications, use a device from TI's TXS family of level translators.

6.4 Device Functional Modes

The TXB0106-Q1 device has two functional modes, enabled and disabled. To disable the device, set the OE input to low, which places all I/Os in a high-impedance state. Setting the OE input to high will enable the device.

Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

1 Application Information

The TXB0106-Q1 device can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another. It can only translate push-pull CMOS logic outputs. For open-drain signal translation, see TI's TXS products. Any external pulldown or pullup resistors are recommended to be larger than 50 kΩ.

2 Typical Application

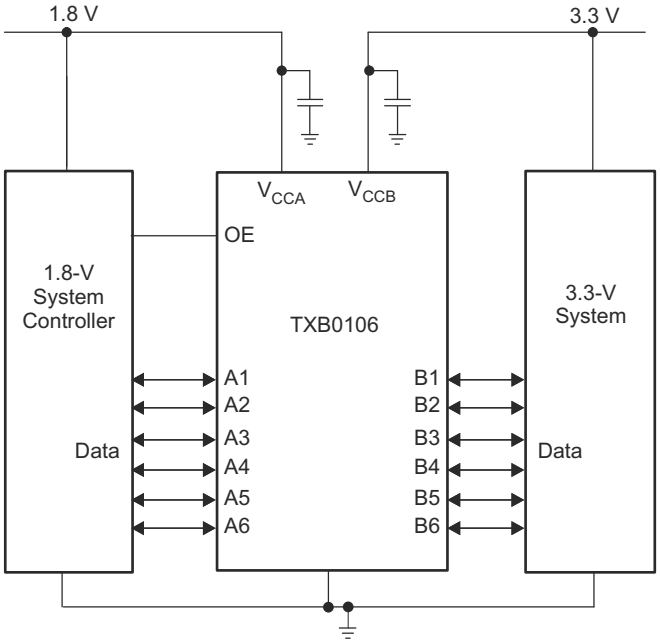


Figure 7-1. Typical Operating Circuit

2.1 Design Requirements

For this design example, use the parameters listed in Table 7-1. And make sure that $V_{CCA} \leq V_{CCB}$.

Table 7-1. Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUE
Input voltage range	1.2V to 3.6V
Output voltage range	1.65V to 5.5V

2.2 Detailed Design Procedure

To begin the design process, determine the following:

• Input voltage range

- Use the supply voltage of the device that is driving the TXB0106-Q1 device to determine the input voltage range. For a valid logic high the value must exceed the V_{IH} of the input port. For a valid logic low the value must be less than the V_{IL} of the input port.

• Output voltage range

- Use the supply voltage of the device that the TXB0106-Q1 device is driving to determine the output voltage range.

- Avoid the use of external pullup or pulldown resistors, if possible. If not possible, it is recommended the value should be larger than 50 kΩ.

• An external pulldown or pullup resistor decreases the output V_{OH} and V_{OL}. Use the following equations to estimate the V_{OH} and V_{OL} as a result of an external pulldown and pullup resistor. See *Effects of External Pullup and Pulldown Resistors on TXS and TXB Devices* and *Factors Affecting VOL for TXS and LSF Auto-bidirectional Translation Devices*.

$V_{OH} = V_{CCx} \times R_{PD} / (R_{PD} + 4.5\ k\Omega)$

$V_{OL} = V_{CCx} \times 4.5\ k\Omega / (R_{PU} + 4.5\ k\Omega)$

Where

• V_{CCx} is the output port supply voltage on either V_{CCA} or V_{CCB}

• R_{PD} is the value of the external pulldown resistor

• R_{PU} is the value of the external pullup resistor

• 4.5 kΩ accounts for the tolerance of the serial 4-kΩ resistor in the I/O line.

2.3 Application Curve

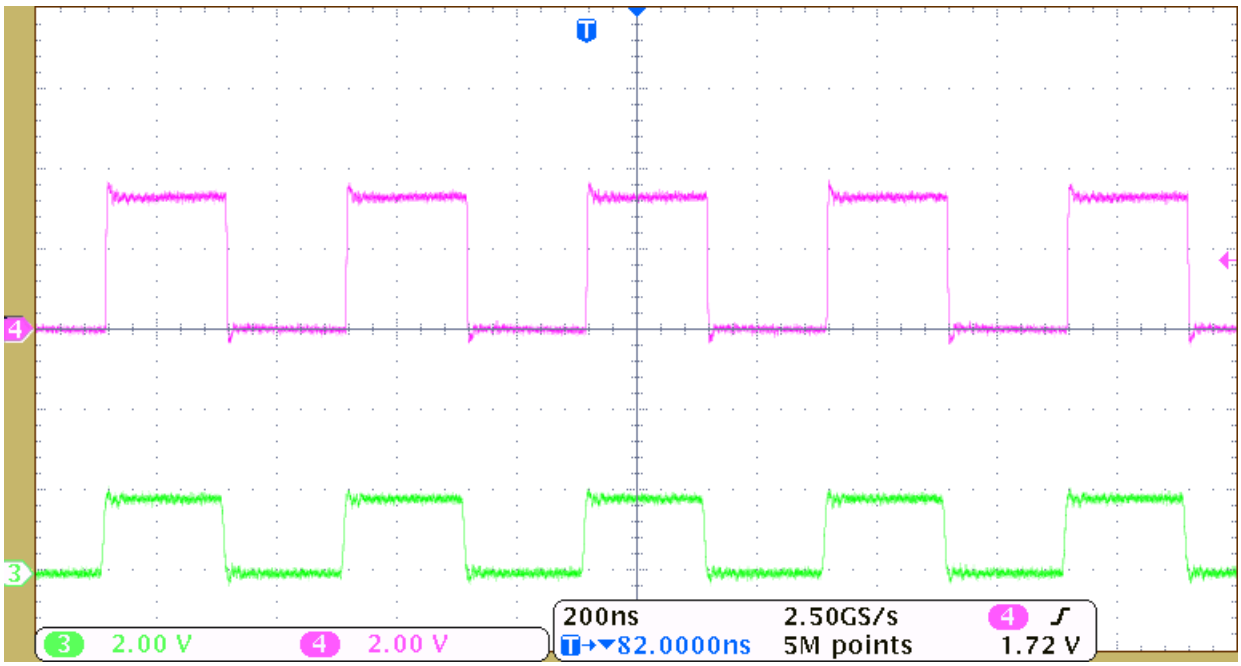


Figure 7-2. Level Translation of a 2.5MHz Signal

3 Power Supply Recommendations

During operation, ensure that $V_{CCA} \leq V_{CCB}$ at all times. During power-up sequencing, $V_{CCA} \geq V_{CCB}$ does not damage the device, so any power supply can be ramped up first. The TXB0106-Q1 device has circuitry that disables all output ports when either V_{CC} is switched off (V_{CCA} or V_{CCB}= 0V). The output-enable (OE) input circuit is designed so that it is supplied by V_{CCA}, and when the (OE) input is low, all outputs are placed in the high-impedance state. To ensure the high-impedance state of the outputs during power up or power down, the OE input pin must be tied to GND through a pulldown resistor and must not be enabled until V_{CCA} and V_{CCB} are fully ramped and stable. The minimum value of the pulldown resistor to ground is determined by the current-sourcing capability of the driver.

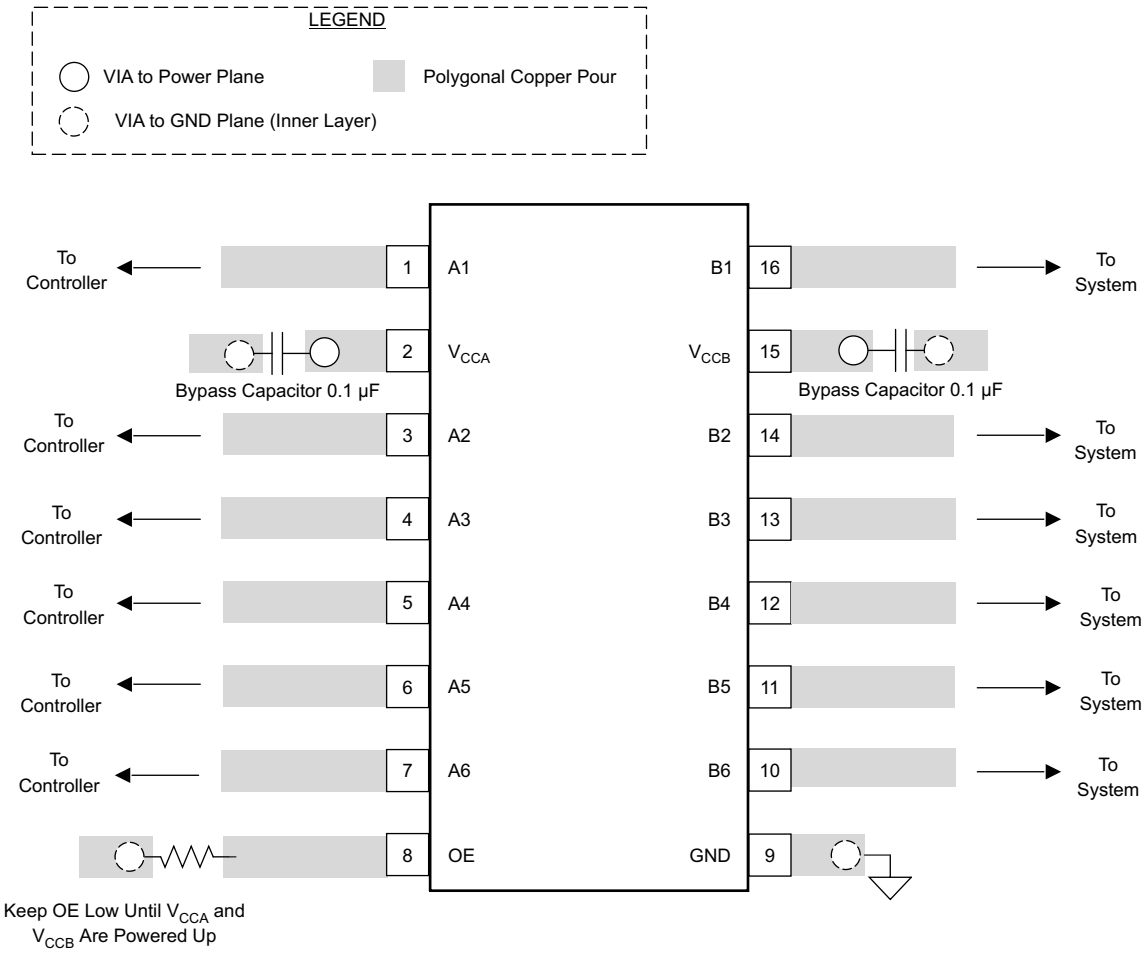
4 Layout

4.1 Layout Guidelines

To ensure reliability of the device, the following common printed-circuit board layout guidelines are recommended:

- Bypass capacitors should be used on power supplies, and should be placed as close as possible to the V_{CCA} and V_{CCB} pins and the GND pin
- Short trace-lengths should be used to avoid excessive loading.
- PCB signal trace-lengths must be kept short enough so that the round-trip delay of any reflection is less than the O.S. duration, approximately 10ns, ensuring that any reflection encounters low impedance at the source driver.

4.2 Layout Example



7 Device and Documentation Support

7.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

7.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

7.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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7.4 Trademarks

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7.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (April 2018) to Revision B (August 2025) **Page**

- Added Operating ambient temperature for TXB0106-Q1 5
- Added BQB column in Section 5.4 6
- Added Section 5.6 for TXB0106Q1 7
- Added Section 5.14 for TXB0106-Q1 9
- Added Section 5.16 for TXB0106-Q1 10
- Added Section 5.18 for TXB0106-Q1 11
- Added Section 5.20 for TXB0106-Q1 12

Changes from Revision * (August 2009) to Revision A (April 2018) **Page**

- Added *Applications* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes* section, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section 1
- Changed the entry in the TYPE column from "—" to "I" for V_{CCA} and V_{CCB} 4
- Added row for junction temperature to *Absolute Maximum Ratings* 5
- Added parameter descriptons to *Electrical Characteristics* table 6
- Added "-Q1" to the device name throughout the document 15
- Changed I to I_{CC} in *Section 6.3.4* 17
- Changed TXS01xx series to TXS family in *Section 6.3.6* 17
- Changed TXS010X to TXS in *Section 7.1* 18
- Clarified wording of sentences and added references to two application reports 19

DATE	REVISION	NOTES
August 2009	*	Initial Release

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated device. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TXB0106IPWRQ1	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	YE06Q1
TXB0106IPWRQ1.A	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	YE06Q1
TXB0106IPWRQ1.B	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	YE06Q1
TXB0106QWBQBRQ1	Active	Production	WQFN (BQB) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	YE06Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF TXB0106-Q1 :

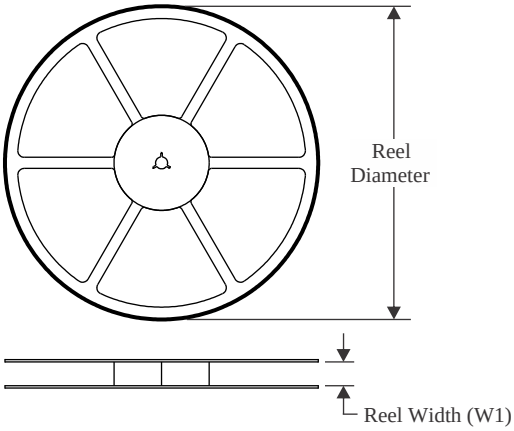
- Catalog : TXB0106

NOTE: Qualified Version Definitions:

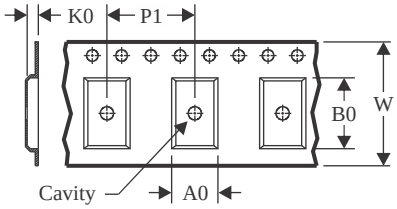
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

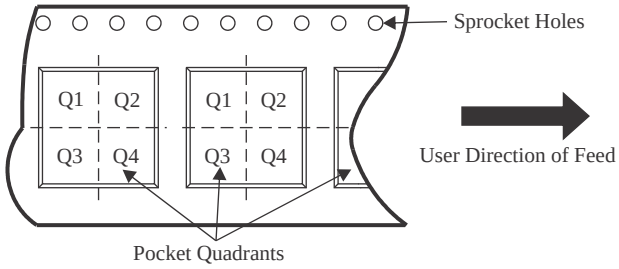


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

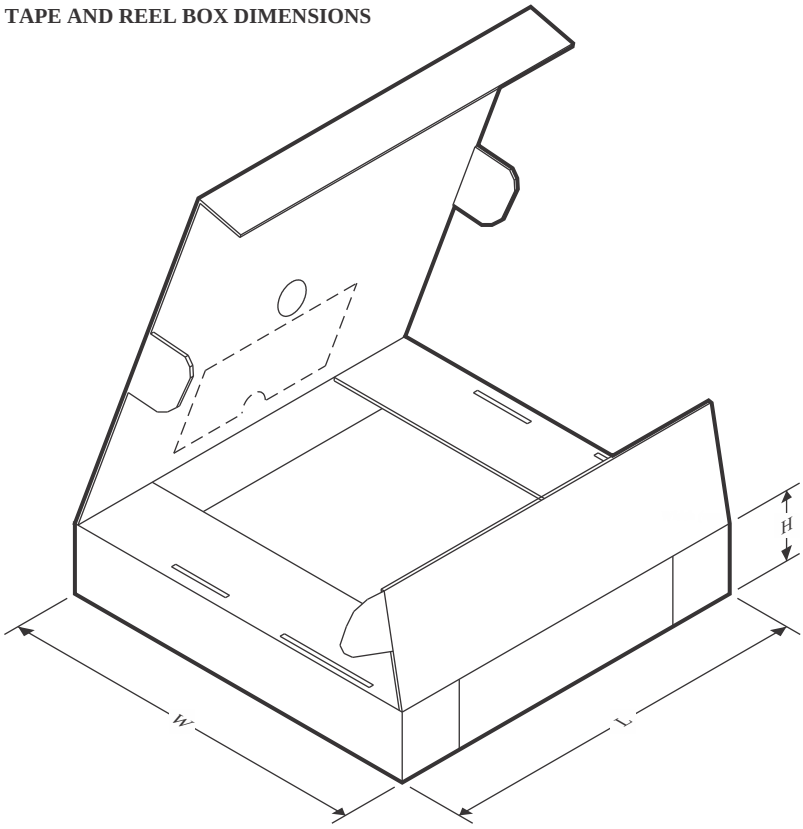
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TXB0106IPWRQ1	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TXB0106QWBQBRQ1	WQFN	BQB	16	3000	180.0	12.4	2.8	3.8	1.2	4.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TXB0106IPWRQ1	TSSOP	PW	16	2000	353.0	353.0	32.0
TXB0106QWBQBRQ1	WQFN	BQB	16	3000	210.0	185.0	35.0

GENERIC PACKAGE VIEW

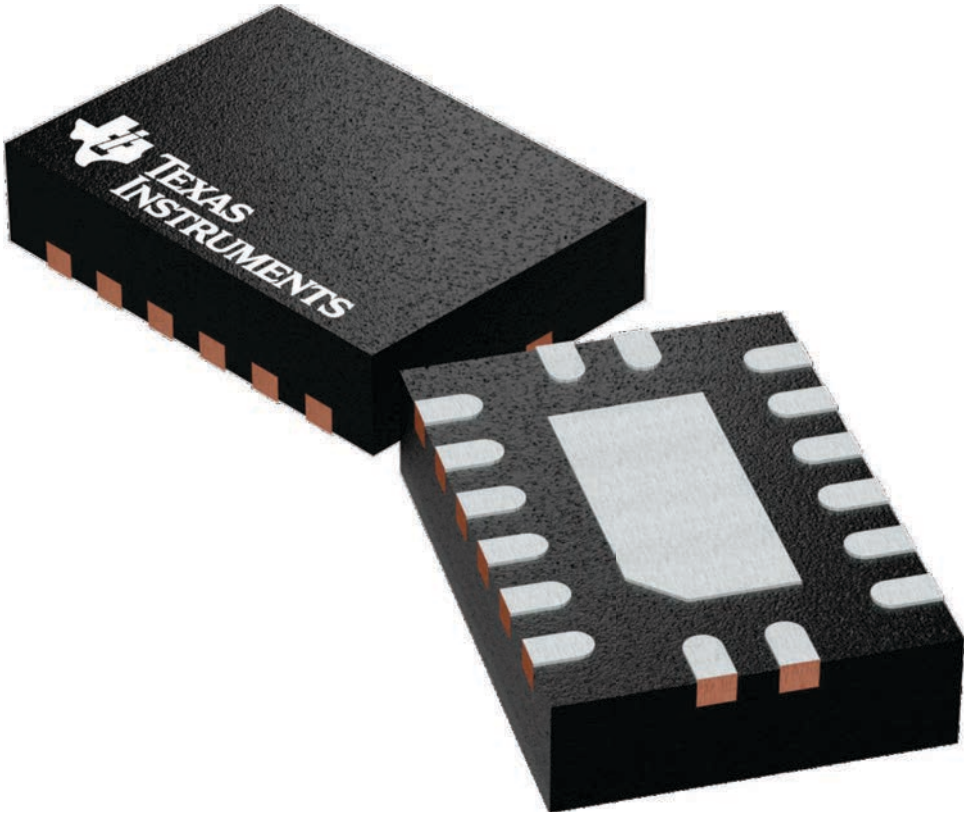
BQB 16

WQFN - 0.8 mm max height

2.5 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



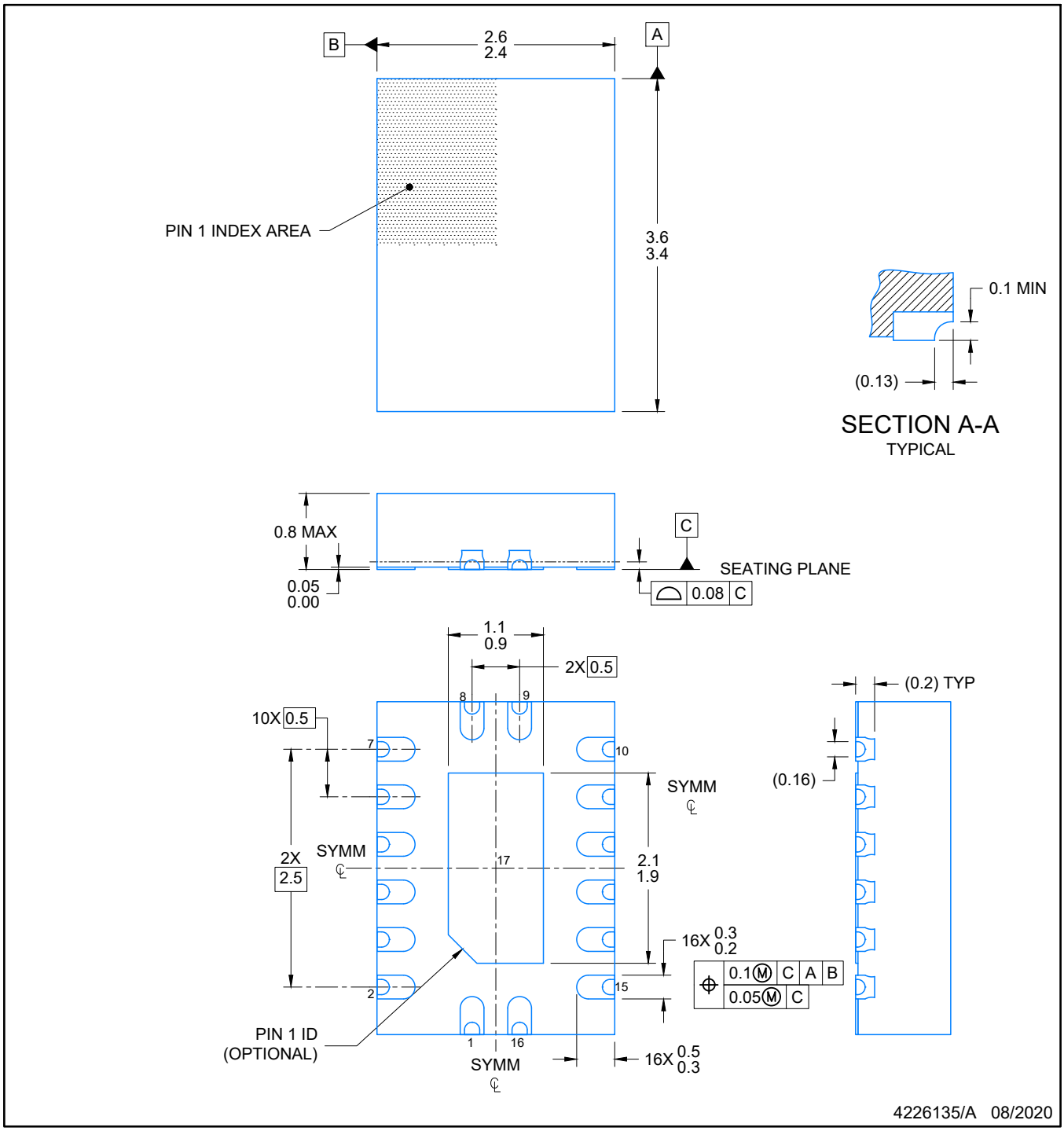
4226161/A

PACKAGE OUTLINE

BQB0016B

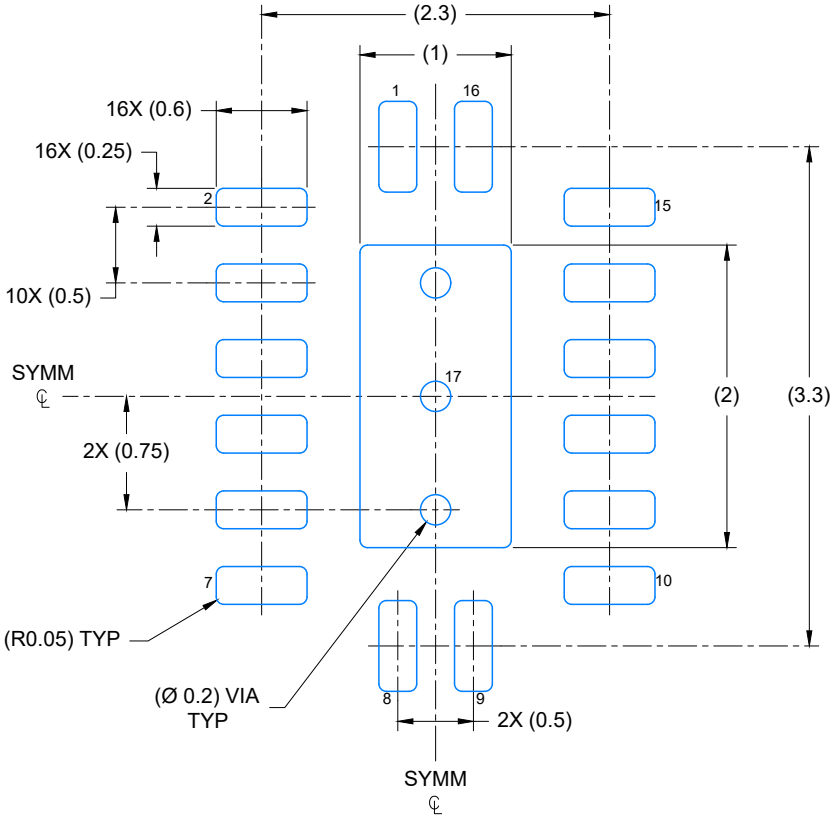
WQFN - 0.8 mm max height

INDSTNAME



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

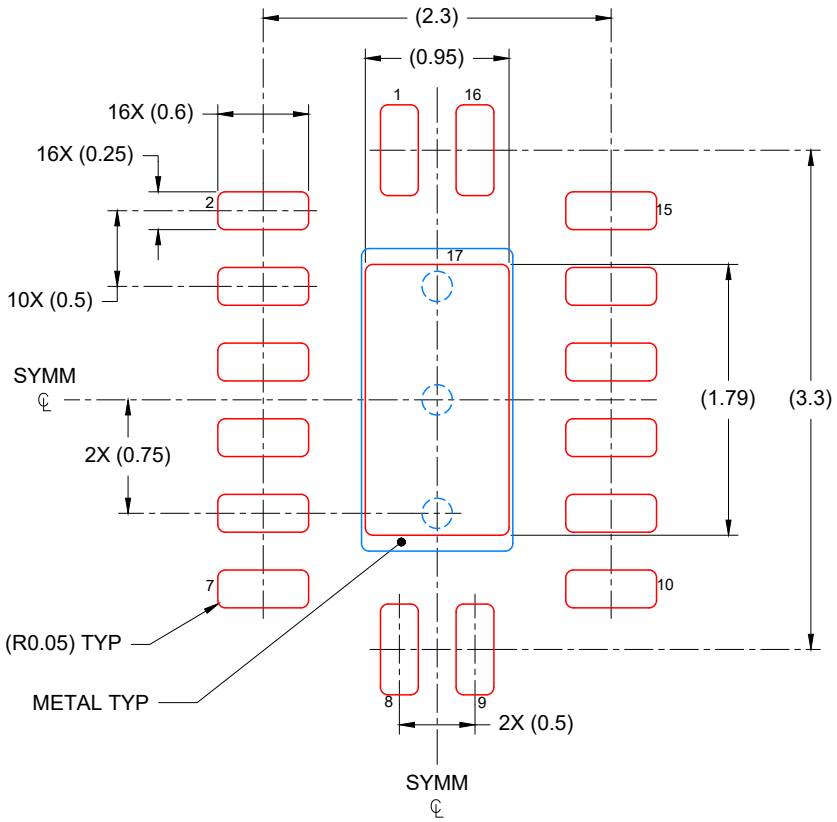


LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

4226135/A 08/2020

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
85% PRINTED COVERAGE BY AREA
SCALE: 20X

4226135/A 08/2020

NOTES: (continued)

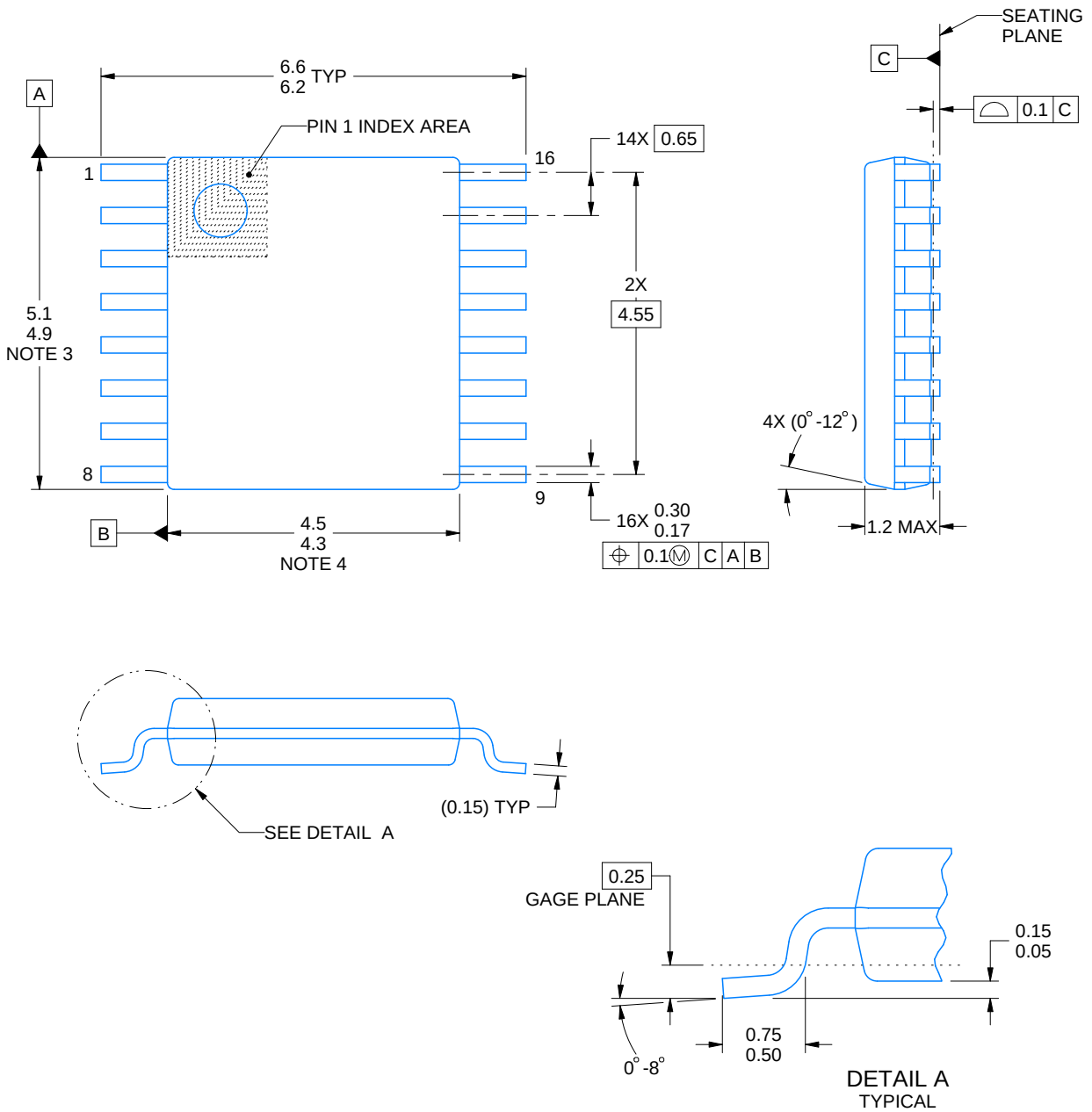
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

PW0016A

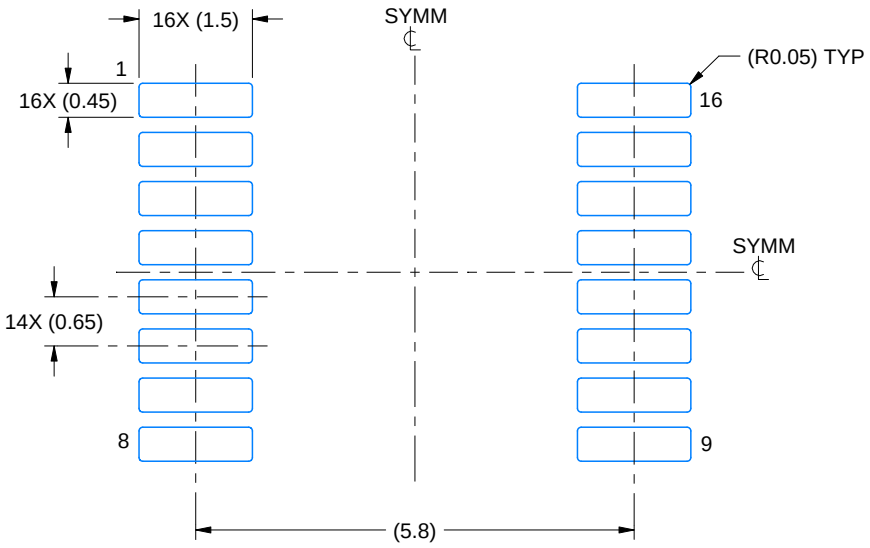
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



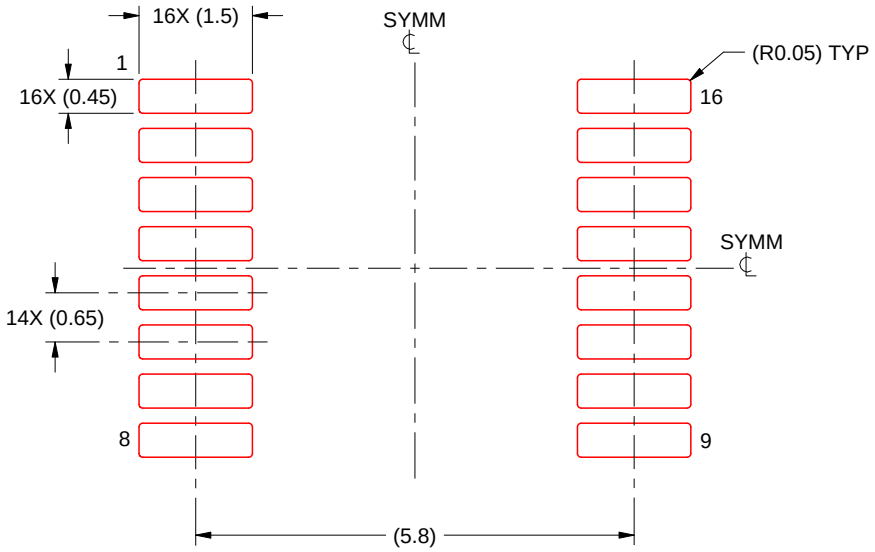
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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