TXB0606 Auto-Bidirectional Level Translator for High-Speed Interfaces

1 Features

- 0.9V to 2V on A port and 1.65V to 3.6V on B port
- Minimum data rates:
  - >130 Mbps (15pF load, 1.8V to 3.3V)
  - >100 Mbps (100pF load, 1.8V to 3.3V)
- Supports high-speed interfaces such as QSPI, OSPI, eSPI
- V_{CCA} <, =, > V_{CCB} is acceptable
- No direction control signal needed
- V_{CC} isolation feature: if either V_{CC} input is at GND, all outputs are in the high-impedance state
- Schmitt-trigger inputs allow for slow or noisy inputs
- Output enable (OE) input circuit referenced to V_{CCA}
- I_{OFF} supports partial power-down mode operation
- Latch-up Performance Exceeds 100mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - A Port:
    - 2000V Human-Body Model (A114-B)
    - 1000V Charged-Device Model (C101)
  - B Port:
    - 2000V Human-Body Model (A114-B)
    - 1000V Charged-Device Model (C101)

2 Applications

- Data Center and Enterprise Computing
- Desktop PC
- Personal Electronics

3 Description

The TXB0606 is an 6-bit non-inverting auto-bidirectional translator that uses two separate configurable power-supply rails. This voltage translator/ line redriver can be used to remedy voltage domain mismatches in addition to signal boosting in long-cabling transmission applications.

The TXB0606 leverages a patented design to achieve high data throughput for memory-intensive interfaces like Quad-SPI between BMC and Flash devices without signal integrity losses associated with excessive output parasitic capacitance.

The A port is designed to track V_{CCA}. V_{CCA} accepts any supply voltage from 0.9V to 2V. The B port is designed to track V_{CCB}. V_{CCB} accepts any supply voltage from 1.65V to 3.6V.

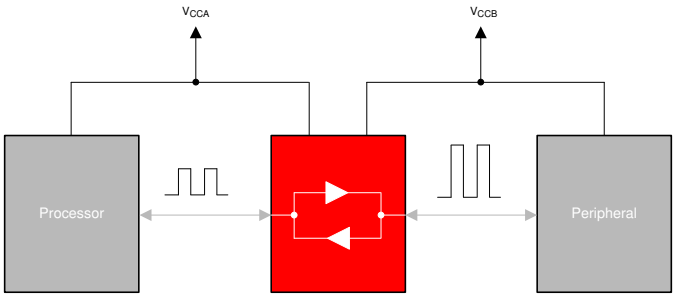
When the OE input is low, all outputs are placed in the high-impedance state. To ensure the high-impedance state during power up or power down, OE must be tied to GND through a pulldown resistor. The current sourcing capability of the driver determines the minimum value of the resistor. The TXB0606 device is designed so the OE input circuit is supplied by V_{CCA}.

This device is fully specified for partial power-down applications using I_{OFF}. The I_{OFF} circuitry disables the outputs, which prevents damaging current backflow through the device when the device is powered down.

Package Information

PART NUMBER	PACKAGE(1)	BODY SIZE
TXB0606	PW (TSSOP, 16)	5.00mm × 6.1mm
	RGY (VQFN, 16)	4.00mm × 3.50mm
	BQB (WQFN, 16)	3.50mm × 2.50mm
	DYY (SOT, 16)	4.20mm × 3.31mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.



Typical Application Block Diagram for TXB0606

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4 Pin Configuration and Functions

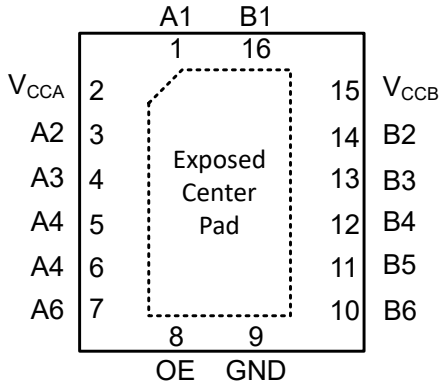


Figure 4-1. BQB, RGY Package, 16-Pin WQFN With Exposed Thermal Pad (Top View)

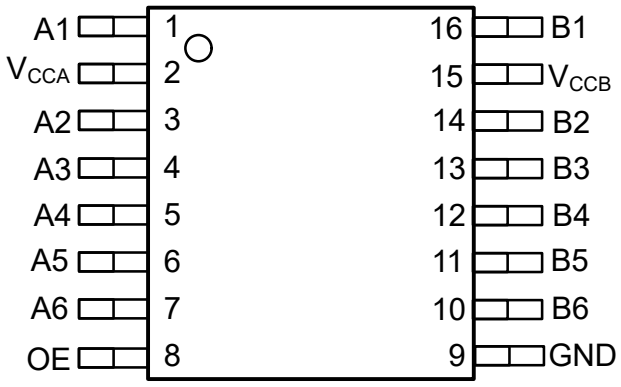


Figure 4-2. DYY, PW Package, 16-Pin SOT (Top View)

A. The exposed center pad, if used, must be connected as a secondary ground or left electrically open.

Table 4-1. Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	A1		Input/output 1. Referenced to V_{CCA}.
2	V_{CCA}	-	A-port supply voltage.
3	A2	I/O	Input/output 2. Referenced to V_{CCA}.
4	A3	I/O	Input/output 3. Referenced to V_{CCA}.
5	A4	I/O	Input/output 4. Referenced to V_{CCA}.
6	A5	I/O	Input/output 5. Referenced to V_{CCA}.
7	A6	I/O	Input/output 6. Referenced to V_{CCA}.
8	OE	-	Output enable. Pull OE low to place all outputs in tri-state mode. Referenced to V_{CCA}.
9	GND	-	Ground
10	B6	I/O	Input/output 6. Referenced to V_{CCB}.
11	B5	I/O	Input/output 5. Referenced to V_{CCB}.
12	B4	I/O	Input/output 4. Referenced to V_{CCB}.
13	B3	I/O	Input/output 3. Referenced to V_{CCB}.
14	B2	I/O	Input/output 2. Referenced to V_{CCB}.
15	V_{CCB}	-	B-port supply voltage.
16	B1	I/O	Input/output 1. Referenced to V_{CCB}.

5 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CCA}	Supply voltage A		–0.5	2.5	V
V_{CCB}	Supply voltage B		–0.5	4.6	V
V_I	Input Voltage(2)	I/O Ports (A Port)	–0.5	2.5	V
V_I	Input Voltage(2)	I/O Ports (B Port)	–0.5	4.6	V
V_I	Input Voltage(2)	OE	–0.5	2.5	V
V_O	Voltage applied to any output in the high-impedance or power-off state(2)	A Port	–0.5	2.5	V
		B Port	–0.5	4.6	
V_O	Voltage applied to any output in the high or low state(2) (3)	A Port	–0.5	V_{CCA} + 0.5	V
		B Port	–0.5	V_{CCB} + 0.5	
I_{IK}	Input clamp current	V_I < 0		–50	mA
I_{OK}	Output clamp current	V_O < 0		–50	mA
I_O	Continuous output current		–50	50	mA
	Continuous current through V_{CC} or GND		–100	100	mA
T_{stg}	Storage temperature		–65	150	°C
T_j	Junction Temperature			150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* Exposure beyond the limits listed in *Recommended Operating Conditions* may affect device reliability.
(2) The input voltage and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The value of V_{CCA} and V_{CCB} are provided in the recommended operating conditions table.

6 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	A/B Port	±2	kV
		Charged device model (CDM), per JEDEC specification, JESD220C101 (2)	A/B Port	±1	kV

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

7 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted) (1) (2) (3)

			V_{CCA}	V_{CCB}	MIN	MAX	UNIT
V_{CCA}	Supply voltage A				0.9	2	V
V_{CCB}	Supply voltage B				1.65	3.6	V
V_I	Input voltage	A-port I/O's	0.9V to 2V	1.65V to 3.6V	0	V_{CCA}	V
		B-port I/O's	0.9V to 2V	1.65V to 3.6V	0	V_{CCB}	
		OE Input	0.9V to 2V	1.65V to 3.6V	0	2	
T_A	Operating free-air temperature				–40	125	°C

(1) V_{CCI} is the V_{CC} associated with the input port.
(2) V_{CCO} is the V_{CC} associated with the output port.
(3) All control inputs and data I/Os of this device have weak pulldowns to ensure the line is not floating when undefined external to the device. The input leakage from these weak pulldowns is defined by the I_I specification indicated under *Electrical Characteristics*.

8 Thermal Information

THERMAL METRIC[1]		TXB0606 PW (TSSOP) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	113.41	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	53.74	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	71.52	°C/W
Y_{JT}	Junction-to-top characterization parameter	13.90	°C/W
Y_{JB}	Junction-to-board characterization parameter	71.07	°C/W
$R_{\theta JC(bottom)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

9 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)(1) (2)

PARAMETER		TEST CONDITIONS	V_{CCA}	V_{CCB}	Operating free-air temperature (T_A)						UNIT
					–40°C to 85°C			–40°C to 125°C			
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{T+}	Positive-going input-threshold voltage	Data Inputs (Ax) (Referenced to V_{CCI})	0.9V	1.65 – 3.6V	0.53		0.66	0.52		0.66	V
			1.2V ± 0.1V	1.65 – 3.6V	0.65		0.93	0.64		0.93	V
			1.5V ± 0.1V	1.65 – 3.6V	0.82		1.12	0.82		1.12	V
			1.8V ± 0.15V	1.65 – 3.6V	0.96		1.33	0.96		1.33	V
			2V	1.65 – 3.6V	1.15		1.36	1.14		1.36	V
		Data Inputs (Bx) (Referenced to V_{CCI})	0.9 – 2V	1.8 ± 0.15V	0.85		1.31	0.84		1.31	V
			0.9 – 2V	2.5 ± 0.2V	1.14		1.66	1.13		1.66	V
			0.9 – 2V	3.3 ± 0.3V	1.45		2.11	1.45		2.12	V
		OE (Referenced to V_{CCA})	0.9V	1.65 – 3.6V	0.52		0.67	0.52		0.67	V
			1.2V ± 0.1V	1.65 – 3.6V	0.63		0.92	0.63		0.92	V
			1.5V ± 0.1V	1.65 – 3.6V	0.79		1.08	0.78		1.08	V
			1.8V ± 0.15V	1.65 – 3.6V	0.9		1.24	0.89		1.24	V
			2V	1.65 – 3.6V	1.05		1.27	1.04		1.27	V
V_{T-}	Negative-going input-threshold voltage	Data Inputs (Ax) (Referenced to V_{CCI})	0.9V	1.65 – 3.6V	0.28		0.41	0.28		0.41	V
			1.2V ± 0.1V	1.65 – 3.6V	0.35		0.55	0.35		0.56	V
			1.5V ± 0.1V	1.65 – 3.6V	0.45		0.67	0.45		0.67	V
			1.8V ± 0.15V	1.65 – 3.6V	0.53		0.81	0.53		0.82	V
			2V	1.65 – 3.6V	0.66		0.83	0.66		0.84	V
		Data Inputs (Bx) (Referenced to V_{CCI})	0.9 – 2V	1.8 ± 0.15V	0.57		0.99	0.57		1.01	V
			0.9 – 2V	2.5 ± 0.2V	0.89		1.39	0.89		1.4	V
			0.9 – 2V	3.3 ± 0.3V	1.21		1.83	1.21		1.85	V
		OE (Referenced to V_{CCA})	0.9V	1.65 – 3.6V	0.28		0.41	0.28		0.41	V
			1.2V ± 0.1V	1.65 – 3.6V	0.35		0.55	0.35		0.56	V
			1.5V ± 0.1V	1.65 – 3.6V	0.45		0.67	0.45		0.67	V
			1.8V ± 0.15V	1.65 – 3.6V	0.53		0.81	0.53		0.82	V
			2V	1.65 – 3.6V	0.66		0.83	0.66		0.84	V
ΔV_T	Input-threshold hysteresis ($V_{T+} – V_{T-}$)	Data Inputs (Ax) (Referenced to V_{CCI})	0.9V	1.65 – 3.6V	0.21		0.31	0.2		0.31	V
			1.2V ± 0.1V	1.65 – 3.6V	0.27		0.41	0.25		0.41	V
			1.5V ± 0.1V	1.65 – 3.6V	0.33		0.5	0.32		0.5	V
			1.8V ± 0.15V	1.65 – 3.6V	0.38		0.58	0.36		0.58	V
			2V	1.65 – 3.6V	0.43		0.59	0.42		0.59	V
		Data Inputs (Bx) (Referenced to V_{CCI})	0.9 – 2V	1.8 ± 0.15V	0.19		0.45	0.17		0.45	V
			0.9 – 2V	2.5 ± 0.2V	0.19		0.41	0.17		0.41	V
			0.9 – 2V	3.3 ± 0.3V	0.2		0.34	0.19		0.34	V
		OE (Referenced to V_{CCA})	0.9V	1.65 – 3.6V	0.21		0.31	0.19		0.31	V
			1.2V ± 0.1V	1.65 – 3.6V	0.25		0.4	0.23		0.4	V
			1.5V ± 0.1V	1.65 – 3.6V	0.29		0.46	0.28		0.46	V
			1.8V ± 0.15V	1.65 – 3.6V	0.31		0.49	0.3		0.49	V
			2V	1.65 – 3.6V	0.34		0.5	0.33		0.5	V
V_{OHA}	Port A output high voltage	I_{OH} = –20µA	0.9V to 1. 2V	1.65V to 3.6V	VCCA - 0.2			VCCA - 0.2			V
			1.2V to 2V		VCCA - 0.4			VCCA - 0.4			
V_{OLA}	Port A output low voltage	I_{OL} = 20µA	0.9V to 2V	1.65V to 3.6V			0.04			0.04	V

over operating free-air temperature range (unless otherwise noted)(1) (2)

PARAMETER		TEST CONDITIONS	V_{CCA}	V_{CCB}	Operating free-air temperature (T_A)						UNIT
					–40°C to 85°C			–40°C to 125°C			
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{OHB}	Port B output high voltage	I_{OH} = –20µA	0.9V to 1.2V	1.65V to 3.6V	VCCB - 0.2			VCCB - 0.2			V
			1.2V to 2V		VCCB - 0.4			VCCB - 0.4			
V_{OLB}	Port B output low voltage	I_{OL} = 20µA	0.9V to 2V	1.65V to 3.6V			0.06			0.06	V
I_I	Input leakage current	OE V_I = V_{CC} or GND	0.9V to 2V	1.65V to 3.6V			±0.08			±0.43	µA
I_{OFF}	Input leakage current	A Port V_I = V_{CC} or GND	0V	0V to 3.6V			±0.68			±3.85	µA
		B Port V_I = V_{CC} or GND	0V to 2V	0V			±0.62			±1.45	µA
I_{OZ}	High-impedance state output current	OE = GND	0.9V to 2V	1.65V to 3.6V			±0.34			±2.01	µA
I_{CCA}	V_{CCA} supply current	V_I = V_{CCI} or GND, I_O = 0	0.9V	1.65V to 3.6V			6.34			20.94	µA
	V_{CCA} supply current	V_I = V_{CCI} or GND, I_O = 0	1.1V to 2V	1.65V to 3.6V			10.73			30.22	µA
	V_{CCA} supply current	V_I = V_{CCI} or GND, I_O = 0	2V	0V			5.07			24.65	µA
	V_{CCA} supply current	V_I = V_{CCI} or GND, I_O = 0	0V	3.6V			2.5			15	µA
I_{CCB}	V_{CCB} supply current	V_I = V_{CCI} or GND, I_O = 0	0.9V	1.65V to 3.6V			11.51			15.75	µA
	V_{CCB} supply current	V_I = V_{CCI} or GND, I_O = 0	1.1V to 2V	1.65V to 3.6V			11.51			15.75	µA
	V_{CCB} supply current	V_I = V_{CCI} or GND, I_O = 0	2V	0V			0.6			5	µA
	V_{CCB} supply current	V_I = V_{CCI} or GND, I_O = 0	0V	3.6V			1.61			6.72	µA
I_{CCA} + I_{CCB}	Combined supply current	V_I = V_{CCI} or GND I_O = 0	0.9V to 1.2V	1.65V to 3.6V			17.77			33.45	µA
			1.2V to 2V	1.65V to 3.6V			22.16			43.85	
I_{CCZA}	High-impedance state V_{CCA} supply current	V_I = V_{CCI} or GND I_O = 0, OE = GND	0.9V to 2V	1.65V to 3.6V			6.87			26.76	µA
I_{CCZB}	High-impedance state V_{CCB} supply current	V_I = V_{CCI} or GND I_O = 0, OE = GND	0.9V to 2V	1.65V to 3.6V			4.16			9.39	µA
C_i	Control Input Capacitance	OE	0.9V to 2V	1.65V to 3.6V			3.01			3.02	pF
C_{io}	Input-to-output internal capacitance	A port	0.9V to 2V	1.65V to 3.6V			4.71			6.57	pF
		B port	0.9V to 2V	1.65V to 3.6V			7.45			7.49	pF

(1) V_{CCI} is the V_{CC} associated with the input port
(2) V_{CCO} is the V_{CC} associated with the output port

10 Switching Characteristics, V_{CCA} = 0.9V

over recommended operating free-air temperature range, VCCA = 0.9V (unless otherwise noted)

PARAMETER		FROM	TO	TEST CONDITIONS	LOAD	B-Port Supply Voltage (V_{CCB})									UNIT
						1.8 ± 0.15V			2.5 ± 0.2V			3.3 ± 0.3V			
						MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PHL}	Propagation Delay (High-to-Low)	A	B	-40°C to 85°C	C_L =15pF	5.3		13.2	4.6		9.4	4.2		9.6	ns
				-40°C to 85°C	C_L =100pF	7		17.9	5.9		12.6	5.4		11.3	
				-40°C to 125°C	C_L =15pF	5.3		13.2	4.6		9.4	4.2		9.6	ns
				-40°C to 125°C	C_L =100pF	7		17.9	5.9		12.6	5.4		11.3	
t_{PLH}	Propagation Delay (Low-to-High)			-40°C to 85°C	C_L =15pF	5.9		15.1	5.2		10.7	4.8		10.6	ns
				-40°C to 85°C	C_L =100pF	7.8		18.9	6.8		13.6	6.2		12.4	
				-40°C to 125°C	C_L =15pF	5.9		15.1	5.2		10.7	4.8		10.6	ns
				-40°C to 125°C	C_L =100pF	7.8		18.9	6.8		13.6	6.2		12.4	
t_{PHL}	Propagation Delay (Hight-to-Low)	B	A	-40°C to 85°C	C_L =15pF	4.1		9.8	3.8		8.3	3.7		7.7	ns
				-40°C to 85°C	C_L =100pF	5.4		12.3	5.1		11	4.9		10.5	
				-40°C to 125°C	C_L =15pF	4.1		9.8	3.8		8.3	3.7		7.7	ns
				-40°C to 125°C	C_L =100pF	5.4		12.3	5.1		11	4.9		10.5	
t_{PLH}	Propagation Delay (Low-to-High)			-40°C to 85°C	C_L =15pF	4		8.8	3.7		7.6	3.6		7.3	ns
				-40°C to 85°C	C_L =100pF	5.4		11.3	5.1		10.2	5		9.9	
				-40°C to 125°C	C_L =15pF	4		8.8	3.7		7.6	3.6		7.3	ns
				-40°C to 125°C	C_L =100pF	5.4		11.3	5.1		10.2	5		9.9	
t_{DCW}	Direction Change Wait Time	A or B	B or A	-40°C to 125°C				40			37			37	ns
t_{en}	Enable Time	OE	B	-40°C to 125°C				590			591			654	ns
		OE	A	-40°C to 125°C				450			356			333	
t_{dis}	Disable Time	OE	B	-40°C to 125°C				101			102			103	ns
		OE	A	-40°C to 125°C				97			97			98	
t_{rA} ,t_{fA}	Ouput Rise/ Fall Time	B	A	-40°C to 85°C	C_L =15pF			0.9			1			1	ns
				-40°C to 85°C	C_L =100pF			7.8			7.8			7.9	ns
				-40°C to 125°C	C_L =15pF			1.1			1			1	ns
				-40°C to 125°C	C_L =100pF			7.8			7.8			7.9	ns

over recommended operating free-air temperature range, VCCA = 0.9V (unless otherwise noted)

PARAMETER		FROM	TO	TEST CONDITIONS	LOAD	B-Port Supply Voltage (V_{CCB})									UNIT
						1.8 ± 0.15V			2.5 ± 0.2V			3.3 ± 0.3V			
						MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{rB} ,t_{fB}	Ouput Rise/ Fall Time	A	B	-40°C to 85°C	C_L =15pF			2.8			2.3			1	ns
				-40°C to 85°C	C_L =100pF			11.8			8.2			7	ns
				-40°C to 125°C	C_L =15pF			2.8			2.3			1.5	ns
				-40°C to 125°C	C_L =100pF			14			9.9			8.9	ns
$t_{sk(o)}$	Channel-to-channel skew	A or B	B or A	-40°C to 125°C	C_L =15pF			0.64			0.62			0.61	ns
$Z_{OS,B}$	One-Shot Impedance	A or B	B or A	-40°C to 125°C			28			22			21		Ω
Data Rate	Maximum data rate	A or B	B or A	-40°C to 125°C	C_L =15pF (1)	46	93		48	100		40	86		Mbps
		A or B	B or A	-40°C to 125°C	C_L =100pF (1)	40	78		35	78		28	41		Mbps

(1) C_L is given as a lumped capacitance at the output.

11 Switching Characteristics, V_{CCA} = 1.2V ± 0.1V

over recommended operating free-air temperature range, VCCA = 1.2V ± 0.1V (unless otherwise noted)

PARAMETER		FROM	TO	TEST CONDITIONS	LOAD	B-Port Supply Voltage (V_{CCB})									UNIT
						1.8 ± 0.15V			2.5 ± 0.2V			3.3 ± 0.3V			
						MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PHL}	Propagation Delay (High-to-Low)	A	B	-40°C to 85°C	C_L =15pF	4.3		12.1	3.6		8.1	3.3		6.8	ns
				-40°C to 85°C	C_L =100pF	6		16.9	4.9		11.3	4.4		9.4	
				-40°C to 125°C	C_L =15pF	4.3		12.1	3.6		8.1	3.3		6.8	ns
				-40°C to 125°C	C_L =100pF	6		16.9	4.9		11.3	4.4		9.4	
t_{PLH}	Propagation Delay (Low-to-High)			-40°C to 85°C	C_L =15pF	4.6		13.6	3.9		9.1	3.5		7.6	ns
				-40°C to 85°C	C_L =100pF	6.6		17.4	5.5		12	4.9		10.1	
				-40°C to 125°C	C_L =15pF	4.6		13.6	3.9		9.1	3.5		7.6	ns
				-40°C to 125°C	C_L =100pF	6.6		17.4	5.5		12	4.9		10.1	
t_{PHL}	Propagation Delay (Hight-to-Low)	B	A	-40°C to 85°C	C_L =15pF	3.1		7.2	2.7		5.7	2.5		5.2	ns
				-40°C to 85°C	C_L =100pF	4.2		8.8	3.9		7.3	3.7		6.7	
				-40°C to 125°C	C_L =15pF	3.1		7.2	2.7		5.7	2.5		5.2	ns
				-40°C to 125°C	C_L =100pF	4.2		8.8	3.9		7.3	3.7		6.7	
t_{PLH}	Propagation Delay (Low-to-High)			-40°C to 85°C	C_L =15pF	2.9		6.7	2.6		5.4	2.5		4.8	ns
				-40°C to 85°C	C_L =100pF	4.2		8.5	3.9		7.1	3.7		6.7	
				-40°C to 125°C	C_L =15pF	2.9		6.7	2.6		5.4	2.5		4.8	ns
				-40°C to 125°C	C_L =100pF	4.2		8.5	3.9		7.1	3.7		6.7	
t_{DCW}	Direction Change Wait Time	A or B	B or A					40			30			27	ns
t_{en}	Enable Time	OE	B	-40°C to 125°C				472			437			433	ns
		OE	A	-40°C to 125°C				414			320			298	
t_{dis}	Disable Time	OE	B	-40°C to 125°C				100			101			102	ns
		OE	A	-40°C to 125°C				97			97			98	
t_{rA} ,t_{fA}	Ouput Rise/ Fall Time	B	A	-40°C to 85°C	C_L =15pF			0.9			0.9			0.9	ns
					C_L =100pF			6.8			6.9			7	
				-40°C to 125°C	C_L =15pF			0.9			1.1			1.1	
					C_L =100pF			6.8			6.9			7	

over recommended operating free-air temperature range, VCCA = 1.2V ± 0.1V (unless otherwise noted)

PARAMETER		FROM	TO	TEST CONDITIONS	LOAD	B-Port Supply Voltage (V_{CCB})									UNIT
						1.8 ± 0.15V			2.5 ± 0.2V			3.3 ± 0.3V			
						MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{rB} ,t_{fB}	Ouput Rise/ Fall Time	A	B	-40°C to 85°C	C_L =15pF			2.8			2.4			1	ns
					C_L =100pF			11.8			8.2			7	
				-40°C to 125°C	C_L =15pF			2.8			2.4			1.5	
					C_L =100pF			14			9.9			8.9	
$t_{sk(o)}$	Channel-to-channel skew	A or B	B or A	-40°C to 125°C	C_L =15pF			0.27			0.22			0.22	ns
$Z_{OS,A}$	One-Shot Impedance	A or B	B or A				28			22			21		Ω
Data Rate	Maximum data rate	A or B	B or A		C_L =15pF (1)	99	136		129	139		130	141		Mbps
		A or B	B or A		C_L =100pF (1)	69	99		99	112		99	106		Mbps

(1) C_L is given as a lumped capacitance at the output.

12 Switching Characteristics, V_{CCA} = 1.5V ± 0.1V

over recommended operating free-air temperature range, VCCA = 1.5V ± 0.1V (unless otherwise noted)

PARAMETER		FROM	TO	TEST CONDITIONS	LOAD	B-Port Supply Voltage (V_{CCB})									UNIT
						1.8 ± 0.15V			2.5 ± 0.2V			3.3 ± 0.3V			
						MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PHL}	Propagation Delay (High-to-Low)	A	B	-40°C to 85°C	C_L =15pF	4.1		11.5	3.4		7.4	3		6.1	ns
				-40°C to 85°C	C_L =100pF	5.8		16.3	4.7		10.6	4.2		8.6	
				-40°C to 125°C	C_L =15pF	4.1		11.5	3.4		7.4	3		6.1	ns
				-40°C to 125°C	C_L =100pF	5.8		16.3	4.7		10.6	4.2		8.6	
t_{PLH}	Propagation Delay (Low-to-High)			-40°C to 85°C	C_L =15pF	4.4		12.8	3.7		8.2	3.2		6.7	ns
				-40°C to 85°C	C_L =100pF	6.3		16.6	5.2		11.1	4.6		9.1	
				-40°C to 125°C	C_L =15pF	4.4		12.8	3.7		8.2	3.2		6.7	ns
				-40°C to 125°C	C_L =100pF	6.3		16.6	5.2		11.1	4.6		9.1	
t_{PHL}	Propagation Delay (Hight-to-Low)	B	A	-40°C to 85°C	C_L =15pF	2.9		6.4	2.5		4.8	2.3		4.2	ns
				-40°C to 85°C	C_L =100pF	4.1		7.9	3.7		6.3	3.5		5.7	
				-40°C to 125°C	C_L =15pF	2.9		6.4	2.5		4.8	2.3		4.2	ns
				-40°C to 125°C	C_L =100pF	4.1		7.9	3.7		6.3	3.5		5.7	
t_{PLH}	Propagation Delay (Low-to-High)			-40°C to 85°C	C_L =15pF	2.7		6	2.4		4.6	2.3		4.1	ns
				-40°C to 85°C	C_L =100pF	4		7.6	3.7		6.2	3.5		5.7	
				-40°C to 125°C	C_L =15pF	2.7		6	2.4		4.6	2.3		4.1	ns
				-40°C to 125°C	C_L =100pF	4		7.6	3.7		6.2	3.5		5.7	
t_{DCW}	Direction Change Wait Time	A or B	B or A	-40°C to 125°C	C_L =15pF			40			30			27	ns
t_{en}	Enable Time	OE	B	-40°C to 125°C				390			361			353	ns
			A	-40°C to 125°C				409			314			292	
t_{dis}	Disable Time		B	-40°C to 125°C				99			100			101	
			A	-40°C to 125°C				96			97			97	
t_{rA} ,t_{fA}	Ouput Rise/ Fall Time	B	A	-40°C to 85°C	C_L =15pF			0.9			0.9			0.9	ns
				-40°C to 85°C	C_L =100pF			6.6			6.7			6.8	
				-40°C to 125°C	C_L =15pF			0.9			0.9			0.9	
				-40°C to 125°C	C_L =100pF			6.6			6.7			6.8	

over recommended operating free-air temperature range, VCCA = 1.5V ± 0.1V (unless otherwise noted)

PARAMETER		FROM	TO	TEST CONDITIONS	LOAD	B-Port Supply Voltage (V_{CCB})									UNIT
						1.8 ± 0.15V			2.5 ± 0.2V			3.3 ± 0.3V			
						MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{rB} ,t_{fB}	Ouput Rise/ Fall Time	A	B	-40°C to 85°C	C_L =15pF			2.8			2.4			1	ns
				-40°C to 85°C	C_L =100pF			14.0			9.9			8.9	
				-40°C to 125°C	C_L =15pF			2.8			2.4			1.5	
				-40°C to 125°C	C_L =100pF			14.0			9.9			8.9	
$t_{sk(o)}$	Channel-to-channel skew	A or B	B or A					0.6			0.6			0.6	ns
$Z_{OS,A}$	One-Shot Impedance	A or B	A or B				28			22			21		Ω
Data Rate	Maximum data rate	A or B	B or A	C_L =15pF (1)		115	139		126	141		133	142		Mbps
		A or B	B or A	C_L =100pF (1)		90	99		90	115		90	115		Mbps

(1) C_L is given as a lumped capacitance at the output.

13 Switching Characteristics, V_{CCA} = 1.8V ± 0.15V

over recommended operating free-air temperature range, VCCA = 1.8V ± 0.15V (unless otherwise noted)

PARAMETER		FROM	TO	TEST CONDITIONS	LOAD	B-Port Supply Voltage (V_{CCB})									UNIT
						1.8 ± 0.15V			2.5 ± 0.2V			3.3 ± 0.3V			
						MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PHL}	Propagation Delay (High-to-Low)	A	B	-40°C to 85°C	C_L =15pF	4		11.3	3.3		7.2	2.9		5.8	ns
				-40°C to 85°C	C_L =100pF	5.7		16	4.6		10.4	4.1		8.3	
				-40°C to 125°C	C_L =15pF	4.4		11.6	3.3		7.2	2.9		5.8	ns
				-40°C to 125°C	C_L =100pF	5.7		16	4.6		10.4	4.1		8.3	
t_{PLH}	Propagation Delay (Low-to-High)			-40°C to 85°C	C_L =15pF	4.2		12.4	3.5		7.9	3.1		6.3	ns
				-40°C to 85°C	C_L =100pF	6.2		16.3	5		10.8	4.5		8.8	
				-40°C to 125°C	C_L =15pF	4.2		12.4	3.5		7.9	3.1		6.3	ns
				-40°C to 125°C	C_L =100pF	6.2		16.3	5		10.8	4.5		8.8	
t_{PHL}	Propagation Delay (Hight-to-Low)	B	A	-40°C to 85°C	C_L =15pF	2.8		6.3	2.4		4.6	2.2		3.9	ns
				-40°C to 85°C	C_L =100pF	4		7.8	3.6		6	3.4		5.4	
				-40°C to 125°C	C_L =15pF	2.8		6.3	2.4		4.6	2.2		3.9	ns
				-40°C to 125°C	C_L =100pF	4		7.8	3.6		6	3.4		5.4	
t_{PLH}	Propagation Delay (Low-to-High)			-40°C to 85°C	C_L =15pF	2.7		5.8	2.3		4.4	2.2		3.8	ns
				-40°C to 85°C	C_L =100pF	3.9		7.4	3.6		5.9	3.4		5.3	
				-40°C to 125°C	C_L =15pF	2.7		5.8	2.3		4.4	2.0		3.8	ns
				-40°C to 125°C	C_L =100pF	3.9		7.4	3.6		5.9	3.4		5.3	
t_{DCW}	Direction Change Wait Time	A or B	B or A					40			30			27	ns
t_{en}	Enable Time	OE	A or B	-40°C to 125°C				354			324			318	ns
			A or B	-40°C to 125°C				408			313			290	
t_{dis}	Disable Time		A or B	-40°C to 125°C				99			100			100	
			A or B	-40°C to 125°C				95			97			97	
t_{rA} ,t_{fA}	Ouput Rise/ Fall Time	B	A	-40°C to 85°C	C_L =15pF			0.8			0.8			0.8	ns
				-40°C to 85°C	C_L =100pF			6.6			6.7			6.7	
				-40°C to 125°C	C_L =15pF			1.1			1.1			1.1	
				-40°C to 125°C	C_L =100pF			6.6			6.7			6.7	

over recommended operating free-air temperature range, VCCA = 1.8V ± 0.15V (unless otherwise noted)

PARAMETER		FROM	TO	TEST CONDITIONS	LOAD	B-Port Supply Voltage (V_{CCB})									UNIT
						1.8 ± 0.15V			2.5 ± 0.2V			3.3 ± 0.3V			
						MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{rB} ,t_{fB}	Ouput Rise/ Fall Time	A	B	-40°C to 85°C	C_L =15pF			2.8			2.4			1	ns
				-40°C to 85°C	C_L =100pF			11.8			8.2			7	
				-40°C to 125°C	C_L =15pF			2.8			2.4			1.5	
				-40°C to 125°C	C_L =100pF			14.0			9.9			8.9	
$t_{sk(o)}$	Channel-to-channel skew	A or B	B or A	-40°C to 125°C	C_L =15pF			0.6			0.6			0.6	ns
$Z_{OS,A}$	One-Shot Impedance	A or B	A or B				28			22			21		Ω
Data Rate	Maximum data rate	A or B	B or A	C_L =15pF (1)		120	160		139	190		138	146		Mbps
		A or B	B or A	C_L =100pF (1)		80	102		90	120		109	127		Mbps

(1) C_L is given as a lumped capacitance at the output.

14 Switching Characteristics: T_{MAX} (-40°C to 125°C)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CCI}	V_{CCO}	Operating free-air temperature (T_A)			UNIT
					-40°C to 125°C			
					MIN	TYP	MAX	
T_{MAX} - Maximum Data Rate	50% Duty Cycle Input 20% of pulse > 0.7*V_{CCO} 20% of pulse < 0.3*V_{CCO}	TX Line: 20-inch + 50pF Cload	0.9V	1.8 ± 0.15V	63	84		Mbps
			0.9V	2.5 ± 0.2V	62	89		Mbps
			0.9V	3.3 ± 0.3V	39	87		Mbps
			1.2V ± 0.1V	1.8 ± 0.15V	70	101		Mbps
			1.2V ± 0.1V	2.5 ± 0.2V	96	147		Mbps
			1.2V ± 0.1V	3.3 ± 0.3V	100	145		Mbps
			1.5V ± 0.1V	1.8 ± 0.15V	71	102		Mbps
			1.5V ± 0.1V	2.5 ± 0.2V	99	148		Mbps
			1.5V ± 0.1V	3.3 ± 0.3V	100	148		Mbps
			1.8 ± 0.15V	1.8 ± 0.15V	73	104		Mbps
			1.8 ± 0.15V	2.5 ± 0.2V	100	153		Mbps
			1.8 ± 0.15V	3.3 ± 0.3V	124	171		Mbps

15 Operating Characteristics

PARAMETER		TEST CONDITIONS	VCCA	VCCB	MAX	UNIT
C_{pdA}	A-port input, B-port output to B: outputs enabled	C_L = 0. f= 10MHz, t_r = t_f = 1ns, OE = V_{CCA} (outputs enabled)	0.9V	1.8V	11.29	pF
	B-port input, A-port output to B: outputs enabled		0.9V	1.8V	17.2	
C_{pdB}	A-port input, B-port output to B: outputs enabled		0.9V	1.8V	22.74	
	B-port input, A-port output to B: outputs enabled		0.9V	1.8V	12.39	
C_{pdA}	A-port input, B-port output to B: outputs disabled	C_L = 0. f= 10MHz, t_r = t_f = 1ns, OE = GND (outputs disabled)	0.9V	1.8V	0.01	pF
	B-port input, A-port output to B: outputs disabled		0.9V	1.8V	0.01	
C_{pdB}	A-port input, B-port output to B: outputs disabled		0.9V	1.8V	0.01	
	B-port input, A-port output to B: outputs disabled		0.9V	1.8V	0.02	
C_{pdA}	A-port input, B-port output to B: outputs enabled	C_L = 0. f= 10MHz, t_r = t_f = 1ns, OE = V_{CCA} (outputs enabled)	1.2V	1.8V	13.17	pF
	B-port input, A-port output to B: outputs enabled		1.2V	1.8V	17.87	
C_{pdB}	A-port input, B-port output to B: outputs enabled		1.2V	1.8V	22.76	
	B-port input, A-port output to B: outputs enabled		1.2V	1.8V	11.66	
C_{pdA}	A-port input, B-port output to B: outputs disabled	C_L = 0. f= 10MHz, t_r = t_f = 1ns, OE = GND (outputs disabled)	1.2V	1.8V	0.01	pF
	B-port input, A-port output to B: outputs disabled		1.2V	1.8V	0.01	
C_{pdB}	A-port input, B-port output to B: outputs disabled		1.2V	1.8V	0.01	
	B-port input, A-port output to B: outputs disabled		1.2V	1.8V	0.02	

PARAMETER		TEST CONDITIONS	VCCA	VCCB	MAX	UNIT
C_{pdA}	A-port input, B-port output to B: outputs enabled	C_L = 0. f= 10MHz, t_r = t_f = 1ns, OE = V_{CCA} (outputs enabled)	1.8V	2.5V	12.42	pF
	B-port input, A-port output to B: outputs enabled		1.8V	2.5V	19.51	
C_{pdB}	A-port input, B-port output to B: outputs enabled		1.8V	2.5V	25.18	
	B-port input, A-port output to B: outputs enabled		1.8V	2.5V	11.98	
C_{pdA}	A-port input, B-port output to B: outputs disabled	C_L = 0. f= 10MHz, t_r = t_f = 1ns, OE = GND (outputs disabled)	1.8V	2.5V	0.02	pF
	B-port input, A-port output to B: outputs disabled		1.8V	2.5V	0.01	
C_{pdB}	A-port input, B-port output to B: outputs disabled		1.8V	2.5V	0.01	
	B-port input, A-port output to B: outputs disabled		1.8V	2.5V	0.03	
C_{pdA}	A-port input, B-port output to B: outputs disabled	C_L = 0. f= 10MHz, t_r = t_f = 1ns, OE = V_{CCA} (outputs enabled)	2V	3.3V	11.95	pF
	B-port input, A-port output to B: outputs disabled		2V	3.3V	20.17	
C_{pdB}	A-port input, B-port output to B: outputs disabled		2V	3.3V	29.22	
	B-port input, A-port output to B: outputs disabled		2V	3.3V	12.57	
C_{pdA}	A-port input, B-port output to B: outputs disabled	C_L = 0. f= 10MHz, t_r = t_f = 1ns, OE = GND (outputs disabled)	2V	3.3V	0.03	pF
	B-port input, A-port output to B: outputs disabled		2V	3.3V	0.01	
C_{pdB}	A-port input, B-port output to B: outputs disabled		2V	3.3V	0.01	
	B-port input, A-port output to B: outputs disabled		2V	3.3V	0.03	

16 Typical Characteristics

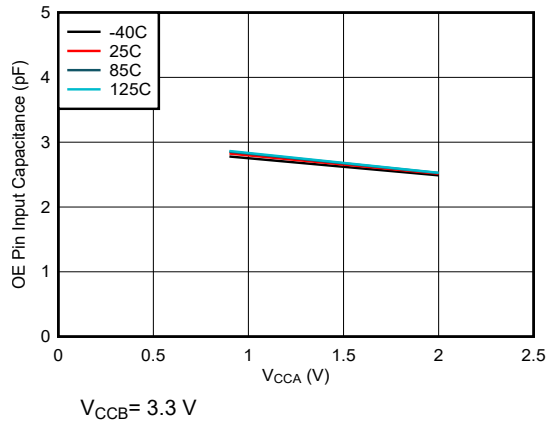


Figure 16-1. Input Capacitance for OE Pin (C_I) vs Power Supply (V_{CCA})

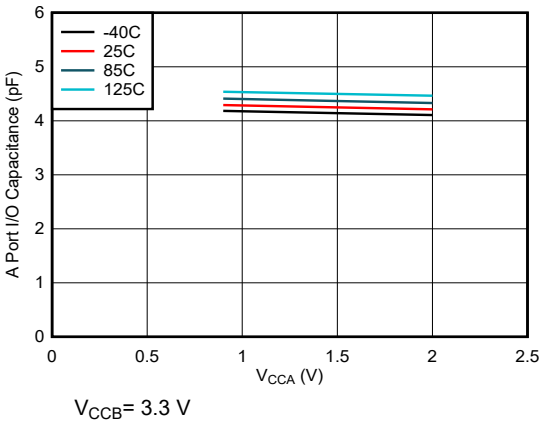


Figure 16-2. Capacitance for A port I/O Pins (C_{iO}) vs Power Supply (V_{CCA})

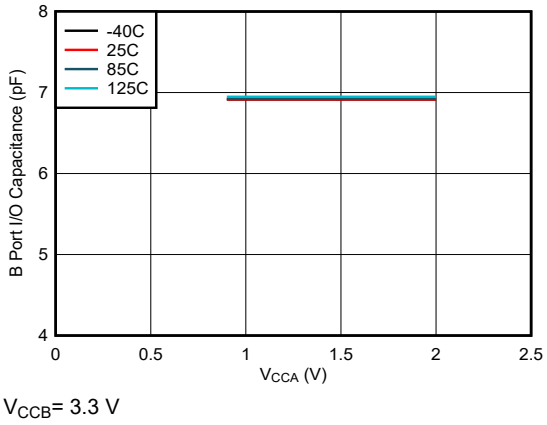


Figure 16-3. Capacitance for B Port I/O Pins (C_{iO}) vs Power Supply (V_{CCB})

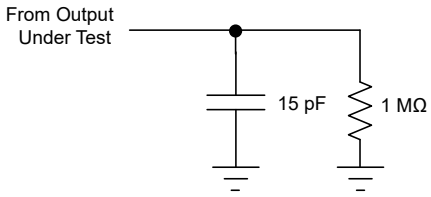
17 Parameter Measurement Information

Unless otherwise noted, all input pulses are supplied by generators that have the following characteristics:

- PRR 10MHz
- Z_O = 50W
- dv/dt ≥ 1V/ns

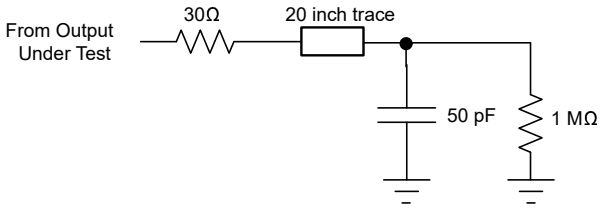
Note

All parameters and waveforms are not applicable to all devices.



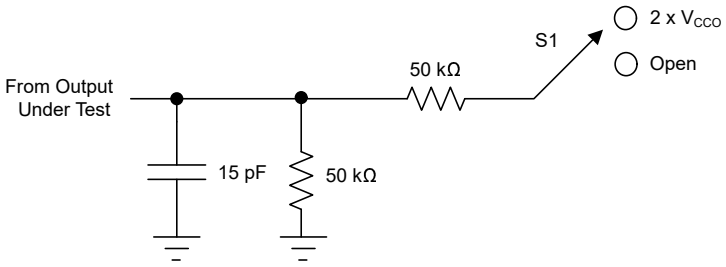
A. The outputs are measured one at a time, with one transition per measurement.

Figure 17-1. Lumped Capacitive Load Circuit For Maximum Data Rate & Propagation Delay, Output Rise, And Fall Time Measurement



A. The outputs are measured one at a time, with one transition per measurement.

Figure 17-2. Long Trace + Capacitive Load Circuit For Maximum Data Rate



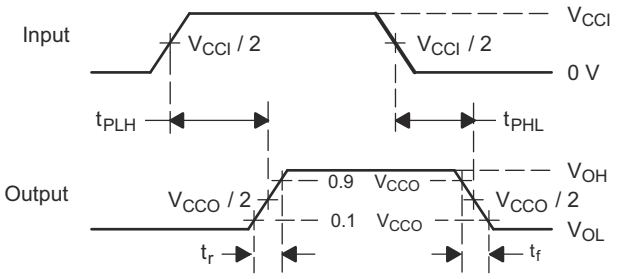
A. The outputs are measured one at a time, with one transition per measurement.

Figure 17-3. Load Circuit For Enable and Disable Time Measurement

Table 17-1. Switch Position For Enable and Disable Time Measurement

TEST(1)	S1
t_{PZL}, t_{PLZ}	2 × V_{CCO}
t_{PHZ}, t_{PZH}	Open

(1) See *Figure 17-3*.



A. V_{CCI} is the V_{CC} associated with the input port.
B. V_{CCO} is the V_{CC} associated with the output port.
C. t_{PLH} and t_{PHL} are the same as t_{pd}.
D. The outputs are measured one at a time, with one transition per measurement.

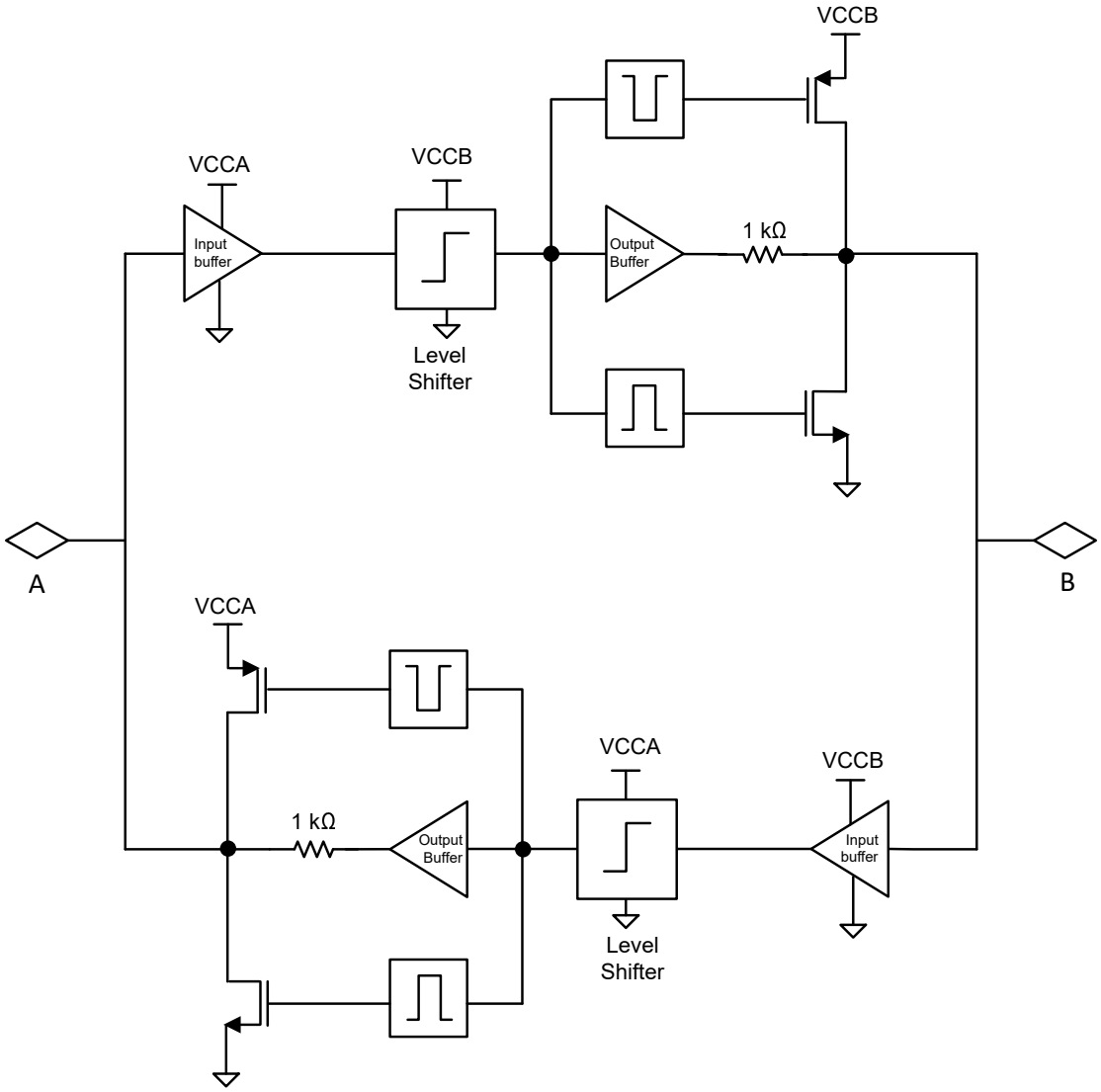
Figure 17-4. Voltage Waveforms Propagation Delay Times

18 Detailed Description

18.1 Overview

The TXB0606 device is a 6-bit, bidirectional voltage-level translator with auto-direction sensing specifically designed for translating logic voltage levels. The A port is able to accept I/O voltages ranging from 0.9V to 2V, while the B port can accept I/O voltages from 1.65V to 3.6V. The device is a buffered architecture with edge-rate accelerators (one-shots) to improve the overall data rate. This device can only translate push-pull CMOS logic outputs. If for open-drain signal translation, please refer to TI's TXS010X products.

18.2 Functional Block Diagram



18.3 Feature Description

18.3.1 Architecture

The TXB0606 architecture (see Figure 18-1) does not require a direction-control signal to control the direction of data flow from A to B or from B to A. In a DC state, the output drivers of the device maintain a high or low, but are designed to be weak, so the output drivers can be overdriven by an external driver when data on the bus flows the opposite direction.

The output one-shots detect rising or falling edges on the A or B ports. During a rising edge, the one-shot turns on the PMOS transistors (T1, T3) for a short duration, which speeds up the low-to-high transition. Similarly, during a falling edge, the one-shot turns on the NMOS transistors (T2, T4) for a short duration, which speeds up the high-to-low transition. The typical output impedance during output transition is 28Ω at V_{CCO} = 1.8V , 22Ω at V_{CCO} = 2.5V, and 21Ω at V_{CCO} = 2.5V.

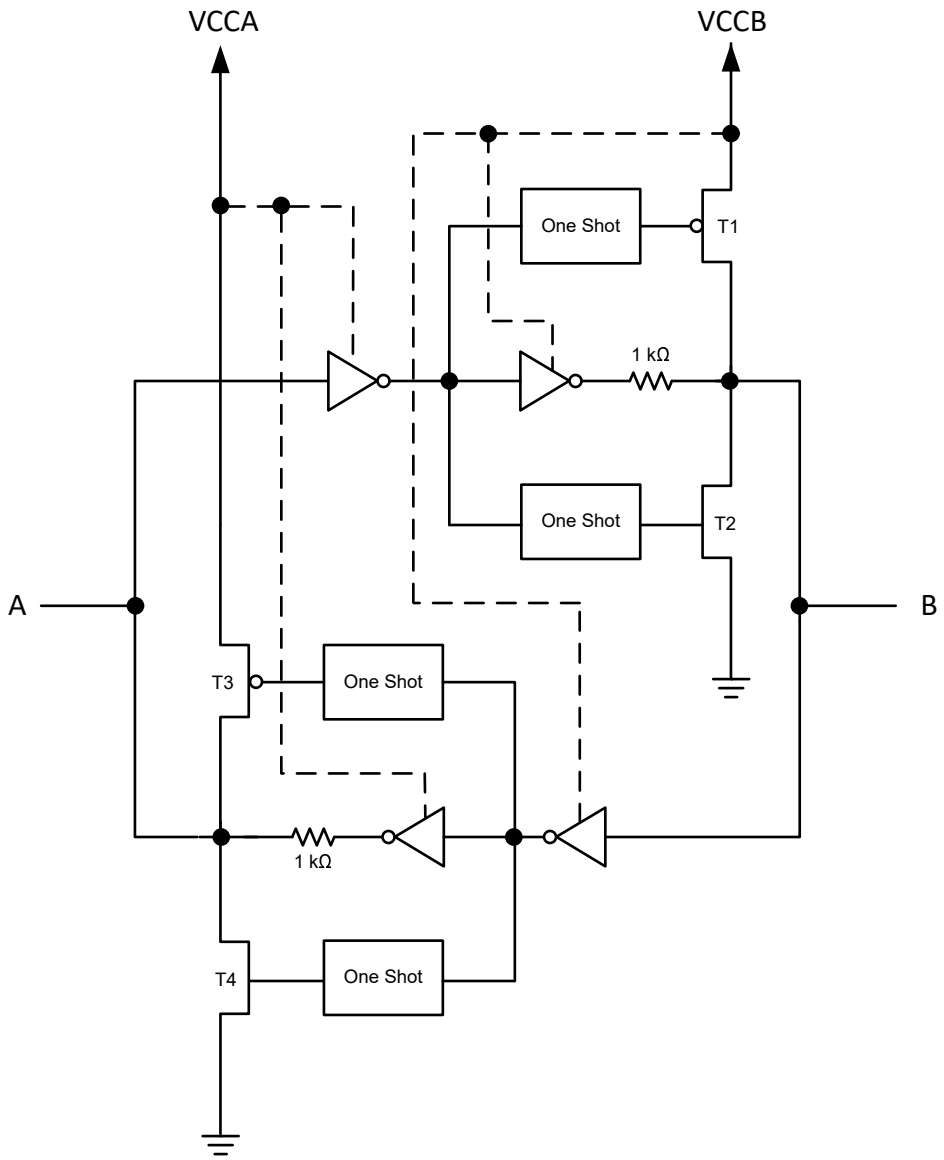
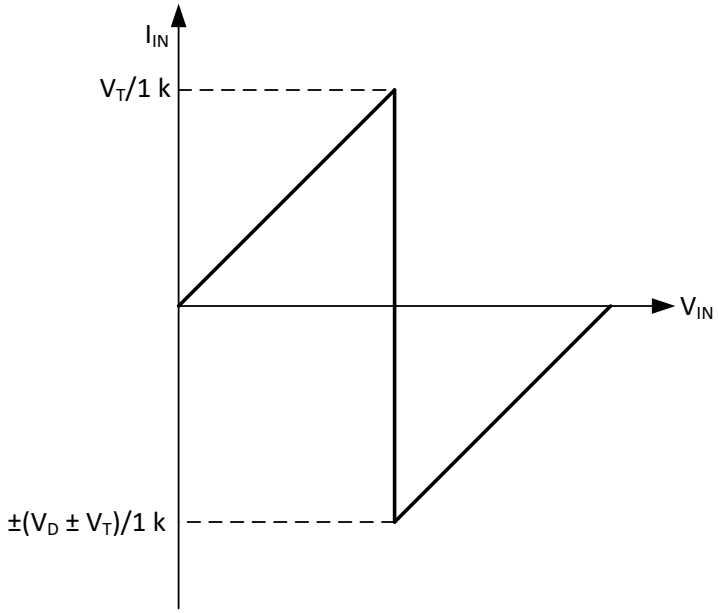


Figure 18-1. Architecture of TXB0606 Device I/O Cell

18.3.2 Input Driver Requirements

Typical I_{IN} vs V_{IN} characteristics of the TXB0606 are shown in Figure 18-2. For proper operation, the device driving the data I/Os of the TXB0606 must have drive strength of at least ± 3mA.



A. V_T is the input threshold voltage of the TXB0606 (typically $V_{CCI}/2$).
B. V_D is the supply voltage of the external driver.

Figure 18-2. Typical I_{IN} vs V_{IN} Curve

18.3.3 Output Load Considerations

TI recommends following careful PCB layout practices to minimize signal distortion and ringing. Impedance matching techniques muat be implemented to reduce output oscillations and ensure signal integrity. Improper impedance matching can result in reflections that introduce overshoot and undershoot on signal transitions. Series termination resistors are recommended at the device outputs to match the total output impedance to the transmission line.

For example, given that the device output impedance is 21Ω (V_{CCA} = 0.9 to 2V and V_{CCB} = 3.3V), adding a series resistor value of 30Ω provides an effective source impedance close to 50Ω, matching a typical controlled-impedance trace or cable.

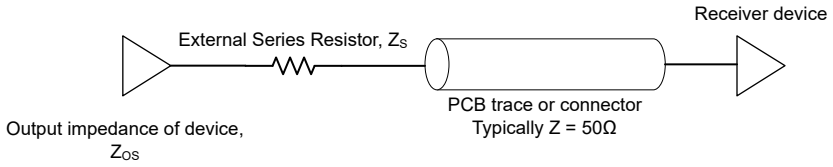


Figure 18-3. Source Termination for Impedance Matching

18.3.4 Enable and Disable

The TXB0606 has an OE input that is used to disable the device by setting OE = low, which places all I/Os in the high-impedance (Hi-Z) state. The disable time (t_{dis}) indicates the delay between when OE goes low and when the outputs actually get disabled (Hi-Z). The enable time (t_{en}) indicates the amount of time the user must allow for the one-shot circuitry to become operational after OE is taken high.

18.3.5 Pullup or Pulldown Resistors on I/O Lines

The device is designed to support high-drive applications with either a lumped capacitive load of up to 100pF or a signal trace length of up to 20 inches with a 50pF load. The output drivers of the TXB0606 device have low DC drive strength. If pullup or pulldown resistors are connected externally to the data I/Os, their values must be kept higher than 20kΩ to ensure that they do not contend with the output drivers of the TXB0606 device.

For the same reason, the TXB0606 device must not be used in applications such as I^2C or 1-Wire where an open-drain driver is connected on the bidirectional data I/O. For these applications, use a device from the TI TXS series of level translators.

18.3.6 Dummy Cycles

When TXB0606 is used in Quad-SPI (QSPI) interfaces between a microcontroller and serial flash memory, the direction of the data flow can change dynamically between the controller and the memory device. Given the TXB0606 features automatic direction sensing, a minimum turn-around time of 40ns is required for the device to transition from one direction to the other. This is shown under the Switching Characteristics table as t_{DCW} - Direction Change Wait Time.

The ensure proper bus timing, the QSPI controller must insert sufficient dummy clock cycles after the command and address phase before data is sampled from the flash memory. The total dummy period must be greater or equal to the TXB0606 turn-around time of 40ns.

As an example, at a QSPI clock frequency of 104MHz:

$$1/104MHz \quad = \quad 9.6ns \tag{1}$$

$$40ns/9.6ns \quad = \quad 4.16ns \quad \rightarrow \quad 5 \quad dummy \quad cycles \tag{2}$$

Many flash devices, such as the ISSI IS25LQ040B, specificy 8 dummy cycles at 104MHz frequency, which satisfies the TXB0606 requirement and provides additional margin.

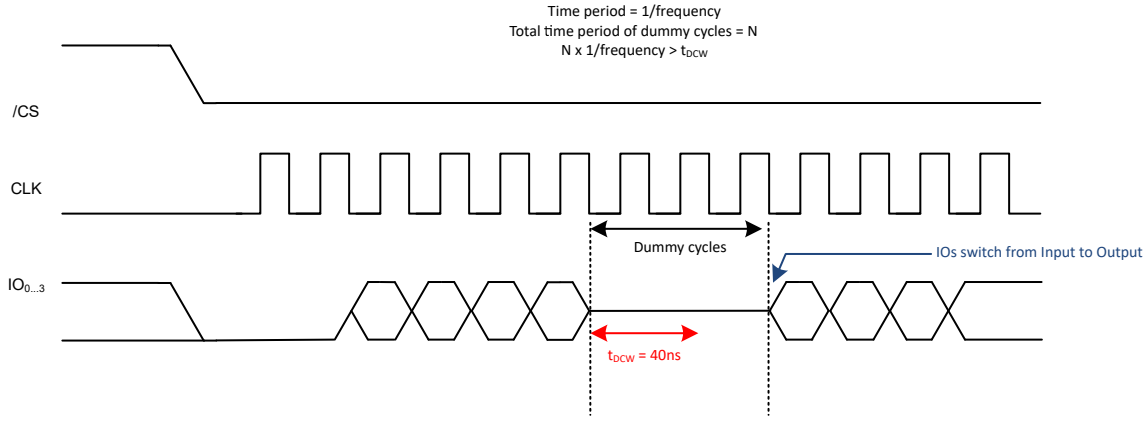


Figure 18-4. QSPI Dummy Clock Cycles to meet TXB0606 Direction-Change Timing

18.4 Device Functional Modes

The device has two functional modes, enabled and disabled. To disable the device, set the OE input to low, which places all I/Os in a high impedance state. Setting the OE input to high will enable the device.

19 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

19.1 Application Information

The TXB0606 device can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another. It can only translate push-pull CMOS logic outputs. If for open-drain signal translation, please refer to TI TXS010X products. Any external pulldown or pullup resistors are recommended larger than 20kΩ.

The device features enhanced output drive strength for use in high-speed interfaces such as QSPI, OSPI, eSPI, etc. The device is designed to support high-drive applications with either a lumped capacitive load of up to 100pF at 109Mbps (1.8 to 3.3V translation) or a signal trace length of up to 20 inches with a 50pF load at 124Mbps (1.8 to 3.3V translation).

19.2 Typical Application

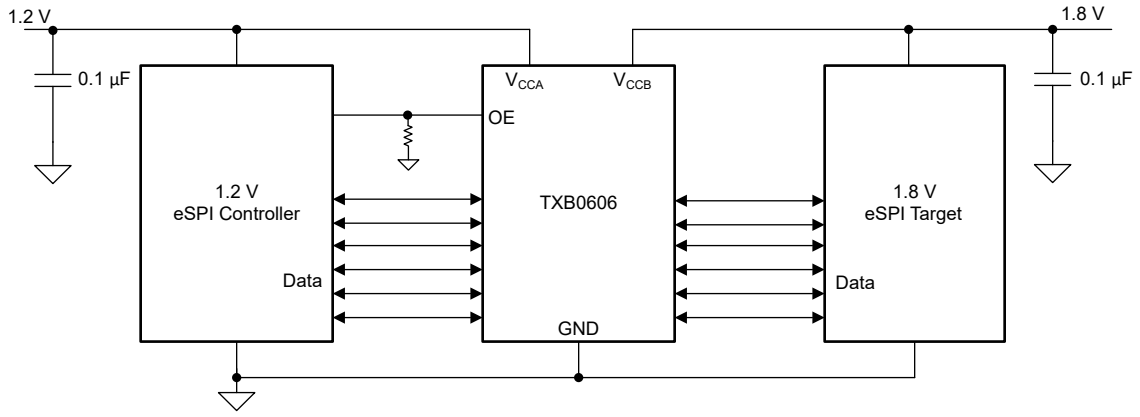


Figure 19-1. Typical Operating Circuit

19.2.1 Design Requirements

For this design example, use the parameters listed in Table 19-1.

Table 19-1. Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUE
Input voltage range	0.9V to 2V
Output voltage range	1.65V to 3.6V

19.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Series resistor at the device outputs
  - Series resistors must be placed at the device outputs to improve signal integrity and to match the total output impedance to the external transmission path. For example, given that the device output impedance is 21Ω, a 30Ω series resistor provides an effective source impedance close to 50Ω, matching a typical controlled-impedance PCB trace or cable connection.
- Input voltage range

– Use the supply voltage of the device that is driving the TXB0606 device to determine the input voltage range. For a valid logic high, the value must exceed the V_{IH} of the input port. For a valid logic low, the value must be less than the V_{IL} of the input port.

- An external pulldown or pullup resistor decreases the output V_{OH} and V_{OL}. Use the below equations to draft estimate the V_{OH} and V_{OL} as a result of an external pulldown and pullup resistor.

$$V_{OH} = V_{CCx} \times R_{PD} / (R_{PD} + 1.5k\Omega) \quad (3)$$

$$V_{OL} = V_{CCx} \times 1.5k\Omega / (R_{PU} + 1.5k\Omega) \quad (4)$$

Where

- V_{CCx} is the output port supply voltage on either V_{CCA} or V_{CCB}
- R_{PD} is the value of the external pull down resistor
- R_{PU} is the value of the external pull up resistor
- 1.5kΩ is the counting the variation of the serial resistor 1kΩ in the I/O line.

19.2.3 Application Curves

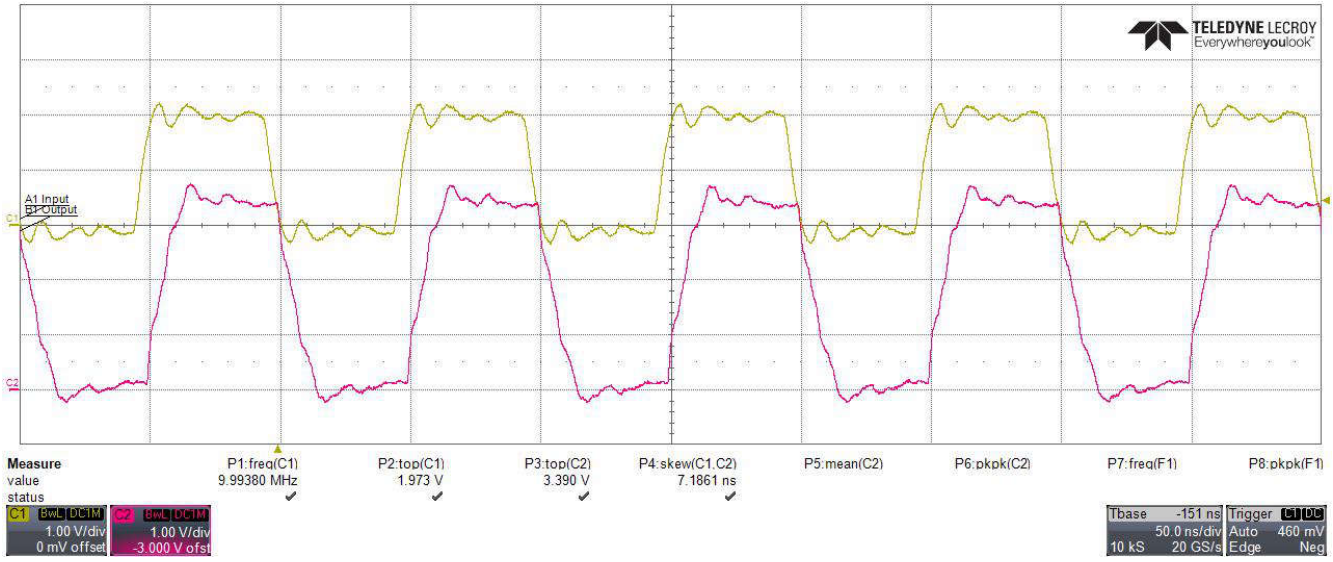


Figure 19-2. Level-Translation of a 10MHz Signal (V_{CCA} = 1.8V, V_{CCB} = 3.6V, C_L= 20inch + 50pF)

19.3 Power Supply Recommendations

During power-up sequencing, $V_{CCA} \geq V_{CCB}$ does not damage the device, so any power supply can be ramped up first. Please ensure that $V_{CCA/B}$ is powered on before the I/O ports.

The output-enable (OE) input circuit is designed so that it is supplied by V_{CCA} and when the (OE) input is low, all outputs are placed in the high-impedance state. To ensure the high-impedance state of the outputs during power up or power down, the OE input pin must be tied to GND through a pulldown resistor and must not be enabled until V_{CCA} and V_{CCB} are fully ramped and stable. The minimum value of the pulldown resistor to ground is determined by the current-sourcing capability of the driver.

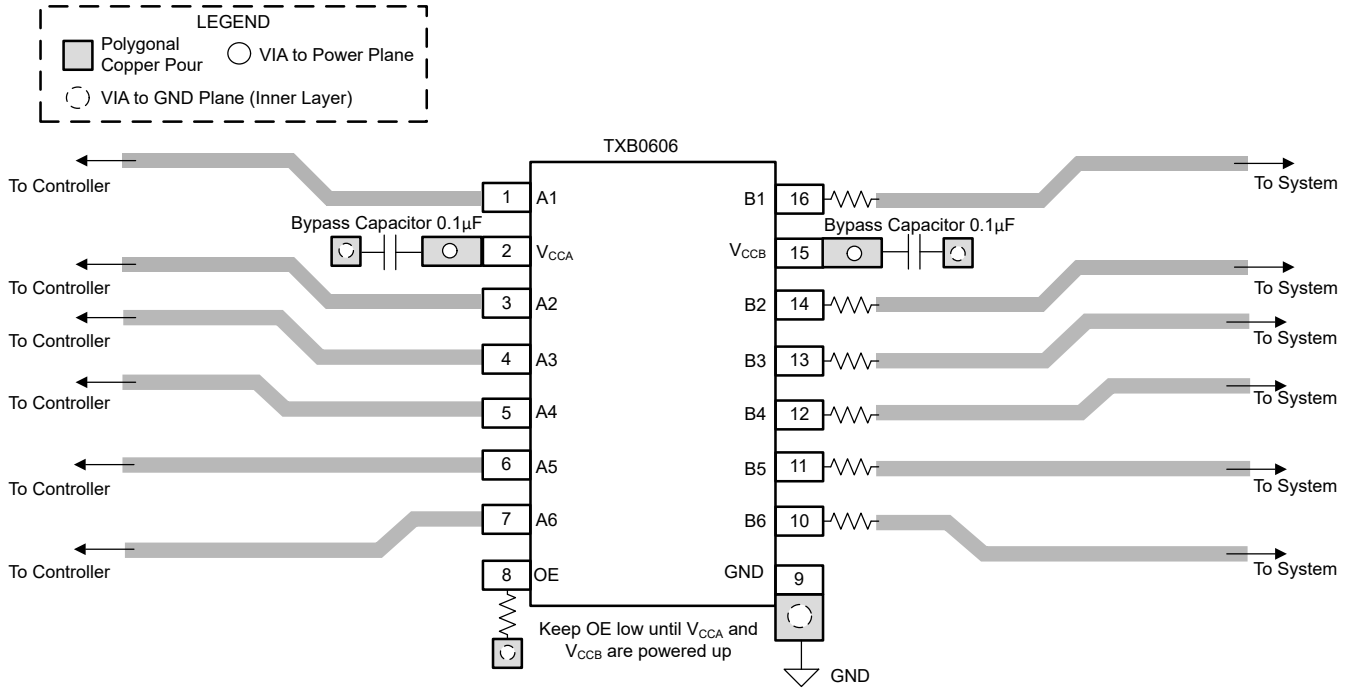
19.4 Layout

19.4.1 Layout Guidelines

To ensure reliability of the device, following common printed-circuit board layout guidelines is recommended.

- The TXB0606 provides bidirectional level translation with symmetrical drive strength on both ports. Therefore, device placement between the host and target is not critical, provided the capacitive load on either side remains within the specified 100pF limit.
- Bypass capacitors must be used on power supplies, and must be placed as close as possible to the V_{CCA}, V_{CCB} pin and GND pin.
- Series resistors must be placed at the device outputs to improve signal integrity and match the total output impedance to the external transmission path. For example, given that the device output impedance is 21Ω, a 30Ω series resistor provides an effective source impedance close to 50Ω, matching a typical controlled-impedance PCB trace or cable connection.
- During operation, the data direction changes dynamically between the host and the target device. A direction-change delay (t_{DCW}) must be provided before the bus switches direction between the host and target device. Ensure that the delay between direction changes meets the t_{DCW} requirement listed in the Switching Characteristics table. In QSPI applications, this delay corresponds to dummy clock cycles inserted between the command/address and data phases to satisfy the required turn-around time.

19.4.2 Layout Example



20 Device and Documentation Support

20.1 Documentation Support

20.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *A Guide to Voltage Translation With TXB-Type Translators*
- Texas Instruments, *Overcoming TXB-Type Translators Design Challenges*
- Texas Instruments, *From Bottleneck to Breakthrough: QSPI Optimization in Data Centers with TXB0604/TXB0606*

20.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

20.3 Trademarks

All trademarks are the property of their respective owners.

20.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

20.5 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

21 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
May 2026	*	Initial Release

22 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TXB0606PWR	Active	Production	TSSOP (PW) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TXB606

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

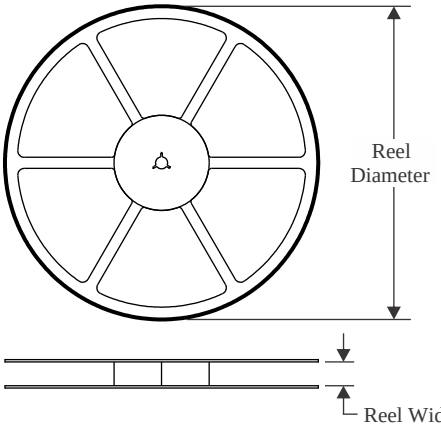
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

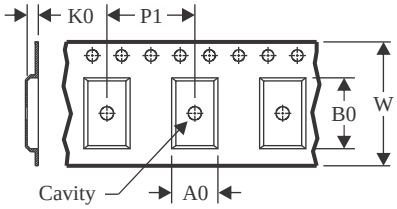
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

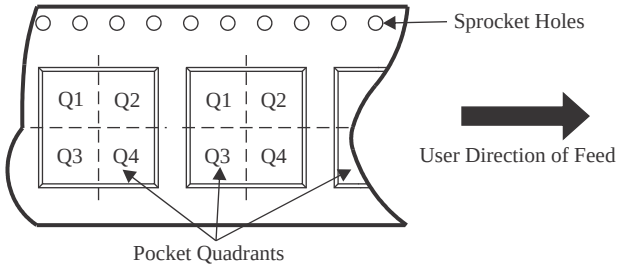


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

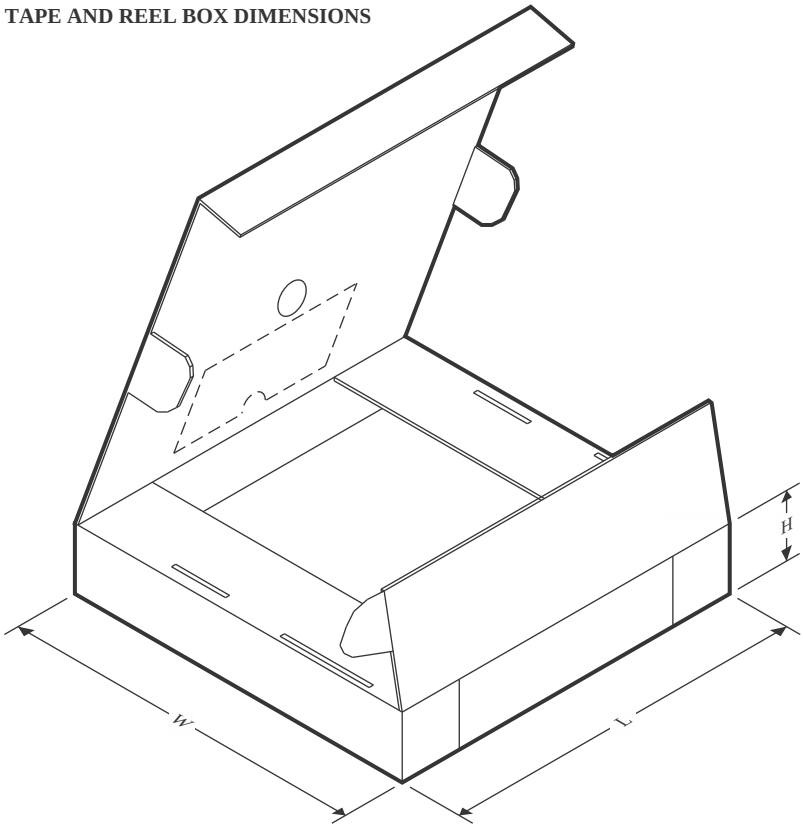
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TXB0606PWR	TSSOP	PW	16	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

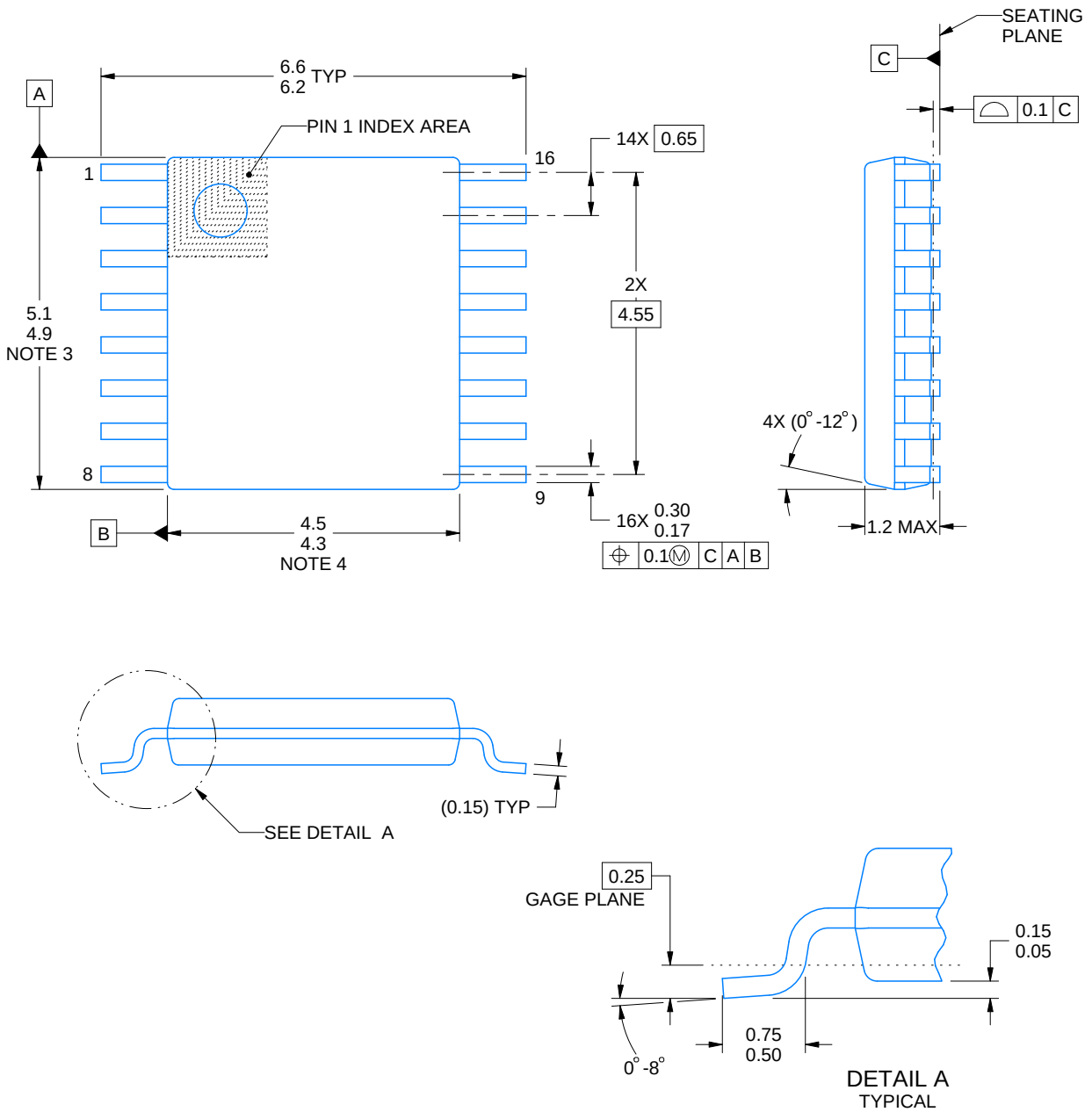
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TXB0606PWR	TSSOP	PW	16	3000	353.0	353.0	32.0

PACKAGE OUTLINE

PW0016A

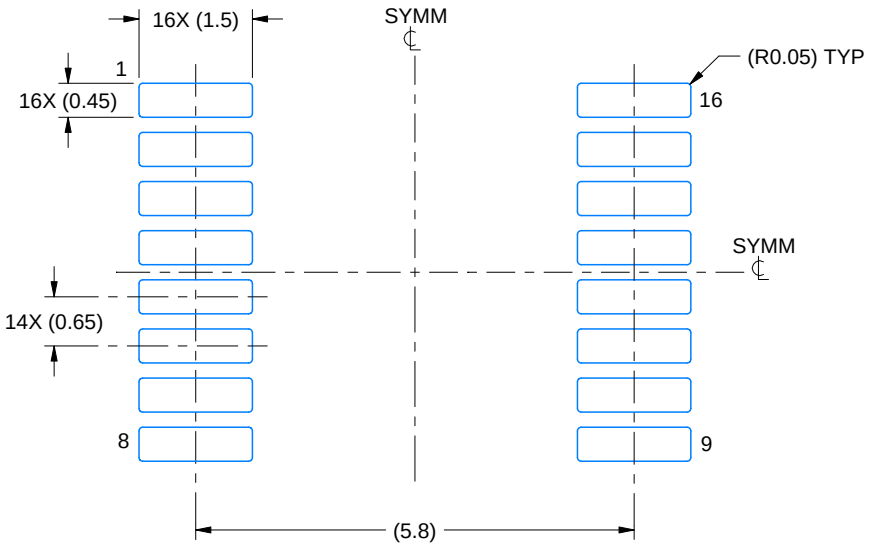
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



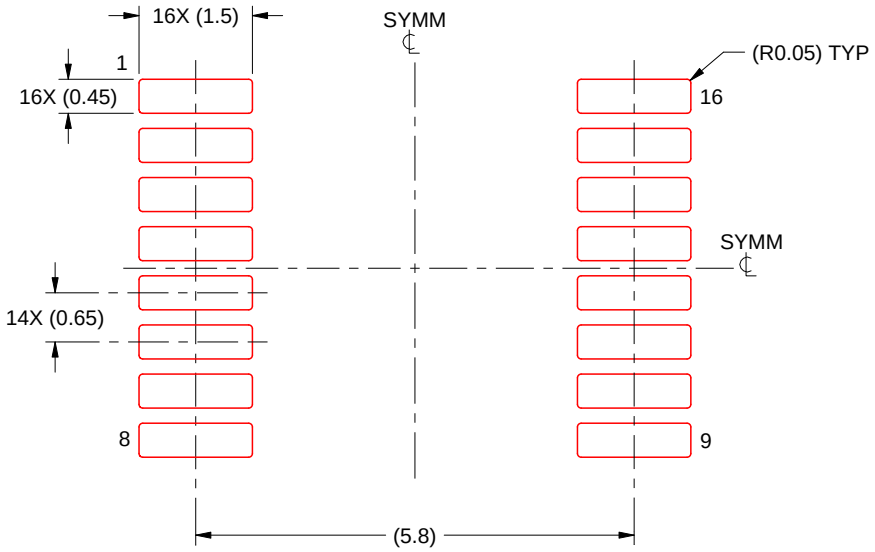
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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Last updated 10/2025