TXH0137D-Q1 Automotive 7-Bit Fixed Direction Voltage-Level Translator with Inverted Open-drain Outputs

1 Features

- This information is only for the automotive device
- Wide voltage-level translation range:
  - 1.5 V ↔ 30 V up and down translation or level shifting
- High drive strength (up to 100 mA I_{OL} per channel)
- High-voltage tolerant I/O (up to 30 V)
- Low power consumption:
  - 30 µA I_{CC} maximum
  - 10 nA I/O leakage
- Overshoot protection with output clamp diode
- Inputs with integrated static pull-down and series resistors allowing for slow, floating or noisy inputs
- Inputs are TTL compatible
- AEC-Q100 qualified with the following results:
  - Device temperature grade 1: –40°C to +125°C ambient operating temperature range
  - Device HBM ESD Classification Level 2
  - Device CDM ESD Classification Level C4B

2 Applications

- High voltage translation or level shifting
- Infotainment and cluster
- Hybrid, electric, and powertrain systems
- Body electronics and lighting
- ADAS
- LED and LCD driver

3 Description

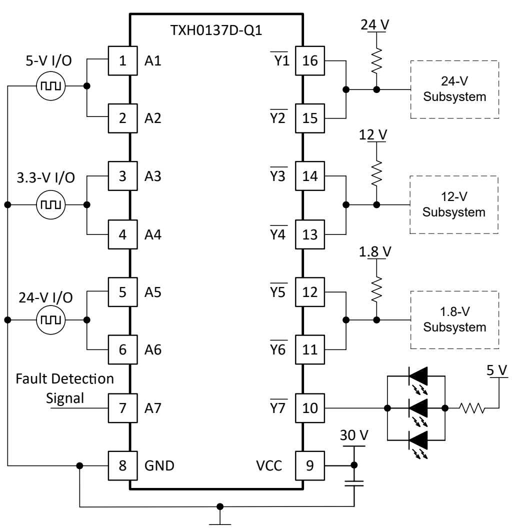
The TXH0137D-Q1 is a 7-bit, single supply inverting fixed direction voltage level translation device. This device has open-drain outputs that support voltages up to 30 V and currents up to 100 mA per channel. These outputs can be used in parallel for even higher current capabilities. Due to these very high currents, the outputs are more susceptible to large overshoots caused by the load reactance. To combat this, the outputs are equipped with overshoot-protection diodes that clamp.

The TXH0137D-Q1 has inputs with improved noise immunity along capable of supporting a wide range of input transition rates. The inputs are also over-voltage tolerant with integrated static 1-MΩ pull-downs.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TXH0137D-Q1	PW (TSSOP, 16)	5 mm × 6.4 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



* VCC must be ≥ 6.5 V or the highest Vo

Simple Application Schematic

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4 Pin Configuration and Functions

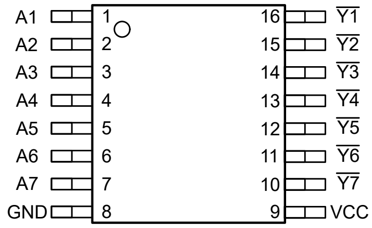

Figure 4-1. PW Package, 16-Pin TSSOP (Top View)

Table 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
A(X)	1	I	Low Leakage Inputs
	2		
	3		
	4		
	5		
	6		
	7		
GND	8	—	Ground pin
VCC	9	—	Supply pin that must be tied to 6.5 V or higher for proper operation (for more information, see *Power Supply Recommendations*).
$\overline{Y(X)}$	10	O	Inverted Open-drain Outputs
	11		
	12		
	13		
	14		
	15		
	16		

(1) I = input, O = output

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted) (1)

		MIN	MAX	UNIT
V_O	Voltage applied to any output in the low or high-impedance state	–0.3	32	V
V_{OK}	Output clamp diode reverse voltage	–0.3	32	V
V_{CC}	Supply voltage	–0.3	32	V
V_I	Input Voltage	–0.3	30	V
I_O	Continuous output current(2) (3)		200	mA
I_{OK}	Output clamp current		500	mA
	Continuous current through V_{CC} or GND	–1	1	A
T_J	Operating junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the *Absolute Maximum Rating* may cause permanent device damage. *Absolute Maximum Rating* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Condition*. If used outside the *Recommended Operating Condition* but within the *Absolute Maximum Rating*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Maximum power dissipation is a function of T_J(max), θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) – T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
(3) The package thermal impedance is calculated in accordance with JESD 51-7.

5.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)		±2000	V
		Charged-device model (CDM), per AEC Q100-011	All pins	±500	
			Corner pins (1, 8, 9, 16)	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

Over operating temperature range

		MIN	MAX	UNIT
V_{CC}	Supply voltage	6.5	30	V
V_{IH}	High-level input voltage	1.5		V
V_{IL}	Low-level input voltage		0.9	V
I_{OL}	Low-level output current	0	100	mA
V_I	Input voltage	1.5	30	V
V_O	Output voltage	0	30	V
T_A	Operating free-air temperature	–40	125	°C

5.4 Thermal Information

THERMAL METRIC[1]		TXH0137D-Q1 TSSOP (PW) 16 PINS	UNIT
θ_{JA}	Junction-to-ambient thermal resistance	113.1	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	46.5	°C/W
θ_{JB}	Junction-to-board thermal resistance	58.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	7	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	58	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.5 Electrical Characteristics

T_J= –40°C to +125°C; Typical Values at T_A= 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OL}	Low-level output voltage	V_I ≥ 1.5 V	I_{OL} = 100 mA		210	450	mV
I_{OZ}	Hi-z output current	V_O = 30 V, V_I ≤ 0.9 V			10	500	nA
V_F	Clamp forward voltage	I_F = 100 mA				1	V
I_I	Input leakage current	V_I = 0 V – 5 V				10	µA
I_{CC}	Supply current	V_{CC} = 6.5 V – 30 V			17	30	µA

5.6 Switching Characteristics

Typical Values at T_A= 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	V_I ≥ 1.5 V, Vpull-up = 30 V, Rpull-up = 480 Ω			250		ns
t_{PHL}	Propagation delay time, high- to low-level output	V_I ≥ 1.5 V, Vpull-up = 30 V, Rpull-up = 480 Ω			250		ns
C_i	Input capacitance	V_I = 0,	f = 100 kHz		5		pF

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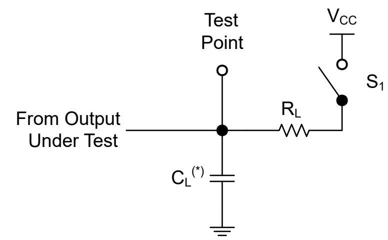
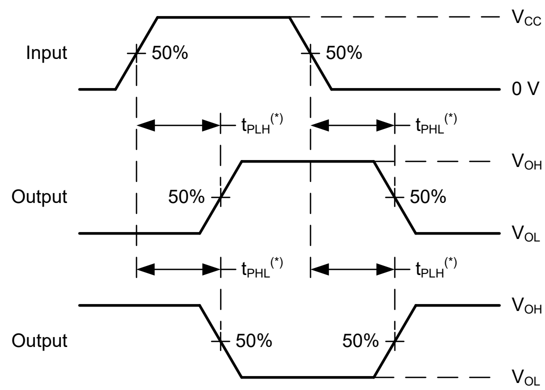


* C_L includes probe and test-fixture Capacitance



* The greater between t_{PLH} and t_{PHL} is the same as t_{pd}

Figure 5-1. Load Circuit and Voltage Waveforms Propagation Delays

5.7 Typical Characteristics

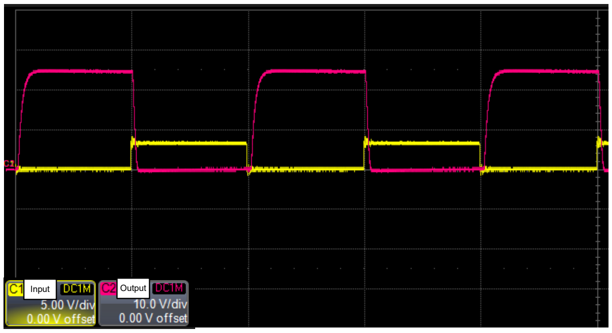


Figure 5-2. Signal Integrity Captured Waveform (3.3 V to 24 V Up Translation at 100 kHz)

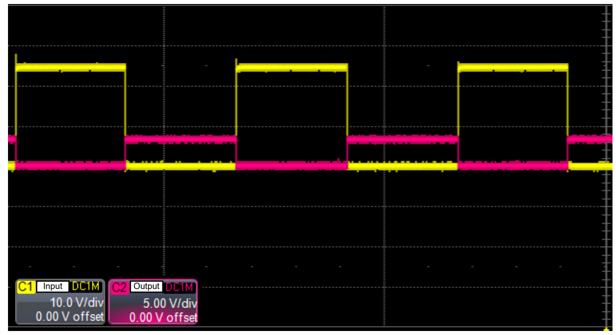


Figure 5-3. Signal Integrity Captured Waveform (24 V to 3.3 V Down Translation at 100 kHz)

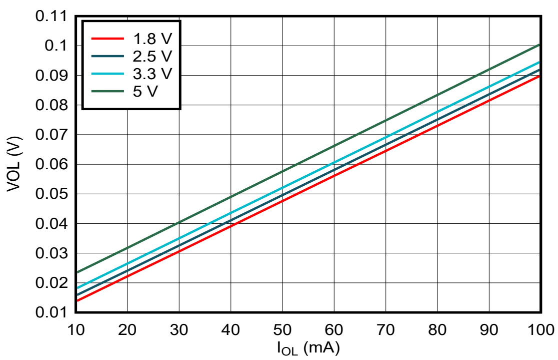


Figure 5-4. Typical (T_A = 25°C) Output Low Voltage ($V_{OL)}$ vs Sink Current($I_{OL)}$ for Lower Voltage Level Shifting

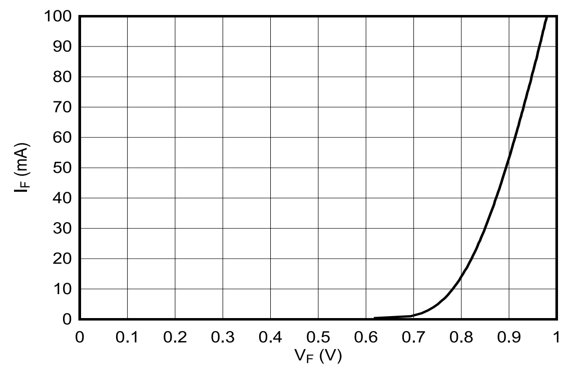


Figure 5-5. Flyback Diode Forward Voltage at 25°C

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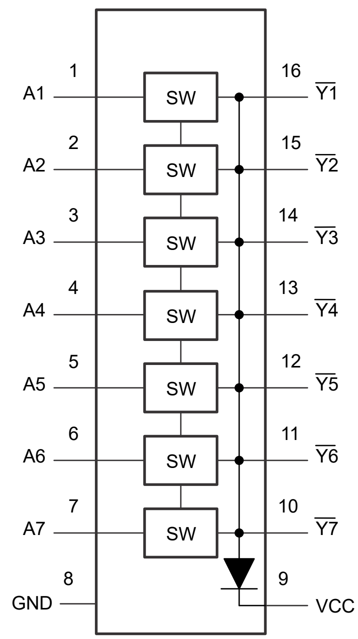
6 Detailed Description

6.1 Overview

The TXH0137D-Q1 is a 7-bit device that can be used in fixed directional level-translation applications for interfacing devices or systems operating at a wide voltage range as low as 1.5 V and as high as 30 V with currents up to 100 mA per channel. The A ports are designed as inputs and the $\overline{Y}$ ports are designed as outputs. The device can operate with A(X) = $\overline{Y(X)}$.

The device enables a wide range of applications with higher input or output capabilities, but more importantly it allows flexible pull-up sizing for voltage translation. Lower value resistors will enable higher frequency operation up to 1 MHz.

6.2 Functional Block Diagram



6.3 Feature Description

The TXH0137D-Q1 device is equipped with high drive open-drain outputs. These outputs are capable of sinking up to 100 mA each. In order to enable floating inputs, a 1-MΩ pull-down resistor exists on each channel. Also included at the input is a filtering circuit with a 50-kΩ series resistor to improve noise immunity and eliminate any erroneous switching.

Higher drive strength is achievable when multiple outputs are paralleled. Each output is equipped with over-voltage protection (OVP) diodes clamping to VCC. The diodes connected between the output and VCC pin is used to suppress any over-shoots caused by load reactance with the high current drive of this device.

6.4 Device Functional Modes

6.4.1 Resistive Load Drive

When driving a resistive load, a pull-up resistor is needed to limit the current through the pass transistor for a logic level of 210 mV to 450 mV when the TXH0137D-Q1 is in the low state to about 100 mA. To calculate the pull-up resistor value use the following equation.

$$R_{PU} = \frac{(V_{PU} - 0.21\,V)}{0.1\,A} \tag{1}$$

where

- R_{PU} is the pull-up resistor
- V_{PU} is the pull-up voltage
- 0.21 V is the low logic level voltage
- 0.1 A is the maximum drive strength for the low logic level current

Table 6-1 provides the resistor values, reference voltages and currents at 100 mA, 50 mA, 25 mA, 15 mA, and 3 mA. The resistor value shown are recommended for typical V_{OL} or less.

Table 6-1. Pull-Up Resistor Values

V_{PU} (V)	Pull-Up Resistor Values (Ω) (1)				
	100 mA	50 mA	25 mA	15 mA	3 mA
30 V	298	596	1192	1986	9930
24 V	238	476	952	1586	7930
12 V	118	236	472	786	3930
5 V	48	96	192	319	1597
3.3 V	31	62	124	206	1030
2.5 V	23	46	92	153	763
1.8 V	16	32	64	106	530
1.5 V	13	26	52	86	430

(1) Use +10% to compensate for V_{PU} range and resistor tolerance

6.4.2 ON State Input Current

The current into the inputs is defined in the electrical characteristics table for input voltages from 1.5 V to 5 V. At higher voltages, this leakage increases, and the input current can be estimated using the approximate clamp voltage for the overshoot-protection diode which is, 6.4 V. Equation 2 shows how to approximate input current for input voltages greater than 6.4 V:

$$I_{IN(ON)} = \frac{V_{IN}}{1\,M\Omega} + \frac{(V_{IN} - 6.4\,V)}{50\,k\Omega} \tag{2}$$

where

- V_{IN} is the input voltage
- 1 MΩ is the input pull-down resistance
- 50 kΩ is the input series resistance
- 6.4 V is the approximate clamp voltage for the OVP diode

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6.4.3 High-Drive Outputs

The outputs of this device are capable of driving larger currents than the device can sustain without being damaged. Two outputs can be connected together for 2X stronger output drive strength. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

The maximum frequency of the TXH0137D-Q1 is dependent on the components of the system. The device can operate at speeds up to 100 kHz for up translation and < 1 MHz for down translation given the correct conditions.

$$Mbps_{datarate} = \frac{1}{(6 \times R_{PU} \times C)} \quad (3)$$

where

- R_{PU} is the pull-up resistor
- C is the load capacitance

Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

1 Application Information

The TXH0137D-Q1 is typically used to translate typical logic levels to higher voltage (up to 30 V) peripherals and vice-versa. Figure 7-1 shows a common application of the TXH0137D-Q1.

2 Typical Application

A common application for the TXH0137D-Q1 is to level shift up to or down from 30 V. With its high sinking currents it can also be used for other applications requiring higher current drive like operating LEDs.

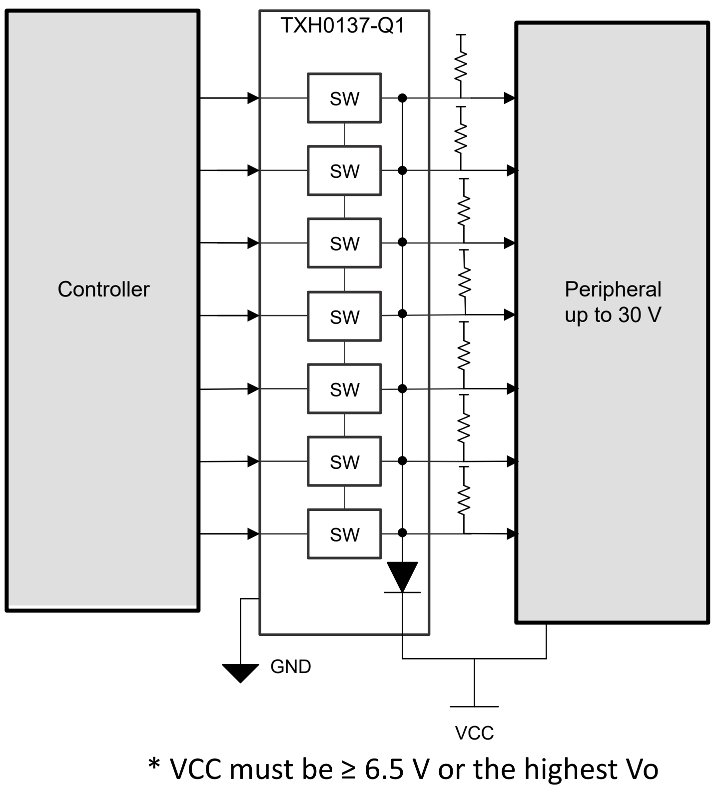

Figure 7-1. Typical Application Schematic

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2.1 Design Requirements

For this design example, use the parameters listed in Table 7-1 as the input parameters.

Table 7-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
V_{IN} supply voltage	1.5 V to 30 V
V_{CC} supply voltage	6.5 V to 30 V
Number of channels	7
Output current	Up to 100 mA per channel
C_{Vcc}	0.1 µF
V_{PU}	0 V to V_o

2.2 Detailed Design Procedure

When using the TXH0137D-Q1 in a voltage translation application, determine the following:

- Output voltage range
- Output drive current
- Temperature range
- Power dissipation

2.2.1 TTL and other Logic Inputs

The TXH0137D-Q1 inputs are specified for standard 1.8 V through 5 V CMOS logic interface and can tolerate up to 30 V. With its input threshold levels, this device can be used with TTL logic. The device features a 1-MΩ input pull-down resistor and a 50-kΩ series resistor allowing for floating or noisy inputs and eliminating the need for slew or input transition rate requirements.

2.2.2 High-Impedance Input Drivers

The TXH0137D-Q1 features a 1-MΩ input pull-down resistor. The presence of this resistor allows the input drivers to be tri-stated. When a high-impedance driver is connected to a channel input, the TXH0137D-Q1 detects the channel input as a low-level input and remains OFF. The input noise rejection circuit helps improve noise tolerance levels if necessary, when input drivers are in the high-impedance state.

2.2.3 Output Low Voltage

The output low voltage (V_{OL}) is drain-to-source (V_{DS}) voltage of the output NMOS transistors when the input is driven high and it is sinking current. For more information, see *Electrical Characteristics* or Figure 5-4.

2.3 Application Curve

The following image was generated with TXH0137D-Q1 for A(X) = $\overline{Y(X)}$; 30 V to 30 V, 100 kHz signal.

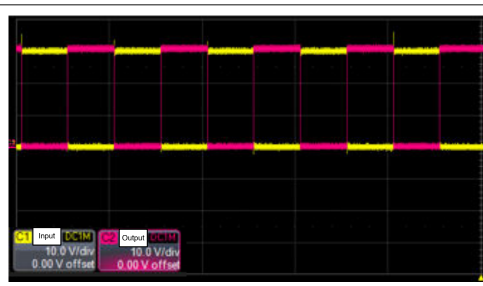

Figure 7-2. Output Response at Maximum Voltage

3 Power Supply Recommendations

The V_{CC} pin is the power supply pin of this device to power the gate drive circuitry. The pin must be supplied with ≥ 6.5 V or the highest output voltage for full functionality. While a bypass capacitor on this pin is recommended for sensitive power supplies, it is not required for proper operation of the device. The V_{CC} pin is designed to supply full drive potential with any GPIOv ≥ 1.5 V. Though 6.5 V minimum is recommended for V_{CC}, the part still functions with a reduced V_{CC} resulting in higher Rds_{on}.

4 Layout

4.1 Layout Guidelines

Thin traces can be used on the input due to the low current logic that is typically used to drive the TXH0137D-Q1. Take care to separate the input channels as much as possible to eliminate cross-talk. Thick traces are recommended for the output to drive high currents that may be needed. Wire thickness can be determined by the trace material's current density and desired drive current.

Since all of the channels currents return to a common ground, it is best to size that trace width to be very wide. The V_{CC} pin only draws up to 30 µA and thick traces may not be necessary.

4.2 Layout Example

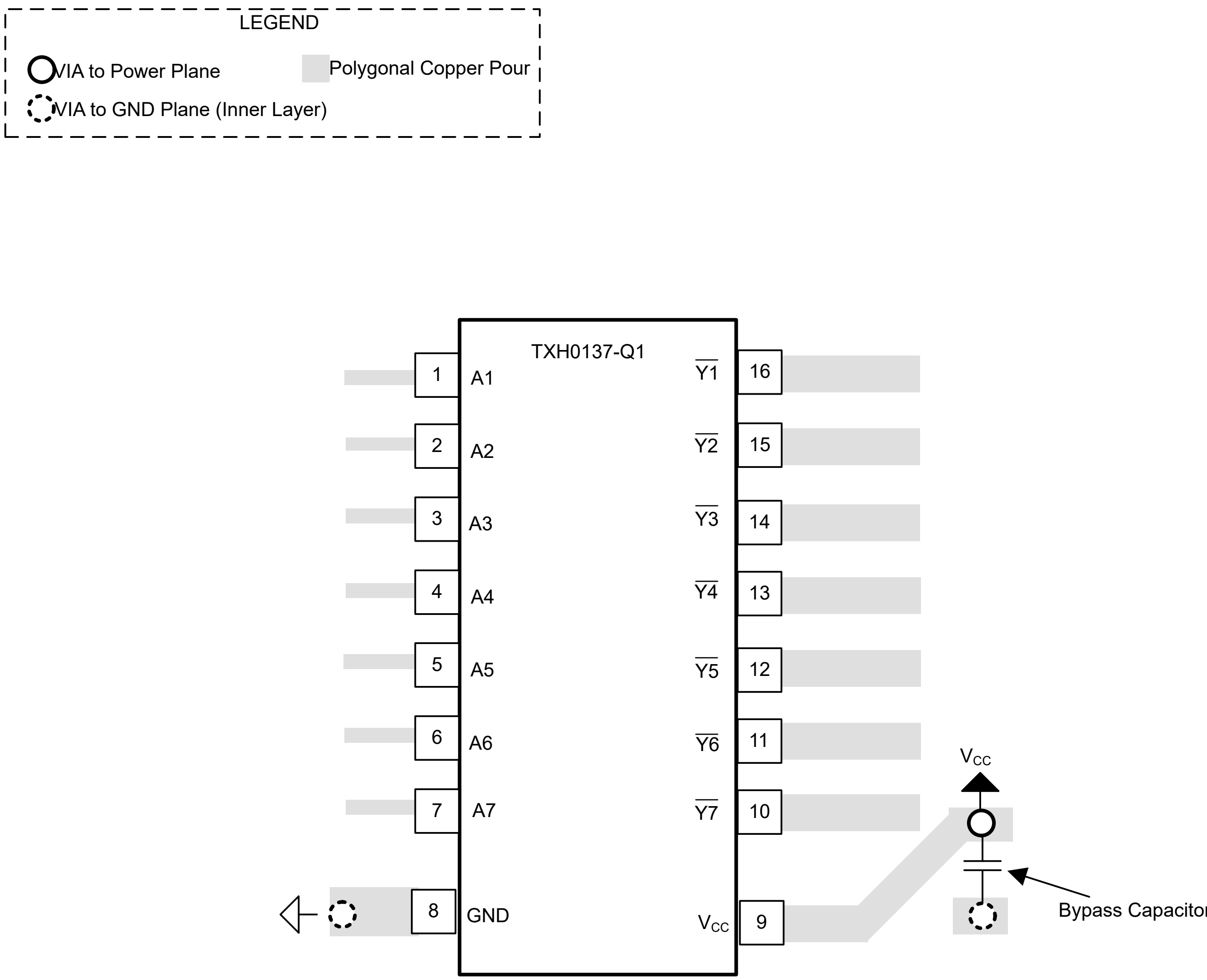

Figure 7-3. Package Layout

4.3 Thermal Considerations

Use Equation 4 to calculate TXH0137D-Q1 on-chip power dissipation P_D:

$$P_D = \sum_{i=1}^{N} V_{OLi} \times I_{Li} \tag{4}$$

where

- N is the number of channels active together
- V_{OLi} is the OUT_i pin voltage for the load current I_{Li}.

For reliability of TXH0137D-Q1 and the system, the on-chip power dissipation must be lower than or equal to the maximum allowable power dissipation ($P_{D(MAX)}$). Equation 5 shows how $P_{D(MAX)}$ is calculated.

$$P_{D(MAX)} = \frac{\left(T_{J(MAX)} - T_A\right)}{\theta_{JA}} \tag{5}$$

where

- $T_{J(MAX)}$ is the target maximum junction temperature
- T_A is the operating ambient temperature
- θ_{JA} is the package junction to ambient thermal resistance

It is recommended to limit the TXH0137D-Q1 IC's die junction temperature to less than 125°C. The IC junction temperature is directly proportional to the on-chip power dissipation.

4.3.1 Improving Package Thermal Performance

θ_{JA} value depends on the PCB layout. An external heat sink and/or a cooling mechanism, like a cold air fan, can help reduce θ_{JA} and thus improve device thermal capabilities. For a general guidance on improving device thermal performance, refer to TI's design support web page at www.ti.com/thermal.

7 Device and Documentation Support

7.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

7.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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7.3 Trademarks

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7.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.5 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

8 Revision History

DATE	REVISION	NOTES
September 2023	*	Initial Release

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

9.1 Packaging Option Addendum

Packaging Information

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish(4)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking(5) (6)
PTXH0137DQPWRQ1	ACTIVE	TSSOP	PW	16	2000	TBD	Call TI	Call TI	-40 to 125	PTHX0137Q1

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

(5) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device

(6) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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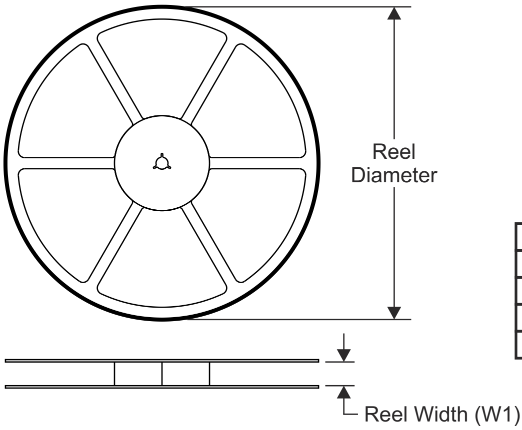
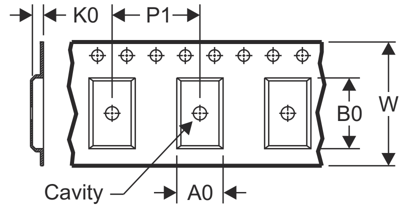
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

9.2 Tape and Reel Information

REEL DIMENSIONS

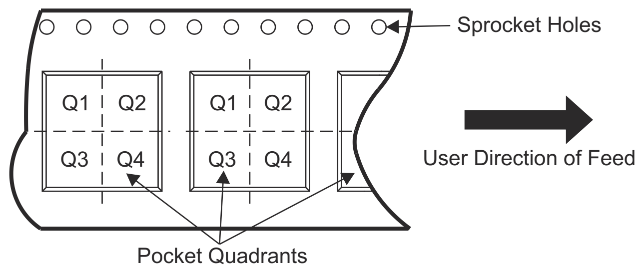


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PTXH0137DQPWRQ1	TSSOP	PW	16	2000	330	12	6.9	5.6	1.6	8	9.2	Q1

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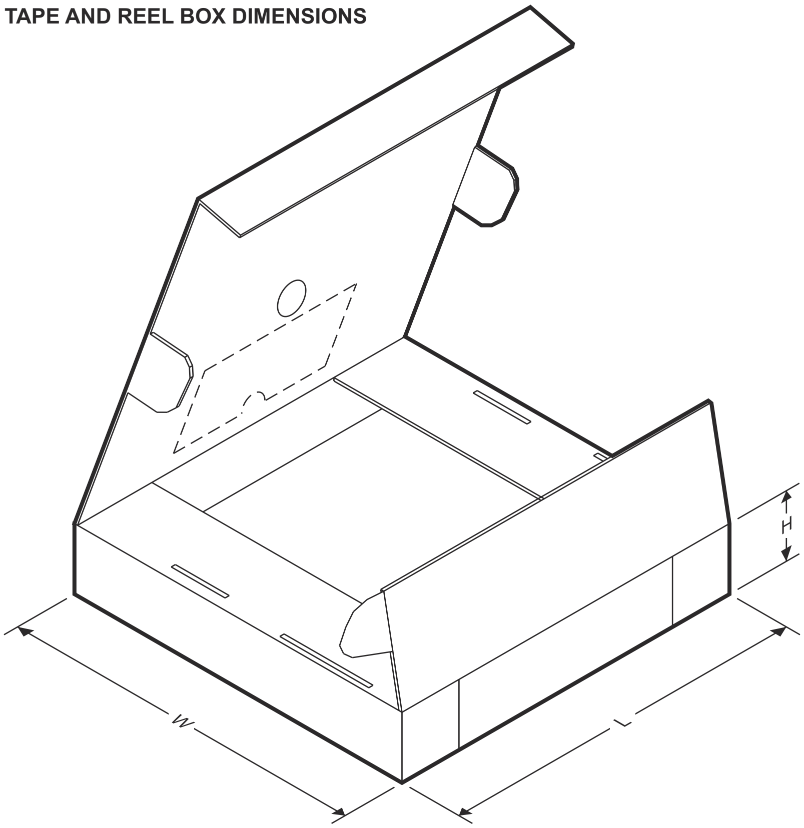
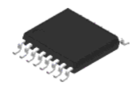
TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PTXH0137DQPWRQ1	TSSOP	PW	16	2000	366	364	50

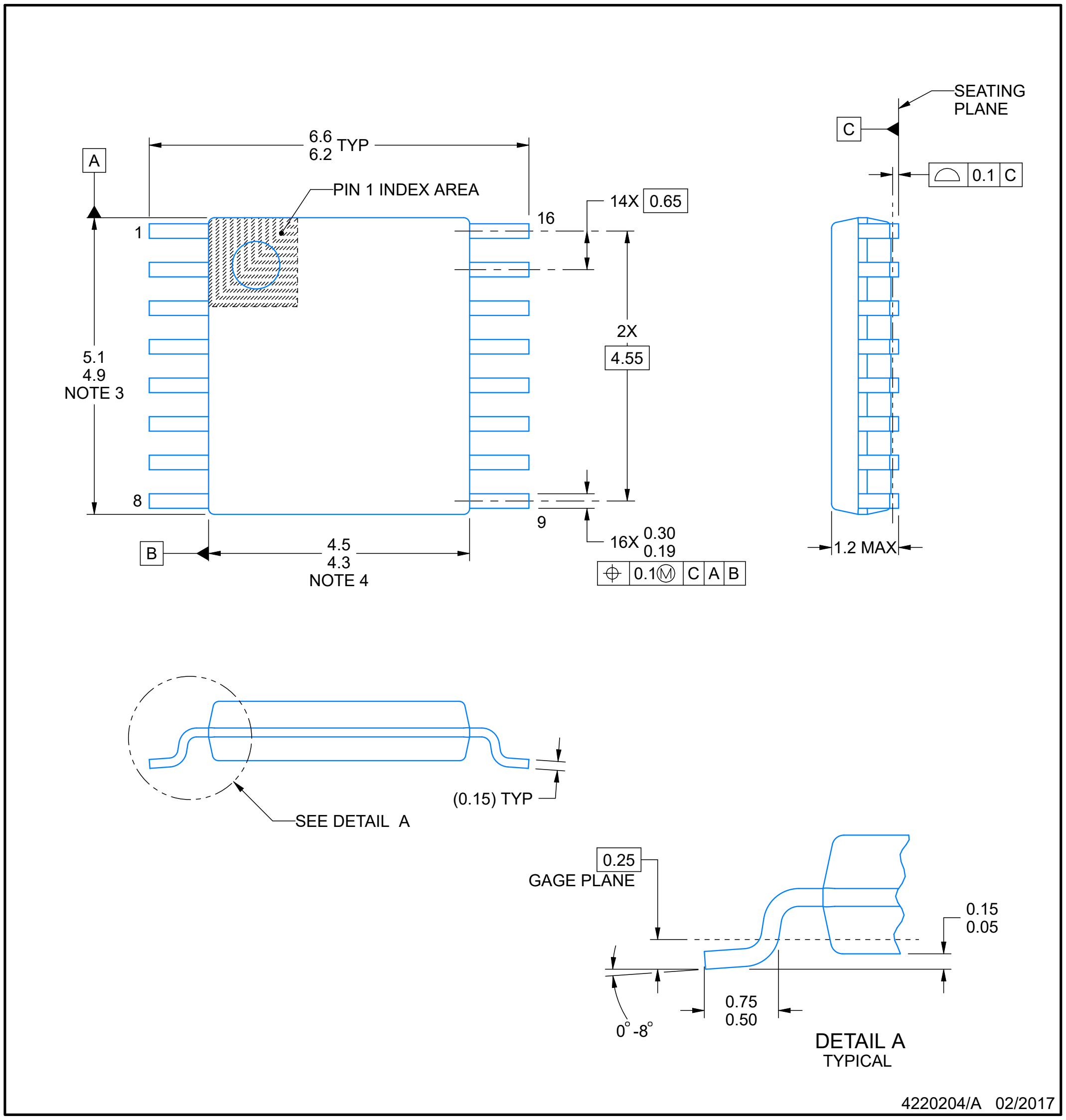
9.3 Mechanical Data



PACKAGE OUTLINE

PW0016A **TSSOP - 1.2 mm max height**

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

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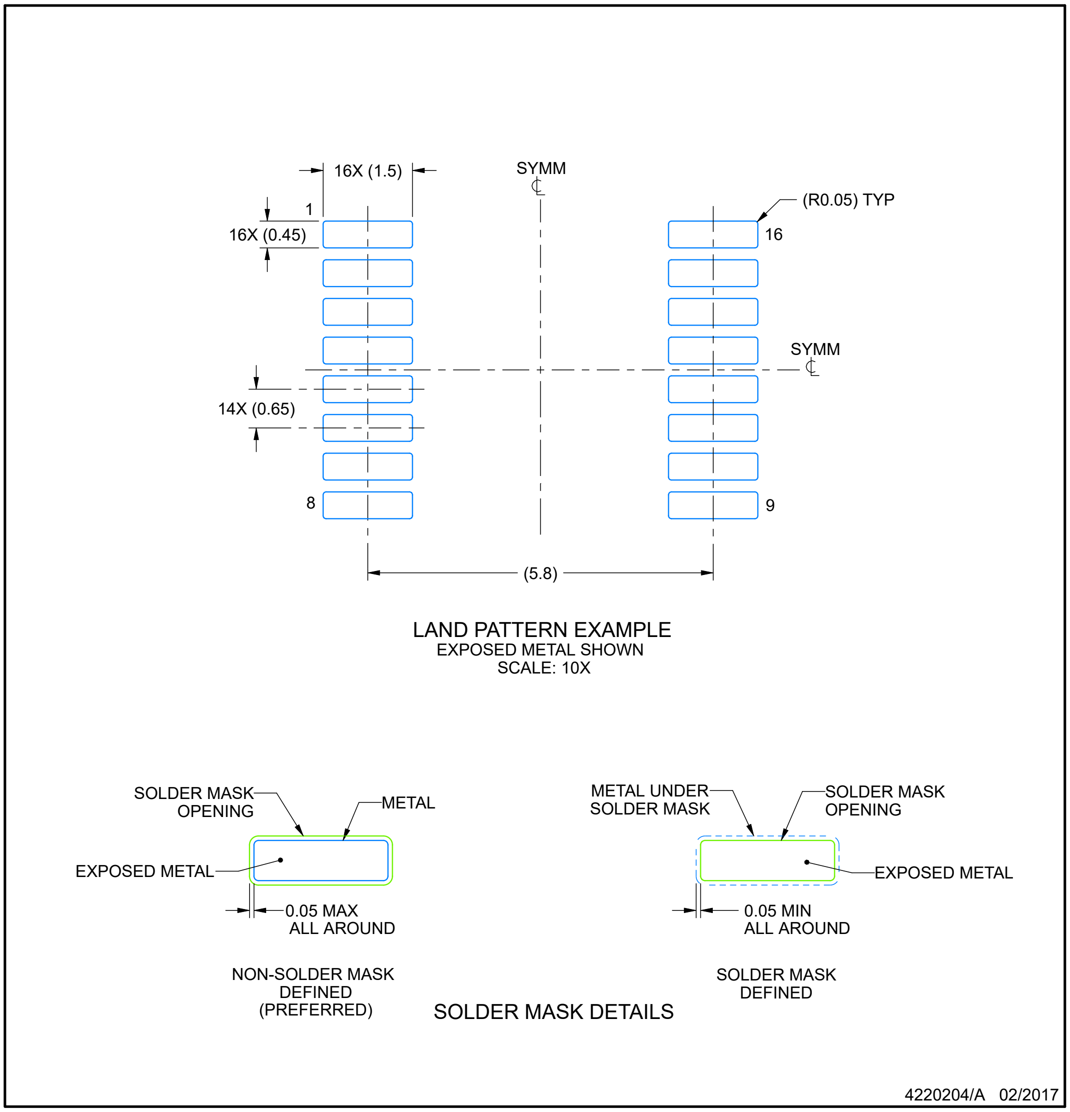
EXAMPLE BOARD LAYOUT

PW0016A **TSSOP - 1.2 mm max height**

SMALL OUTLINE PACKAGE



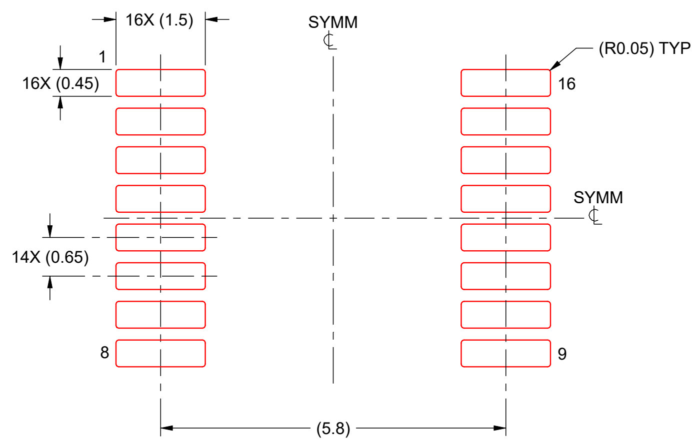
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A **TSSOP - 1.2 mm max height**

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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