

# TXS0102W-Q1 2-Bit Bidirectional Voltage-Level Translator for Open-Drain and Push-Pull Applications

## 1 Features

- No direction-control signal needed
- Maximum data rates:
  - 50Mbps (push pull)
  - 2Mbps (open drain)
- 1.2V to 3.6V on A port and 1.65V to 5.5V on B port
- $V_{CCA}$  can be  $>$ ,  $=$ ,  $<$   $V_{CCB}$
- $V_{CC}$  isolation feature: if either  $V_{CC}$  input is at GND, both ports are in the High-Impedance state
- No power-supply sequencing required: either  $V_{CCA}$  or  $V_{CCB}$  can be ramped first
- $I_{off}$  supports partial-power-down mode operation
- Latch-up performance exceeds 100mA per JESD 78, Class II
- ESD protection exceeds JESD 22:
  - A port:
    - 2500V Human-Body Model (A114-B)
    - 250V Machine Model (A115-A)
    - 1500V Charged-Device Model (C101)
  - B port:
    - 8kV Human-Body Model (A114-B)
    - 250V Machine Model (A115-A)
    - 1500V Charged-Device Model (C101)

## 2 Applications

- I<sup>2</sup>C / SMBus
- UART
- GPIO

## 3 Description

TXS0102W-Q1 is a two-bit non-inverting translator is a bidirectional voltage-level translator and can be used to establish digital switching compatibility between mixed-voltage systems. TXS0102W-Q1 uses two separate configurable power-supply rail. The A ports support operating voltages from 1.2V to 3.6V while tracking the  $V_{CCA}$  supply, and the B ports support operating voltages from 1.65V to 5.5V while tracking the  $V_{CCB}$  supply. This allows the support of both lower and higher logic signal levels while providing bidirectional translation capabilities between any of the 1.8V, 2.5V, 3.3V, and 5V voltage nodes.

When the output-enable (OE) input is low, all I/Os are placed in the high-impedance state, which significantly reduces the power-supply quiescent current consumption.

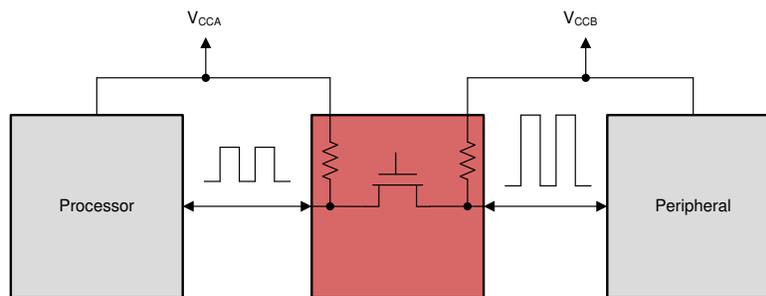
To put the device in the high-impedance state during power up or power down, tie OE to GND through a pulldown resistor. The current-sourcing capability of the driver determines the minimum value of the resistor.

### Package Information

PART NUMBER	PACKAGE (1)	PACKAGE SIZE (2)
TXS0102W-Q1	DCU (VSSOP, 8)	2mm × 3.1mm

(1) For more information, see [Section 11](#)

(2) The package size (length × width) is a nominal value and includes pins, where applicable.



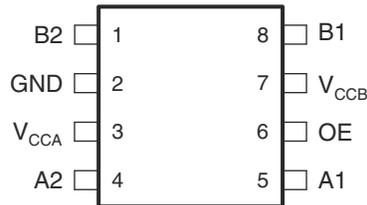
Typical Application Block Diagram for TXS0102W-Q1



## Table of Contents

<b>1 Features</b> .....	<b>1</b>	<b>7 Detailed Description</b> .....	<b>16</b>
<b>2 Applications</b> .....	<b>1</b>	7.1 Overview.....	16
<b>3 Description</b> .....	<b>1</b>	7.2 Functional Block Diagram.....	16
<b>4 Pin Configuration and Functions</b> .....	<b>3</b>	7.3 Feature Description.....	17
<b>5 Specifications</b> .....	<b>4</b>	7.4 Device Functional Modes.....	18
5.1 Absolute Maximum Ratings.....	4	<b>8 Application and Implementation</b> .....	<b>19</b>
5.2 ESD Ratings.....	4	8.1 Application Information.....	19
5.3 Recommended Operating Conditions.....	5	8.2 Typical Application.....	19
5.4 Thermal Information.....	5	8.3 Power Supply Recommendations.....	20
5.5 Electrical Characteristics.....	6	8.4 Layout.....	21
5.6 Switching Characteristics, $V_{CCA} = 1.2V$ .....	7	<b>9 Device and Documentation Support</b> .....	<b>22</b>
5.7 Switching Characteristics, $V_{CCA} = 1.5 \pm 0.1V$ .....	8	9.1 Documentation Support.....	22
5.8 Switching Characteristics, $V_{CCA} = 1.8 \pm 0.15V$ .....	8	9.2 Receiving Notification of Documentation Updates.....	22
5.9 Switching Characteristics, $V_{CCA} = 2.5 \pm 0.2V$ .....	9	9.3 Support Resources.....	22
5.10 Switching Characteristics, $V_{CCA} = 3.3 \pm 0.3V$ .....	10	9.4 Trademarks.....	22
5.11 Switching Characteristics: $T_{sk}, T_{MAX}$ .....	11	9.5 Electrostatic Discharge Caution.....	22
5.12 Operating Characteristics: $V_{CCA} = 1.5V$ to $3.3V$ , $V_{CCB} = 1.5V$ to $3.3V$ .....	12	9.6 Glossary.....	22
5.13 Typical Characteristics.....	13	<b>10 Revision History</b> .....	<b>22</b>
<b>6 Parameter Measurement Information</b> .....	<b>14</b>	<b>11 Mechanical, Packaging, and Orderable Information</b> .....	<b>23</b>

## 4 Pin Configuration and Functions



**Figure 4-1. DCU Package, 8-Pin SSOP and VSSOP (Top View)**

**Table 4-1. Pin Functions**

PIN		TYPE <sup>(1)</sup>	DESCRIPTION
NAME	NO. DCU		
A1	5	I/O	Input/output A. Referenced to $V_{CCA}$ .
A2	4	I/O	Input/output A. Referenced to $V_{CCA}$ .
B1	8	I/O	Input/output B. Referenced to $V_{CCB}$ .
B2	1	I/O	Input/output B. Referenced to $V_{CCB}$ .
GND	2	—	Ground
OE	6	I	Output enable (active High). Pull OE low to place all outputs in 3-state mode. Referenced to $V_{CCA}$ .
$V_{CCA}$	3	P	A-port supply voltage. $1.2V \leq V_{CCA} \leq 3.6V$ and $V_{CCA} \leq V_{CCB}$
$V_{CCB}$	7	P	B-port supply voltage. $1.65V \leq V_{CCB} \leq 5.5V$

(1) I = input, O = output, I/O = input and output, P = power

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

			MIN	MAX	UNIT
V <sub>CCA</sub>	Supply voltage A		-0.5	4.6	V
V <sub>CCB</sub>	Supply voltage B		-0.5	6.5	V
V <sub>I</sub>	Input Voltage <sup>(2)</sup>	I/O Ports (A Port)	-0.5	4.6	V
		I/O Ports (B Port)	-0.5	6.5	
V <sub>O</sub>	Voltage applied to any output in the high-impedance or power-off state <sup>(2)</sup>	A Port	-0.5	4.6	V
		B Port	-0.5	6.5	
V <sub>O</sub>	Voltage applied to any output in the high or low state <sup>(2) (3)</sup>	A Port	-0.5	V <sub>CCA</sub> + 0.5	V
		B Port	-0.5	V <sub>CCB</sub> + 0.5	
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0		-50	mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0		-50	mA
I <sub>O</sub>	Continuous output current			±50	mA
	Continuous current through V <sub>CC</sub> or GND			±100	mA
T <sub>J</sub>	Junction Temperature			150	°C
T <sub>stg</sub>	Storage temperature		-65	150	°C

- (1) Stresses beyond those listed under [Section 5.1](#) may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under [Section 5.3](#). Exposure beyond the limits listed in [Section 5.3](#) may affect device reliability.
- (2) The input voltage and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The output positive-voltage rating may be exceeded up to 6.5V maximum if the output current rating is observed.

### 5.2 ESD Ratings

			VALUE	UNIT	
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001	A Port	±2500	V
			B Port	±8000	
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002	A Port	±1500	
			B Port	±1500	

### 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup> <sup>(2)</sup> <sup>(3)</sup>

			V <sub>CCA</sub>	V <sub>CCB</sub>	MIN	MAX	UNIT
V <sub>CCA</sub>	Supply voltage A				1.2	3.6	V
V <sub>CCB</sub>	Supply voltage B				1.65	5.5	V
V <sub>IH</sub>	High-level input voltage	A-port I/O's	1.2V to 1.6V	1.65V to 5.5V	V <sub>CCI</sub> - 0.2	V <sub>CCI</sub>	V
			1.65V to 3.6V	2.3V to 5.5V	V <sub>CCI</sub> - 0.4	V <sub>CCI</sub>	
		B-port I/O's	1.2V to 3.6V	1.65V to 5.5V	V <sub>CCI</sub> - 0.4	V <sub>CCI</sub>	
		OE Input	1.2V to 3.6V	1.65V to 5.5V	V <sub>CCA</sub> × 0.65	5.5	
V <sub>IL</sub>	Low-level input voltage	A-port I/O's	1.2V to 3.6V	1.65V to 5.5V	0	0.15	V
		B-port I/O's	1.2V to 3.6V	1.65V to 5.5V	0	0.15	
		OE Input	1.2V to 3.6V	1.65V to 5.5V	0	V <sub>CCA</sub> × 0.35	
V <sub>RTA</sub>	RTA Activation Threshold	A-port I/O's	1.2V to 3.6V	1.65V to 5.5V	V <sub>CCI</sub> × 0.30		V
		B-port I/O's	1.2V to 3.6V	1.65V to 5.5V	V <sub>CCI</sub> × 0.30		
Δt/Δv	Input transition rise and fall time	Push-Pull Driving	1.2V to 3.6V	1.65V to 5.5V			10 ns/V
T <sub>A</sub>	Operating free-air temperature				-40	125	°C

- (1) V<sub>CCI</sub> is the V<sub>CC</sub> associated with the input port.
- (2) V<sub>CCO</sub> is the V<sub>CC</sub> associated with the output port.
- (3) All control inputs and data I/Os of this device have weak pulldowns to ensure the line is not floating when undefined external to the device. The input leakage from these weak pulldowns is defined by the I<sub>I</sub> specification indicated under [Section 5.5](#).

### 5.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TXS0102W-Q1	
		DCU	
		8 PINS	
			UNIT
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	239.8	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	88.5	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	151.6	°C/W
Y <sub>JT</sub>	Junction-to-top characterization parameter	30.9	°C/W
Y <sub>JB</sub>	Junction-to-board characterization parameter	150.5	°C/W
R <sub>θJC(bottom)</sub>	Junction-to-case (bottom) thermal resistance	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application note.

## 5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)<sup>(1) (2)</sup>

PARAMETER	TEST CONDITIONS	V <sub>CCA</sub>	V <sub>CCB</sub>	Operating free-air temperature (T <sub>A</sub> )									UNIT	
				25°C			-40°C to 85°C			-40°C to 125°C				
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
V <sub>OHA</sub>	Port A output high voltage	I <sub>OH</sub> = -20μA	1.2V to 3.6V	1.65V to 5.5V	V <sub>CCA</sub> × 0.67			V <sub>CCA</sub> × 0.67			V <sub>CCA</sub> × 0.67			V
			1.65V to 3.6V	1.65V to 5.5V	V <sub>CCA</sub> × 0.67			V <sub>CCA</sub> × 0.67			V <sub>CCA</sub> × 0.67			
V <sub>OLA</sub>	Port A output low voltage	I <sub>OL</sub> = 1mA	1.2V to 3.6V	1.65V to 5.5V				0.3			0.3			V
			1.65V to 3.6V	1.65V to 5.5V				0.3			0.3			
V <sub>OHB</sub>	Port B output high voltage	I <sub>OH</sub> = -20μA	1.2V to 3.6V	1.65V to 5.5V	V <sub>CCB</sub> × 0.67			V <sub>CCB</sub> × 0.67			V <sub>CCB</sub> × 0.67			V
			1.65V to 3.6V	1.65V to 5.5V	V <sub>CCB</sub> × 0.67			V <sub>CCB</sub> × 0.67			V <sub>CCB</sub> × 0.67			
V <sub>OLB</sub>	Port B output low voltage	I <sub>OL</sub> = 1mA	1.2V to 3.6V	1.65V to 5.5V				0.4			0.4			V
			1.65V to 3.6V	1.65V to 5.5V				0.4			0.4			
I <sub>I</sub>	Input leakage current	OE V <sub>I</sub> = V <sub>CC</sub> or GND	1.2V to 3.6V	1.65V to 5.5V	1			2			2			μA
I <sub>off</sub>	Partial power down current	A port	0V	0V to 5.5V	1			2			2			μA
		B port	0V to 3.6V	0V	1			2			2			μA
I <sub>OZ</sub>	Tri-state output current	A or B Port: V <sub>I</sub> = V <sub>CC1</sub> or GND V <sub>O</sub> = V <sub>CC0</sub> or GND OE = GND	1.2V to 3.6V	1.65V to 5.5V	-2	2		-2	2		-3	3		μA
I <sub>CCA</sub>	V <sub>CCA</sub> supply current	V <sub>I</sub> = V <sub>CC1</sub> or GND I <sub>O</sub> = 0	1.2V to 3.6V	1.65V to 5.5V				3			5			μA
			0V	5.5V	-3			-3			-3			
			3.6V	0V	2.2			2.2			2.2			
I <sub>CCB</sub>	V <sub>CCB</sub> supply current	V <sub>I</sub> = V <sub>CC1</sub> or GND I <sub>O</sub> = 0	1.2V to 3.6V	1.65V to 5.5V				12			21			μA
			0V	5.5V	5			5			8			
			3.6V	0V	-1			-1			-1			
I <sub>CCA</sub> + I <sub>CCB</sub>	Combined supply current	V <sub>I</sub> = V <sub>CC1</sub> or GND I <sub>O</sub> = 0	1.2V to 3.6V	1.65V to 5.5V	14.4			14.4			25			μA
C <sub>i</sub>	Input Capacitance	OE	3.3V	3.3V	2.5			3.5			3.5			pF

over operating free-air temperature range (unless otherwise noted)<sup>(1) (2)</sup>

PARAMETER	TEST CONDITIONS	V <sub>CCA</sub>	V <sub>CCB</sub>	Operating free-air temperature (T <sub>A</sub> )									UNIT	
				25°C			-40°C to 85°C			-40°C to 125°C				
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
C <sub>io</sub>	Input-to-output internal capacitance	A or B port	3.3V	3.3V	10									pF
		A port			5			6			6			
		B port			6			7.5			7.5			

- (1) V<sub>CCI</sub> is the V<sub>CC</sub> associated with the input port  
(2) V<sub>CCO</sub> is the V<sub>CC</sub> associated with the output port

### 5.6 Switching Characteristics, V<sub>CCA</sub> = 1.2V

PARAMETER	FROM	TO	Test Conditions		B-Port Supply Voltage (V <sub>CCB</sub> )												UNIT	
					1.8 ± 0.15V			2.5 ± 0.2V			3.3 ± 0.3V			5.0 ± 0.5V				
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t <sub>PHL</sub>	Propagation Delay (Hight-to-Low)	A	B	Push-Pull	-40°C to 125°C	6.7			7.6			8.9			11.7			ns
				Open-Drain	-40°C to 125°C	6.7			7.6			8.9			11.7			ns
t <sub>PLH</sub>	Propagation Delay (Low-to-High)	A	B	Push-Pull	-40°C to 125°C	17.0			14.3			15.6			30.2			ns
				Open-Drain	-40°C to 125°C	56.0			49.0			44.3			51.8			ns
t <sub>PHL</sub>	Propagation Delay (Hight-to-Low)	B	A	Push-Pull	-40°C to 125°C	5.6			4.2			4.4			6.0			ns
				Open-Drain	-40°C to 125°C	6.3			6.5			7.2			8.6			ns
t <sub>PLH</sub>	Propagation Delay (Low-to-High)	B	A	Push-Pull	-40°C to 125°C	5.5			1.1			0.6			0.5			ns
				Open-Drain	-40°C to 125°C	0.5			0.5			0.5			0.5			ns
t <sub>en</sub>	Enable Time	OE	A or B		-40°C to 125°C	250			200			200			200			ns
t <sub>dis</sub>	Disable Time	OE	A or B		-40°C to 125°C	200			200			200			200			ns
t <sub>rA</sub>	Input Rise Time	B	A	Push-Pull	-40°C to 125°C	25.2			21.8			20.1			18.1			ns
				Open-Drain	-40°C to 125°C	158.4			133.9			113			94.2			ns
t <sub>rB</sub>	Input Rise Time	A	B	Push-Pull	-40°C to 125°C	20			16.1			15.8			26			ns
				Open-Drain	-40°C to 125°C	113.9			83.6			64.1			47.8			ns
t <sub>fA</sub>	Input Fall Time	B	A	Push-Pull	-40°C to 125°C	7.8			6.8			7.8			9.0			ns
				Open-Drain	-40°C to 125°C	7.8			7.8			7.9			9.0			ns
t <sub>fB</sub>	Input Fall Time	A	B	Push-Pull	-40°C to 125°C	11.6			13.3			15.9			21.5			ns
				Open-Drain	-40°C to 125°C	11.6			13.3			15.9			23.1			ns

## 5.7 Switching Characteristics, $V_{CCA} = 1.5 \pm 0.1V$

PARAMETER		FROM	TO	Test Conditions		B-Port Supply Voltage ( $V_{CCB}$ )												UNIT
						1.8 ± 0.15V			2.5 ± 0.2V			3.3 ± 0.3V			5.0 ± 0.5V			
						MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
$t_{PHL}$	Propagation Delay (Hight-to-Low)	A	B	Push-Pull	-40°C to 125°C	4.5			5.0			5.8			7.5			ns
		A	B	Open-Drain	-40°C to 125°C	4.5			5.0			5.8			7.5			ns
$t_{PLH}$	Propagation Delay (Low-to-High)	A	B	Push-Pull	-40°C to 125°C	9.7			7.1			6.3			5.9			ns
		A	B	Open-Drain	-40°C to 125°C	14			12			11			11			ns
$t_{PHL}$	Propagation Delay (Hight-to-Low)	B	A	Push-Pull	-40°C to 125°C	4.2			3.0			3.1			4.5			ns
		B	A	Open-Drain	-40°C to 125°C	4.6			4.7			5.3			6.4			ns
$t_{PLH}$	Propagation Delay (Low-to-High)	B	A	Push-Pull	-40°C to 125°C	8			1			1			1			ns
		B	A	Open-Drain	-40°C to 125°C	1.5			0.5			0.5			0.5			ns
$t_{en}$	Enable Time	OE	A or B		-40°C to 125°C	200			200			200			200			ns
$t_{dis}$	Disable Time	OE	A or B		-40°C to 125°C	200			200			200			200			ns
$t_{rA}$	Ouput Rise Time	B	A	Push-Pull	-40°C to 125°C	14			11			10			9			ns
		B	A	Open-Drain	-40°C to 125°C	120			90			75			53			ns
$t_{rB}$	Ouput Rise Time	A	B	Push-Pull	-40°C to 125°C	16			12			10			8			ns
		A	B	Open-Drain	-40°C to 125°C	105			75			55			31			ns
$t_{fA}$	Output Fall Time	B	A	Push-Pull	-40°C to 125°C	5.8			4.7			4.8			4.6			ns
		B	A	Open-Drain	-40°C to 125°C	6.3			6.0			6.3			7.0			ns
$t_{fB}$	Output Fall Time	A	B	Push-Pull	-40°C to 125°C	7.4			8.6			10.0			13.2			ns
		A	B	Open-Drain	-40°C to 125°C	7.4			8.6			10.0			13.2			ns

## 5.8 Switching Characteristics, $V_{CCA} = 1.8 \pm 0.15V$

PARAMETER		FROM	TO	Test Conditions		B-Port Supply Voltage ( $V_{CCB}$ )												UNIT
						1.8 ± 0.15V			2.5 ± 0.2V			3.3 ± 0.3V			5.0 ± 0.5V			
						MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
$t_{PHL}$	Propagation Delay (Hight-to-Low)	A	B	Push-Pull	-40°C to 125°C	3.7			3.9			4.6			5.9			ns
		A	B	Open-Drain	-40°C to 125°C	3.7			3.9			4.6			5.9			ns
$t_{PLH}$	Propagation Delay (Low-to-High)	A	B	Push-Pull	-40°C to 125°C	8.4			6.0			5.2			4.8			ns
		A	B	Open-Drain	-40°C to 125°C	4.9			2.7			3.6			4.7			ns
$t_{PHL}$	Propagation Delay (Hight-to-Low)	B	A	Push-Pull	-40°C to 125°C	4.0			2.4			2.9			4.1			ns
		B	A	Open-Drain	-40°C to 125°C	4.0			3.9			4.3			5.2			ns

PARAMETER		FROM	TO	Test Conditions		B-Port Supply Voltage (V <sub>CCB</sub> )												UNIT
						1.8 ± 0.15V			2.5 ± 0.2V			3.3 ± 0.3V			5.0 ± 0.5V			
						MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t <sub>PLH</sub>	Propagation Delay (Low-to-High)	B	A	Push-Pull	-40°C to 125°C	9.0			1.0			0.5			0.5			ns
		B	A	Open-Drain	-40°C to 125°C	24.5			0.5			0.5			0.5			ns
t <sub>en</sub>	Enable Time	OE	A or B		-40°C to 125°C	200			200			250			275			ns
t <sub>dis</sub>	Disable Time	OE	A or B		-40°C to 125°C	200			200			200			200			ns
t <sub>rA</sub>	Ouput Rise Time	B	A	Push-Pull	-40°C to 125°C	12.6			9.5			8.3			7.5			ns
		B	A	Open-Drain	-40°C to 125°C	120.6			91.4			74.0			53.7			ns
t <sub>rB</sub>	Ouput Rise Time	A	B	Push-Pull	-40°C to 125°C	13.3			10.9			8.9			6.8			ns
		A	B	Open-Drain	-40°C to 125°C	110.8			82.3			61.8			36.3			ns
t <sub>fA</sub>	Output Fall Time	B	A	Push-Pull	-40°C to 125°C	5.1			3.9			3.3			3.3			ns
		B	A	Open-Drain	-40°C to 125°C	6.1			6.0			5.9			6.9			ns
t <sub>fB</sub>	Output Fall Time	A	B	Push-Pull	-40°C to 125°C	6.5			7.1			8.0			10.8			ns
		A	B	Open-Drain	-40°C to 125°C	6.2			7.1			8.0			10.8			ns

### 5.9 Switching Characteristics, V<sub>CCA</sub> = 2.5 ± 0.2V

PARAMETER		FROM	TO	Test Conditions		B-Port Supply Voltage (V <sub>CCB</sub> )												UNIT
						1.8 ± 0.15V			2.5 ± 0.2V			3.3 ± 0.3V			5.0 ± 0.5V			
						MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t <sub>PHL</sub>	Propagation Delay (Hight-to-Low)	A	B	Push-Pull	-40°C to 125°C	3.5			2.7			2.9			3.7			ns
		A	B	Open-Drain	-40°C to 125°C	3.5			2.7			2.9			3.7			ns
t <sub>PLH</sub>	Propagation Delay (Low-to-High)	A	B	Push-Pull	-40°C to 125°C	1.5			2.5			3.7			3.5			ns
		A	B	Open-Drain	-40°C to 125°C	0.5			0.5			1.0			1.0			ns
t <sub>PHL</sub>	Propagation Delay (Hight-to-Low)	B	A	Push-Pull	-40°C to 125°C	3.6			2.0			2.4			3.5			ns
		B	A	Open-Drain	-40°C to 125°C	4.2			2.8			3.0			3.6			ns
t <sub>PLH</sub>	Propagation Delay (Low-to-High)	B	A	Push-Pull	-40°C to 125°C	9.2			1.5			0.8			0.5			ns
		B	A	Open-Drain	-40°C to 125°C	27.1			2.6			0.75			0.5			ns
t <sub>en</sub>	Enable Time	OE	A or B		-40°C to 125°C	250			200			200			250			ns
t <sub>dis</sub>	Disable Time	OE	A or B		-40°C to 125°C	250			200			200			200			ns
t <sub>rA</sub>	Ouput Rise Time	B	A	Push-Pull	-40°C to 125°C	11.8			8.1			6.9			6.2			ns
		B	A	Open-Drain	-40°C to 125°C	103.4			89.9			74.0			54.9			ns
t <sub>rB</sub>	Ouput Rise Time	A	B	Push-Pull	-40°C to 125°C	12.0			8.7			7.5			6.1			ns
		A	B	Open-Drain	-40°C to 125°C	111.6			88.1			69.2			44.0			ns

PARAMETER	FROM	TO	Test Conditions		B-Port Supply Voltage ( $V_{CCB}$ )												UNIT	
					1.8 ± 0.15V			2.5 ± 0.2V			3.3 ± 0.3V			5.0 ± 0.5V				
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
$t_{fA}$	Output Fall Time	B	A	Push-Pull	-40°C to 125°C	5.6			3.4			2.5			2.6			ns
		B	A	Open-Drain	-40°C to 125°C	6.4			5.4			5.3			5.7			ns
$t_{fB}$	Output Fall Time	A	B	Push-Pull	-40°C to 125°C	6.2			5.4			5.6			6.9			ns
		A	B	Open-Drain	-40°C to 125°C	6.2			5.4			5.6			6.9			ns

### 5.10 Switching Characteristics, $V_{CCA} = 3.3 \pm 0.3V$

PARAMETER	FROM	TO	Test Conditions		B-Port Supply Voltage ( $V_{CCB}$ )												UNIT	
					1.8 ± 0.15V			2.5 ± 0.2V			3.3 ± 0.3V			5.0 ± 0.5V				
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
$t_{PHL}$	Propagation Delay (High-to-Low)	A	B	Push-Pull	-40°C to 125°C	3.9			2.8			2.2			2.7			ns
		A	B	Open-Drain	-40°C to 125°C	3.9			2.8			2.2			2.7			ns
$t_{PLH}$	Propagation Delay (Low-to-High)	A	B	Push-Pull	-40°C to 125°C	0.8			1.0			1.7			2.7			ns
		A	B	Open-Drain	-40°C to 125°C	1.0			1.0			0.5			1.0			ns
$t_{PHL}$	Propagation Delay (High-to-Low)	B	A	Push-Pull	-40°C to 125°C	4.1			2.0			2.5			3.3			ns
		B	A	Open-Drain	-40°C to 125°C	4.7			3.0			2.4			3.1			ns
$t_{PLH}$	Propagation Delay (Low-to-High)	B	A	Push-Pull	-40°C to 125°C	10.5			5.4			1.3			0.5			ns
		B	A	Open-Drain	-40°C to 125°C	25.4			14.1			1.6			0.5			ns
$t_{en}$	Enable Time	OE	A or B		-40°C to 125°C	250			250			200			250			ns
$t_{dis}$	Disable Time	OE	A or B		-40°C to 125°C	200			200			200			200			ns
$t_{rA}$	Output Rise Time	B	A	Push-Pull	-40°C to 125°C	12.4			7.7			6.4			5.7			ns
		B	A	Open-Drain	-40°C to 125°C	84.9			88.6			74.7			57.0			ns
$t_{rB}$	Output Rise Time	A	B	Push-Pull	-40°C to 125°C	11.1			7.6			6.6			5.6			ns
		A	B	Open-Drain	-40°C to 125°C	99.1			90.0			75.6			51.5			ns
$t_{fA}$	Output Fall Time	B	A	Push-Pull	-40°C to 125°C	6.4			3.2			2.5			2.5			ns
		B	A	Open-Drain	-40°C to 125°C	7.9			5.5			5.1			4.9			ns
$t_{fB}$	Output Fall Time	A	B	Push-Pull	-40°C to 125°C	6.6			5.4			5.4			5.4			ns
		A	B	Open-Drain	-40°C to 125°C	6.6			5.4			5.4			5.4			ns

**5.11 Switching Characteristics:  $T_{sk}$ ,  $T_{MAX}$**   
over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		$V_{CCA}$	$V_{CCB}$	Operating free-air temperature ( $T_A$ )			UNIT
					-40°C to 125°C			
					MIN	TYP	MAX	
$T_{MAX}$ - Maximum Data Rate	50% Duty Cycle Input One channel switching	Push-Pull Driving	$1.2V \pm 0.1V$	$1.8 \pm 0.15V$	24	Mbps		
				$2.5V \pm 0.2V$	24			
				$3.3V \pm 0.3V$	24			
				$5V \pm 0.5V$	24			
			$1.5V \pm 0.1V$	$1.8 \pm 0.15V$	24			
				$2.5V \pm 0.2V$	24			
				$3.3V \pm 0.3V$	24			
				$5V \pm 0.5V$	50			
			$1.8 \pm 0.15V$	$1.8 \pm 0.15V$	50			
				$2.5V \pm 0.2V$	50			
		$3.3V \pm 0.3V$		50				
		$5V \pm 0.5V$		50				
		$2.5V \pm 0.2V$	$1.8 \pm 0.15V$	50				
			$2.5V \pm 0.2V$	50				
			$3.3V \pm 0.3V$	50				
			$5V \pm 0.5V$	50				
		$3.3V \pm 0.3V$	$1.8 \pm 0.15V$	50				
			$2.5V \pm 0.2V$	50				
			$3.3V \pm 0.3V$	50				
			$5V \pm 0.5V$	50				
	Open-Drain Driving	$1.2V \pm 0.1V$	$1.8 \pm 0.15V$	2				
			$2.5V \pm 0.2V$	2				
			$3.3V \pm 0.3V$	2				
			$5V \pm 0.5V$	2				
		$1.5V \pm 0.1V$	$1.8 \pm 0.15V$	2				
			$2.5V \pm 0.2V$	2				
			$3.3V \pm 0.3V$	2				
			$5V \pm 0.5V$	2				
		$1.8 \pm 0.15V$	$1.8 \pm 0.15V$	2				
			$2.5V \pm 0.2V$	2				
	$3.3V \pm 0.3V$		2					
	$5V \pm 0.5V$		2					
	$2.5V \pm 0.2V$	$1.8 \pm 0.15V$	2					
		$2.5V \pm 0.2V$	2					
		$3.3V \pm 0.3V$	2					
		$5V \pm 0.5V$	2					
	$3.3V \pm 0.3V$	$1.8 \pm 0.15V$	2					
		$2.5V \pm 0.2V$	2					
		$3.3V \pm 0.3V$	2					
		$5V \pm 0.5V$	2					

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V <sub>CCA</sub>	V <sub>CCB</sub>	Operating free-air temperature (T <sub>A</sub> )			UNIT
					-40°C to 125°C			
					MIN	TYP	MAX	
t <sub>w</sub>	Pulse Duration, Data Inputs	Push-Pull Driving	1.2V ± 0.1V to 3.3V ± 0.3V	1.8V ± 0.15V to 5.5V ± 0.5V	20			ns
		Open-Drain Driving	1.2V ± 0.1V to 3.3V ± 0.3V	1.8V ± 0.15V to 5.5V ± 0.5V	500			
t <sub>sk</sub> - Output skew	Skew between any two outputs of the same package switching in the same direction	Push-Pull Driving	1.2V ± 0.1V to 3.3V ± 0.3V	1.8V ± 0.15V to 5.5V ± 0.5V	1			ns
		Open-Drain Driving	1.2V ± 0.1V to 3.3V ± 0.3V	1.8V ± 0.15V to 5.5V ± 0.5V	1			

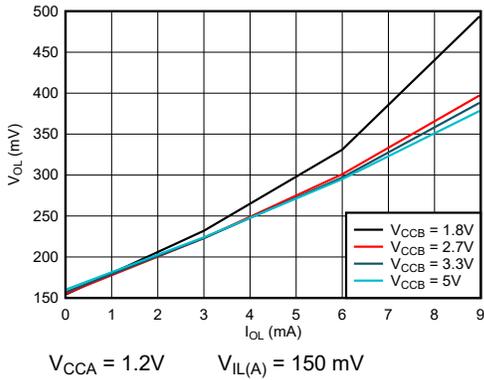
### 5.12 Operating Characteristics: V<sub>CCA</sub> = 1.5V to 3.3V, V<sub>CCB</sub> = 1.5V to 3.3V

T<sub>A</sub> = 25°C <sup>(1)</sup>

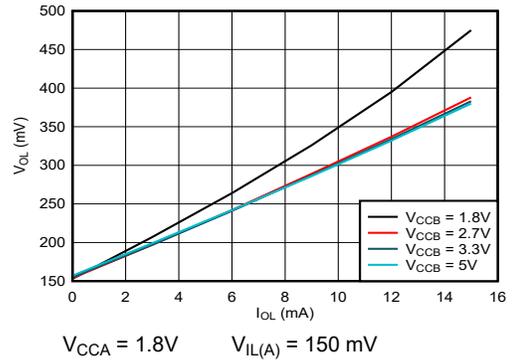
PARAMETER		Test Conditions	Supply Voltage (V <sub>CCA</sub> = V <sub>CCB</sub> , unless otherwise noted)						UNIT		
			1.2 ± 0.1V <sup>(4)</sup>	1.5 ± 0.1V <sup>(4)</sup>	1.8 ± 0.15V	2.5 ± 0.2V	3.3 ± 0.3V	5.0 ± 0.5V			
			TYP	TYP	TYP	TYP	TYP	TYP			
C <sub>pdA</sub> <sup>(2)</sup>	A-port input, B-port output to B: outputs enabled	A Port CL = 0, RL = Open f = 10MHz t <sub>rise</sub> = t <sub>fall</sub> = 1ns	5.0	4.4	4.1	4.2	4.7	5.0	pF		
	B-port input, A-port output to B: outputs enabled		8.8	8.5	9.0	7.3	7.8	3.9			
C <sub>pdB</sub> <sup>(3)</sup>	A-port input, B-port output to B: outputs enabled		12.5	11.7	11.0	9.9	9.2	12.2			
	B-port input, A-port output to B: outputs enabled		4.3	5.3	5.6	7.1	7.4	8.5			
C <sub>pdA</sub> <sup>(2)</sup>	A-port input, B-port output to B: outputs disabled		B Port CL = 0, RL = Open f = 10MHz t <sub>rise</sub> = t <sub>fall</sub> = 1ns	0.1	0.1	0.1	0.1	0.1		0.1	pF
	B-port input, A-port output to B: outputs disabled			0.2	0.1	0.1	0.1	0.1		0.2	
C <sub>pdB</sub> <sup>(3)</sup>	A-port input, B-port output to B: outputs disabled	0.1		0.2	0.2	0.2	0.2	0.1			
	B-port input, A-port output to B: outputs disabled	0.2		0.2	0.2	0.2	0.18	0.2			

- (1) For additional information about how power dissipation capacitance affects power consumption, see the [CMOS Power Consumption and C<sub>pd</sub> Calculation](#) application note.
- (2) A-Port power dissipation capacitance per transceiver.
- (3) B-Port power dissipation capacitance per transceiver.
- (4) V<sub>CCB</sub> = 1.65V

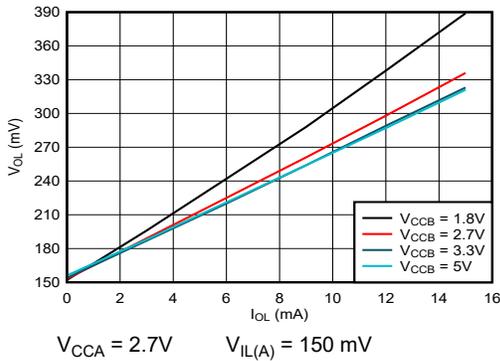
### 5.13 Typical Characteristics



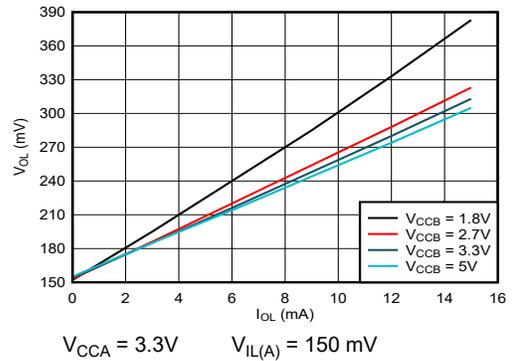
**Figure 5-1. Low-Level Output Voltage ( $V_{OL(Bx)}$ ) vs Low-Level Current ( $I_{OL(Bx)}$ )**



**Figure 5-2. Low-Level Output Voltage ( $V_{OL(Bx)}$ ) vs Low-Level Current ( $I_{OL(Bx)}$ )**



**Figure 5-3. Low-Level Output Voltage ( $V_{OL(Bx)}$ ) vs Low-Level Current ( $I_{OL(Bx)}$ )**



**Figure 5-4. Low-Level Output Voltage ( $V_{OL(Bx)}$ ) vs Low-Level Current ( $I_{OL(Bx)}$ )**

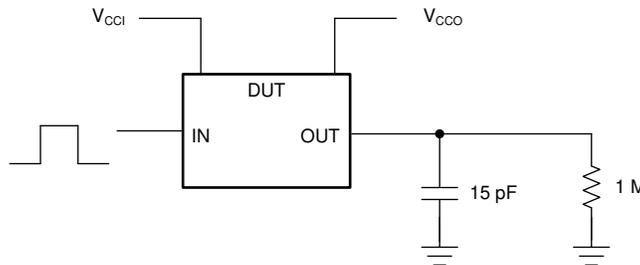
## 6 Parameter Measurement Information

Unless otherwise noted, all input pulses are supplied by generators having the following characteristics:

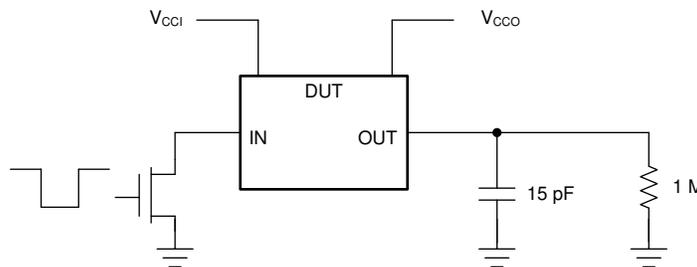
- PRR 10 MHz
- $Z_O = 50\Omega$
- $dv/dt \geq 1V/ns$

**Note**

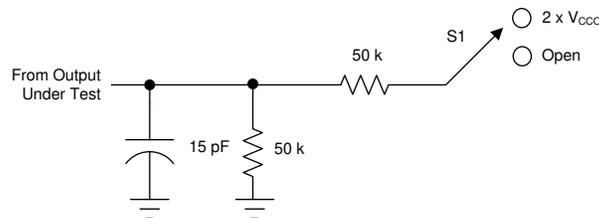
All parameters and waveforms are not applicable to all devices.



**Figure 6-1. Data Rate, Pulse Duration, Propagation Delay, Output Rise And Fall Time Measurement Using A Push-Pull Driver**



**Figure 6-2. Data Rate, Pulse Duration, Propagation Delay, Output Rise And Fall Time Measurement Using An Open-Drain Driver**



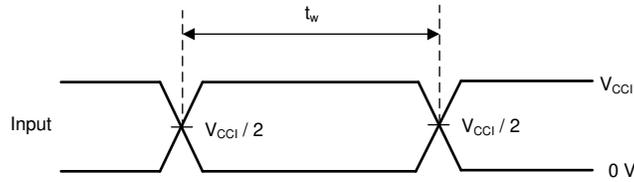
**Figure 6-3. Load Circuit For Enable / Disable Time Measurement**

**Table 6-1. Switch Configuration For Enable / Disable Timing**

TEST	S1
$t_{PZL}^{(2)}, t_{PLZ}^{(1)}$	$2 \times V_{CCO}$
$t_{PHZ}^{(1)}, t_{PZH}^{(2)}$	Open

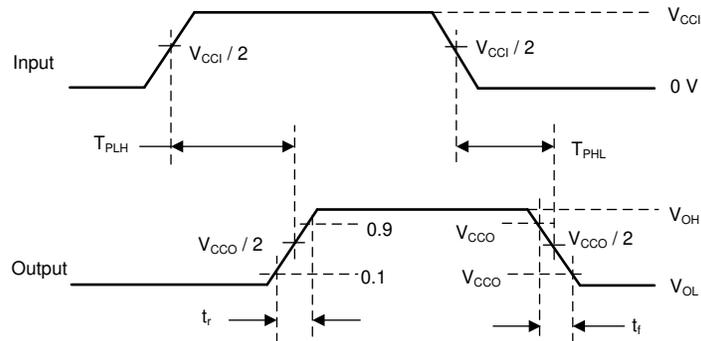
(1)  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .

(2)  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .



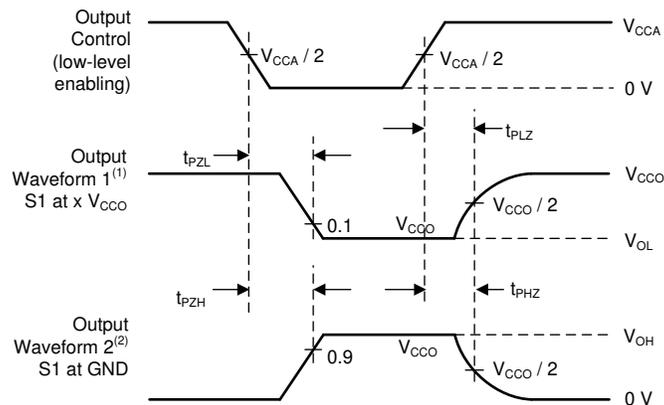
(1) All input pulses are measured one at a time, with one transition per measurement.

**Figure 6-4. Voltage Waveforms Pulse Duration**



(1) All input pulses are measured one at a time, with one transition per measurement.

**Figure 6-5. Voltage Waveforms Propagation Delay Times**



(1) Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.

(2) Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.

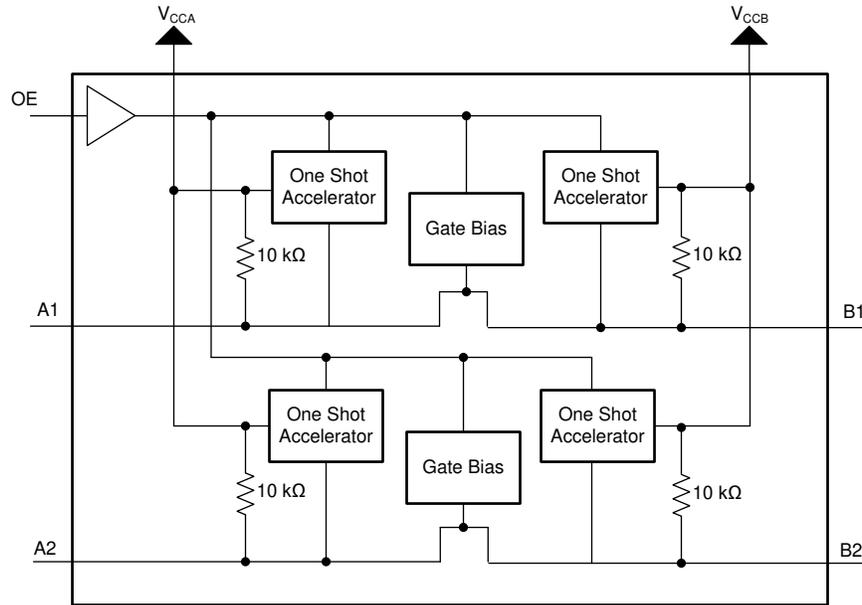
**Figure 6-6. Voltage Waveforms Enable And Disable Times**

## 7 Detailed Description

### 7.1 Overview

The TXS0102W-Q1 device is a directionless voltage-level translator specifically designed for translating logic voltage levels. The A port is able to accept I/O voltages ranging from 1.2V to 3.6V, while the B port can accept I/O voltages from 1.65V to 5.5V. The device is a pass-gate architecture with edge-rate accelerators (one-shots) to improve the overall data rate. 10kΩ pullup resistors, commonly used in open-drain applications, have been conveniently integrated so that an external resistor is not needed. While this device is designed for open-drain applications, the device can also translate push-pull CMOS logic outputs.

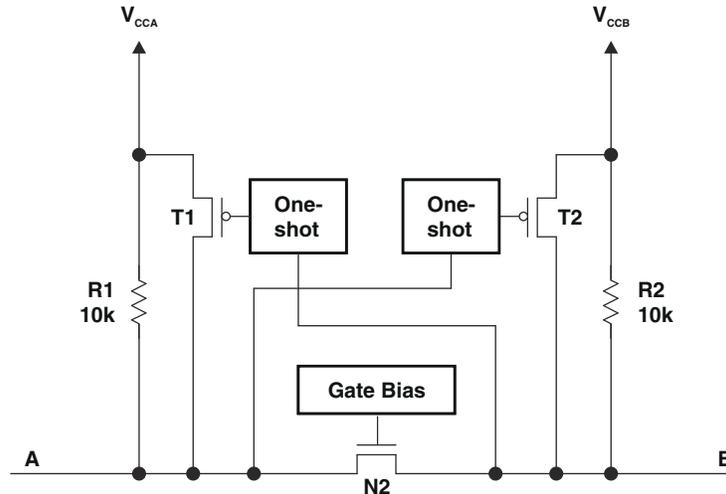
### 7.2 Functional Block Diagram



## 7.3 Feature Description

### 7.3.1 Architecture

The TXS0102W-Q1 architecture (see [Figure 7-1](#)) is an auto-direction-sensing based translator that does not require a direction-control signal to control the direction of data flow from A to B or from B to A.



**Figure 7-1. Architecture of a TXS0102W-Q1 Cell**

These two bidirectional channels independently determine the direction of data flow without a direction-control signal. Each I/O pin can be automatically reconfigured as either an input or an output, which is how this auto-direction feature is realized.

The TXS0102W-Q1 device is part of TI's *Switch* type voltage translator family and employs two key circuits to enable this voltage translation:

1. An N-channel pass-gate transistor topology that ties the A-port to the B-port and
2. Output one-shot (O.S.) edge-rate accelerator circuitry to detect and accelerate rising edges on the A or B ports

For bidirectional voltage translation, pull-up resistors are included on the device for dc current sourcing capability. The  $V_{GATE}$  gate bias of the N-channel pass transistor is set at approximately one threshold voltage ( $V_T$ ) above the  $V_{CC}$  level of the low-voltage side. Data can flow in either direction without guidance from a control signal.

The O.S. rising-edge rate accelerator circuitry speeds up the output slew rate by monitoring the input edge for transitions, helping maintain the data rate through the device. During a low-to-high signal rising edge, the O.S. circuits turn on the PMOS transistors (T1, T2) to increase the current drive capability of the driver for approximately 30ns or 95% of the input edge, whichever occurs first.

This edge-rate acceleration provides high ac drive by bypassing the internal 10k $\Omega$  pull-up resistors during the low-to-high transition to speed up the signal. The output resistance of the driver is decreased to approximately 50 $\Omega$  to 70 $\Omega$  during this acceleration phase. To minimize dynamic  $I_{CC}$  and the possibility of signal contention, the user should wait for the O.S. circuit to turn off before applying a signal in the opposite direction. The worst-case duration is equal to the minimum pulse-width number.

### 7.3.2 Input Driver Requirements

The continuous dc-current *sinking* capability is determined by the external system-level open-drain (or push-pull) drivers that are interfaced to the TXS0102W-Q1 I/O pins. Since the high bandwidth of these bidirectional I/O circuits is used to facilitate this fast change from an input to an output and an output to an input, they have a modest dc-current *sourcing* capability of hundreds of micro-Amps, as determined by the internal 10k $\Omega$  pullup resistors.

The fall time ( $t_{fA}$ ,  $t_{fB}$ ) of a signal depends on the edge-rate and output impedance of the external device driving TXS0102W-Q1 data I/Os, as well as the capacitive loading on the data lines.

Similarly, the  $t_{PHL}$  and max data rates also depend on the output impedance of the external driver. The values for  $t_{fA}$ ,  $t_{fB}$ ,  $t_{PHL}$ , and maximum data rates in the data sheet assume that the output impedance of the external driver is less than 50 $\Omega$ .

### 7.3.3 Output Load Considerations

TI recommends careful PCB layout practices with short PCB trace lengths to avoid excessive capacitive loading and to ensure that proper O.S. triggering takes place. PCB signal trace-lengths must be kept short enough so that the round-trip delay of any reflection is less than the one-shot duration, causing any reflection to encounter low impedance at the source driver. The O.S. circuits are designed to stay on for approximately 30ns. The maximum capacitance of the lumped load that can be driven also depends directly on the one-shot duration.

With very heavy capacitive loads, the one-shot can time-out before the signal is driven fully to the positive rail. The O.S. duration has been set to best optimize trade-offs between dynamic ICC, load driving capability, and maximum bit-rate considerations. Both PCB trace length and connectors add to the capacitance that the TXS0102W-Q1 device output sees, so it is recommended that this lumped-load capacitance be considered to avoid O.S. retriggering, bus contention, output signal oscillations, or other adverse system-level affects.

### 7.3.4 Enable and Disable

The TXS0102W-Q1 device has an OE input that is used to disable the device by setting OE low, which places all I/Os in the Hi-Z state. The disable time ( $t_{dis}$ ) indicates the delay between the time when OE goes low and when the outputs are disabled (Hi-Z). The enable time ( $t_{en}$ ) indicates the amount of time the user must allow for the one-shot circuitry to become operational after OE is taken high.

### 7.3.5 Pullup or Pulldown Resistors on I/O Lines

Each A-port I/O has an internal 10k $\Omega$  pullup resistor to  $V_{CCA}$ , and each B-port I/O has an internal 10k $\Omega$  pullup resistor to  $V_{CCB}$ . If a smaller value of pullup resistor is required, an external resistor must be added from the I/O to  $V_{CCA}$  or  $V_{CCB}$  (in parallel with the internal 10k $\Omega$  resistors). Adding lower value pull-up resistors will effect  $V_{OL}$  levels, however. The internal pull-ups of the TXS0102W-Q1 are disabled when the OE pin is low.

## 7.4 Device Functional Modes

The device has two functional modes, enabled and disabled. To disable the device set the OE input low, which places all I/Os in a high impedance state. Setting the OE input high will enable the device.

## 8 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 8.1 Application Information

The TXS0102W-Q1 device can be used to bridge the digital-switching compatibility gap between two voltage nodes to successfully interface logic threshold levels found in electronic systems. It should be used in a point-to-point topology for interfacing devices or systems operating at different interface voltages with one another. Its primary target application use is for interfacing with open-drain drivers on the data I/Os such as I<sup>2</sup>C or 1-wire, where the data is bidirectional and no control signal is available. The device can also be used in applications where a push-pull driver is connected to the data I/Os, but the TXB0102 might be a better option for such push-pull applications.

### 8.2 Typical Application

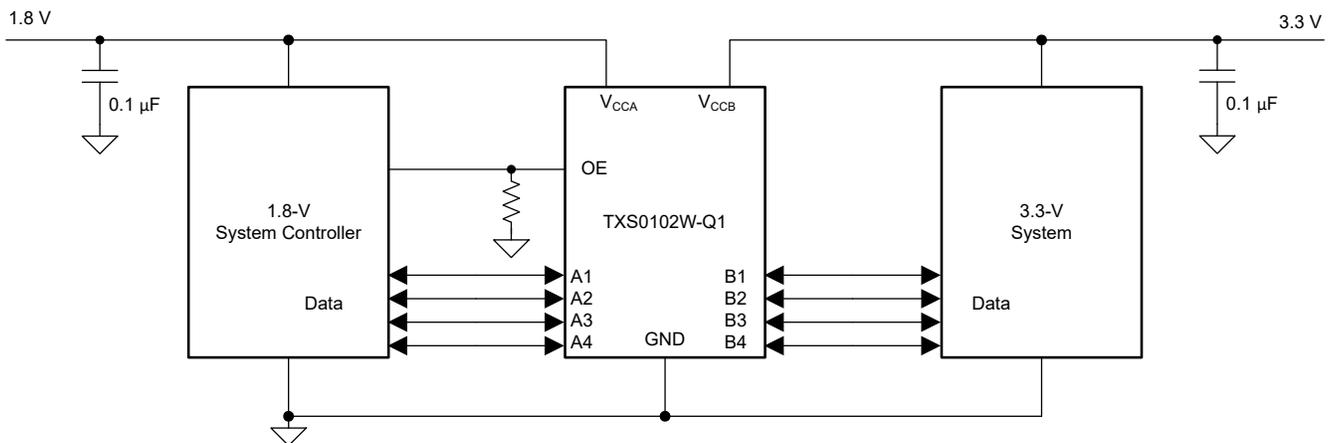


Figure 8-1. Typical Application Circuit

#### 8.2.1 Design Requirements

For this design example, use the parameters listed in [Table 8-1](#). And make sure the  $V_{CCA} \leq V_{CCB}$ .

Table 8-1. Design Parameters

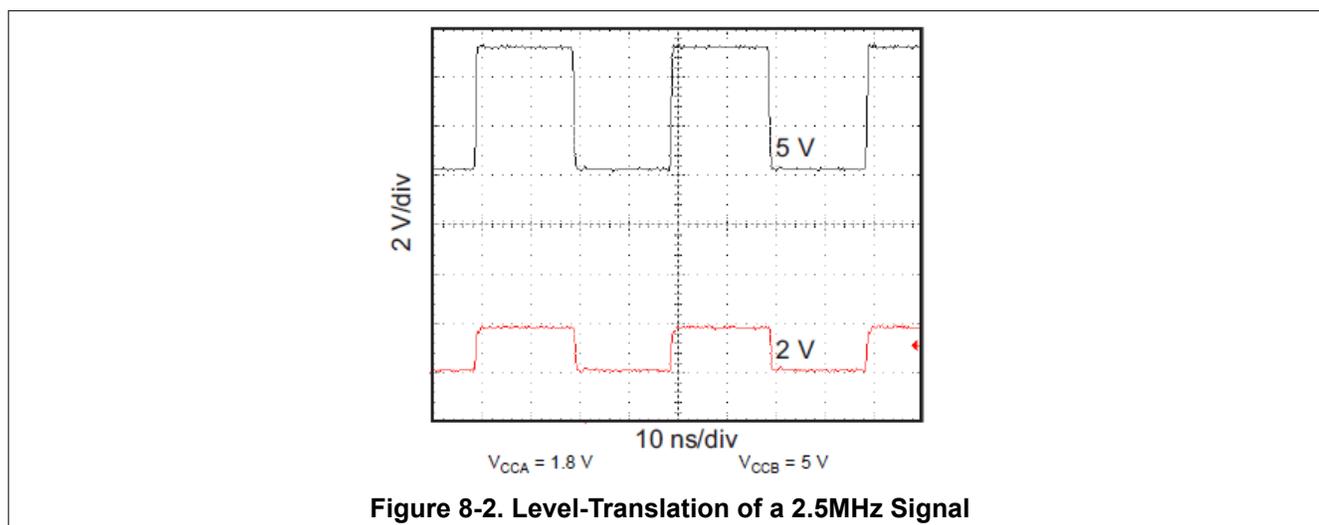
DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	1.2 to 3.6V
Output voltage range	1.65 to 5.5V

### 8.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range:
  - Use the supply voltage of the device that is driving the TXS0102W-Q1 device to determine the input voltage range. For a valid logic high the value must exceed the  $V_{IH}$  of the input port. For a valid logic low the value must be less than the  $V_{IL}$  of the input port.
- Output voltage range:
  - Use the supply voltage of the device that the TXS0102W-Q1 device is driving to determine the output voltage range.
  - The TXS0102W-Q1 device has 10k $\Omega$  internal pullup resistors. External pullup resistors can be added to reduce the total RC of a signal trace if necessary.
  - An external pull down resistor decreases the output  $V_{OH}$  and  $V_{OL}$ . Use Equation 1 to calculate the  $V_{OH}$  as a result of an external pull down resistor.
 
$$V_{OH} = V_{CCx} \times R_{PD} / (R_{PD} + 10k\Omega)$$
 Where:
    - $V_{CCx}$  is the supply voltage on either  $V_{CCA}$  or  $V_{CCB}$
    - $R_{PD}$  is the value of the external pull down resistor

### 8.2.3 Application Curves



### 8.3 Power Supply Recommendations

During operation, ensure that  $V_{CCA} \leq V_{CCB}$  at all times. The sequencing of each power supply will not damage the device during the power up operation, so either power supply can be ramped up first. The output-enable (OE) input circuit is designed so that it is supplied by  $V_{CCA}$  and when the (OE) input is low, all outputs are placed in the high-impedance state. To put the outputs in the high-impedance state during power up or power down, tie the OE input pin to GND through a pulldown resistor and must not be enabled until  $V_{CCA}$  and  $V_{CCB}$  are fully ramped and stable. The current-sourcing capability of the driver determines the minimum value of the pulldown resistor to ground.

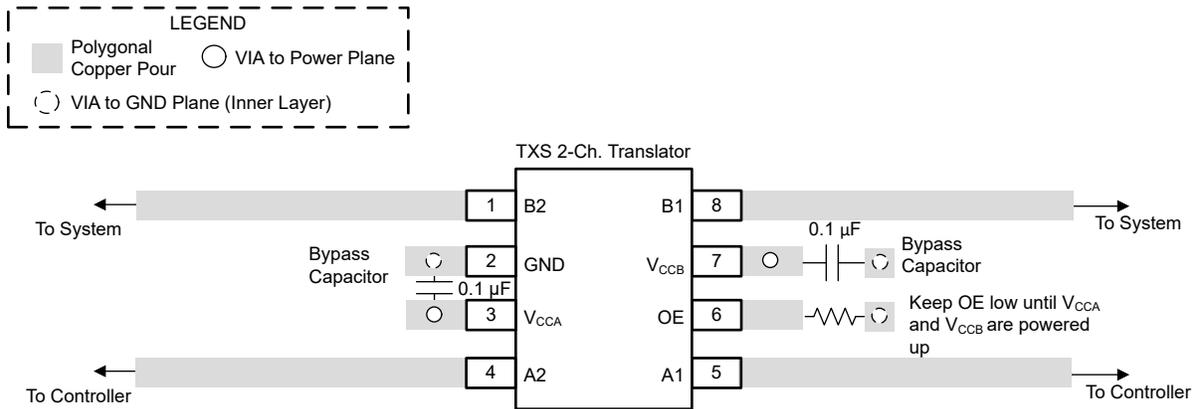
## 8.4 Layout

### 8.4.1 Layout Guidelines

For device reliability, it is recommended to follow common printed-circuit board layout guidelines such as follows:

- Bypass capacitors should be used on power supplies and should be placed as close as possible to the  $V_{CCA}$ ,  $V_{CCB}$  pin, and  $G_{ND}$  pin.
- Short trace lengths should be used to avoid excessive loading.
- PCB signal trace-lengths must be kept short enough so that the round-trip delay of any reflection is less than the one-shot duration (approximately 30ns) causing any reflection to encounter low impedance at the source driver.

### 8.4.2 Layout Example



**Figure 8-3. TXS0102W-Q1 Layout Example**

## 9 Device and Documentation Support

### 9.1 Documentation Support

#### 9.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, [A Guide to Voltage Translation With TXS-Type Translators application note](#)
- Texas Instruments, [Factors Affecting VOL for TXS and LSF Auto-bidirectional Translation Devices application note](#)
- Texas Instruments, [Biasing Requirements for TXS, TXB, and LSF Auto-Bidirectional Translators application note](#)
- Texas Instruments, [Effects of pullup and pulldown resistors on TXS and TXB devices application note](#)
- Texas Instruments, [Introduction to logic application note](#)
- Texas Instruments, [TI Logic and Linear Products Guide selection and solution guides](#)
- Texas Instruments, [Washing Machine Solutions Guide selection and solution guides](#)
- Texas Instruments, [TI Smartphone Solutions Guide selection and solution guides](#)

### 9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 9.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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### 9.4 Trademarks

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### 9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 9.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (April 2025) to Revision A (January 2026)	Page
• First public release of the data sheet.....	1

DATE	REVISION	NOTES
April 2025	*	Initial Release

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TXS0102WQDCURQ1	Active	Production	VSSOP (DCU)   8	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

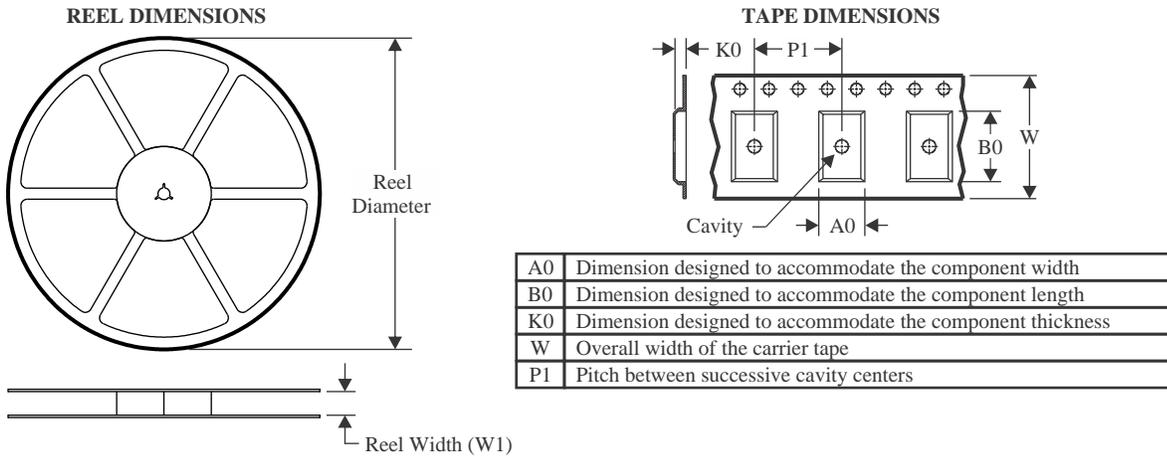
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TXS0102WQDCURQ1	VSSOP	DCU	8	3000	178.0	9.0	2.25	3.35	1.05	4.0	8.0	Q3

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TXS0102WQDCURQ1	VSSOP	DCU	8	3000	180.0	180.0	18.0

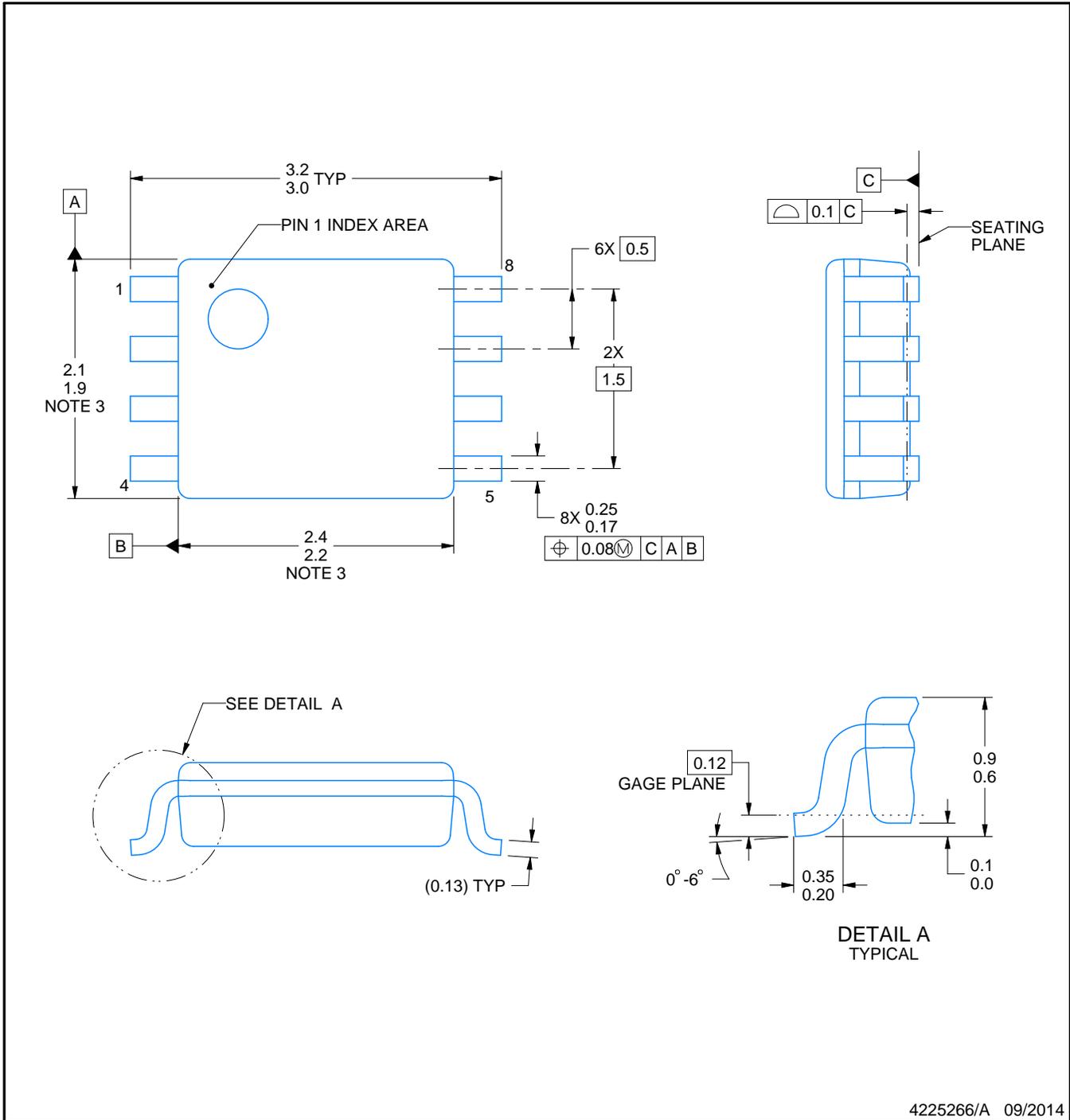
# DCU0008A



# PACKAGE OUTLINE

## VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE



4225266/A 09/2014

**NOTES:**

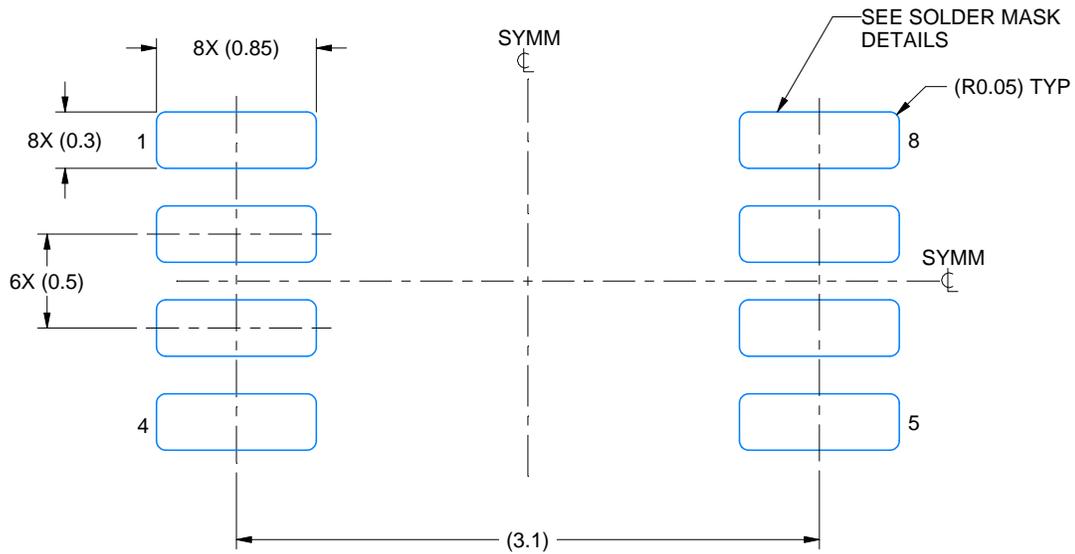
- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- Reference JEDEC registration MO-187 variation CA.

# EXAMPLE BOARD LAYOUT

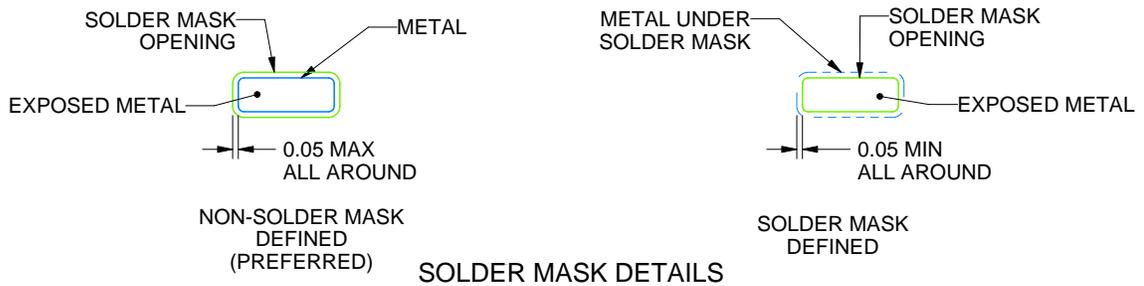
DCU0008A

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 25X



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NOTES: (continued)

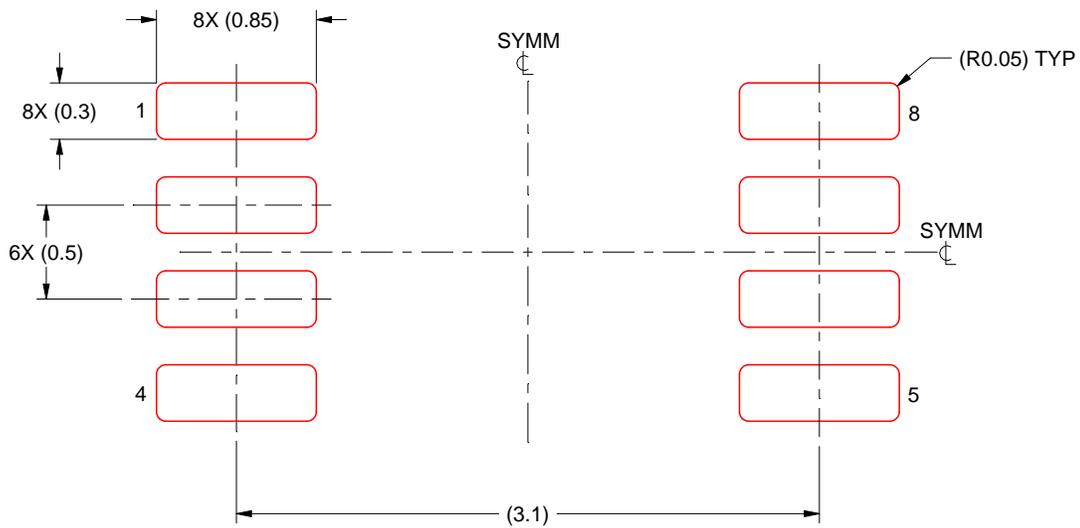
- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DCU0008A

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 25X

4225266/A 09/2014

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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