TXS0108W-Q1 Automotive 8-Bit Bi-directional, Low-Voltage Level Shifter for Open-Drain and Push-Pull Applications

1 Features

- AEC-Q100 qualified for automotive applications:
  - Device temperature grade 1: –40°C to 125°C
  - Device HBM ESD classification level 2
  - Device CDM ESD classification level C6
- No direction-control signal needed
- Maximum data rates:
  - 110Mbps (push pull)
  - 1.2Mbps (open drain)
- 1.2V to 3.6V on A port and 1.65V to 5.5V on B port
- V_{CCA} may be greater than, less than, or equal to V_{CCB}
- No power-supply sequencing required – either V_{CCA} or V_{CCB} can be ramped first
- Latch-up performance exceeds 100mA per JESD 78, class II
- ESD protection exceeds JESD 22 (A port):
  - 2000V Human Body Model (A114-B)
  - 150V Machine Model (A115-A)
  - 1000V Charged-Device Model (C101)
- IEC 61000-4-2 ESD (B-port):
  - ± 8kV Contact Discharge

2 Applications

- Automotive

3 Description

TXS0108W-Q1 is an 8-bit non-inverting level translator which uses two separate configurable power-supply rails. The A port tracks the V_{CCA} pin supply voltage. The V_{CCA} pin accepts any supply voltage between 1.2V and 3.6V. The B port tracks the V_{CCB} pin supply voltage. The V_{CCB} pin accepts any supply voltage between 1.65V and 5.5V. Two input supply pins allows for low Voltage bidirectional translation between any of the 1.2V, 1.8V, 2.5V, 3.3V, and 5V voltage nodes.

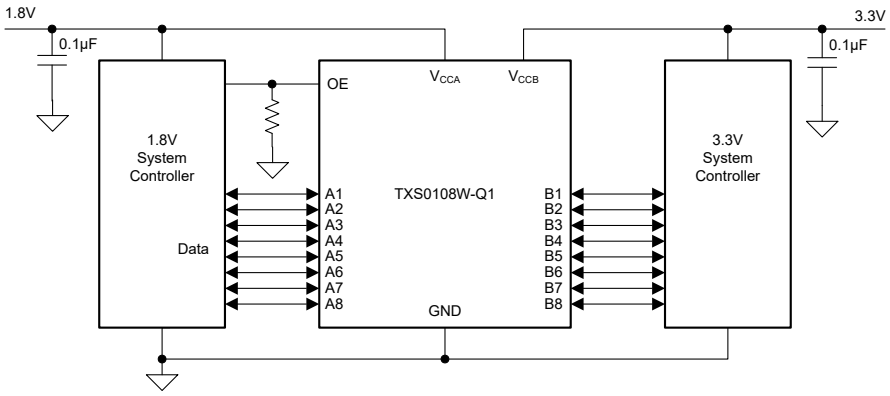
When the output-enable (OE) input is low, all outputs are placed in the high-impedance (Hi-Z) state.

To put the device in the Hi-Z state during power-up or power-down periods, tie OE to GND through a pull-down resistor. The current-sourcing capability of the driver determines the minimum value of the resistor.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TXS0108W-Q1	PW (TSSOP, 20)	6.50mm × 6.40mm
	RKS (VQFN, 20)	4.5mm x 2.5mm
	DGS (VSSOP, 20)	3.00mm x 5.10mm

(1) For more information, see Section 12
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Application

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4 Pin Configuration and Functions

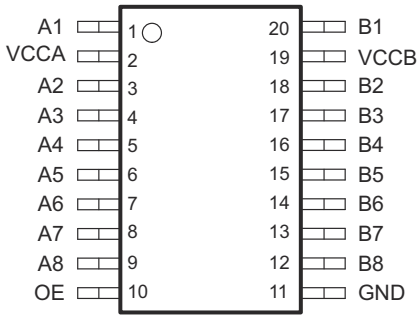


Figure 4-1. PW or DGS Package, 20-Pin TSSOP (Top View)

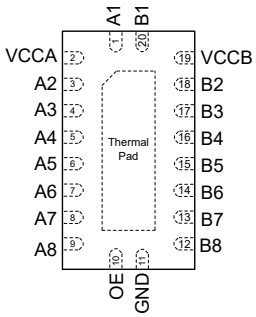


Figure 4-2. RKS Package, 20-Pin VQFN (Top View)

Table 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
A1	1	I/O	Input/output 1. Referenced to V_{CCA}
A2	3	I/O	Input/output 2. Referenced to V_{CCA}
A3	4	I/O	Input/output 3. Referenced to V_{CCA}
A4	5	I/O	Input/output 4. Referenced to V_{CCA}
A5	6	I/O	Input/output 5. Referenced to V_{CCA}
A6	7	I/O	Input/output 6. Referenced to V_{CCA}
A7	8	I/O	Input/output 7. Referenced to V_{CCA}
A8	9	I/O	Input/output 8. Referenced to V_{CCA}
B1	20	I/O	Input/output 1. Referenced to V_{CCB}
B2	18	I/O	Input/output 2. Referenced to V_{CCB}
B3	17	I/O	Input/output 3. Referenced to V_{CCB}
B4	16	I/O	Input/output 4. Referenced to V_{CCB}
B5	15	I/O	Input/output 5. Referenced to V_{CCB}
B6	14	I/O	Input/output 6. Referenced to V_{CCB}
B7	13	I/O	Input/output 7. Referenced to V_{CCB}
B8	12	I/O	Input/output 8. Referenced to V_{CCB}
GND	11	–	Ground
OE	10	I	3-state output-mode enable. Pull OE low to place all outputs in 3-state mode. Referenced to V_{CCA}.
VCCA	2	–	A-port supply voltage. 1.2V ≤ V_{CCA} ≤ 3.6V.
VCCB	19	–	B-port supply voltage. 1.65V ≤ V_{CCB} ≤ 5.5V.

(1) I = input, O = output

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CCA}	Supply voltage A		–0.5	4.6	V
V_{CCB}	Supply voltage B		–0.5	6.5	V
V_I	Input Voltage(2)	I/O Ports (A Port)	–0.5	4.6	V
V_I		I/O Ports (B Port)	–0.5	6.5	V
V_O	Voltage applied to any output in the high-impedance or power-off state(2)	A Port	–0.5	4.6	V
		B Port	–0.5	6.5	
V_O	Voltage applied to any output in the high or low state(2) (3)	A Port	–0.5	V_{CCA} + 0.5	V
		B Port	–0.5	V_{CCB} + 0.5	
I_{IK}	Input clamp current	V_I < 0		–50	mA
I_{OK}	Output clamp current	V_O < 0		–50	mA
I_O	Continuous output current		–50	50	mA
	Continuous current through V_{CC} or GND		–100	100	mA
T_j	Junction Temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Section 5.1* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Section 5.3* Exposure beyond the limits listed in *Section 5.3* may affect device reliability.
(2) The input voltage and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The output positive-voltage rating may be exceeded up to 6.5V maximum if the output current rating is observed.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002	±2000	V
$V_{(ESD)}$	Electrostatic discharge	Charged device model (CDM), per AEC Q100-011	±1000	V
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 ESD (B Port) Contact Discharge	±8000	V

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted) (1) (2) (3)

			V_{CCA}	V_{CCB}	MIN	MAX	UNIT
V_{CCA}	Supply voltage A				1.2	3.6	V
V_{CCB}	Supply voltage B				1.65	5.5	V
V_{IH}	High-level input voltage	A-port I/O's	1.2V to 1.95V	1.65V to 5.5V	V_{CCI} - 0.2	V_{CCI}	V
			1.95V to 3.6V	2.3V to 5.5V	V_{CCI} - 0.4	V_{CCI}	
		B-port I/O's	1.2V to 3.6V	1.65V to 5.5V	V_{CCI} - 0.4	V_{CCI}	
		OE Input	1.2V to 3.6V	1.65V to 5.5V	V_{CCA} x 0.65	5.5	
V_{IL}	Low-level input voltage	A-port I/O's	1.2V to 3.6V	1.65V to 5.5V	0	0.15	V
		B-port I/O's	1,2V to 3.6V	1.65V to 5.5V	0	0.15	
		OE Input	1.2V to 3.6V	1.65V to 5.5V	0	V_{CCA} x 0.35	
V_{RTA}	RTA Activation Threshold	A-port I/O's	1.2V to 3.6V	1.65V to 5.5V	V_{CCI} x 0.30		V
		B-port I/O's	1.2V to 3.6V	1.65V to 5.5V	V_{CCI} x 0.30		
Δt/Δv	Input transition rise and fall time	A/ B-port I/O's, OE Input	1.2V to 3.6V	1.65V to 5.5V		10	ns/V
T_A	Operating free-air temperature				–40	125	°C

(1) V_{CCI} is the V_{CC} associated with the input port.
(2) V_{CCO} is the V_{CC} associated with the output port.
(3) All control inputs and data I/Os of this device have weak pulldowns to ensure the line is not floating when undefined external to the device. The input leakage from these weak pulldowns is defined by the I_I specification indicated under *Section 5.5*.

5.4 Thermal Information

THERMAL METRIC (1)		TXS0108W-Q1			
		PW (TSSOP)	DGS(VSSOP)	RKS (VQFN)	
		20 PINS	20 PINS	20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	88.9	96.0	54.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	32.9	38.7	54.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	50.9	53.0	27.8	°C/W
Y_{JT}	Junction-to-top characterization parameter	1.4	2.1	2.9	°C/W
Y_{JB}	Junction-to-board characterization parameter	50.5	52.6	27.7	°C/W
$R_{\theta JC(bottom)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	11.5	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)(1) (2)

PARAMETER		TEST CONDITIONS	V_{CCA}	V_{CCB}	Operating free-air temperature (T_A)									UNIT
					25°C			–40°C to 85°C			–40°C to 125°C			
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{OHA}	Port A output high voltage	I_{OH} = –20uA, $V_{IB} \geq V_{CCB} - 0.4V$	1.2V to 3.6V	1.65V to 5.5V	V_{CCA} x 0.67			V_{CCA} x 0.67			V_{CCA} x 0.67			V
V_{OLA}	Port A output low voltage	I_{OL} = 180uA, $V_{IB} \leq 0.15V$	1.2	1.65V to 5.5V		0.16				0.2			0.2	V
		I_{OL} = 220uA, $V_{IB} \leq 0.15V$	1.65	1.65V to 5.5V		0.16				0.2			0.2	
		I_{OL} = 300uA, $V_{IB} \leq 0.15V$	2.3	1.65V to 5.5V		0.16				0.2			0.2	
		I_{OL} = 400uA, $V_{IB} \leq 0.15V$	3	1.65V to 5.5V		0.16				0.2			0.2	
V_{OHB}	Port B output high voltage	I_{OH} = –20uA, $V_{IA} \geq V_{CCA} - 0.2V$	1.2V to 3.6V	1.65V to 5.5V	V_{CCB} x 0.67			V_{CCB} x 0.67			V_{CCB} x 0.67			V
V_{OLB}	Port B output low voltage	I_{OL} = 220uA, $V_{IA} \leq 0.15V$	1.2V to 3.6V	1.65V		0.16				0.2			0.2	V
		I_{OL} = 300uA, $V_{IA} \leq 0.15V$	1.2V to 3.6V	2.3V		0.16				0.2			0.2	
		I_{OL} = 400uA, $V_{IA} \leq 0.15V$	1.2V to 3.6V	3V		0.17				0.25			0.25	
		I_{OL} = 620uA, $V_{IA} \leq 0.15V$	1.2V to 3.6V	4.5		0.17				0.25			0.25	
I_I	Input leakage current	OE $V_I = V_{CC}$ or GND	1.2V to 3.6V	1.65V to 5.5V	-1		1			1			1	µA
I_{OZ}	High-impedance state output current	A or B Port: $V_I = V_{CCI}$ or GND $V_O = V_{CCO}$ or GND OE = GND	1.2V to 3.6V	1.65V to 5.5V	–1		1	–2		2	–2		2	µA
I_{CCA}	V_{CCA} supply current	$V_I = V_O$ = Open, I_O = 0	1.2V	1.65V to 5.5V		1.5		-5		2			2	µA
			1.4V to 3.6V	1.65V to 5.5V						5			11	
			3.6V	0V						3.6			11	
			0V	5.5V				-2			-2.6			
I_{CCB}	V_{CCB} supply current	$V_I = V_O$ = Open, I_O = 0	1.2V	1.65V to 5.5V		1.5				8.3			13.5	µA
			1.4V to 3.6V	1.65V to 5.5V						9.5			15.2	
			3.6V	0V						1			1	
			0V	5.5V						5.5			14.6	
I_{CCA} + I_{CCB}	Combined supply current	$V_I = V_O$ = Open, I_O = 0	1.2	1.65V to 5.5V		2.4				4			10	µA
			1.4V to 3.6V	1.65V to 5.5V						8			16	
C_i	Control Input Capacitance	OE	3.3V	3.3V		4.5				5.5			6.75	pF

over operating free-air temperature range (unless otherwise noted)(1) (2)

PARAMETER		TEST CONDITIONS	V_{CCA}	V_{CCB}	Operating free-air temperature (T_A)									UNIT
					25°C			–40°C to 85°C			–40°C to 125°C			
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
C_{io}	Input-to-output internal capacitance	A port	3.3V	3.3V		6				7			7.6	pF
		B port	3.3V	3.3V		6.8				8			8	
I_{CCZA}	High-impedance state V_{CCA} supply current	V_I = V_{CCI} or GND I_O = 0, OE = GND	1.2V to 3.6V	1.65V to 5.5V		0.05		-3			-3			µA
I_{CCZB}	High-impedance state V_{CCB} supply current	V_I = V_{CCI} or GND I_O = 0, OE = GND	1.2V to 3.6V	1.65V to 5.5V		4				4			8.5	µA

(1) V_{CCI} is the V_{CC} associated with the input port
(2) V_{CCO} is the V_{CC} associated with the output port

5.6 Switching Characteristics, V_{CCA} = 1.2V

PARAMETER		FROM	TO	Test Conditions		B-Port Supply Voltage (V_{CCB})										UNIT
						1.8 ± 0.15V			2.5 ± 0.2V			3.3 ± 0.3V			5.0 ± 0.5V		
						MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PHL}	Propagation Delay (Hight-to-Low)	A	B	Push-Pull	-40°C to 125°C			6.9			6.8			7.9			10.5	ns
t_{PHL}	Propagation Delay (Hight-to-Low)			Open-Drain	-40°C to 125°C			7.0			6.5			8.0			10.9	ns
t_{PLH}	Propagation Delay (Low-to-High)			Push-Pull	-40°C to 125°C			18.1			14.4			13.8			19.4	ns
t_{PLH}	Propagation Delay (Low-to-High)			Open-Drain	-40°C to 125°C			285.6			282.5			236.3			180.6	ns
t_{PHL}	Propagation Delay (Hight-to-Low)	B	A	Push-Pull	-40°C to 125°C			5.8			5.5			6.4			8.9	ns
t_{PHL}	Propagation Delay (Hight-to-Low)			Open-Drain	-40°C to 125°C			5.8			5.4			6.3			8.9	ns
t_{PLH}	Propagation Delay (Low-to-High)			Push-Pull	-40°C to 125°C			16.2			0.4			1			1	ns
t_{PLH}	Propagation Delay (Low-to-High)			Open-Drain	-40°C to 125°C			39.9			0.5			0.5			0.5	ns
t_{en}	Enable Time	OE	A or B		-40°C to 125°C			304			209			173			149	ns
t_{dis}	Disable Time				-40°C to 125°C			300			300			300			300	ns
t_{rA}	Ouput Rise Time	B	A	Push-Pull	-40°C to 125°C			18.2			13.8			3.1			2.4	ns
t_{rA}	Ouput Rise Time			Open-Drain	-40°C to 125°C			650			422			313			220	ns
t_{rB}	Ouput Rise Time	A	B	Push-Pull	-40°C to 125°C			18.7			14.8			13.7			8	ns
t_{rB}	Ouput Rise Time			Open-Drain	-40°C to 125°C			425			292			174			31.7	ns
t_{fA}	Output Fall Time	B	A	Push-Pull	-40°C to 125°C			5.8			5.1			5.1			5.6	ns
t_{fA}	Output Fall Time			Open-Drain	-40°C to 125°C			6			5.4			5.5			5.6	ns
t_{fB}	Output Fall Time	A	B	Push-Pull	-40°C to 125°C			7.6			8.7			11.2			16.8	ns
t_{fB}	Output Fall Time			Open-Drain	-40°C to 125°C			7.8			9.7			12.8			17	ns

5.7 Switching Characteristics, V_{CCA} = 1.5 ± 0.1V

PARAMETER		FROM	TO	Test Conditions		B-Port Supply Voltage (V_{CCB})								UNIT
						1.8 ± 0.15V			2.5 ± 0.2V			3.3 ± 0.3V			5.0 ± 0.5V			
						MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PHL}	Propagation Delay (Hight-to-Low)	A	B	Push-Pull	-40°C to 125°C			4.9			5.2			6.4			8.0	ns
t_{PHL}	Propagation Delay (Hight-to-Low)			Open-Drain	-40°C to 125°C			4.9			5.2			6.5			8.9	
t_{PLH}	Propagation Delay (Low-to-High)			Push-Pull	-40°C to 125°C			14.1			10			9.2			9.3	
t_{PLH}	Propagation Delay (Low-to-High)			Open-Drain	-40°C to 125°C			211			247			212			144	
t_{PHL}	Propagation Delay (High-to-Low)	B	A	Push-Pull	-40°C to 125°C			4.7			4.3			5.6			7.5	ns
t_{PHL}	Propagation Delay (High-to-Low)			Open-Drain	-40°C to 125°C			4.8			4.3			5.3			7.4	
t_{PLH}	Propagation Delay (Low-to-High)			Push-Pull	-40°C to 125°C			10.7			0.5			1			1.9	
t_{PLH}	Propagation Delay (Low-to-High)			Open-Drain	-40°C to 125°C			102			1			1			1	
t_{en}	Enable Time	OE	A or B	Push-Pull	-40°C to 125°C			282			202			165			136	ns
t_{dis}	Disable Time			Push-Pull	-40°C to 125°C			300			300			300			300	
t_{rA}	Ouput Rise Time	B	A	Push-Pull	-40°C to 125°C			14.2			10.0			8.4			2.4	ns
t_{rA}	Ouput Rise Time			Open-Drain	-40°C to 125°C			630			465			342			227	
t_{rB}	Ouput Rise Time	A	B	Push-Pull	-40°C to 125°C			15.2			11.5			9.6			7.8	
t_{rB}	Ouput Rise Time			Open-Drain	-40°C to 125°C			482			378			245			78.1	
t_{fA}	Output Fall Time	B	A	Push-Pull	-40°C to 125°C			5.4			4.4			4.9			5.3	ns
t_{fA}	Output Fall Time			Open-Drain	-40°C to 125°C			5.4			4.6			4.7			5.5	
t_{fB}	Output Fall Time	A	B	Push-Pull	-40°C to 125°C			6.0			6.1			7.6			9.5	
t_{fB}	Output Fall Time			Open-Drain	-40°C to 125°C			6.0			6.5			8.4			9.3	

5.8 Switching Characteristics, V_{CCA} = 1.8 ± 0.15V

PARAMETER		FROM	TO	Test Conditions		B-Port Supply Voltage (V_{CCB})								UNIT
						1.8 ± 0.15V			2.5 ± 0.2V			3.3 ± 0.3V			5.0 ± 0.5V			
						MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PHL}	Propagation Delay (Hight-to-Low)	A	B	Push-Pull	-40°C to 125°C			4.3			4.0			5.1			6.4	ns
t_{PHL}	Propagation Delay (Hight-to-Low)			Open-Drain	-40°C to 125°C			4.3			4.2			5.1			7.0	
t_{PLH}	Propagation Delay (Low-to-High)			Push-Pull	-40°C to 125°C			12.5			8.6			7.7			7.1	ns
t_{PLH}	Propagation Delay (Low-to-High)			Open-Drain	-40°C to 125°C			190			229			210			141	

PARAMETER		FROM	TO	Test Conditions		B-Port Supply Voltage (V_{CCB})										UNIT
						1.8 ± 0.15V			2.5 ± 0.2V			3.3 ± 0.3V			5.0 ± 0.5V		
						MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PHL}	Propagation Delay (Hight-to-Low)	B	A	Push-Pull	-40°C to 125°C			4.4			3.7			4.3			6.2	ns
t_{PHL}	Propagation Delay (Hight-to-Low)			Open-Drain	-40°C to 125°C			4.5			3.8			4.4			6.2	
t_{PLH}	Propagation Delay (Low-to-High)			Push-Pull	-40°C to 125°C			11.2			1			0.2			2.2	ns
t_{PLH}	Propagation Delay (Low-to-High)			Open-Drain	-40°C to 125°C			160			1			1			1	
t_{en}	Enable Time	OE	A or B	Push-Pull	-40°C to 125°C			347			172			163			133	ns
t_{dis}	Disable Time			Push-Pull	-40°C to 125°C			300			300			300			300	
t_{rA}	Ouput Rise Time	B	A	Push-Pull	-40°C to 125°C			13.1			9.0			7.4			2.4	ns
t_{rA}	Ouput Rise Time			Open-Drain	-40°C to 125°C			627			553			397			261	
t_{rB}	Ouput Rise Time	A	B	Push-Pull	-40°C to 125°C			15			10.0			8.5			6.8	ns
t_{rB}	Ouput Rise Time			Open-Drain	-40°C to 125°C			544			468			334			139	
t_{fA}	Output Fall Time	B	A	Push-Pull	-40°C to 125°C			5.1			4.1			4.4			4.4	ns
t_{fA}	Output Fall Time			Open-Drain	-40°C to 125°C			5.2			4.2			4.3			4.3	
t_{fB}	Output Fall Time	A	B	Push-Pull	-40°C to 125°C			5.2			5.0			6.0			8	ns
t_{fB}	Output Fall Time			Open-Drain	-40°C to 125°C			5.3			5.3			6.5			7.7	

5.9 Switching Characteristics, V_{CCA} = 2.5 ± 0.2V

PARAMETER		FROM	TO	Test Conditions		B-Port Supply Voltage (V_{CCB})										UNIT
						1.8 ± 0.15V			2.5 ± 0.2V			3.3 ± 0.3V			5.0 ± 0.5V		
						MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PHL}	Propagation Delay (Hight-to-Low)	A	B	Push-Pull	-40°C to 125°C			3.6			3.1			3.2			4.2	ns
t_{PHL}	Propagation Delay (Hight-to-Low)			Open-Drain	-40°C to 125°C	2.6		3.7	2.1		3.1	2.4		3.3	2.9		4.5	
t_{PLH}	Propagation Delay (Low-to-High)	A	B	Push-Pull	-40°C to 125°C			1			2			5.6			5.3	ns
t_{PLH}	Propagation Delay (Low-to-High)			Open-Drain	-40°C to 125°C	0.5		1	0.5		118	58		194	97		172	
t_{PHL}	Propagation Delay (Hight-to-Low)	B	A	Push-Pull	-40°C to 125°C			4.4			3.2			3.3			4.4	ns
t_{PHL}	Propagation Delay (Hight-to-Low)			Open-Drain	-40°C to 125°C	2		4.4	2		3.2	2		3.4	2.8		4.6	
t_{PLH}	Propagation Delay (Low-to-High)	B	A	Push-Pull	-40°C to 125°C			11.6			1.5			0.6			0.5	ns
t_{PLH}	Propagation Delay (Low-to-High)			Open-Drain	-40°C to 125°C	66		325	0.5		117	0.5		1	0.5		1	
t_{en}	Enable Time	OE	A or B	Push Pull	-40°C to 125°C			220			138			136			124	ns
t_{dis}	Disable Time				-40°C to 125°C			300			300			300			300	
t_{rA}	Ouput Rise Time	B	A	Push-Pull	-40°C to 125°C	6.2		12.4	4.2		8.2	2.0		6.7	1.9		2.7	ns
t_{rA}	Ouput Rise Time			Open-Drain	-40°C to 125°C	210		532	302		617	226		519	150		342	

PARAMETER		FROM	TO	Test Conditions		B-Port Supply Voltage (V_{CCB})									UNIT
						1.8 ± 0.15V			2.5 ± 0.2V			3.3 ± 0.3V			5.0 ± 0.5V			
						MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{rB}	Ouput Rise Time	A	B	Push-Pull	-40°C to 125°C	6.8		13.4	5.5		8.7	5.8		7.3	4.8		6.1	ns
t_{rB}	Ouput Rise Time			Open-Drain	-40°C to 125°C	311		576	344		591	272		483	108		263	
t_{fA}	Output Fall Time	B	A	Push-Pull	-40°C to 125°C	3.0		5.1	2.6		3.9	2.2		3.6	1.0		3.4	ns
t_{fA}	Output Fall Time			Open-Drain	-40°C to 125°C	3.0		5.3	2.6		3.9	2.1		3.6	0.9		3.3	
t_{fB}	Output Fall Time	A	B	Push-Pull	-40°C to 125°C	3.0		4.4	2.8		4.1	3.2		4.1	3.6		5.5	ns
t_{fB}	Output Fall Time			Open-Drain	-40°C to 125°C	3.1		4.3	2.8		4.1	3.2		4.3	3.8		5.8	

5.10 Switching Characteristics, V_{CCA} = 3.3 ± 0.3V

PARAMETER		FROM	TO	Test Conditions		B-Port Supply Voltage (V_{CCB})									UNIT
						1.8 ± 0.15V			2.5 ± 0.2V			3.3 ± 0.3V			5.0 ± 0.5V			
						MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PHL}	Propagation Delay (Hight-to-Low)	A	B	Push-Pull	-40°C to 125°C			4.3			3.2			2.7			3.2	ns
t_{PHL}	Propagation Delay (Hight-to-Low)			Open-Drain	-40°C to 125°C			4.2			3.4			2.8			3.2	
t_{PLH}	Propagation Delay (Low-to-High)			Push-Pull	-40°C to 125°C			0.4			0.7			1.4			4.4	
t_{PLH}	Propagation Delay (Low-to-High)			Open-Drain	-40°C to 125°C			1			1			129			187	
t_{PHL}	Propagation Delay (Hight-to-Low)	B	A	Push-Pull	-40°C to 125°C			5.6			3.4			2.8			3.7	ns
t_{PHL}	Propagation Delay (Hight-to-Low)			Open-Drain	-40°C to 125°C			5.2			3.5			2.8			3.9	
t_{PLH}	Propagation Delay (Low-to-High)			Push-Pull	-40°C to 125°C			13.1			7.2			1.3			0.2	
t_{PLH}	Propagation Delay (Low-to-High)			Open-Drain	-40°C to 125°C			347			275			118			1	
t_{en}	Enable Time	OE	A or B		-40°C to 125°C			229			128			117			104	ns
t_{dis}	Disable Time				-40°C to 125°C			300			300			300			300	
t_{rA}	Ouput Rise Time	B	A	Push-Pull	-40°C to 125°C			13.3			8.1			6.6			3.5	ns
t_{rA}	Ouput Rise Time			Open-Drain	-40°C to 125°C			381			568			568			424	
t_{rB}	Ouput Rise Time	A	B	Push-Pull	-40°C to 125°C			11.9			8.1			6.8			5.7	
t_{rB}	Ouput Rise Time			Open-Drain	-40°C to 125°C			481			593			558			386	
t_{fA}	Output Fall Time	B	A	Push-Pull	-40°C to 125°C			6.4			4.1			3.7			3.2	ns
t_{fA}	Output Fall Time			Open-Drain	-40°C to 125°C			6.5			4.3			3.5			3.1	
t_{fB}	Output Fall Time	A	B	Push-Pull	-40°C to 125°C			4.1			3.9			3.6			4.1	
t_{fB}	Output Fall Time			Open-Drain	-40°C to 125°C			4.2			3.7			3.5			4.2	

5.11 Switching Characteristics: T_{sk}, T_{MAX}

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CCA}	V_{CCB}	Operating free-air temperature (T_A) -40°C to 125°C			UNIT
					MIN	TYP	MAX	
TMAX - Maximum Data Rate	50% Duty Cycle InputOne channel switching	Push-Pull Driving	1.2V ± 0.1V	1.8 ± 0.15V			20	Mbps
				2.5V ± 0.2V			20	
				3.3V ± 0.3V			20	
				5V ± 0.5V			20	
			1.5V ± 0.1V	1.8 ± 0.15V			40	
				2.5V ± 0.2V			60	
				3.3V ± 0.3V			60	
				5V ± 0.5V			60	
			1.8 ± 0.15V	1.8 ± 0.15V			45	
				2.5V ± 0.2V			65	
				3.3V ± 0.3V			70	
				5V ± 0.5V			70	
			2.5V ± 0.2V	1.8 ± 0.15V			25	
				2.5V ± 0.2V			75	
				3.3V ± 0.3V			90	
				5V ± 0.5V			100	
			3.3V ± 0.3V	1.8 ± 0.15V			100	
				2.5V ± 0.2V			100	
				3.3V ± 0.3V			100	
				5V ± 0.5V			110	
TMAX - Maximum Data Rate	50% Duty Cycle InputOne channel switching	Open-Drain Driving	1.2V ± 0.1V	1.8 ± 0.15V			1	Mbps
				2.5 V ± 0.2V			1	
				3.3V ± 0.3V			1	
				5V ± 0.5V			1	
			1.5V ± 0.1V	1.8 ± 0.15V			0.8	
				2.5V ± 0.2V			0.8	
				3.3V ± 0.3V			1	
				5V ± 0.5V			1	
			1.8 ± 0.15V	1.8 ± 0.15V			0.8	
				2.5V ± 0.2V			0.8	
				3.3V ± 0.3V			0.8	
				5V ± 0.5V			1	
			2.5V ± 0.2V	1.8 ± 0.15V			1	
				2.5V ± 0.2V			0.8	
				3.3V ± 0.3V			0.8	
				5V ± 0.5V			1	
			3.3V ± 0.3V	1.8 ± 0.15V			1	
				2.5V ± 0.2V			1	
				3.3V ± 0.3 V			0.8	
				5V ± 0.5V			1.2	
t_w	Pulse Duration, Data Inputs	Push-Pull Driving	1.2V ± 0.1V to 3.3V ± 0.3V	1.8V ± 0.15V to 5.5V ± 0.5V	16.7			ns
		Open-Drain Driving	1.2V ± 0.1V to 3.3V ± 0.3V	1.8V ± 0.15V to 5.5V ± 0.5V	500			

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CCA}	V_{CCB}	Operating free-air temperature (T_A)			UNIT
					-40°C to 125°C			
					MIN	TYP	MAX	
t_{sk} - Output skew	Skew between any two outputs of the same package switching in the same direction	Push-Pull Driving	1.2V ± 0.1V to 3.3V ± 0.3V	1.8V ± 0.15V to 5.5V ± 0.5V			1	ns
		Open-Drain Driving	1.2V ± 0.1V to 3.3V ± 0.3V	1.8V ± 0.15V to 5.5V ± 0.5V			1	

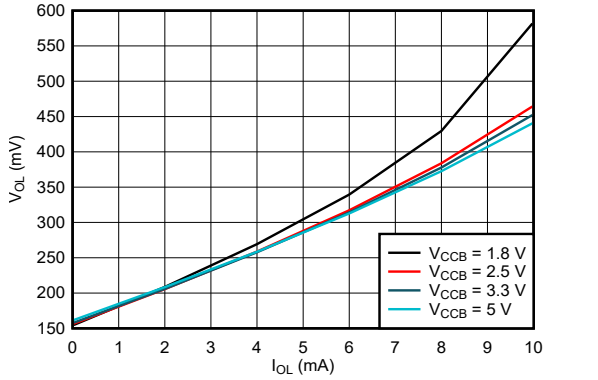
5.12 Operating Characteristics: V_{CCA} = 1.5V to 3.3V, V_{CCB} = 1.5V to 3.3V

T_A = 25°C (1)

PARAMETER		Test Conditions	Supply Voltage (V_{CCA} = V_{CCB} ,unless otherwise noted)						UNIT
			1.2 ± 0.1V (4)	1.5 ± 0.1V (4)	1.8 ± 0.15V	2.5 ± 0.2V	3.3 ± 0.3V	5.0 ± 0.5V	
			TYP	TYP	TYP	TYP	TYP	TYP	
C_{pdA} (2)	A-port input, B-port output to B: outputs enabled	A Port CL = 0, RL = Open f = 10MHz t_{rise} = t_{fall} = 1ns	5.9	5.9	6.8	7.1	8	5.9	pF
	B-port input, A-port output to B: outputs enabled		9.9	9.9	9.9	9.9	9.9	9.9	
C_{pdB} (3)	A-port input, B-port output to B: outputs enabled		21.5	21.5	21.5	21.5	21.5	21.5	
	B-port input, A-port output to B: outputs enabled		16.7	16.7	16.7	16.7	16.7	16.7	
C_{pdA} (2)	A-port input, B-port output to B: outputs disabled	B Port CL = 0, RL = Open f = 10MHz t_{rise} = t_{fall} = 1ns	0.01	0.01	0.01	0.01	0.01	0.01	pF
	B-port input, A-port output to B: outputs disabled		0.01	0.01	0.01	0.01	0.01	0.01	
C_{pdB} (3)	A-port input, B-port output to B: outputs disabled		0.01	0.01	0.01	0.01	0.01	0.01	
	B-port input, A-port output to B: outputs disabled		0.01	0.01	0.01	0.01	0.01	0.01	

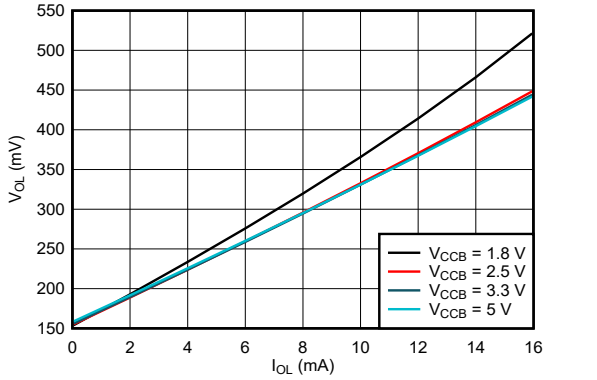
(1) For additional information about how power dissipation capacitance affects power consumption, see the CMOS Power Consumption and C_{pd} Calculation application report
(2) A-Port power dissipation capacitance per transceiver
(3) B-Port power dissipation capacitance per transceiver
(4) V_{CCB}= 1.65V

6 Typical Characteristics



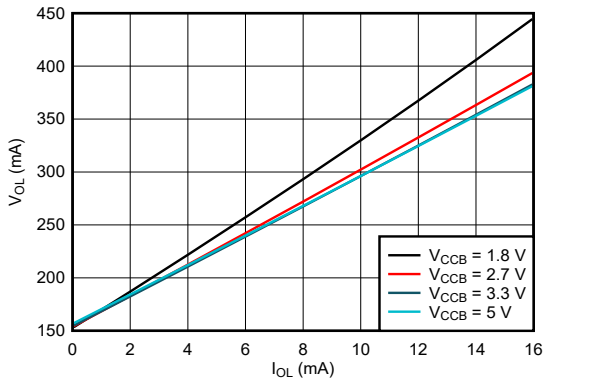
V_{CCA} = 1.2V $V_{IL(A)}$ = 150mV

Figure 6-1. Low-Level Output Voltage ($V_{OL(Bx)}$) vs Low-Level Current ($I_{OL(Bx)}$)



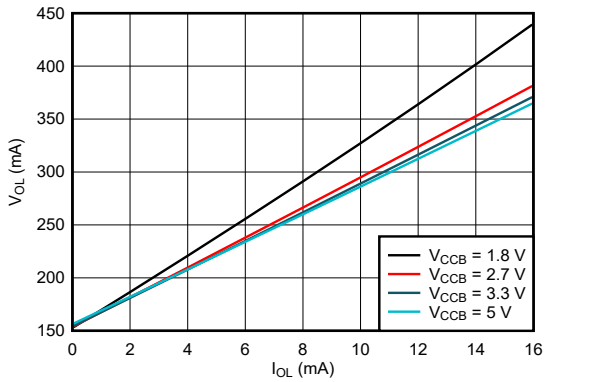
V_{CCA} = 1.8V $V_{IL(A)}$ = 150mV

Figure 6-2. Low-Level Output Voltage ($V_{OL(Bx)}$) vs Low-Level Current ($I_{OL(Bx)}$)



V_{CCA} = 3.3V $V_{IL(A)}$ = 150 mV

Figure 6-3. Low-Level Output Voltage ($V_{OL(Bx)}$) vs Low-Level Current ($I_{OL(Bx)}$)



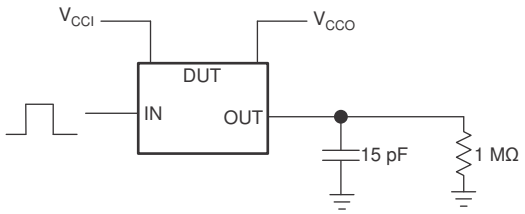
V_{CCA} = 5V $V_{IL(A)}$ = 150 mV

Figure 6-4. Low-Level Output Voltage ($V_{OL(Bx)}$) vs Low-Level Current ($I_{OL(Bx)}$)

7 Parameter Measurement Information

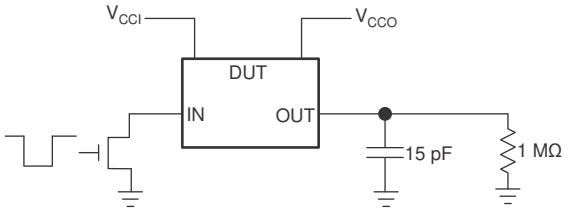
7.1 Load Circuits

Figure 7-1 shows the push-pull driver circuit used for measuring data rate, pulse duration, propagation delay, output rise-time and fall-time. Figure 7-2 shows the open-drain driver circuit used for measuring data rate, pulse duration, propagation delay, output rise-time and fall-time.



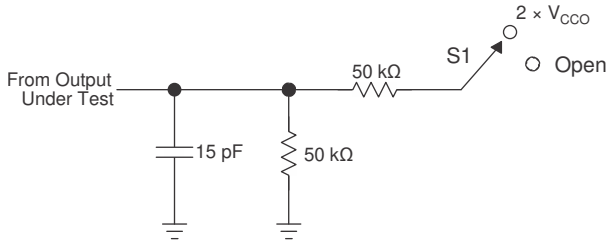
A. V_{CCI} is the V_{CC} associated with the input port.
B. V_{CCO} is the V_{CC} associated with the output port.

Figure 7-1. Data Rate, Pulse Duration, Propagation Delay, Output Rise-Time And Fall-Time Measurement Using a Push-Pull Driver



A. V_{CCI} is the V_{CC} associated with the input port.
B. V_{CCO} is the V_{CC} associated with the output port.

Figure 7-2. Data Rate (10pF), Pulse Duration (10pF), Propagation Delay, Output Rise-Time And Fall-Time Measurement Using an Open-Drain Driver



TEST	S1
t_{PZL}, t_{PLZ} (t_{dis})	2 × V_{CCO}
t_{PHZ}, t_{PZH} (t_{en})	Open

A. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
B. t_{PZL} and t_{PZH} are the same as t_{en}.

Figure 7-3. Load Circuit for Enable-Time and Disable-Time Measurement

7.2 Voltage Waveforms

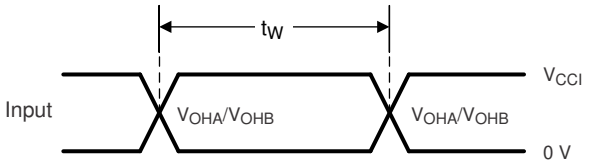


Figure 7-4. Pulse Duration (Push-Pull)

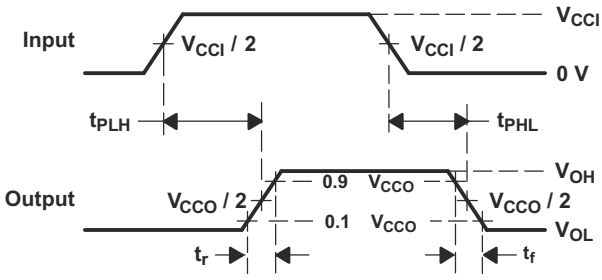
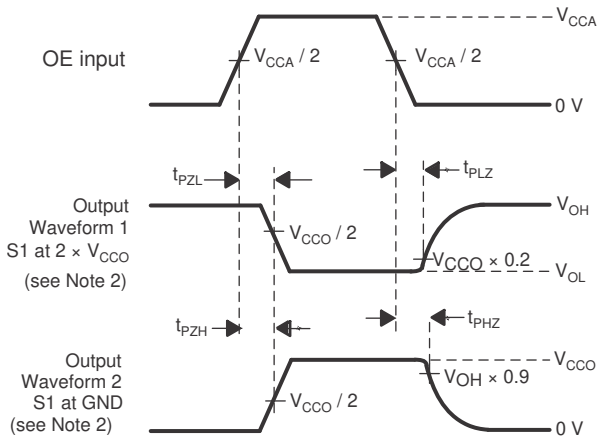


Figure 7-5. Propagation Delay Times



- C_L includes probe and jig capacitance.
- Waveform 1 in Figure 7-6 is for an output with internal such that the output is high, except when OE is high (see Figure 7-3). Waveform 2 in Figure 7-6 is for an output with conditions such that the output is low, except when OE is high.
- All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50Ω, dv/dt ≥ 1V/ns.
- The outputs are measured one at a time, with one transition per measurement.
- t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- t_{PZL} and t_{PZH} are the same as t_{en}.
- t_{PLH} and t_{PHL} are the same as t_{pd}.
- V_{CCI} is the V_{CC} associated with the input port.
- V_{CCO} is the V_{CC} associated with the output port.

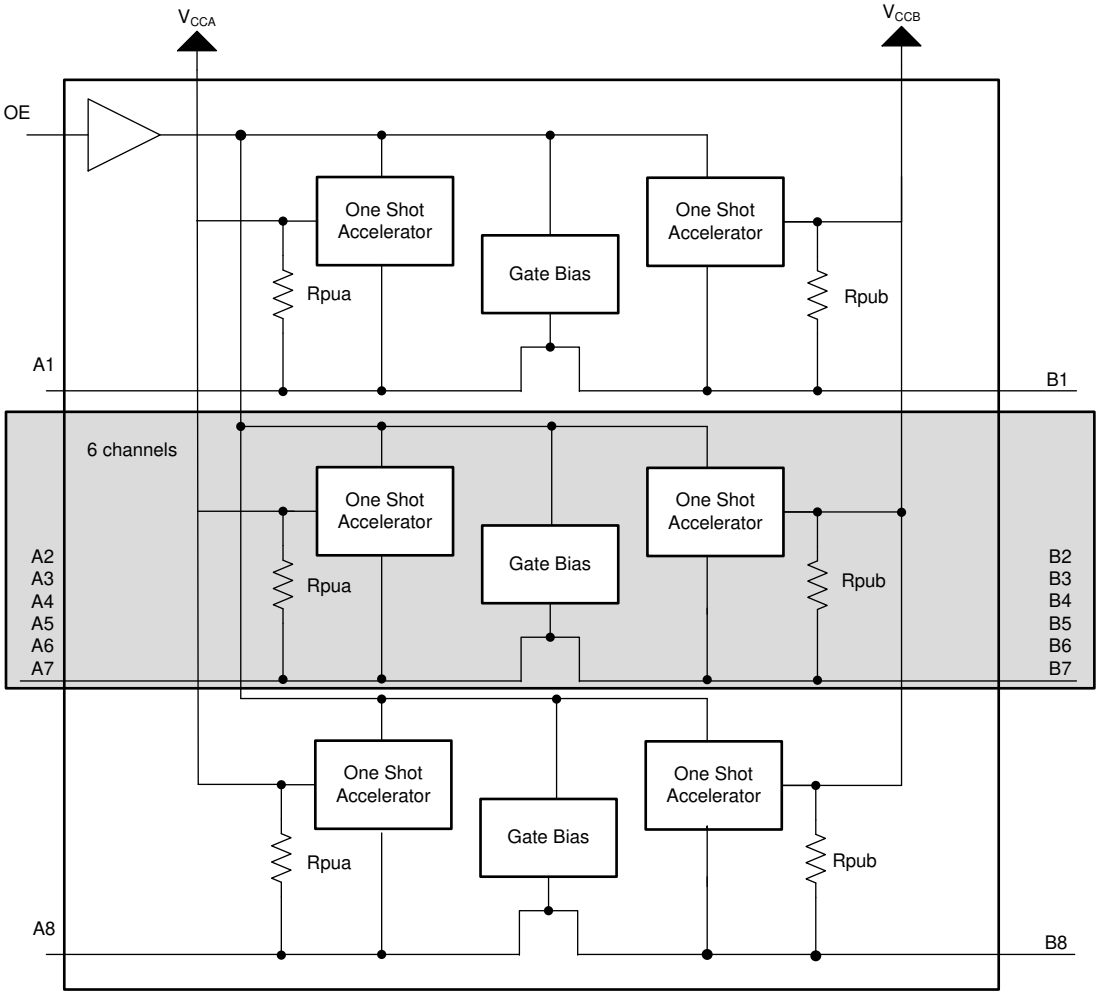
Figure 7-6. Enable and Disable Times

8 Detailed Description

8.1 Overview

The TXS0108W-Q1 device is a directionless voltage-level translator specifically designed for translating logic voltage levels. The A-port accepts I/O voltages ranging from 1.2V to 3.6V. The B-port accepts I/O voltages from 1.65V to 5.5V. The device uses pass gate architecture with edge rate accelerators (one shots) to improve the overall data rate. The pull-up resistors, commonly used in open-drain applications, have been conveniently integrated so that an external resistor is not needed. While this device is designed for open-drain applications, the device can also translate push-pull CMOS logic outputs.

8.2 Functional Block Diagram



Each A-port I/O has a pull-up resistor (R_{PUA}) to V_{CCA} and each B-port I/O has a pull-up resistor (R_{PUB}) to V_{CCB}. R_{PUA} and R_{PUB} have a value of 40kΩ when the output is driving low. R_{PUA} and R_{PUB} have a value of 4kΩ when the output is driving high. R_{PUA} and R_{PUB} are disabled when OE = Low.

8.3 Feature Description

8.3.1 Architecture

Figure 8-1 shows semi-buffered architecture design this application requires for both push-pull and open-drain mode. This application uses edge-rate accelerator circuitry (for both the high-to-low and low-to-high edges), a high-on-resistance N-channel pass-gate transistor (on the order of 10Ω to 50Ω) and pull-up resistors (to provide DC-bias and drive capabilities) to meet these requirements. This design does not need a direction-control signal to control the direction of data flow from A to B or from B to A. The resulting implementation supports both low-speed open-drain operation as well as high-speed push-pull operation.

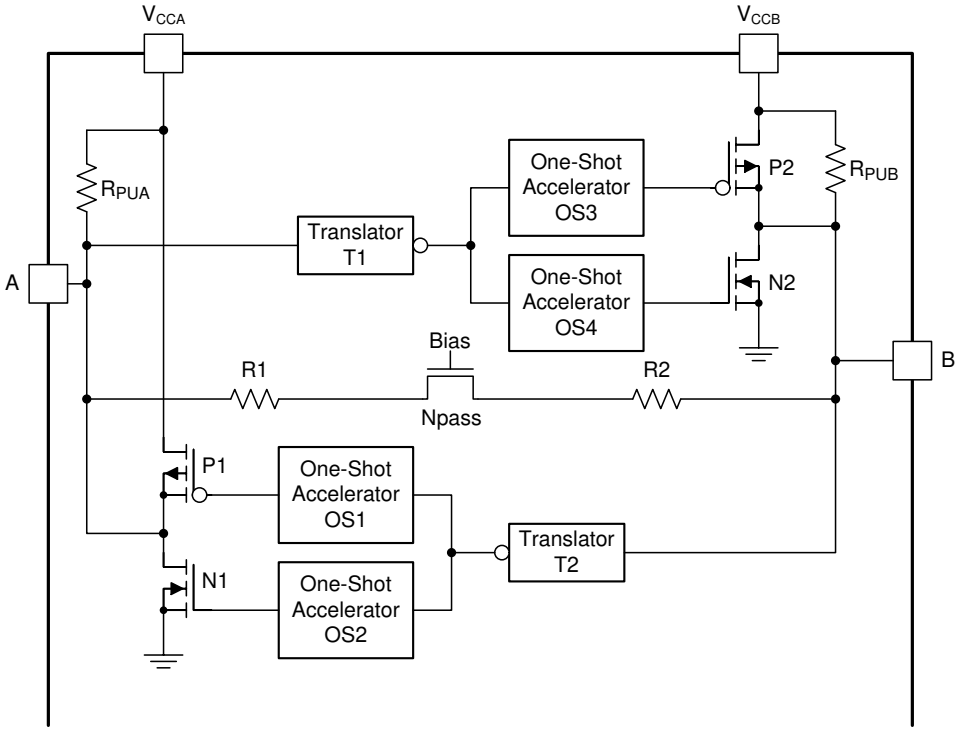


Figure 8-1. Architecture of a TXS0108W-Q1 Cell

When transmitting data from A-ports to B-ports, during a rising edge the one-shot circuit (OS3) turns on the PMOS transistor (P2) for a short-duration which reduces the low-to-high transition time. Similarly, during a falling edge, when transmitting data from A to B, the one-shot circuit (OS4) turns on the N-channel MOSFET transistor (N2) for a short-duration which speeds up the high-to-low transition. The B-port edge-rate accelerator consists of one-shot circuits OS3 and OS4. Transistors P2 and N2 and serves to rapidly force the B port high or low when a corresponding transition is detected on the A port.

When transmitting data from B- to A-ports, during a rising edge the one-shot circuit (OS1) turns on the PMOS transistor (P1) for a short-duration which reduces the low-to-high transition time. Similarly, during a falling edge, when transmitting data from B to A, the one-shot circuit (OS2) turns on NMOS transistor (N1) for a short-duration and this speeds up the high-to-low transition. The A-port edge-rate accelerator consists of one-shots OS1 and OS2, transistors P1 and N1 components and form the edge-rate accelerator and serves to rapidly force the A port high or low when a corresponding transition is detected on the B port.

8.3.2 Input Driver Requirements

The continuous DC-current *sinking* capability is determined by the external system-level open-drain (or push-pull) drivers that are interfaced to the TXS0108W-Q1 I/O pins. Because the high bandwidth of these bidirectional I/O circuits is used to facilitate this fast change from an input to an output and an output to an input, they have a modest DC-current *sourcing* capability of hundreds of micro-amperes, as determined by the internal pull-up resistors.

The fall time (t_{fA}, t_{fB}) of a signal depends on the edge-rate and output impedance of the external device driving TXS0108W-Q1 data I/Os, as well as the capacitive loading on the data lines.

Similarly, the t_{PHL} and maximum data rates also depend on the output impedance of the external driver. The values for t_{fA}, t_{fB}, t_{PHL}, and maximum data rates in the data sheet assume that the output impedance of the external driver is less than 50Ω.

8.3.3 Output Load Considerations

TI recommends careful PCB layout practices with short PCB trace lengths to avoid excessive capacitive loading and so that proper one-shot triggering takes place. PCB signal trace-lengths should be kept short enough such that the round trip delay of any reflection is less than the one-shot duration. This improves signal integrity by allowing any reflection to see a low impedance at the driver. The one-shot circuits have been designed to stay on for approximately 30ns. The maximum capacitance of the lumped load that can be driven also depends directly on the one-shot duration. With very heavy capacitive loads, the one-shot can time-out before the signal is driven fully to the positive rail. The one-shot duration has been set to best optimize trade-offs between dynamic I_{CC}, load driving capability, and maximum bit-rate considerations. Both PCB trace length and connectors add to the capacitance of the TXS0108W-Q1 output. Therefore, TI recommends that this lumped-load capacitance is considered to avoid one-shot retriggering, bus contention, output signal oscillations, or other adverse system-level affects.

8.3.4 Enable and Disable

The TXS0108W-Q1 has an OE pin input that is used to disable the device by setting the OE pin low, which places all I/Os in the Hi-Z state. The disable time (t_{dis}) indicates the delay between the time when the OE pin goes low and when the outputs actually get disabled (Hi-Z). The enable time (t_{en}) indicates the amount of time the design must allow for the one-shot circuitry to become operational after the OE pin goes high.

8.3.5 Pull-up or Pull-down Resistors on I/O Lines

The TXS0108W-Q1 has the smart pull-up resistors dynamically change value based on whether a low or a high is being passed through the I/O line. Each A-port I/O has a pull-up resistor (R_{PUA}) to V_{CCA} and each B-port I/O has a pull-up resistor (R_{PUB}) to V_{CCB}. R_{PUA} and R_{PUB} have a value of 40kΩ when the output is driving low. R_{PUA} and R_{PUB} have a value of 4kΩ when the output is driving high. R_{PUA} and R_{PUB} are disabled when OE = Low. This feature provides lower static power consumption (when the I/Os are passing a low), and supports lower V_{OL} values for the same size pass-gate transistor, and helps improve simultaneous switching performance.

8.4 Device Functional Modes

The TXS0108W-Q1 device has two functional modes, enabled and disabled. To disable the device set the OE pin input low, which places all I/Os in a high impedance state. Setting the OE pin input high enables the device.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The TXS0108W-Q1 can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another. The device is an excellent choice for use in applications where an open-drain driver is connected to the data I/Os. The device is appropriate for applications where a push-pull driver is connected to the data I/Os, but the TXB0104 device, *4-Bit Bidirectional Voltage-Level Translator* might be a better option for such push-pull applications. The device is a semi-buffered auto-direction-sensing voltage translator design is optimized for translation applications (for example, MMC Card Interfaces) that require the system to start out in a low-speed open-drain mode and then switch to a higher speed push-pull mode.

9.2 Typical Application

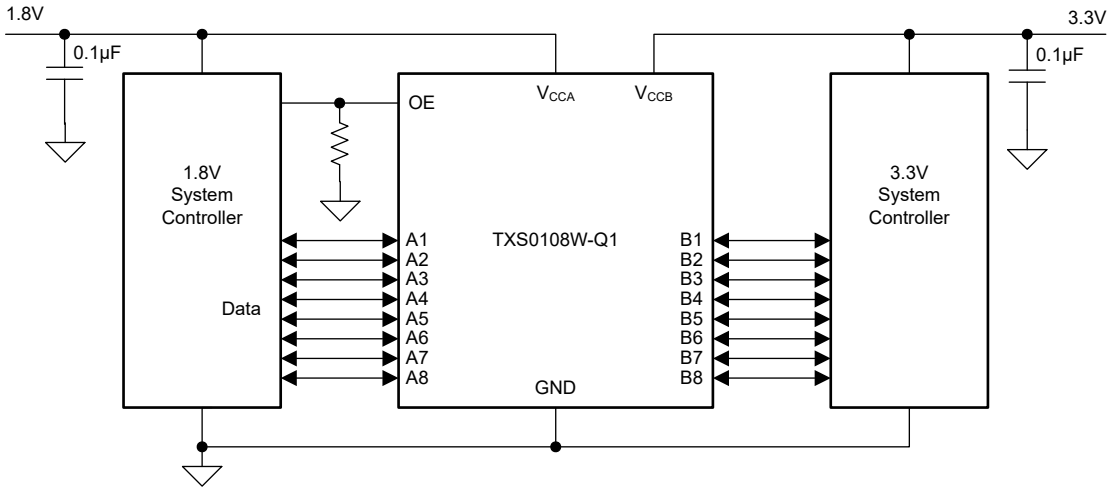


Figure 9-1. Typical Application Circuit

9.2.1 Design Requirements

For this design example, use the parameters listed in Table 9-1. V_{CCA} may be greater than, equal to, or less than V_{CCB}.

Table 9-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	1.2V to 3.6V
Output voltage range	1.65V to 5.5V

9.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
  - Use the supply voltage of the device that is driving the TXS0108W-Q1 device to determine the input voltage range. For a valid logic high the value must exceed the V_{IH} of the input port. For a valid logic low the value must be less than the V_{IL} of the input port.

- Output voltage range
  - Use the supply voltage of the device that the TXS0108W-Q1 device is driving to determine the output voltage range.
  - The TXS0108W-Q1 device has smart internal pull-up resistors. External pull-up resistors can be added to reduce the total RC of a signal trace if necessary.
- An external pull-down resistor decreases the output VOH and VOL. Use Equation 1 to calculate the VOH as a result of an external pull-down resistor.

$$V_{OH} = V_{CCx} \times R_{PD} / (R_{PD} + 4k\Omega) \quad (1)$$

9.2.3 Application Curves

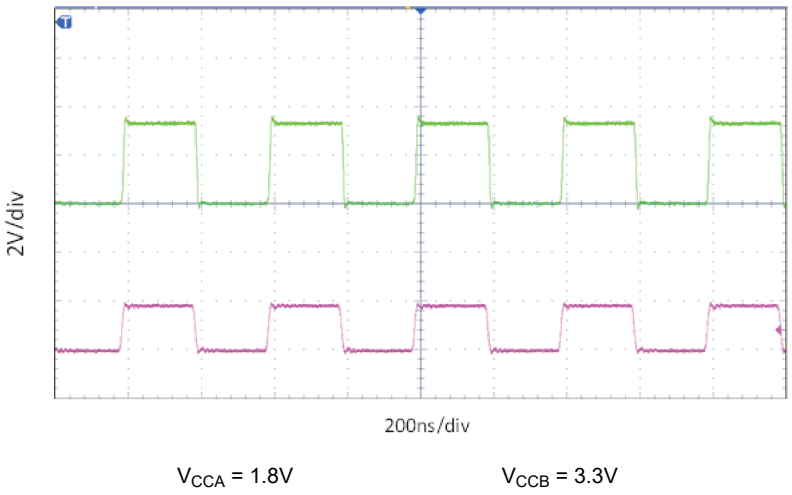


Figure 9-2. Level-Translation of a 2.5MHz Signal

9.3 Power Supply Recommendations

During operation, V_{CCA} can be <, = or > V_{CCB}. The sequencing of each power supply will not damage the device during the power up operation, so either power supply can be ramped up first. The output-enable (OE) input circuit is designed so that it is supplied by V_{CCA} and when the (OE) input is low, all outputs are placed in the high-impedance state. To put the outputs in the high-impedance state during power up or power down, tie the OE input pin to GND through a pull-down resistor, and do not enable the OE input until V_{CCA} and V_{CCB} are fully ramped and stable. The current-sourcing capability of the driver determines the minimum value of the pull-down resistor to ground.

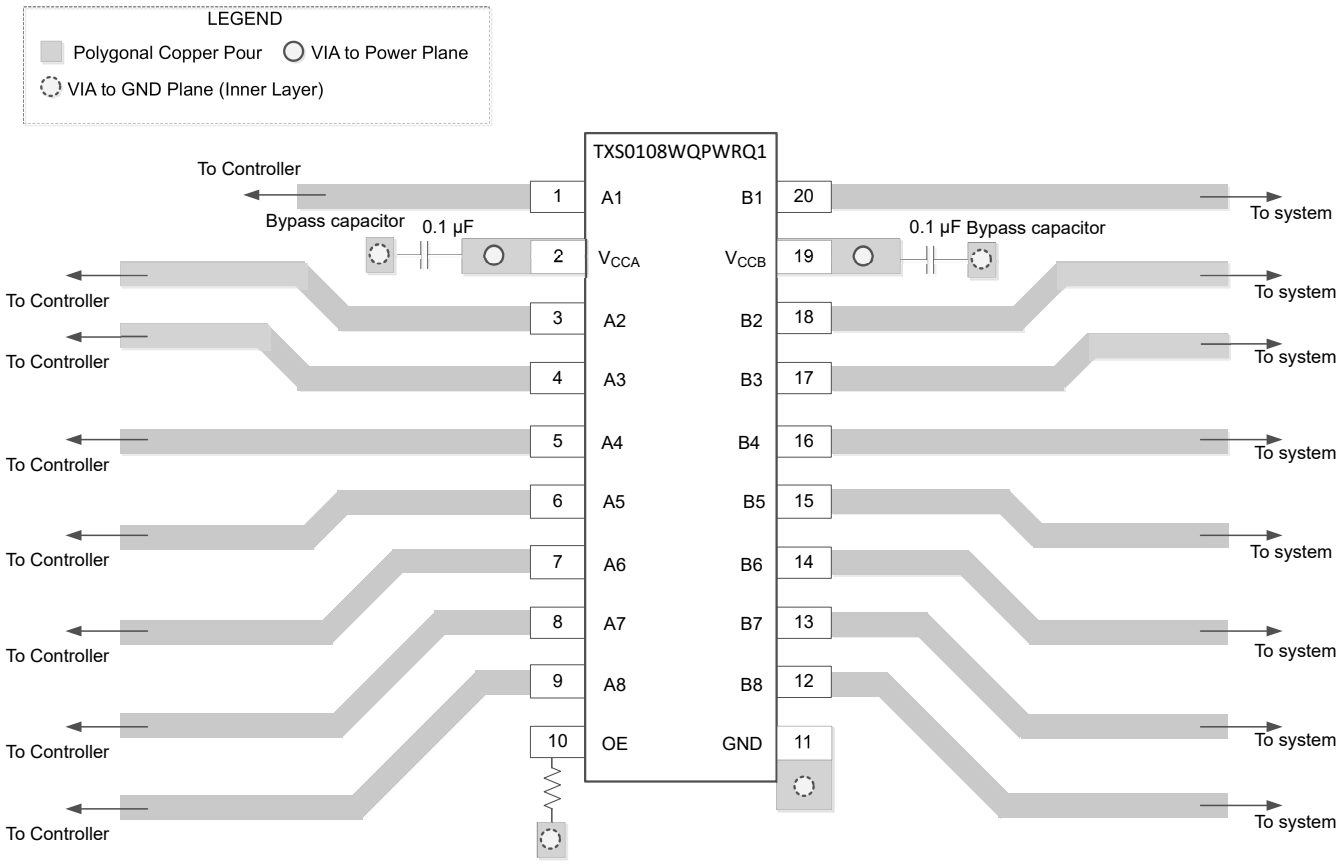
9.4 Layout

9.4.1 Layout Guidelines

For device reliability, following common printed-circuit board layout guidelines is recommended.

- Bypass capacitors should be used on power supplies. Place the capacitors as close as possible to the VCCA, VCCB, and GND pin.
- Short trace lengths should be used to avoid excessive loading.
- PCB signal trace-lengths must be kept short enough so that the round-trip delay of any reflection is less than the one shot duration, approximately 30ns, causing any reflection to encounter low impedance at the source driver.

9.4.2 Layout Example



Keep OE low until V_{CCA} and V_{CCB} are powered up

Figure 9-3. Layout Example

10 Device and Documentation Support

10.1 Documentation Support

Related Documentation

For related documentation, see the following:

- Texas Instruments, A guide to Voltage level translation using TXS devices
- Texas Instruments, Factors affecting the Vol of TXS Auto Bidirectional Devices
- Texas Instruments, Effects of Pullup and Pulldown resistors on TXS Devices

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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10.4 Trademarks

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10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (April 2025) to Revision A (January 2026)	Page
• First public release of the data sheet	1

DATE	REVISION	NOTES
April 2025	*	Initial Release

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TXS0108WQPWRQ1	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	YF08WQ1

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

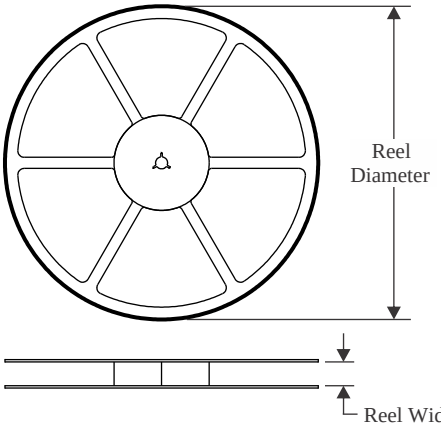
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

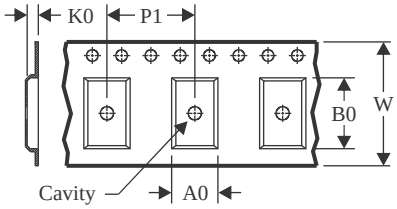
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

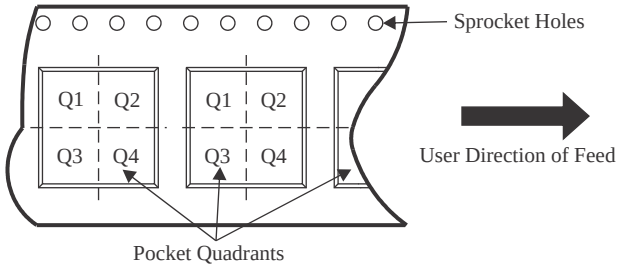


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

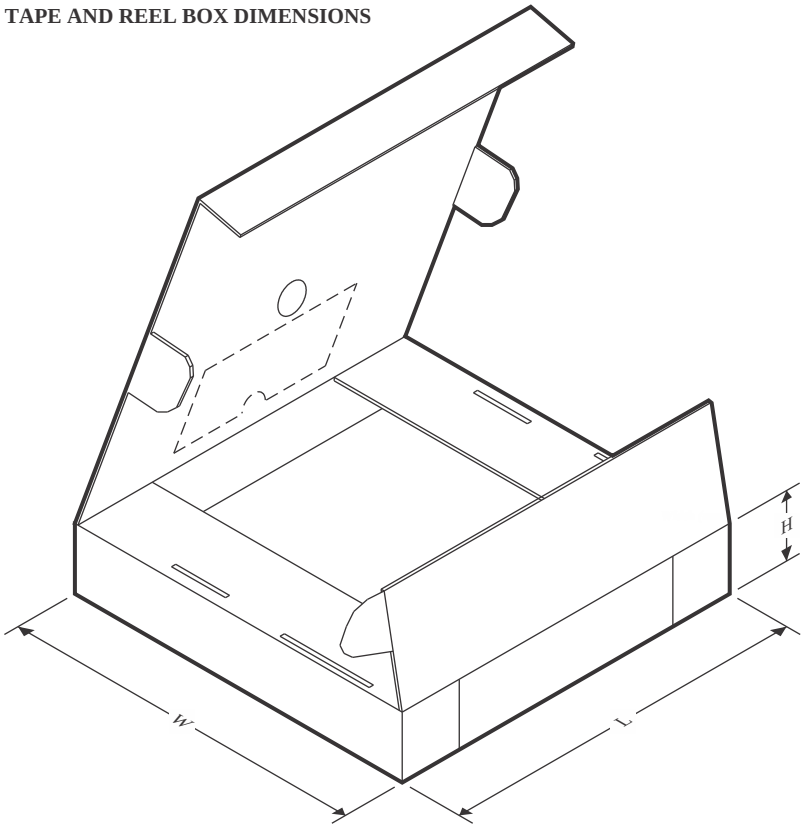
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TXS0108WQPWRQ1	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

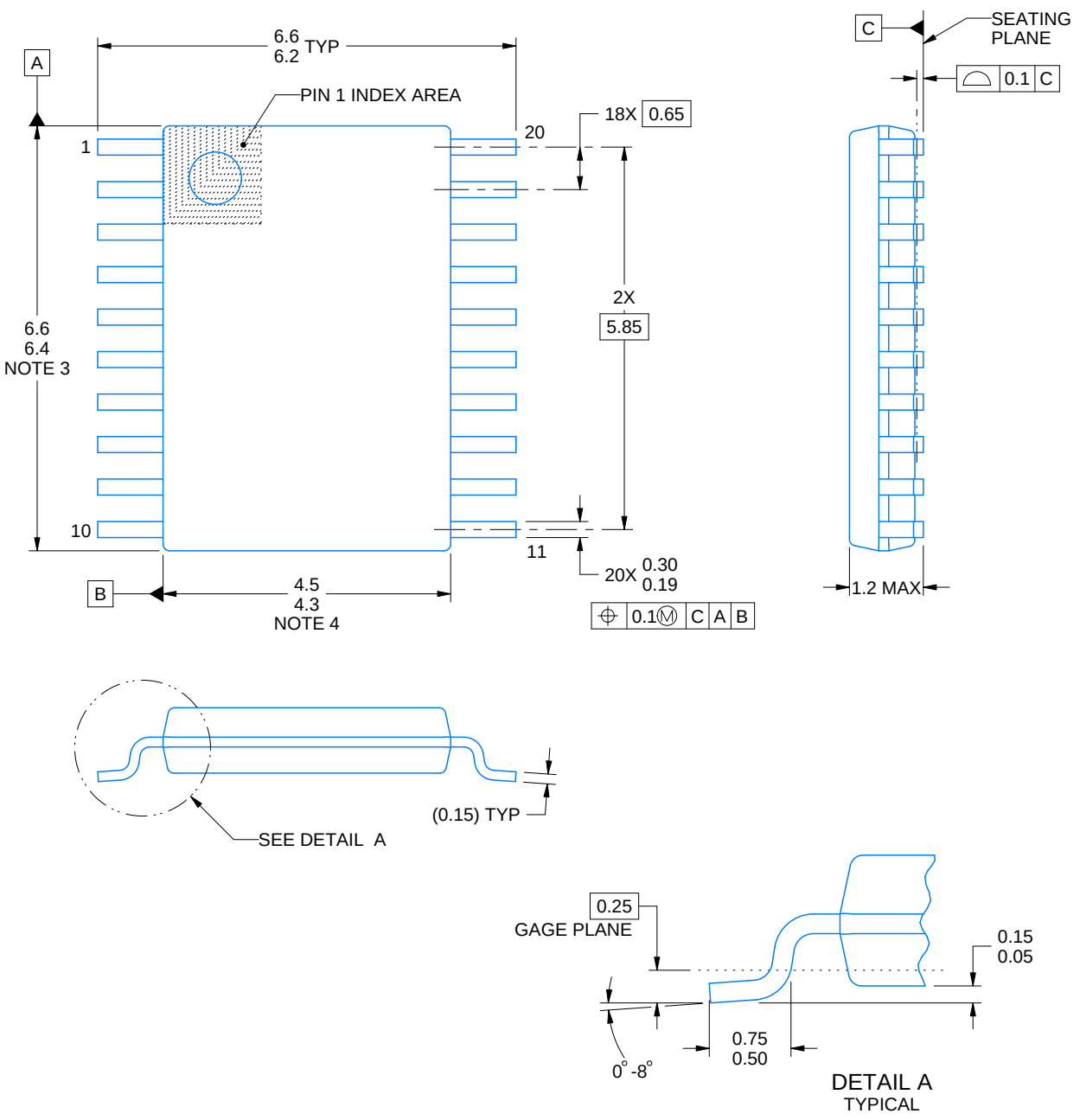
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TXS0108WQPWRQ1	TSSOP	PW	20	2000	353.0	353.0	32.0

PACKAGE OUTLINE

PW0020A

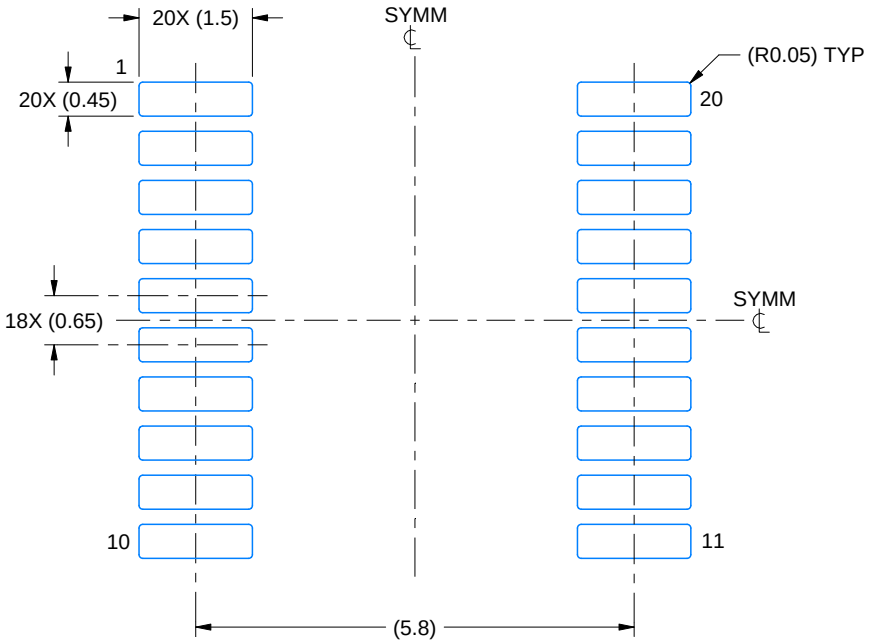
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



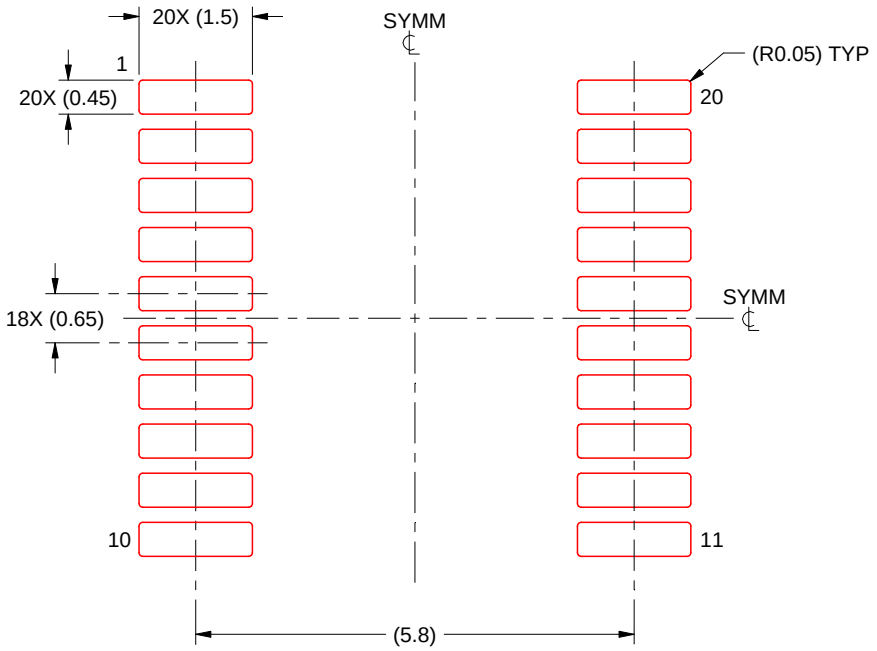
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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