TXS4555 1.8V/3V SIM Card Power Supply With Level Translator

1 Features

- Level translator
  - V_{CC} range of 1.65V to 3.3V
  - V_{BATT} range from 2.3V to 5.5V
- Low-dropout (LDO) regulator
  - 50mA LDO regulator with enable
  - Selectable output voltage of 1.8V or 2.95V
  - Input voltage range of 2.3V to 5.5V
  - Very low dropout of 100mV (maximum) at 50mA
- Incorporates shutdown for the SIM card signals according to ISO7816-3
- ESD protection exceeds JESD 22
  - 2000V Human-body model (A114-B)
  - 500V Charged-device model (C101)
  - 8kV HBM for SIM pins
- Package
  - 16-Pin VQFN (3mm × 3mm)
  - 12-Pin UQFN (2mm × 1.7mm)

2 Description

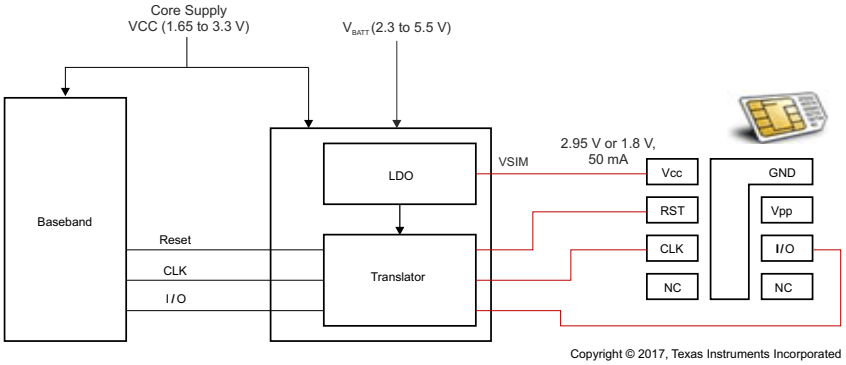
The TXS4555 device is a Smart Identity Module (SIM) card option that interfaces wireless baseband processors with a SIM card to store I/O for mobile handheld applications. The device complies with ISO/IEC Smart-Card Interface requirements as well as GSM and 3G mobile standards. The device includes a high-speed level translator that can support Class-B (2.95V) and Class-C (1.8V) interfaces, and a low dropout (LDO) voltage regulator with output voltages that are selectable between these interfaces.

The device has two supply voltage pins. VCC can operate over the full range of 1.65V to 3.3V and V_{BATT} from 2.3 to 5.5V. VPWR is set to 1.8V or 2.95V, and is supplied by an internal LDO. The integrated LDO accepts input voltages as high as 5.5V and outputs 1.8V or 2.95V at 50mA to the B-side circuitry and to the external SIM card. The TXS4555 enables system designers to interface low-voltage microprocessors to SIM cards operating at 1.8V or 2.95V.

The TXS4555 incorporates shutdown sequence for the SIM card pins based on the ISO 7816-3 specification for SIM cards. During an accidental shutdown of the phone, shutting down the SIM card helps prevent data corruption. The device has 8 kV HBM protection for the SIM pins and standard 2 kV HBM protection for all other pins.

Device Information

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TXS4555	VQFN (16)	3.00mm × 3.00mm
	UQFN (12)	2.00mm × 1.70mm



Interfacing With SIM Card

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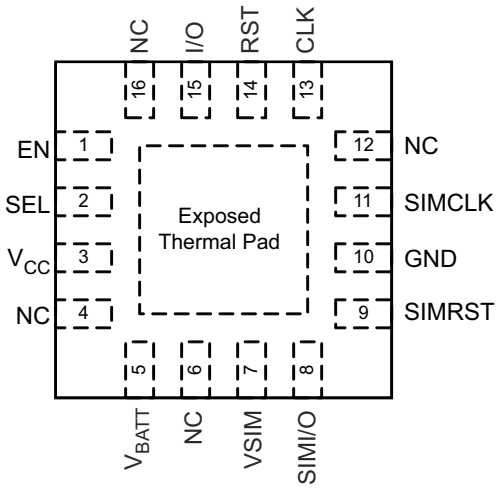
3 Pin Configuration and Functions



A. The exposed center thermal pad must be connected to Ground.

Figure 3-1. RGT Package(1) 16-Pin VQFN With Exposed Thermal Pad Top View

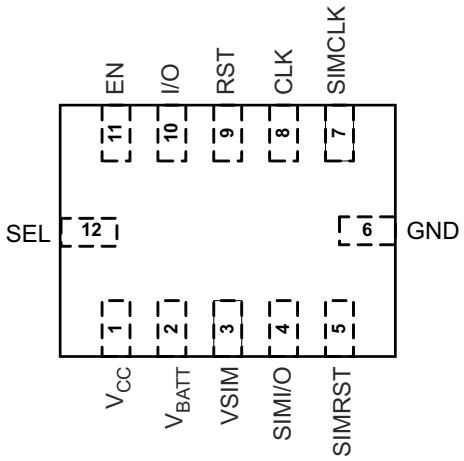


Figure 3-2. RUT Package 12-Pin UQFN Top View

Table 3-1. Pin Functions

NAME	NO.		TYPE[1]	DESCRIPTION
	RGT	RUT		
CLK	13	8	I	Clock signal pin connected from baseband processor
EN	1	11	I	Enable and disable control input. Pull EN low to place all outputs in Hi-Z state and to disable the LDO. Referenced to VCC.
GND	10	6	—	Ground
I/O	15	10	I/O	Bidirectional SIM I/O pin which connected from baseband processor
NC	4, 6, 12, 16	–	—	No internal connection
RST	14	9	I	SIM reset pin connected from baseband processor
SEL	2	12	I	Pin to program VSIM value (Low = 1.8 V, High = 2.95 V)
SIM_CLK	11	7	O	Clock signal pin connects to CLK pin of the SIM card connector
SIM_I/O	8	4	I/O	Bidirectional SIM I/O pin connects to I/O pin of the SIM card connector
SIM_RST	9	5	O	SIM reset pin connects to RESET pin of the SIM card connector
VBATT	5	2	P	Battery power supply
V_{CC}	3	1	P	Power supply voltage that powers all A-port I/Os and control inputs
VSIM	7	3	O	SIM card power-supply pin (1.8V or 2.95 V)

(1) G = Ground, I = Input, O = Output, P = Power

4 Specifications

4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
LEVEL TRANSLATOR					
V_{CC}	Supply voltage range		–0.3	4.0	V
V_I	Input voltage range	V_{CC} port	–0.5	4.6	V
		SIM port	–0.5	4.6	
		Control inputs	–0.5	4.6	
V_O	Voltage range applied to any output in the high-impedance or power-off state	V_{CC} port	–0.5	4.6	V
		VSIM port	–0.5	4.6	
		Control inputs	–0.5	4.6	
V_O	Voltage range applied to any output in the high or low state	V_{CC} port	–0.5	4.6	V
		SIM-port	–0.5	4.6	
		Control inputs	–0.5	4.6	
I_{IK}	Input clamp current	$V_I < 0$		–50	mA
I_{OK}	Output clamp current	$V_O < 0$		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through VCCA or GND			±100	mA
T_{stg}	Storage temperature range		–65	150	°C
LDO					
VBAT	Input voltage range		–0.3	6	V
V_{OUT}	Output voltage range		–0.3	6	V
	Peak output current		TBD		mA
	Continuous total power dissipation			TBD	
T_J	Junction temperature range		–55	150	°C
T_{stg}	Storage temperature range		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

4.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge (host side)	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2	kV
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	V
$V_{(ESD)}$	Electrostatic discharge (SIM side)	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±8	kV

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

4.3 Thermal Information

THERMAL METRIC[1]		TXS4555		UNIT
		RGT	RUT	
		16 PINS	12 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	47	87.2	°C/W
θ_{JB}	Junction-to-board thermal resistance	25.12	N/A	
ψ_{JT}	Junction-to-top characterization parameter	1.3	1.7	
$\theta_{JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.6	N/A	

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

4.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted) (1)

				MIN	MAX	UNIT
LEVEL TRANSLATOR						
V_{CC}	Supply voltage			1.65	3.3	V
V_{IH}	High-level input voltage	VCC port	EN, SEL, RST, CLK, I/O	V_{CC} × 0.7	V_{CC}	V
		SIM port	SIM_I/O	V_{sim} × 0.7	V_{sim}	
V_{IL}	Low-level input voltage	VCC port	EN, SEL, RST, CLK, I/O	0	V_{CC} × 0.3	V
		SIM port	SIM_I/O	0	V_{sim} × 0.3	
Δt/Δv	Input transition rise or fall rate				5	ns/V
T_A	Operating free-air temperature			–40	85	°C
T_J	Operating junction temperature			–40	125	°C

(1) All unused data inputs of the device must be held at VCCI or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

4.5 Electrical Characteristics – Level Translator

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP[1]	MAX	UNIT
V_{OH}	SIM_RST	I_{OH} = –1 mA, V_{CC} = 1.65 V to 3.3 V VSIM = 1.8 V or 2.95 V (2)	V_{SIM} × 0.8			V
	SIM_CLK	I_{OH} = –1 mA	V_{SIM} × 0.8			
	SIM_I/O	I_{OH} = –20 µA	V_{SIM} × 0.8			
	I/O	I_{OH} = –20 µA	V_{CC} × 0.8			
V_{OL}	SIM_RST	I_{OL} = 1 mA, V_{CC}= 1.65 V to 3.3 V VSIM = 1.8 V or 2.95 V (2)			V_{SIM} × 0.2	V
	SIM_CLK	I_{OL} = 1 mA			V_{SIM} × 0.2	
	SIM_I/O	I_{OL} = 1 mA			0.3	
	I/O	I_{OL} = 1 mA			0.3	
I_I	Control inputs	V_I = EN, 1.8 V / 3 V, V_{CC} = 1.65 V to 3.3 V VSIM = 1.8 V or 2.95 V (2)			±1	µA
I_{CC}	I/O	V_I = V_{CCI}, I_O = 0, V_{CC} = 1.65 V to 3.3 V VSIM = 1.8 V or 2.95 V (2)			±5	µA
C_{io}	I/O port			8		pF
	SIM ports			4		
C_i	Control inputs	V_I = V_{CC} or GND		4		pF

(1) All typical values are at T_A = 25°C.

(2) (Supplied by LDO)

4.6 LDO Electrical Characteristics

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{BAT}	Input voltage			2.3		5.5	V
V_{SIM}	Output voltage	Class-B Mode (SEL = V_{CC})		2.85	2.95	3.05	V
		Class-C Mode (SEL = 0)		1.7	1.8	1.9	
V_{DO}	Dropout voltage	I_{OUT} = 50 mA				100	mV
I_{GND}	Ground-pin current	I_{OUT} = 0 mA				35	µA
I_{SHDN}	Shutdown current (IGND)	$V_{ENx} \le 0.4$ V, (VSIM + V_{DO}) ≤ VBAT ≤ 5.5 V, T_J = 85°C				3.5	µA
$I_{OUT(SC)}$	Short-circuit current	R_L = 0 Ω			145		mA
C_{OUT}	Output Capacitor				1		µF
PSRR	Power-supply rejection ratio	VBAT = 3.25 V, VSIM = 1.8 V or 2.95 V C_{OUT} = 1 µF, I_{OUT} = 50 mA	f = 1 kHz	50			dB
			f = 10 kHz	40			
T_{STR}	Start-up time	VSIM = 1.8 V or 2.95 V, I_{OUT} = 50 mA, C_{OUT} = 1 µF				400	µS
T_J	Operating junction temperature			–40		125	°C

(1) All typical values are at T_A = 25°C.

4.7 General Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{I/OPU}$	I/O pull-up		16	20	24	kΩ
R_{SIMPU}	SIM_I/O pull-up		10	14	18	kΩ
R_{SIMPD}	SIM_I/O pull-down	Active pull-downs are connected to the VSIM regulator output to the SIM_CLK, SIM_RST, SIM_I/O when EN = 0			3	kΩ

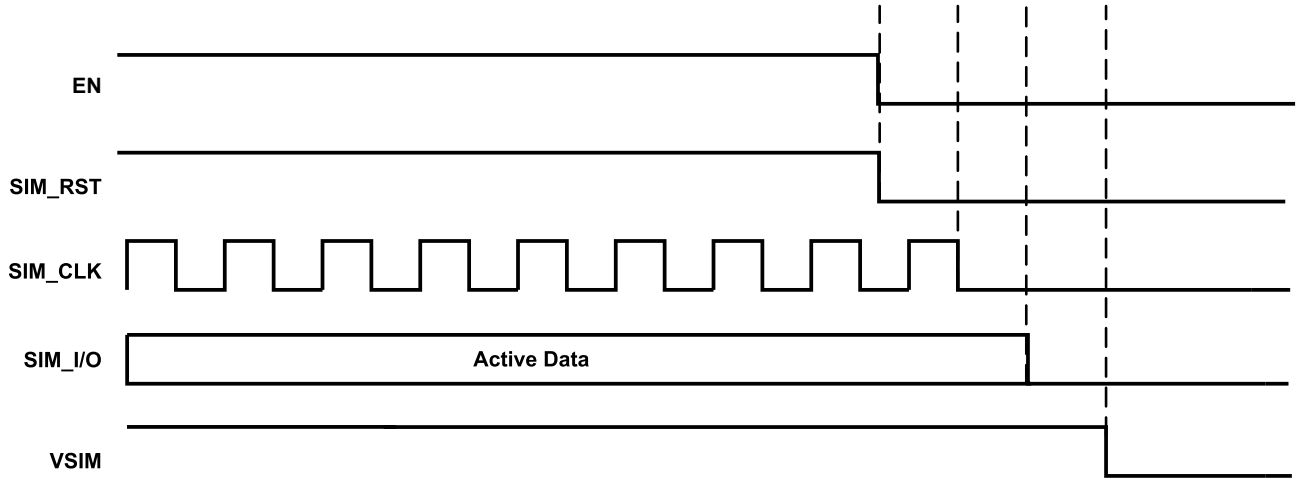


Figure 4-1. Shutdown Sequence for SIM_RST, SIM_CLK, SIM_IO and VSIM

The shutdown sequence for the SIM signals is based on the ISO 7816-3 specification. The shutdown sequence of these signals helps to properly disable these channels and not have any corruption of data accidently. Also, this is also helpful when the SIM card is present in a hot swap slot and when pulling out the SIM card, the orderly shutdown of these signals help avoid any improper write or corruption of data.

When EN is lowered, the shutdown sequence happens by powering of the SIM_RST channel. Once that is achieved, SIM_CLK, SIM_I/O and VSIM are then powered sequentially one by one. There is an internal 2K pull-down value on the SIM pins, and this helps to pull the channels low. The shutdown time sequence is ordered to a few microseconds. EN needs to be lowered first for the shutdown to occur, which will then control the SIM IO, RST, and CLK. When EN and VCC are both lowered, the shutdown sequence will not be triggered.

4.8 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC} = 1.8 V ± 0.15 V		UNIT
				MIN	MAX	
VSIM = 1.8 V or 2.95 V SUPPLIED BY INTERNAL LDO						
t_{rA}	SIM_I/O	C_L = 50 pF	V_{CC} = 1.8 V ± 0.15 V		1	µs
t_{rB}	SIM_RST	C_L = 50 pF	V_{CC} = 1.8 V ± 0.15 V		1	µs
	SIM_CLK	C_L = 50 pF	V_{CC} = 1.8 V ± 0.15 V		18	ns
	SIM_I/O	C_L = 50 pF	V_{CC} = 1.8 V ± 0.15 V		1	µs
f_{max}	SIM_CLK	C_L = 50 pF	V_{CC} = 1.8 V ± 0.15 V		25	MHz
Duty cycle	SIM_CLK	C_L = 50 pF	V_{CC} = 1.8 V ± 0.15 V	40%	60%	

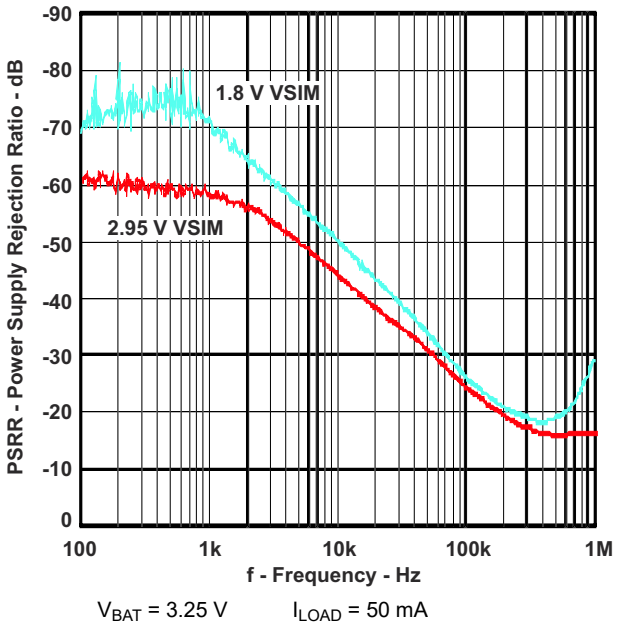
4.9 Operating Characteristics

T_A = 25°C, V_{SIM} = 1.8 V

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pdA} (1)	Class B	C_L = 0, f = 5 MHz, t_r = t_f = 1 ns, V_{CC} = 1.8 V	13	pF
	Class C	C_L = 0, f = 5 MHz, t_r = t_f = 1 ns, V_{CC} = 1.8 V	11	pF

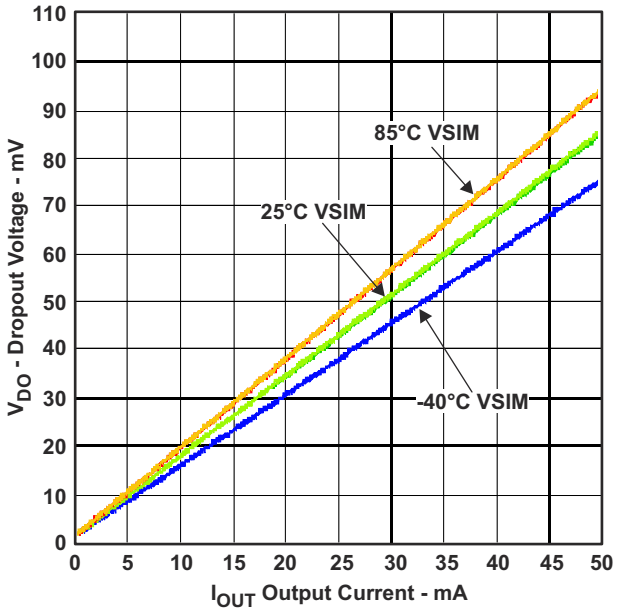
(1) Power dissipation capacitance per transceiver.

4.10 Typical Characteristics



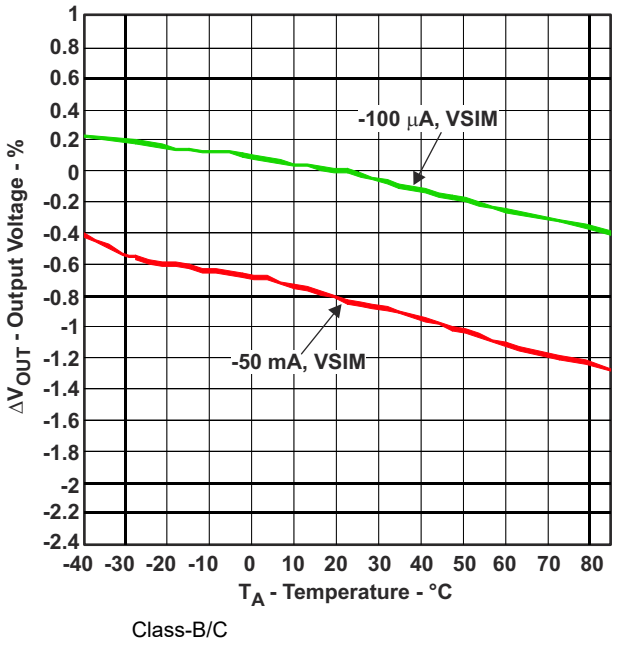
V_{BAT} = 3.25 V I_{LOAD} = 50 mA

Figure 4-2. PSRR



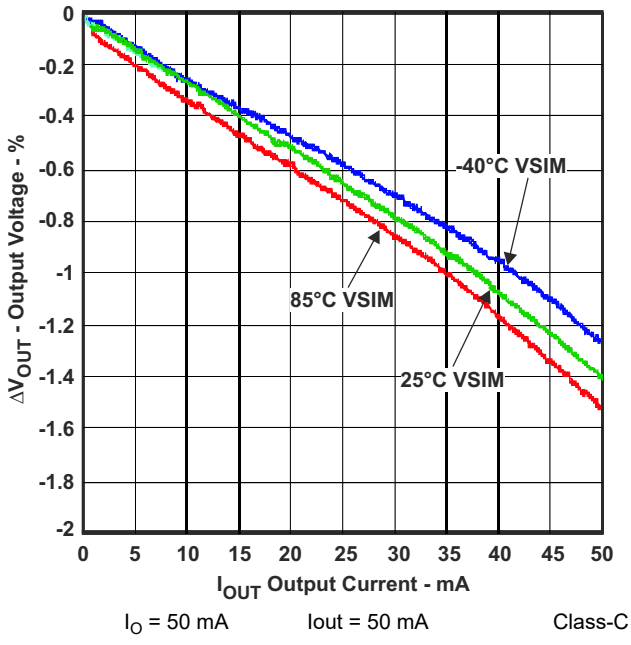
V_{BAT} = 5.5 V

Figure 4-3. Dropout Voltage vs Output Current



Class-B/C

Figure 4-4. Output Voltage vs Temperature



I_O = 50 mA Iout = 50 mA Class-C

Figure 4-5. Load Regulation

5 Detailed Description

5.1 Functional Block Diagram

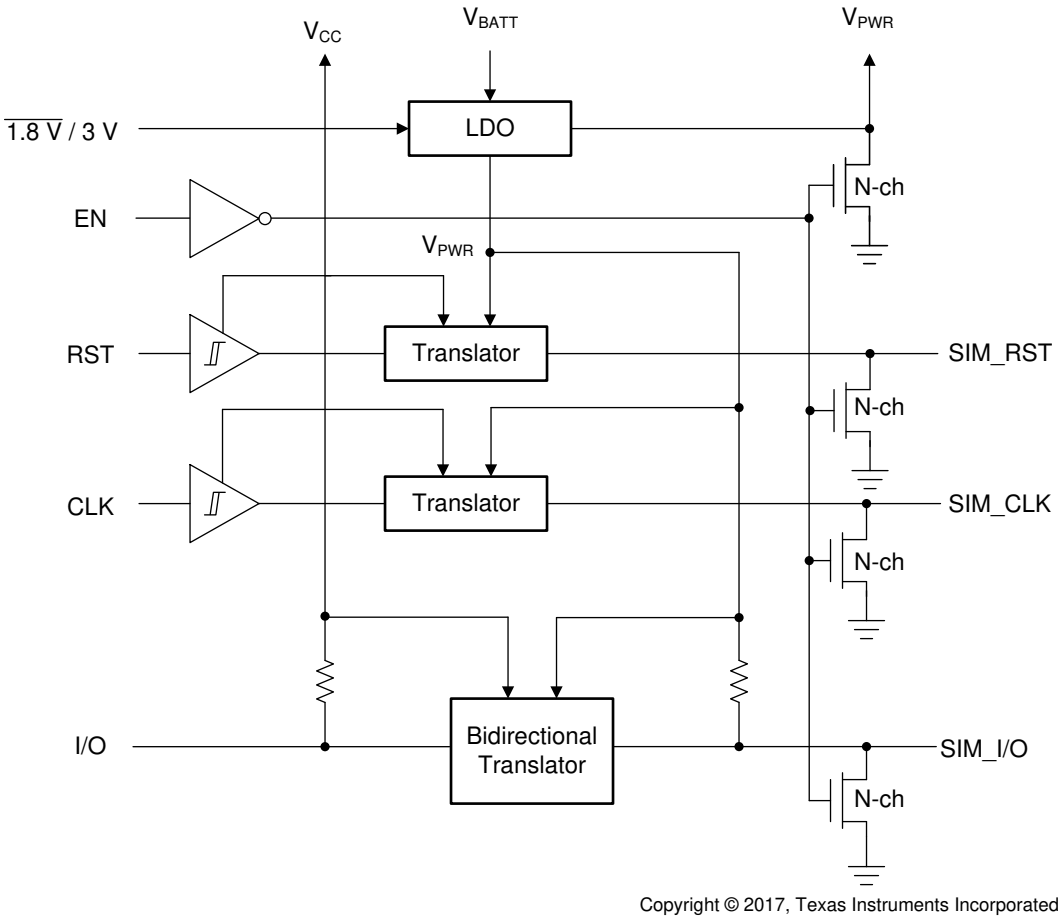


Figure 5-1. Block Diagram

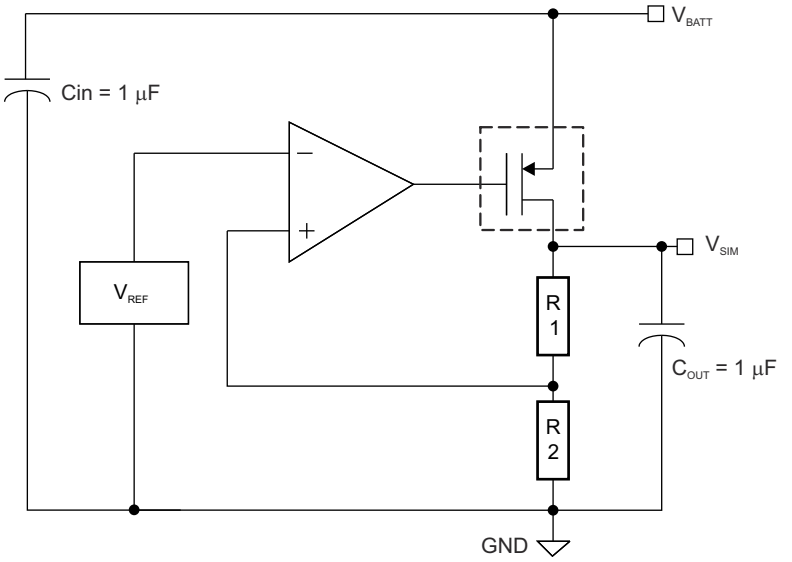


Figure 5-2. Block Diagram of the LDO

6 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

6.1 Application Information

The LDOs included on the TXS4555 achieve ultra-wide bandwidth and high loop gain, resulting in extremely high PSRR at very low headroom (V_{BAT} – V_{SIM}). The TXS4555 provides fixed regulation at 1.8 V or 2.95 V. Low noise, enable, low ground pin current make the device designed for portable applications. The device offers sub-bandgap output voltages, current limit and thermal protection, and is fully specified from –40°C to +125°C.

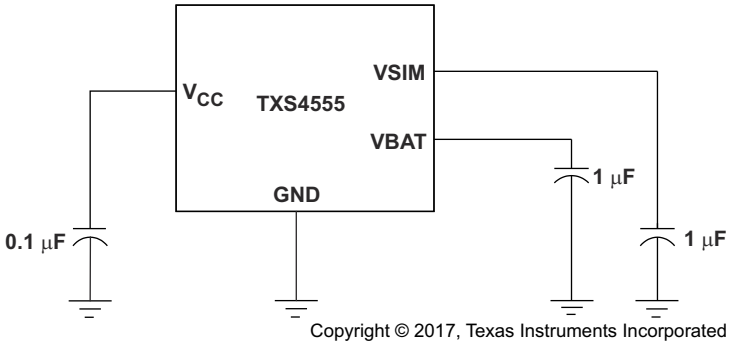


Figure 6-1. Typical Application Circuit for TXS4555

6.1.1 Input And Output Capacitor Requirements

It is good analog design practice to connect a 1 µF low equivalent series resistance (ESR) capacitor across the input supply (VBAT) near the regulator. A 0.1 µF is required for the logic core supply (VDDIO).

This capacitor counteracts reactive input sources and improve transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated or if the device is located several inches from the power source. The LDO's are designed to be stable with standard ceramic capacitors with values of 1 µF or larger. X5R- and X7R-type capacitors are recommended. These capacitors have minimal variation in value and ESR over temperature. Maximum ESR must be less than 1 Ω.

6.1.2 Output Noise

In most LDOs, the bandgap is the dominant noise source. To improve AC performance such as PSRR, output noise, and transient response, it is recommended that the board is designed with separate ground planes for V_{IN} and V_{OUT}, with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the bypass capacitor must connect directly to the GND pin of the device.

6.1.3 Internal Current Limit

The TXS4555 internal current limit helps protect the regulator during fault conditions. During current limit, the output sources a fixed amount of current that is largely independent of output voltage. For reliable operation, the device should not be operated in a current limit state for extended periods of time.

The PMOS pass element in the TXS4555 has a built-in body diode that conducts current when the voltage at VSIM exceeds the voltage at VBAT. This current is not limited, so if extended reverse voltage operation is anticipated, external limiting may be appropriate.

6.1.4 Dropout Voltage

The TXS4555 uses a PMOS pass transistor to achieve low dropout. When (V_{BAT} – V_{SIM}) is less than the dropout voltage (V_{DO}), the PMOS pass device is in its linear region of operation and the input-to-output resistance is the $R_{DS(ON)}$ of the PMOS pass element. V_{DO} approximately scales with the output current because the PMOS device behaves like a resistor in dropout.

6.1.5 Startup

The TXS4555 uses a quick-start circuit which allows the combination of very low output noise and fast start-up times.

6.1.6 Transient Response

As with any regulator, increasing the size of the output capacitor reduces over or undershoot magnitude, but increases duration of the transient response.

6.1.7 Minimum Load

The TXS4555 is stable and well-behaved with no output load. Traditional PMOS LDO regulators suffer from lower loop gain at very light output loads. The TXS4555 uses an innovative low-current mode circuit to increase loop gain under light or no-load conditions, resulting in improved output voltage regulation performance down to zero output current.

6.1.8 Thermal Information

6.1.8.1 Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately 160°C, allowing the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry is then enabled again. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, and protects the regulator from damage because of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heat sink. For reliable operation, maximum junction temperature must be limited to 125°C. To estimate the margin of safety in a complete design (including heat sink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection must trigger at least 35°C above the maximum expected ambient condition of your particular application. This configuration produces a worst-case junction temperature of 125°C, at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TXS4555 is designed to protect against overload conditions. It is not intended to replace proper heat sinking. Continuously running the TXS4555 into thermal shutdown degrades device reliability.

7 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

7.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

7.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

7.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

7.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.5 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (August 2013) to Revision C (May 2026)	Page
• Updated format to match new TI layout and flow. Tables, figures and cross-references use a new numbering sequence throughout the document	1
• Added VSIM to *Interfacing With SIM Card*	1

Changes from Revision A (February 2011) to Revision B (August 2013)	Page
• Removed Ordering Information table	3
• Updated V_{IH} and V_{IL} to specify additional information	6

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TXS4555RGTR	Active	Production	VQFN (RGT) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ZUT
TXS4555RGTR.B	Active	Production	VQFN (RGT) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ZUT
TXS4555RUTR	Active	Production	UQFN (RUT) | 12	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	69R
TXS4555RUTR.B	Active	Production	UQFN (RUT) | 12	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	69R

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

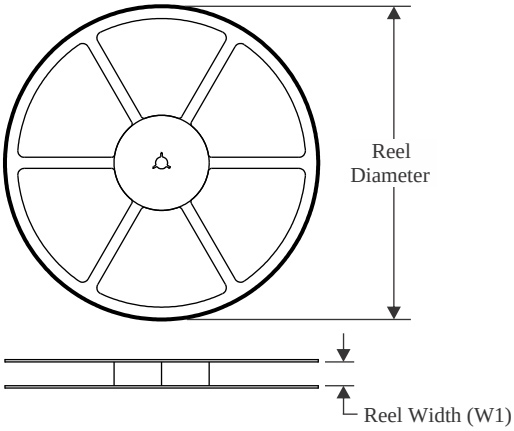
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

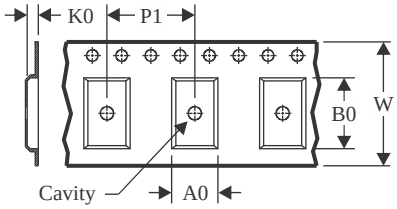
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

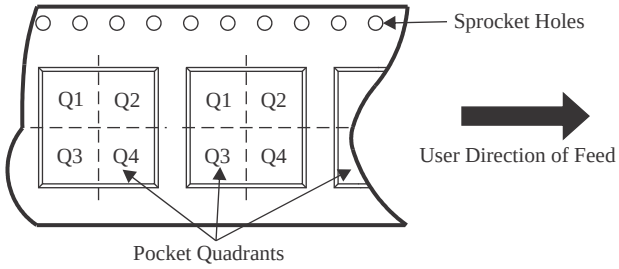


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

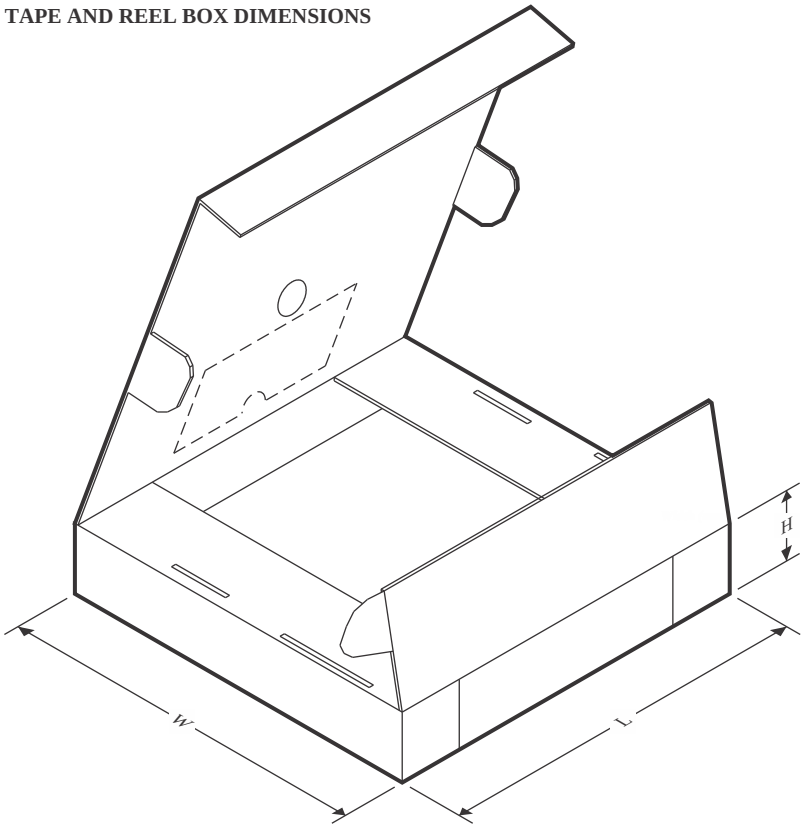
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TXS4555RGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TXS4555RUTR	UQFN	RUT	12	3000	180.0	8.4	1.95	2.3	0.75	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS

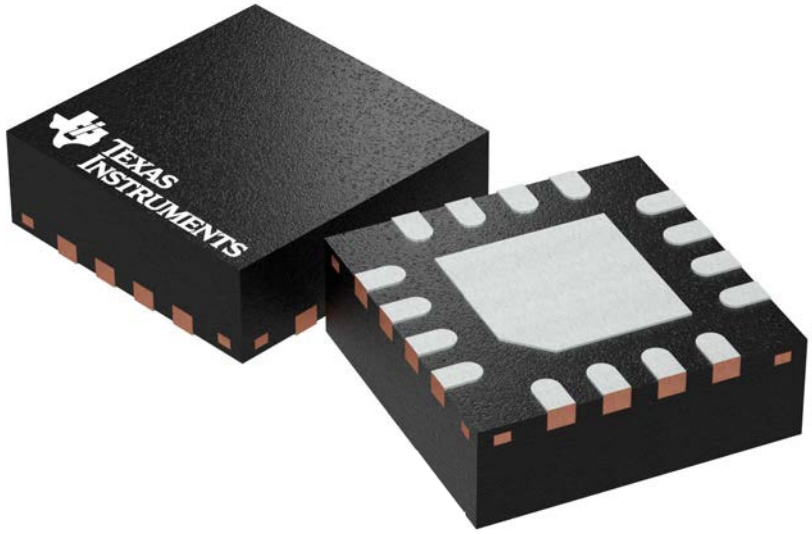


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TXS4555RGTR	VQFN	RGT	16	3000	353.0	353.0	32.0
TXS4555RUTR	UQFN	RUT	12	3000	202.0	201.0	28.0

RGT 16 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



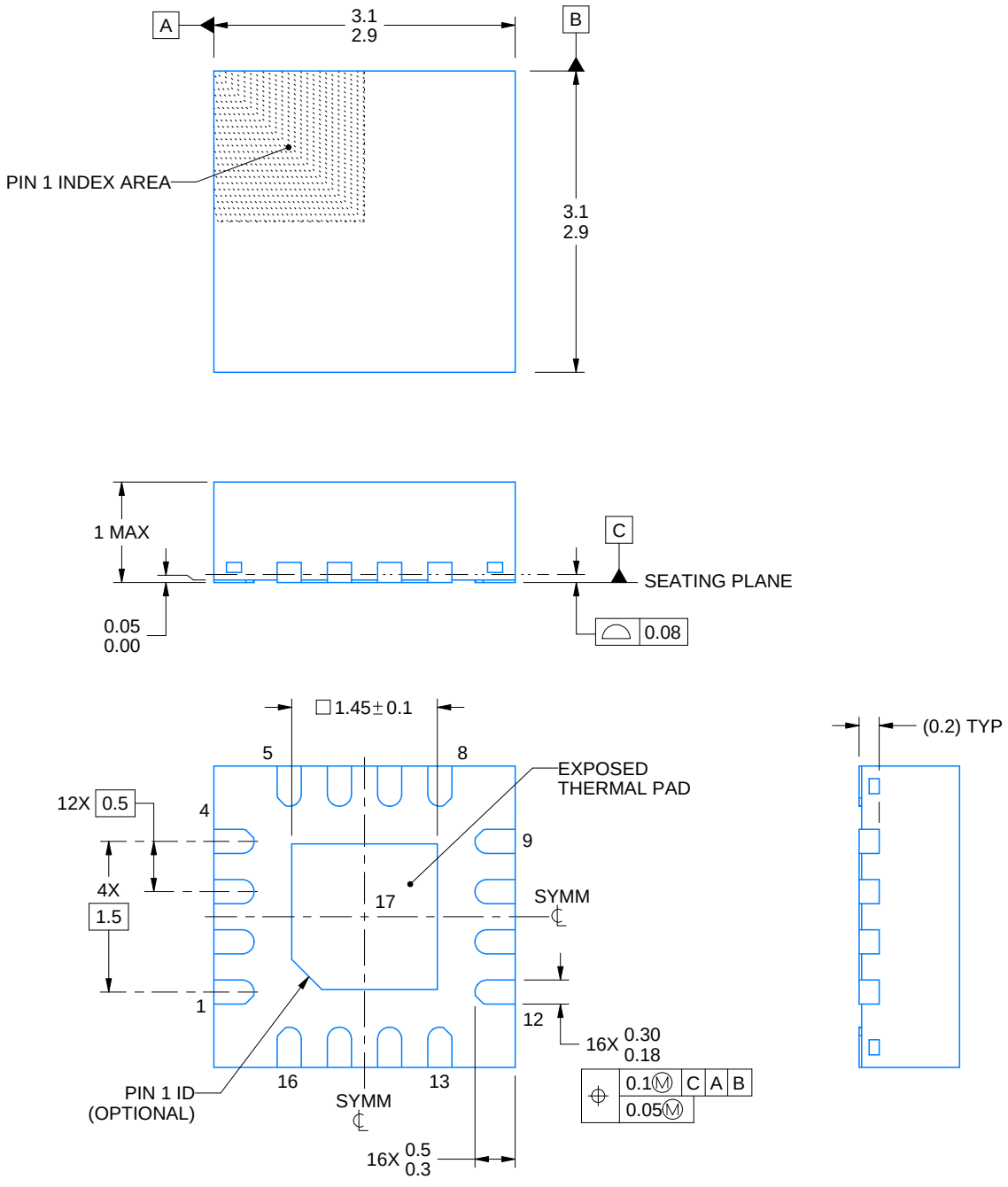
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

RGT0016A

PACKAGE OUTLINE

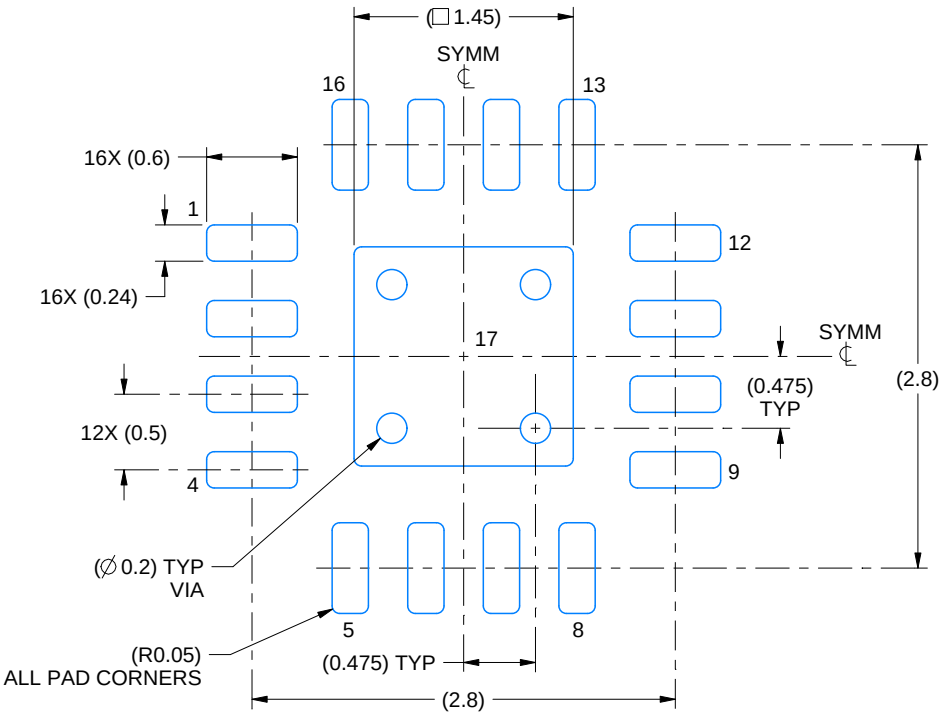
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

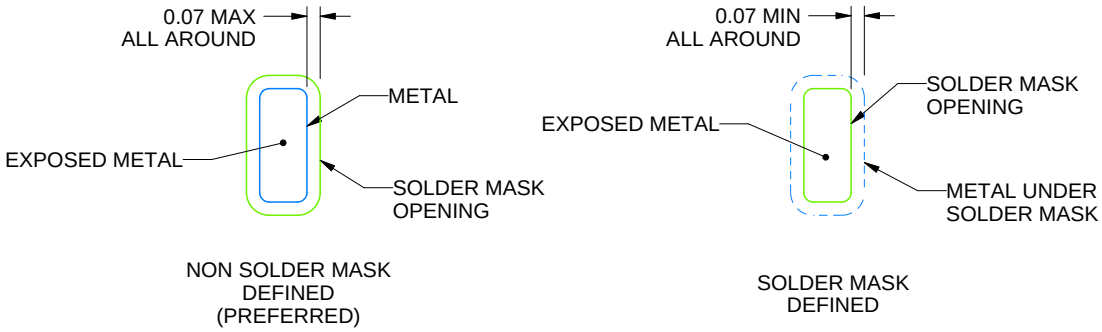


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Reference JEDEC registration MO-220



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

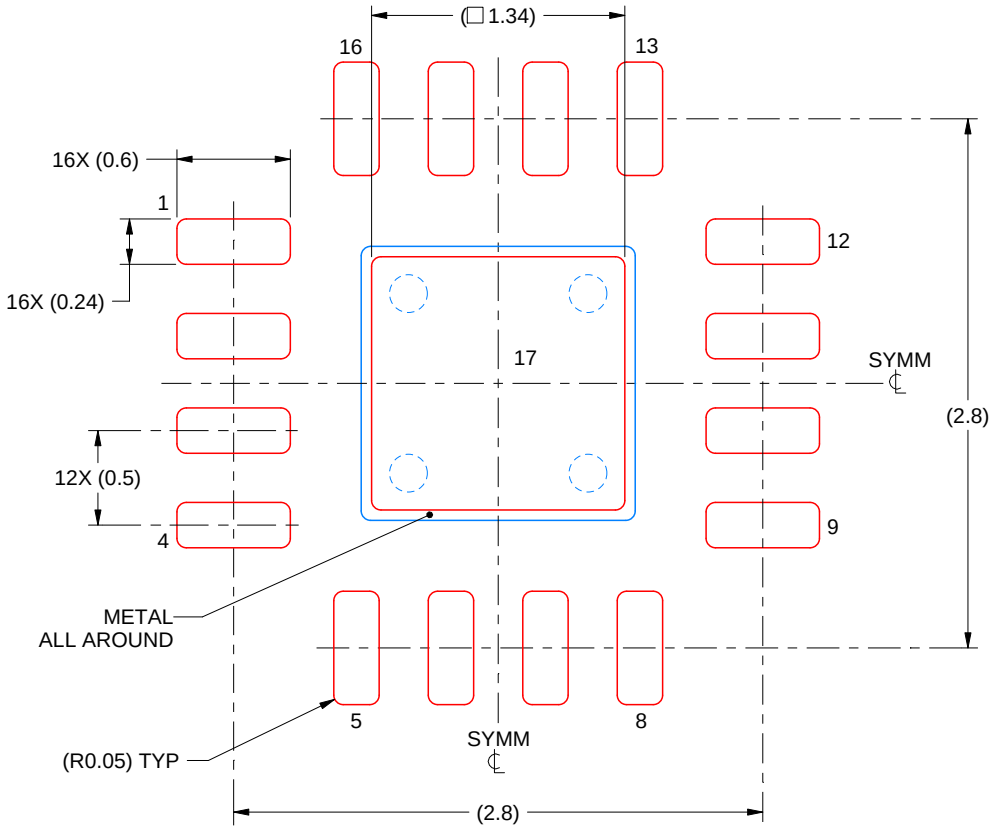


SOLDER MASK DETAILS

4219032/A 02/2017

NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
86% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4219032/A 02/2017

NOTES: (continued)

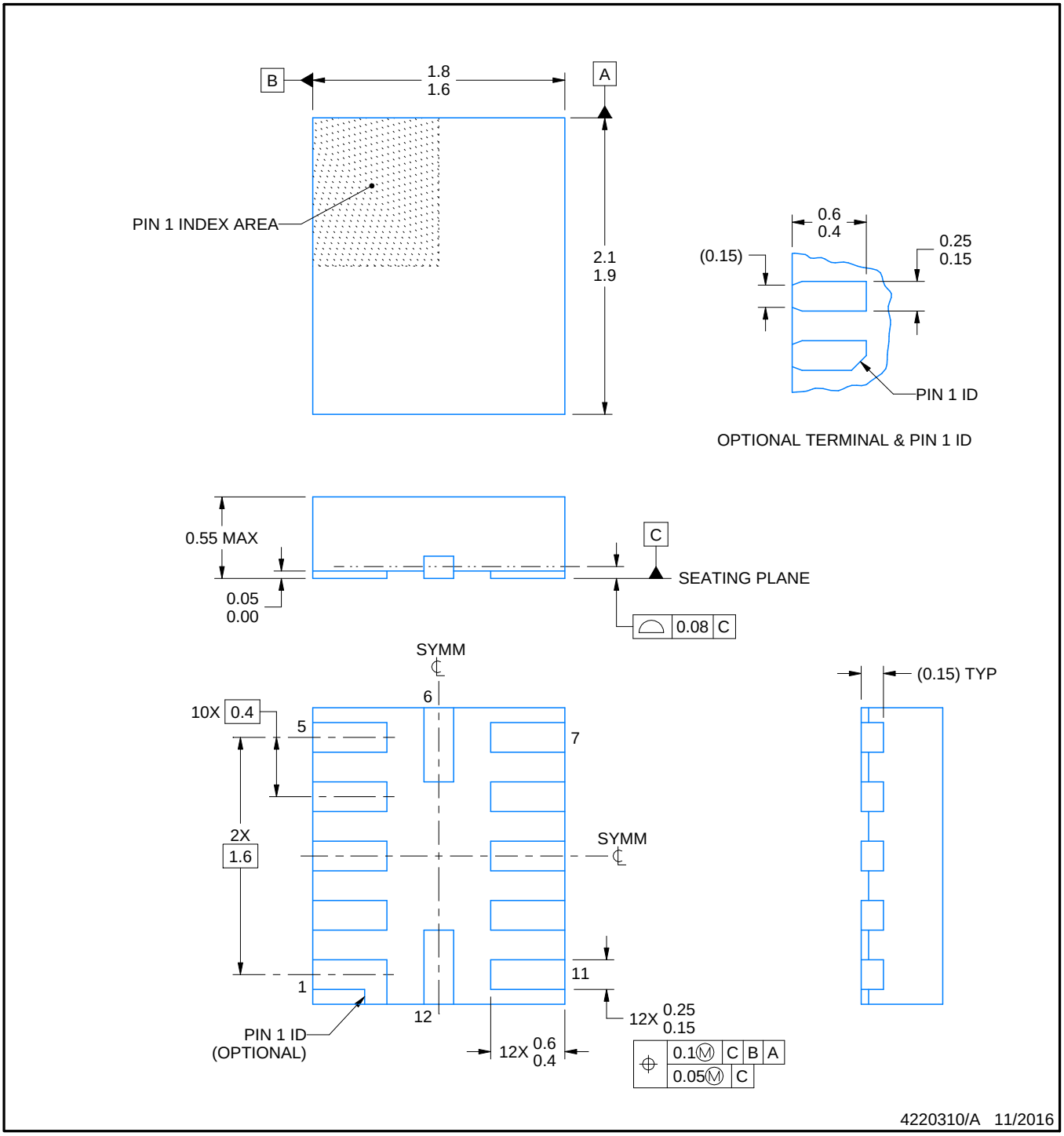
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

RUT0012A

PACKAGE OUTLINE

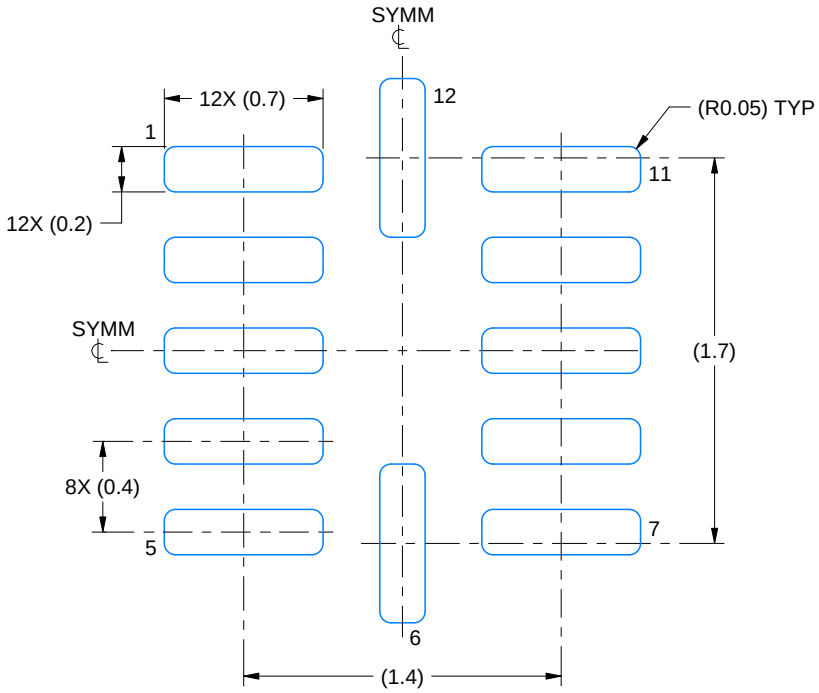
UQFN - 0.55 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

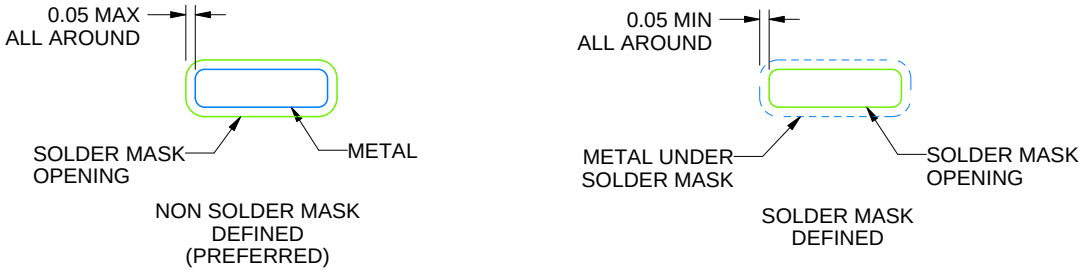


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:30X

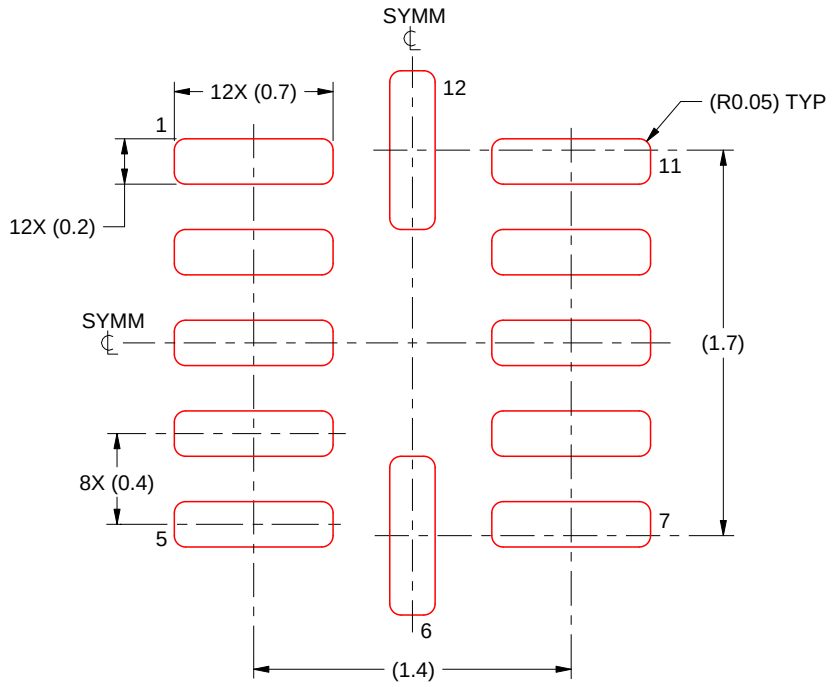


SOLDER MASK DETAILS

4220310/A 11/2016

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 30X

4220310/A 11/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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