UCC24630 Synchronous Rectifier Controller With Ultra-Low-Standby Current

1 Features

- Secondary-side SR controller optimized for flyback systems from 5V to 24V
- Operating frequency up to 200kHz
- Volt-second balance SR on-time control
- Minimize effect of MOSFET device and layout inductance
- CCM operation compatibility
- Compatible with PSR and SSR control
- Auto low-power detect and 110µA standby mode current
- Wide VDD range from 3.6V to 28V
- Rail-to-rail gate driver with 13V clamp
- Open and short pin fault protection

2 Applications

- 5V to 24V output flyback and forward converters
- USB-PD adapters and chargers with type-C connector
- Chargers for smart phones and tablets
- Notebook and Ultrabook adapters
- High efficiency auxiliary power in server, desktop and appliance applications
- Industrial and medical SMPS

3 Description

The UCC24630 SR controller is a high-performance controller and driver for N-channel MOSFET power devices used for secondary-side synchronous rectification.

The combination of controller and MOSFET emulates a near-ideal diode rectifier. This solution not only directly reduces power dissipation of the rectifier but also reduces primary-side losses as well, due to compounding of efficiency gains.

Utilizing a volt-second balancing control method, the UCC24630 is designed for flyback power supplies over a wide-output voltage range since the device is not connected directly to the MOSFET drain. The SR drive turn-off threshold is not dependent on the MOSFET $R_{DS(on)}$ which allows optimizing for maximum conduction time. Also secondary current ringing due to device and layout inductance does not affect the SR turn-off threshold.

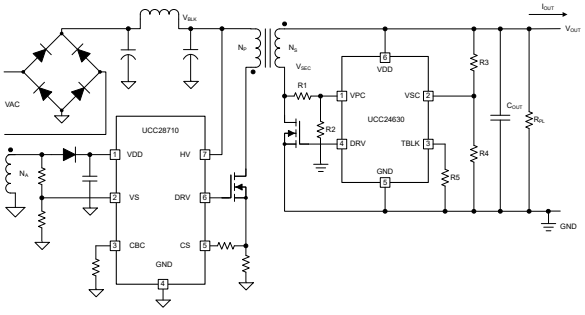
The UCC24630 controller offers a programmable false-trigger filter, a frequency detector to automatically switch to standby mode during low power conditions and pin fault protections. The UCC24630 is compatible with DCM, TM and CCM operation.

The wide VDD operating range, wide programming range of the VPC voltage and blanking time, allows use in a variety of flyback converter designs.

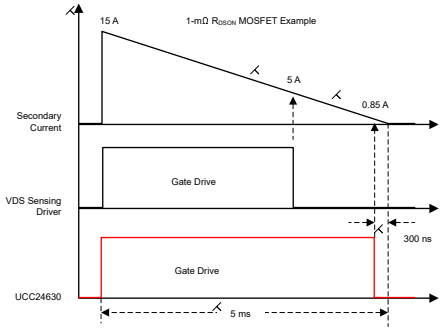
Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
UCC24630	DBV (SOT23, 6)	2.92mm × 1.30mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Schematic



Gate-Drive Timing vs VDS Sensing SR Driver

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4 Pin Configuration and Functions

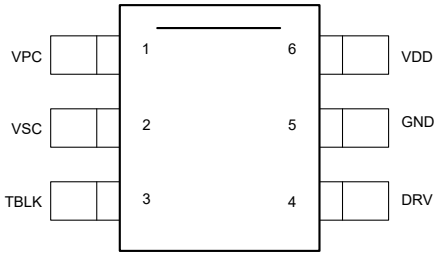


Figure 4-1. DBV Package 6-Pin SOT23 Top View

Table 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
DRV	4	O	**DRiVe** is an output used to drive the gate of an external synchronous rectifier N-channel MOSFET switching transistor, with source pin connected to GND.
GND	5	G	The **GrouND** pin is both the reference pin for the controller and the low-side return for the drive output. Take special care to return all AC decoupling capacitors as close as possible to this pin and avoid any common trace length with analog signal return paths.
TBLK	3	–	**Time BLanK** pin is used to select the blanking time of the VPC rising edge. A programmable range from 200ns to 1µs is available to prevent false detection of the primary on-time due to ringing during DCM operation.
VDD	6	P	**VDD** is the bias supply input pin to the controller. A carefully placed bypass capacitor to GND is required on this pin.
VPC	1	I	The **Voltage during Primary Conduction** pin is connected to a resistor divider from the SR MOSFET drain. This pin determines a sample of the primary-side MOSFET volt seconds during the primary on-time. This voltage programs a voltage controlled current source for the internal VPC ramp charging current.
VSC	2	I	The **Voltage during Secondary Conduction** pin is connected to a resistor divider from the power-supply output. This pin determines a sample of the secondary-side output voltage used to determine SR MOSFET conduction time. This voltage programs a voltage controlled current source for the internal VSC ramp charging current.

(1) P = Power, G = Ground, I = Input, O = Output, I/O = Input/Output

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
V_{VDD}	Bias supply voltage, VDD	–0.3	30	V
I_{DRV}	Continuous gate current sink, DRV		50	mA
I_{DRV}	Continuous gate current source, DRV		–50	mA
I_{VPC}	Peak VPC pin current		–1.2	mA
V_{DRV}	Gate drive voltage at DRV	–0.3	Self limiting	V
V_{VPC}, V_{VSC}	Voltage range, VPC, VSC	–0.3	4.5	V
T_J	Operating junction temperature range	–55	150	°C
T_L	Lead temperature 0.6mm from case for 10 seconds		260	°C
T_{STG}	Storage temperature	–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 2000V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±2000V may actually have higher performance.
(2) JEDEC document JEP157 states that 500V CDM allows safe manufacturing with a standard ESD control process. Pins listed as ±500V may actually have higher performance.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{VDD}	Bias supply operating voltage	3.75	28	V
C_{VDD}	VDD bypass capacitor	0.47		µF
T_J	Operating junction temperature	-40	125	°C
V_{VPC}, V_{VSC}	Operating Range	–0.3	2.3	V

5.4 Thermal Information

THERMAL METRIC(1)		UCC24630 DBV (6 PINS)	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	180	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	71.2	
$R_{\theta JB}$	Junction-to-board thermal resistance	44	
ψ_{JT}	Junction-to-top characterization parameter	5.1	
ψ_{JB}	Junction-to-board characterization parameter	13.8	

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.5 Electrical Characteristics

Over operating free-air temperature range, VDD = 12V, T_A = –40°C to 125°C, T_A = T_J (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
SUPPLY INPUT						
I_{RUN}	Supply current, run	I_{DRV} = 0, run state, F_{SW} = 0kHz		0.9	1.2	mA
I_{STBY}	Supply current, standby	I_{DRV} = 0, standby mode		110	160	µA
UNDER-VOLTAGE LOCKOUT						
$V_{VDD(on)}$	VDD turn-on threshold	V_{VDD} low to high	3.9	4	4.3	V
$V_{VDD(off)}$	VDD turn-off threshold	V_{VDD} high to low	3.3	3.6	3.7	V
DRV						
R_{DRVLS}	DRV low-side drive resistance	I_{DRV} = 100mA		1	2	Ω
V_{DRVST}	DRV pull down in start-up	V_{DD}= 0 to 2V, I_{DRV}= 10 µA			0.95	V
V_{DRCL}	DRV clamp voltage	V_{VDD} = 30V	11	13	15	V
V_{PMOS}	Disable PMOS high-side drive	V_{DD} voltage to disable rail-to-rail drive, V_{DD} rising	9.3	10	10.5	V
$V_{PMOS-HYS}$	PMOS enable hysteresis	V_{DD} voltage hysteresis to enable rail to rail drive, V_{DD} falling	0.75	1	1.25	V
V_{DRHI}	DRV pull-up high voltage	V_{VDD} = 5V, I_{DRV} = 15mA	4.6	4.75	5	V
VSC INPUT						
V_{VSCEN}	SR enable voltage	V_{VSC} > V_{VSCEN}, V_{VSC} rising	250	300	340	mV
$V_{VSC-HYS}$	SR enable hysteresis	V_{VSC} falling		50		mV
V_{VSCDIS}	SR disable voltage		220		280	mV
I_{VSC}	Input bias current	V_{VSC} = 2V	–0.25	0	0.4	µA
VPC INPUT						
V_{VPCEN}	SR enable voltage	V_{VPCEN} < V_{VPC}	345	400	450	mV
V_{VPCDIS}	VPC threshold to disable SR	V_{VPC} > V_{VPCDIS}	2.6	2.85	3.1	V
V_{VPC-TH}	Threshold of V_{VPC} rising edge	V_{VPC} = 0.95V, V_{VPC-TH} = 0.85x V_{VPC} previous cycle	0.76	0.808	0.86	V
$V_{VPC-TH-CLP}$	Clamp threshold of V_{VPC} rising edge	V_{VPC} = 2V	0.9	1	1.1	V
I_{VPC}	Input bias current	V_{VPC} = 2V	–0.25	0	0.4	µA
CURRENT EMULATOR						
$Ratio_{VPC\_VSC}$	K_{VPC}/K_{VSC}	V_{VPC} = 1.25V, t_{VPC} = 1µs, V_{VSC} = 1.25V	3.97	4.17	4.35	
		V_{VPC} = 1.25V, t_{VPC} = 5µs, V_{VSC} = 1.25V	3.95	4.17	4.37	
		V_{VPC} = 2V, t_{VPC} = 1µs, V_{VSC} = 1.25V	3.85	4.09	4.26	
		V_{VPC} = 1.25V, t_{VPC} = 1µs, V_{VSC} = 0.45V	3.85	4.07	4.28	
CCM DEAD TIME						
$K_{CCM-FAULT}$	If t_{SW} (N+1) > t_{SW} (N) x $K_{CCM-FAULT}$, disable SR		140%	150%	165%	
$n_{CCM-FLT}$	Number of cycles to exit CCM fault if t_{SW} (N+1) < t_{SW} (N) x $K_{CCM-FAULT}$			4		

5.5 Electrical Characteristics (continued)

Over operating free-air temperature range, VDD = 12V, T_A = –40°C to 125°C, T_A = T_J (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
STANDBY OPERATION						
n_{ENTO}	Number of switching cycles to enter standby operation during t_{ENTO}			64		
n_{EN}	Number of switching cycles to exit standby operation during t_{EN} (1)			32		
OVER TEMPERATURE PROTECTION						
$T_{(STOP)}$	Thermal shutdown temperature	Internal junction temperature		165		°C

(1) The device exits standby operation as soon as n_{EN} occurs within t_{EN}.

5.6 Timing Requirements

Over operating free-air temperature range, VDD = 12V, T_A = –40°C to 125°C, T_A = T_J (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
DRV						
t_R	DRV high-side rise time	V_{VDD} = 12V, C_L = 3.3nF, V_{DRV} = 2V to 8V		27	54	ns
		V_{VDD} = 5V, C_L = 3.3nF, V_{DRV} = 1V to 4V		50	100	ns
t_F	DRV low-side fall time	V_{VDD} = 12V, C_L = 3.3nF, V_{DRV} = 8V to 2V		20	54	ns
		V_{VDD} = 5V, C_L = 3.3nF, V_{DRV} = 4V to 1V		15	50	ns
t_{DRVON}	Propagation delay to DRV High	V_{VPC} = 1V to –0.05V falling to DRV high, V_{VDD} = 12V, V_{DRV} = 0V to 2V		80	160	ns
t_{DRVOFF}	Propagation delay to DRV Low	Test mode		65	95	ns
VPC Input						
$t_{VPC-SPL}$	VPC sampling time window		81	100	125	ns
$t_{VPC-BLK}$	Minimum VPC pulse for SR DRV operation	R_{TBLK} = 5kΩ	169	203	239	ns
		R_{TBLK} = 50kΩ	0.87	1.04	1.2	µs
SR On Control						
$t_{SRONMIN}$	SR minimum on time after VPC falling.		300	350	425	ns
t_{OFF}	SR off blanking time from DRV falling.		2.35	2.5	2.65	us
CCM Dead Time						
t_{CCMDT}	SR turn-off dead time in CCM cycle limit	F_{SW} = 100kHz, R_{TBLK} = 50kΩ (1µs $t_{VPC-BLK}$ setting)	500	600	700	ns
Standby Operation						
t_{ENTO}	Time to disable SR operation, enter standby	Time to disable DRV	11.5	12.8	14.1	ms
t_{EN}	Time to enable SR operation, exit standby operation	Time to enable DRV(1)	2.3	2.56	2.82	ms

(1) The device exits standby operation as soon as n_{EN} occurs within t_{EN}.

5.7 Typical Characteristics

V_{VDD} = 12V, T_J = 25°C, unless otherwise noted.

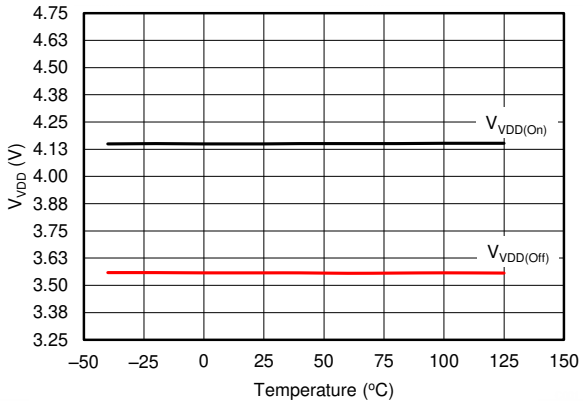


Figure 5-1. VDD Turn-On and Turn-Off Threshold vs Temperature

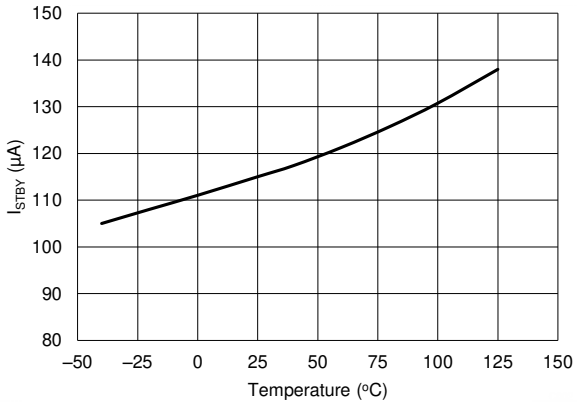


Figure 5-2. Standby Current vs Temperature

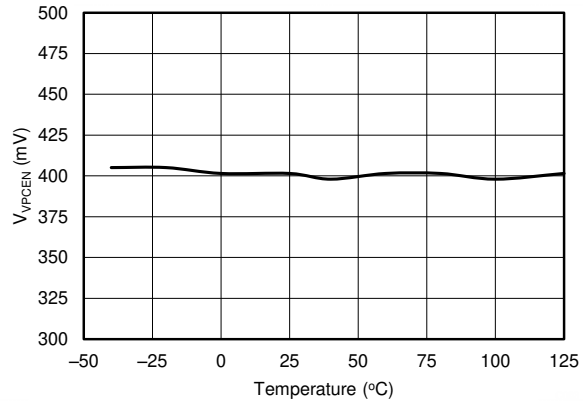


Figure 5-3. VPC Enable Threshold vs Temperature

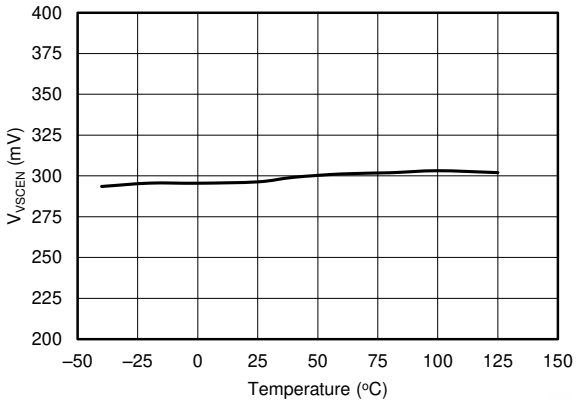


Figure 5-4. VSC Enable Threshold vs Temperature

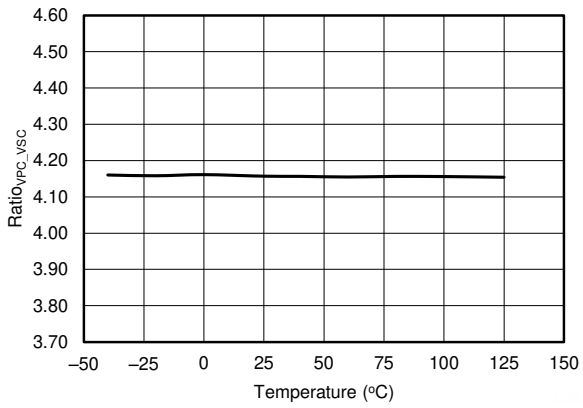


Figure 5-5. VPC-to-VSC Ramp Gain Ratio vs Temperature

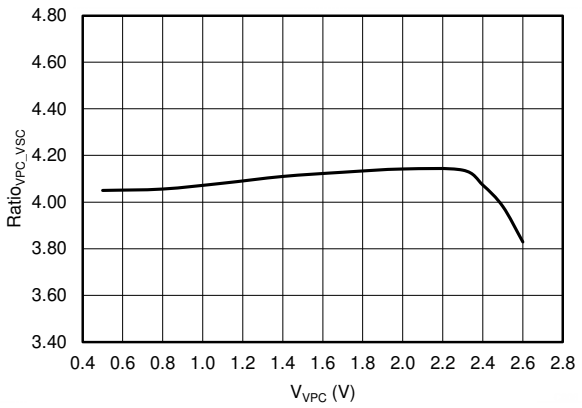
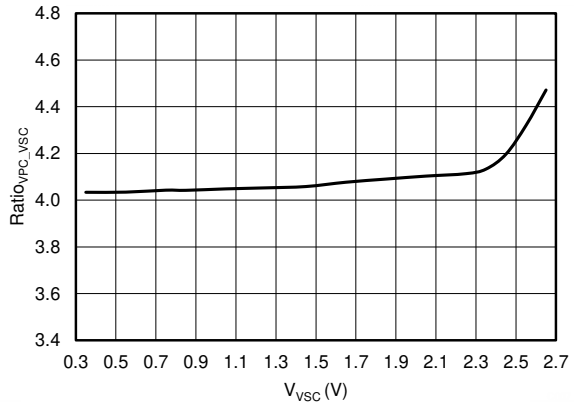


Figure 5-6. VPC-to-VSC Ramp-Gain Ratio vs VPC Voltage

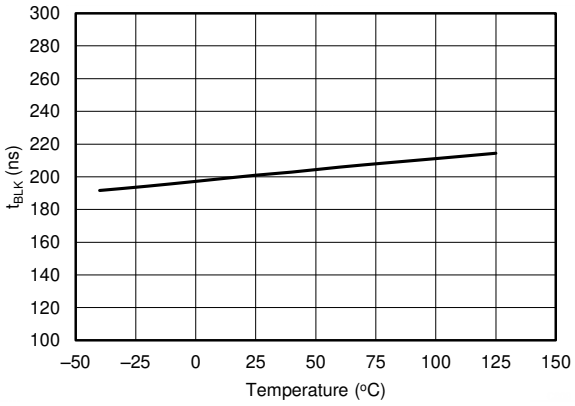
5.7 Typical Characteristics (continued)

V_{VDD} = 12V, T_J = 25°C, unless otherwise noted.



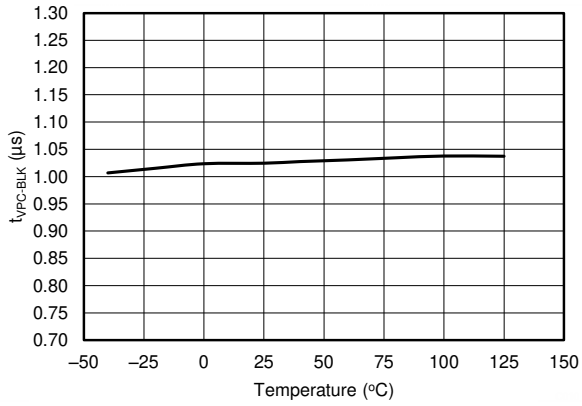
V_{VPC} = 12V t_{VPC} = 2µs

Figure 5-7. VPC-to-VSC Ramp-Gain Ratio vs VSC Voltage



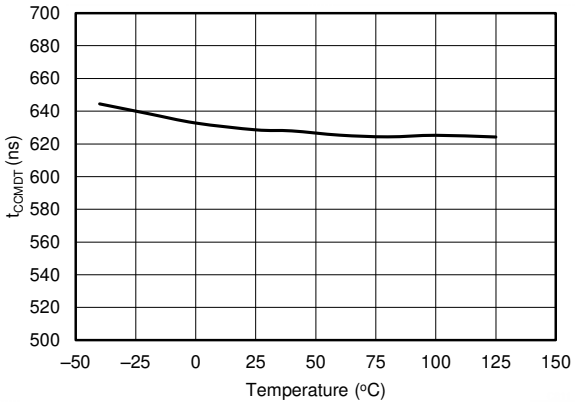
R_{TBLK} = 5kΩ

Figure 5-8. VPC Blanking Time vs Temperature (minimum setting)



R_{TBLK} = 50kΩ

Figure 5-9. VPC Blanking Time vs Temperature (maximum setting)



Fsw = 100kHz R_{TBLK} = 50k

Figure 5-10. CCM Dead Time vs Temperature

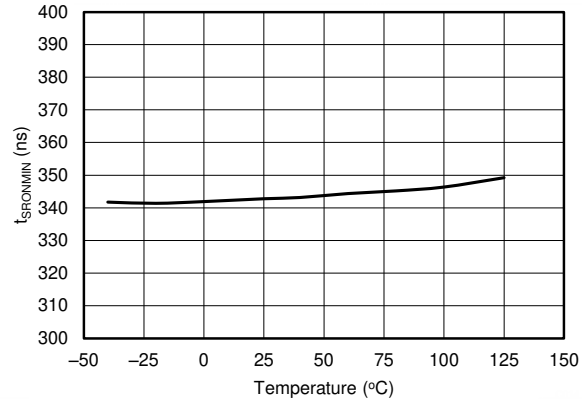


Figure 5-11. DRV Minimum On Time vs Temperature

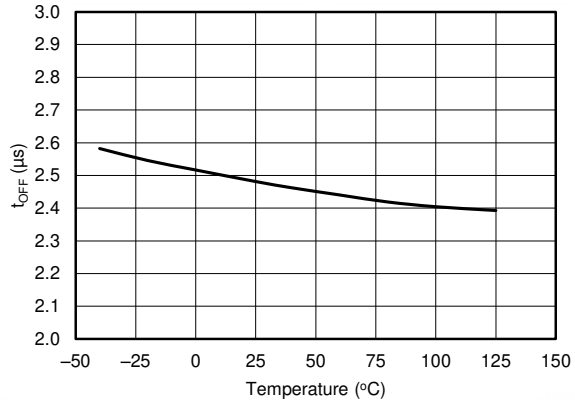


Figure 5-12. DRV Minimum Off Time vs Temperature

6 Detailed Description

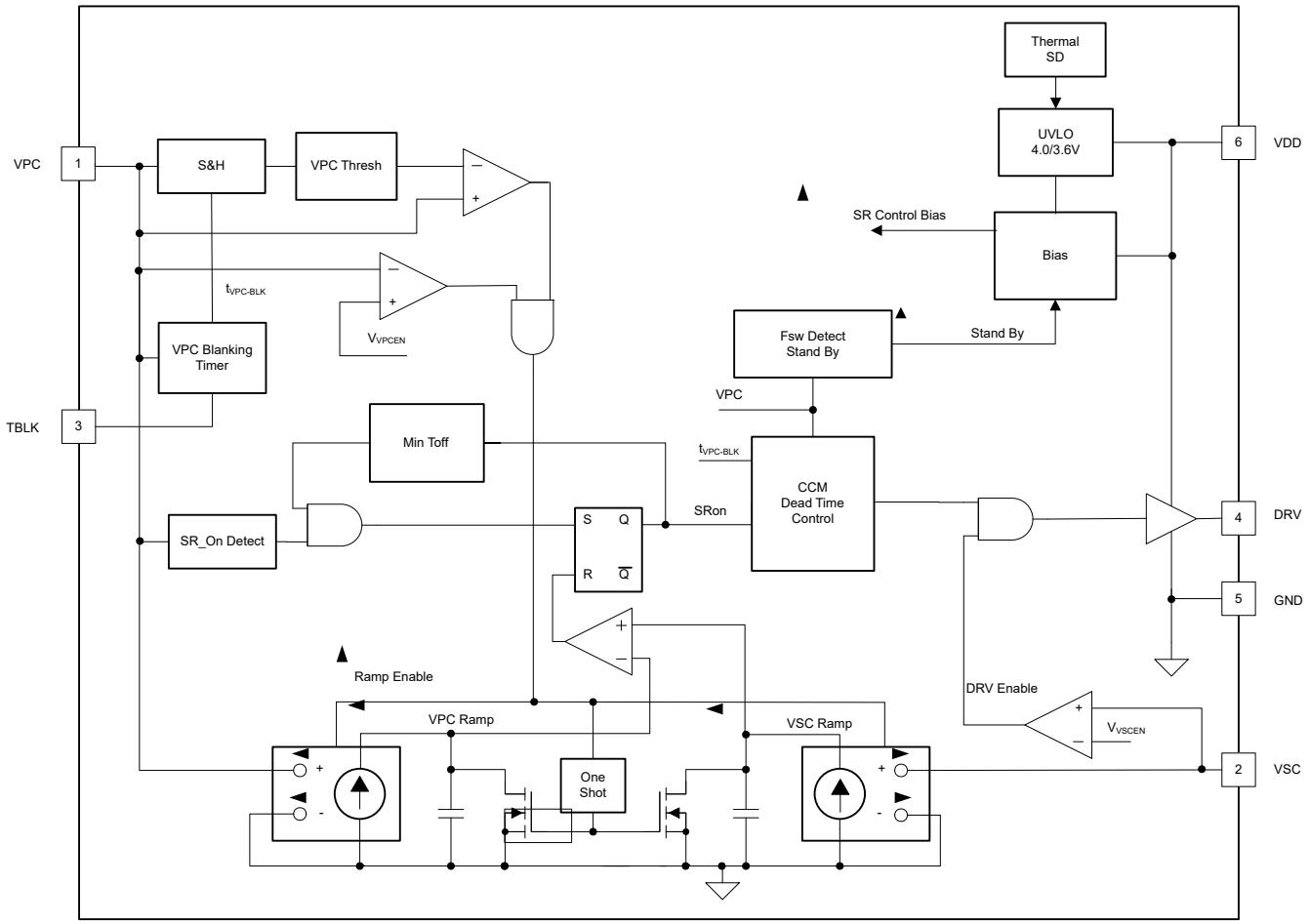
6.1 Overview

The UCC24630 SR controller is targeted for flyback converters operating in DCM, TM, and CCM modes of operation. The control method to determine SR on time is based on the volt-second balance principle of primary and secondary conduction volt-second product. In converters operating in DCM and TM, the secondary current always returns to zero in each cycle. In CCM operation, volt-second balance occurs in steady state operation. The inductor charge voltage and time product is equal to the discharge voltage and time product. The device uses internal current ramp emulators to predict the proper SR on time based on voltage and time information on the VPC and VSC pins.

In CCM converters during the transition from DCM operation into CCM, volt-second balance does not occur for several cycles. In this case CCM operation compatibility is achieved by limiting the maximum SR MOSFET on time with a CCM dead-time function, based on the previous switching period. There is fault protection to disable the SR in the event the operating periods become unstable during extreme operating transients.

To achieve very low standby power in the converter, the UCC24630 has a standby mode of operation that disables the SR MOSFET drive and reduces the device bias current to I_{STBY}. The device monitors the average switching frequency of the converter to enter and exit the standby mode of operation. The device is compatible with converters operating in burst mode or constant frequency in light-load mode.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Start Up and UVLO

The UCC24630 features a wide operating VDD range and low UVLO thresholds. The start up of the device depends on voltage levels on three pins: VDD, VPC and VSC. The VDD pin can be directly connected to the power supply output on converters from 5V to 24V nominal outputs. The start UVLO threshold is $V_{VDD(on)}$, 4.0V typical, and stop threshold is $V_{VDD(off)}$, 3.6V typical. The DRV output is not enabled unless the voltage on the VPC pin is greater than V_{VPCEN} for a time longer than $t_{VPC-BLK}$ and the voltage on the VSC pin is greater than V_{VSCEN}. Once the VDD, VSC and VPC voltage and time thresholds are met, there is an internal initialization time and a four-cycle-initialization start sequence before the DRV output is enabled.

See Figure 6-1 for a startup sequence that shows the timing sequence and configurable DRV output based on VDD level. In most converter designs, the conditions for the VPC and VSC voltage to enable the device are met before the VDD start-voltage threshold, this is reflected in the timing diagram. When VDD exceeds $V_{VDD(on)}$ UVLO threshold the device starts the initialization sequence from 150µs to 250µs illustrated as $t_{INITIALIZE}$. After the device initialization, there is a logic initialization of 20µs at which time V_{TBLK} is enabled (high). After the device is enabled, the CCM dead-time block requires four cycles to initialize the dead-time control before the DRV output is enabled. At VDD < V_{PMOS} the driver high-side PMOS device is enabled and the DRV peak is close to VDD. When VDD exceeds V_{PMOS} the PMOS device is disabled and the driver is operating as a high-side NMOS only and DRV is approximately from 1.2V to 1.5V lower than VDD. As VDD continues to increase, the DRV output is limited to V_{DRCL} regardless of VDD up to the recommended maximum rating.

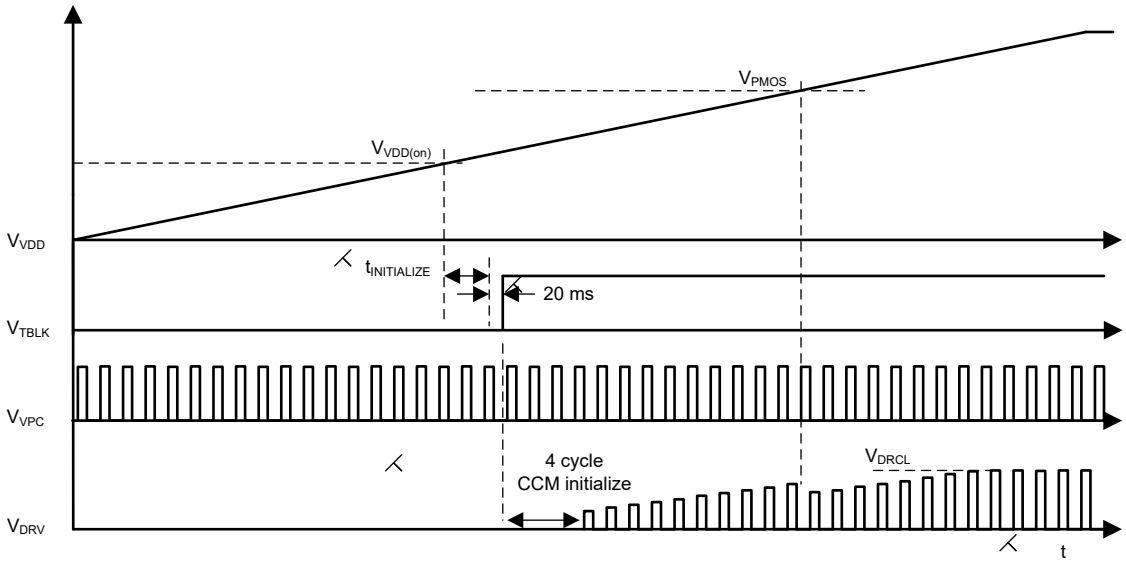


Figure 6-1. Start-Up Operation

6.3.2 Volt-Sec SR Driver On-Time Control

See the timing diagrams in Figure 6-2 and Figure 6-3 for functional details of the UCC24630 volt-sec on-time control.

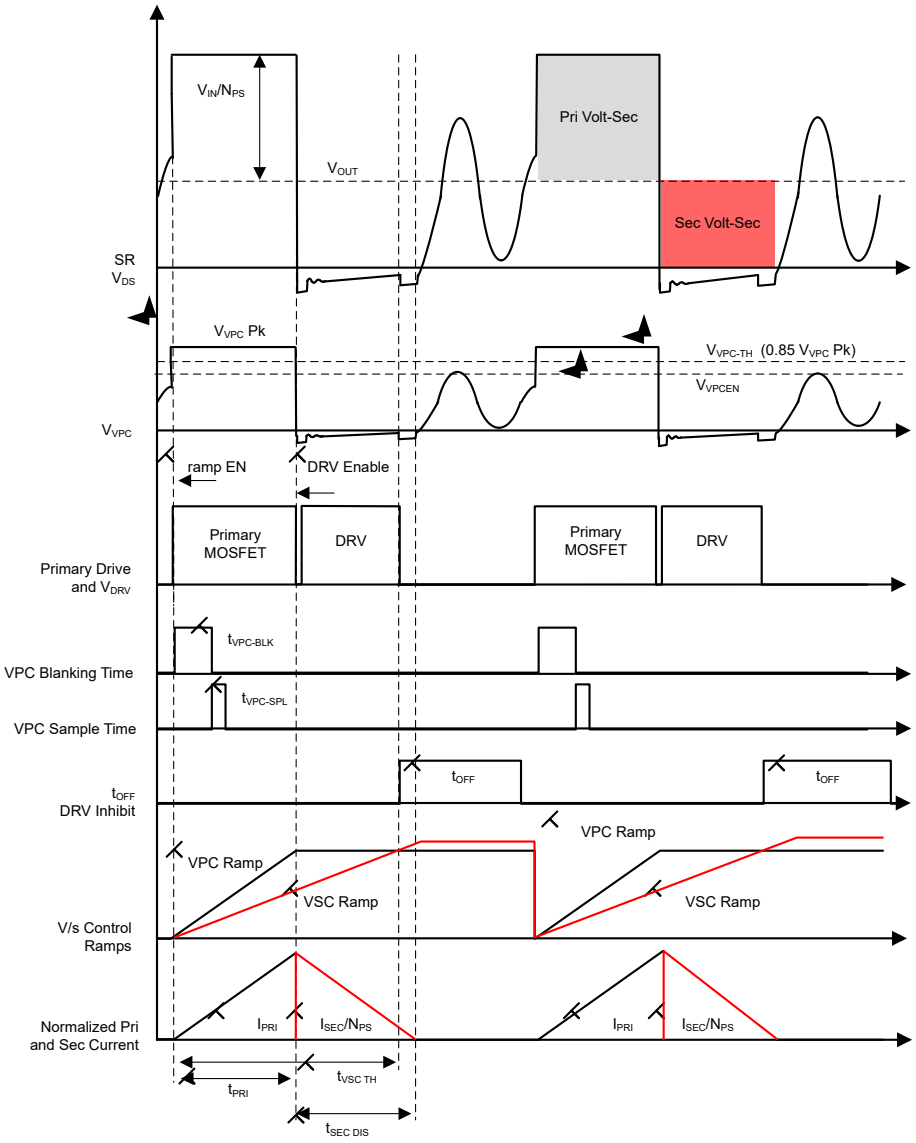


Figure 6-2. Operation in DCM

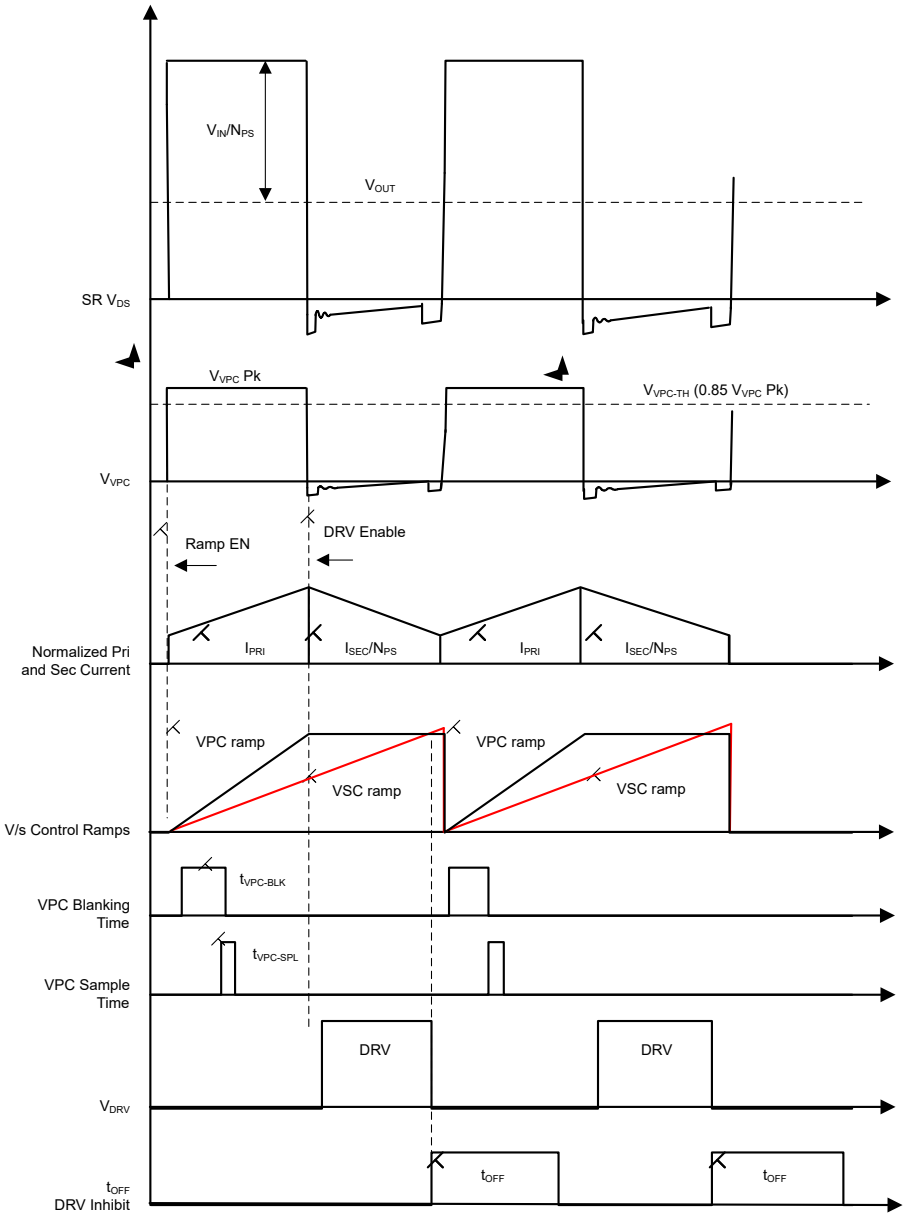


Figure 6-3. Operation in CCM

The UCC24630 uses the VPC and VSC pins to sense the SR MOSFET V_{DS} voltage and converter V_{OUT} voltage through resistor dividers. The information of V_{IN}/N_{PS}, t_{PRI}, and V_{OUT} is obtainable from the information on VPC and VSC pins. The SR MOSFET turn-on is determined when the SR MOSFET body diode starts conducting and the VPC pin voltage falls to near zero; the SR MOSFET turn-off is determined by the current emulator control ramps. The SR timing determined by the volt-sec balance function is the dominant mode of operation with all flyback converters, including CCM.

The UCC24630 volt-sec control generates the internal VPC ramp and VSC ramp to emulate the transformer Volt-Sec balancing as shown in Figure 6-2 and Figure 6-3.

The secondary current discharge time, $t_{SEC-DIS}$ is indirectly determined. The primary volt-sec ramp and secondary volt-sec ramp both start when VPC rises above V_{VPCEN} and V_{VPC-TH}. The charge currents for the VPC and VSC ramps are determined by the voltage on the VPC and VSC pins respectively.

When VPC is higher than V_{VPCEN} and V_{VPC-TH} for t > $t_{VPC-BLK}$, the VPC pulse is qualified as a primary conduction pulse and the SR is enabled on the VPC falling edge. The VPC ramp continues to rise until the VPC falling edge based on the real-time voltage on the VPC pin and holds the peak for the cycle. The DRV output is turned on during the VPC falling edge near zero volts, and DRV is turned off when the VSC rising ramp crosses the VPC ramp held level.

Both VPC and VSC ramps are reset to zero on each VPC rising edge above the V_{VPCEN} and V_{VPC-TH} thresholds.

To discriminate primary on-time pulses from DCM ringing, there are voltage and time criteria that must be satisfied on the VPC pin to enable the DRV output. $t_{VPC-BLK}$ can be adjusted through the resistor on TBLK pin.

At the rising edge of VPC when the voltage exceeds V_{VPCEN} and V_{VPC-TH} the blanking time $t_{VPC-BLK}$ is initiated. At the end of $t_{VPC-BLK}$, the VPC voltage is sampled during $t_{VPC-SPL}$ window, which is 100ns nominal. Also at the end of $t_{VPC-BLK}$, the DRV output is enabled.

The VPC voltage sampled during $t_{VPC-SPL}$ determines the VPC dynamic threshold V_{VPC-TH} which is normally 85% of the sampled VPC voltage. The dynamic threshold provides the ability to reject the DCM ringing and detect the primary on-time. Noise immunity during the turn-on event of DRV at the falling edge of the VPC pin is enhanced by a minimum DRV on time of $t_{SRONMIN}$, which is 350ns nominal.

During the falling edge of DRV, the t_{OFF} timer is initiated which inhibits turn-on of the SR until t_{OFF} expires. This eliminates false turn-on of DRV if the DCM ringing is close to ground.

The UCC24630 is designed to operate in a variety of flyback converter applications over a wide operating range. The internal volt-sec control ramps do have a dynamic range limit based on volt-sec on the VPC pin. As shown in Figure 6-4, a Volt-sec product exceeding 7V-µs on the VPC pin results in saturation of the VPC volt-sec control ramp. Operation beyond this point results in a DRV on-time less than expected. For example, if V_{VPC} = 0.5V, t_{VPC} must be < 14µs, or if V_{VPC} = 2.0V, t_{VPC} must be < 3.5µs, to operate within the dynamic range of the device. Assuming a converter operating in transition mode at low line and full load with a 50% duty cycle, the operating period is 28µs which results in a frequency that is under 40kHz. The UCC24630 low-frequency operating range extends to the standby mode threshold of 5kHz; but each switching cycle V_{VPC} Volt-sec product must be less than 7V-µs.

The device can support switching frequencies exceeding 200kHz but the following timing limits need to be confirmed to be compatible with the power train. The minimum primary on time when the device is expected to be active must be compatible with the minimum VPC blanking time ($t_{VPC-BLK}$) setting of 203ns plus the sampling window ($t_{VPC-SPL}$) of 100ns. The minimum secondary current conduction time must be larger than the minimum SR on time ($t_{SR(min)}$) of 350ns. The minimum time from the SR drive turn-off until the next SR drive turn-on must be greater than the SR minimum off time (t_{OFF}) of 2.5µs.

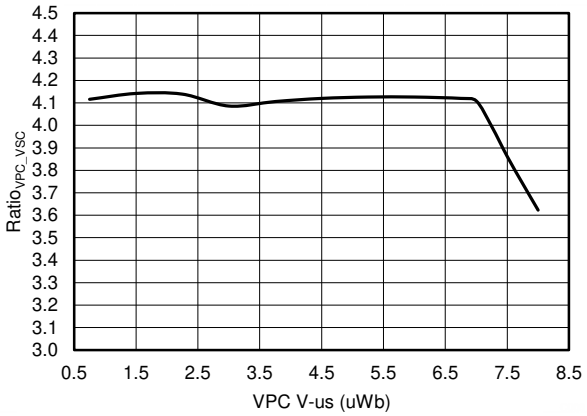


Figure 6-4. $Ratio_{VPC\_VSC}$ vs VPC V-µs

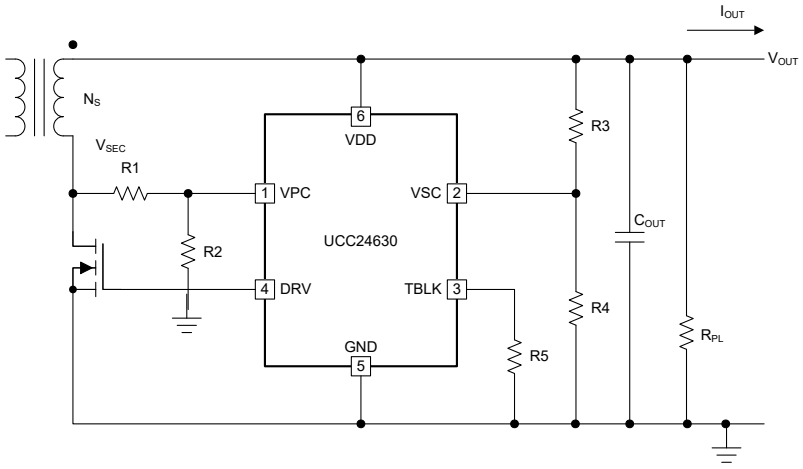


Figure 6-5. SR Controller Components

Determining the VPC and VSC divider resistors is based on the operating voltage ranges of the converter and $Ratio_{VPC-VSC}$ gain ratio. Referring to Figure 6-5, the following equation determines the VPC divider values.

For R2a value of 10kΩ is recommended for minimal impact on time delay, and low-resistor dissipation. A higher R2 value reduces resistor divider dissipation but can increase the DRV turn-on delay due to the time constant of ~2pF pin capacitance and divider resistance. A lower R2 value can be used with the trade-off of higher dissipation in the resistor divider. A factor of 10% over the VPC threshold, V_{VPCEN}, is shown in Equation 1 for design margin.

$$R1 = \frac{\left(\left[\frac{V_{IN(min)}}{N_{PS}} + V_{OUT(min)}\right] - V_{VPCEN} \times 1.1\right) \times R2}{V_{VPCEN} \times 1.1} \quad (1)$$

where

- $V_{IN(min)}$ is the converter minimum primary bulk capacitor voltage.
- $V_{OUT(min)}$ is the minimum converter output voltage in normal operation.
- V_{VPCEN} is the VPC enable threshold, use the specified maximum value.
- N_{PS} is the transformer primary to secondary turns ratio.

The operating voltage range on the VPC pin must be within the range of 0.45V < V_{VPC} < 2V. Referring to Figure 5-6, if V_{VPC} is greater than 2.3V the dynamic range is exceeded and $Ratio_{VPC\_VSC}$ is reduced; in this condition the DRV on time is less than expected. If V_{VPC} is greater than 2.6V for 500ns, a fault is generated and DRV is disabled for the cycle, see Section 6.3.5. To establish the maximum voltage is within range confirm with Equation 2.

$$V_{VPC(max)} = \frac{\left[\frac{V_{IN(max)}}{N_{PS}} + V_{OUT(max)}\right] \times R2}{R1 + R2} \quad (2)$$

where

- $V_{IN(max)}$ is the converter maximum primary bulk capacitor voltage.
- $V_{OUT(max)}$ is the maximum converter output voltage at OVP.
- N_{PS} is the transformer primary-to-secondary turns ratio.

The program voltage on the VSC pin is determined by the VPC divider ratio and the device's parameter $Ratio_{VPC\_VSC}$. The current emulator ramp gain is higher on the VPC pin by the multiple $Ratio_{VPC\_VSC}$, so the VSC resistor divider ratio is reduced by the same $Ratio_{VPC\_VSC}$ accordingly. Determine the VSC divider resistors using equation 3 below. To minimize resistor divider dissipation, a recommended range for R4 is from 25kΩ to 50kΩ. Higher R4 values results in increasing offset due to VSC input current, I_{VSC}. Lower R4 values increases

the resistor divider dissipation. To establish DRV turn off slightly before the secondary current reaches zero, 10% margin is shown for initial values. Use a nominal value of 4.15 for $Ratio_{VPC\_VSC}$.

$$R3 = \left[\left(\frac{\frac{R1 + R2}{R2}}{Ratio_{VPC\_VSC} \times 1.1}\right) - 1\right] \times R4 \quad (3)$$

where

- $Ratio_{VPC\_VSC}$ is the device parameter VPC and VSC gain ratio, use a value of 4.15.

The operating voltage on the VSC pin must be within the range of 0.3V < V_{VSC} < 2V. Referring to Figure 5-7, if V_{VSC} is greater than 2.3V, the dynamic range is exceeded and $Ratio_{VPC\_VSC}$ is increased; in this condition the DRV on time is more than expected. To establish the VSC voltage is within range confirm with Equation 4 and Equation 5.

$$\frac{R4}{R3 + R4} \times V_{OUT(min)} \geq 0.3V \quad (4)$$

$$\frac{R4}{R3 + R4} \times V_{OUT(min)} \leq 2.0V \quad (5)$$

where

- $V_{OUT(min)}$ is the minimum converter output operating voltage of the SR controller.
- $V_{OUT(max)}$ is the maximum converter output operating voltage of the voltage at OVP.

Discrimination of ringing during DCM operation from valid primary on-time is achieved by a dynamic VPC rising threshold and programmable blanking time. The dynamic threshold V_{VPC-TH} is 85% typical ratio of the previous VPC pin peak voltage. Referring to Figure 6-2, the VPC pin voltage is sampled after the VPC voltage is greater than V_{VPCEN} and V_{VPC-TH} for t > $t_{VPC-BLK}$. The function of the dynamic threshold V_{VPC-TH} is to reject the ringing in DCM operation from the primary conduction pulses. The dynamic threshold has an active range from the minimum V_{VPCEN} voltage to a maximum of 1V clamp. The blanking time is programmable from 200ns to 1µs to accommodate a variety of converter designs.

See Figure 6-6 for guidance on selecting the blanking time. The blanking time must be selected as long as reasonable and still accommodate the minimum primary on-time at light-load condition and high-line voltage. In the high-line minimum load condition, select a blanking time that meets the following criteria (Equation 6) to accommodate tolerance of the blanking time and the $t_{VPC-SPL}$ sampling time window.

$$t_{VPC-BLK} = (t_{PRI} \times 0.85) - 120ns \quad (6)$$

For rejection of DCM ringing, the blanking time must be longer than the time that the ring is above the V_{VPC-TH} dynamic threshold, which is 85% of the minimum SR VDS peak voltage. Determine these criteria at low line and maximum load condition. It is recommended that the transformer turns ratio be selected such that the secondary reflected voltage is < 85% of $V_{IN(min)}$ bulk capacitor voltage at the highest load when DCM operation occurs at the low line input condition.

To determine the resistor value for $t_{VPC-BLK}$ use Equation 7 to select from a range from 200ns to 1µs.

$$R5 = \frac{t_{VPC-BLK} - 100ns}{18pF} \quad (7)$$

where

- $t_{VPC-BLK}$ is the target blanking time.

Additional discrimination for proper SR timing control is provided by the t_{OFF} function. See Figure 6-2 and Figure 6-3 for the timing details. After the DRV turn-off, the DRV is inhibited from turning on again until the t_{OFF} timer expires. This protects against SR false turn-on from SR V_{DS} DCM ringing below ground.

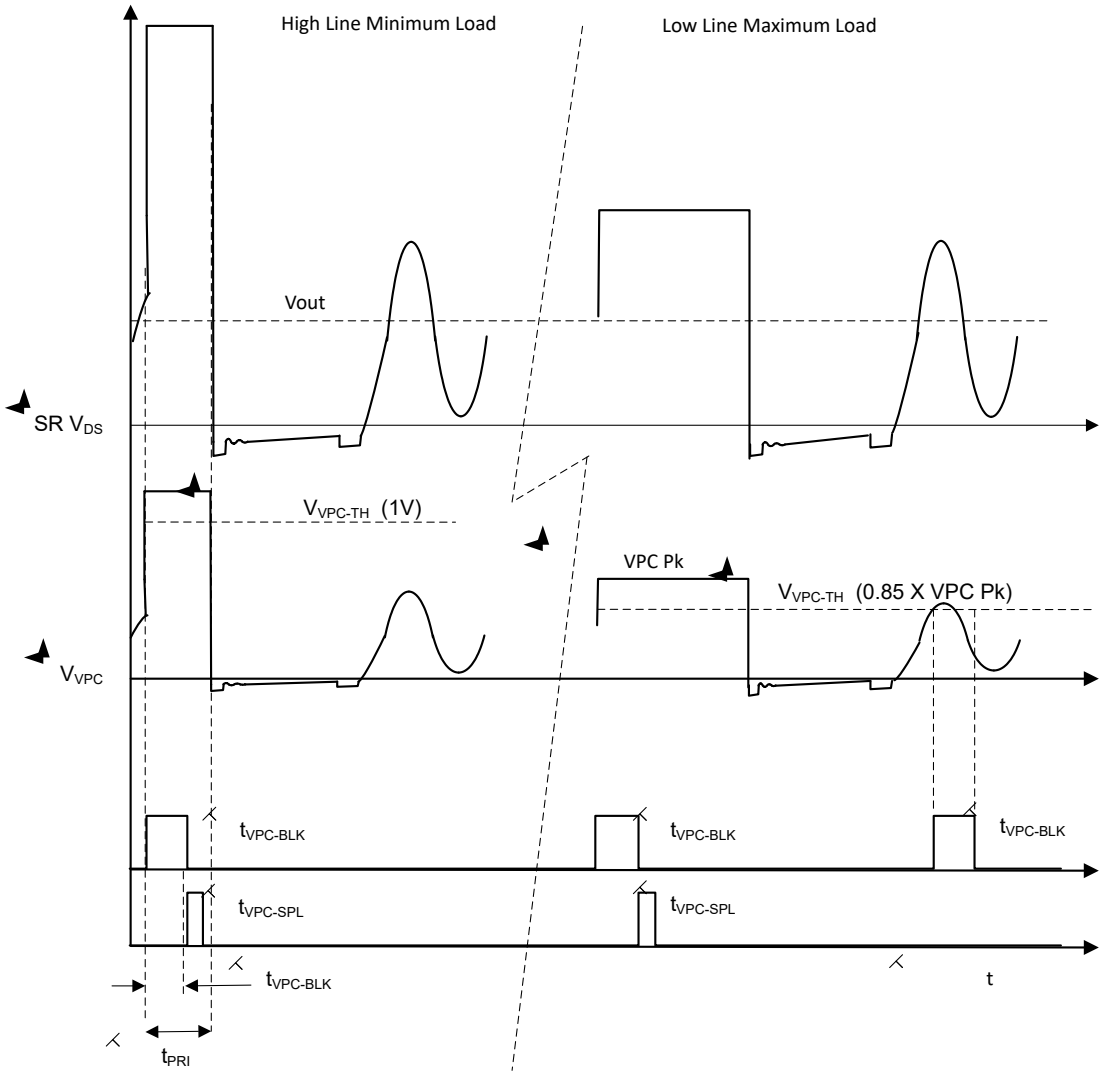


Figure 6-6. VPC Blanking Time Criteria

6.3.3 CCM Dead Time

Operation of CCM converters during transition from DCM to CCM results in several switching cycles where volt-sec balance is not achieved. To accommodate CCM operation the UCC24630 SR controller incorporates CCM dead-time protection to verify turn off of the SR MOSFET before the next primary MOSFET turn-on. The function provides a limit of the total period of the primary on time plus SR on time to the previous cycle minus the dead time, 600ns typical. This is accomplished by limiting the SR on time of the active cycle, t (N+1), to the previous recorded cycle, t (N), minus t_{CCMDT}. As can be seen in Figure 6-7, the CCM dead time limits the DRV on time even though the VSC volt-sec ramp threshold is not satisfied.

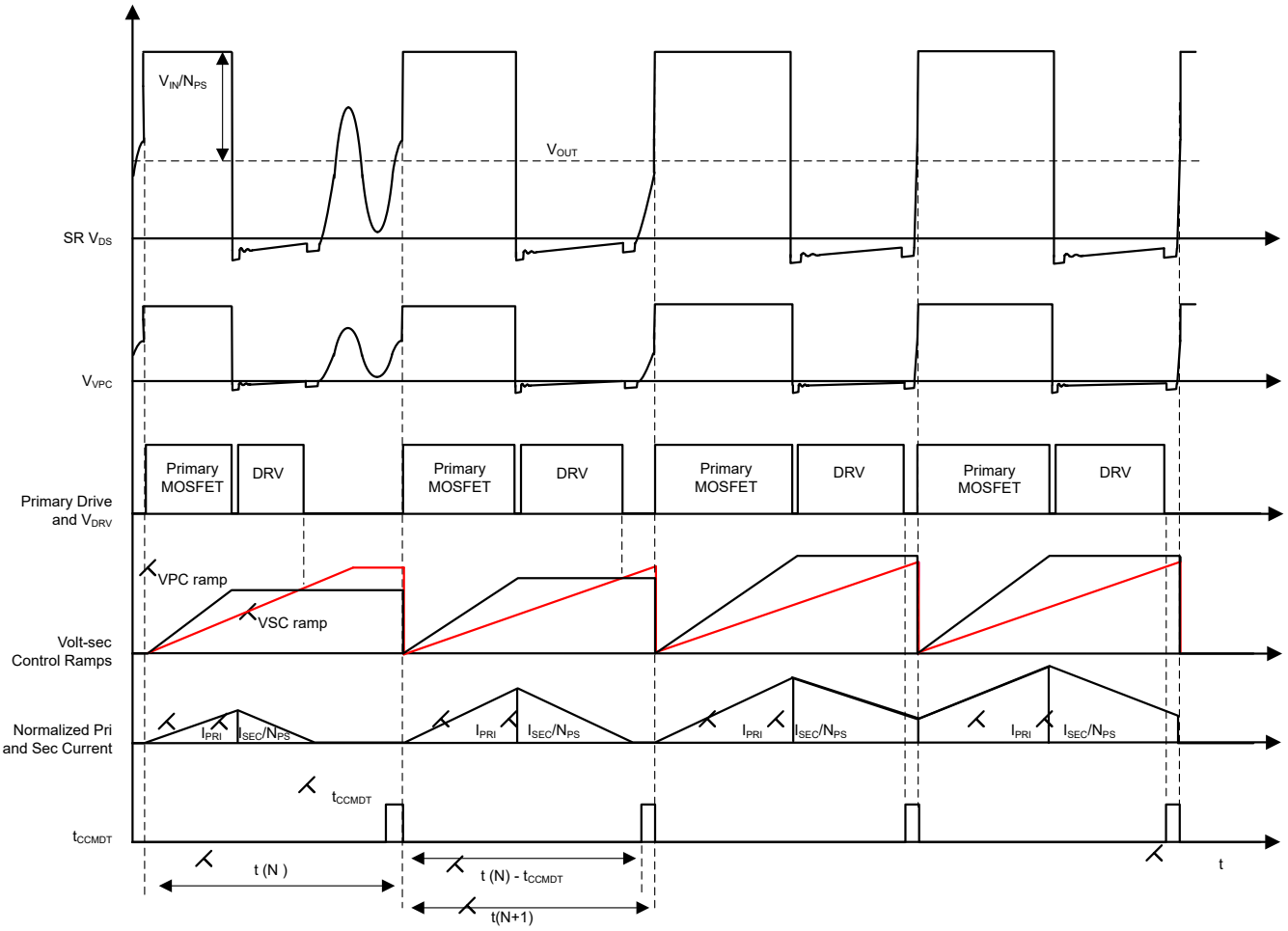


Figure 6-7. CCM Dead-Time Function

CCM cycle fault provides protection if the switching frequency is unstable during abnormal conditions. The CCM cycle fault triggers if the switching period exceeds the previous switching period by KCCM-FAULT, 150% typical. The CCM cycle fault disables the DRV output for four consecutive cycles. During the four-cycle disable interval if another CCM cycle fault occurs the fault is retriggered for another four cycles, DRV is not enabled until four consecutive cycles occur that do not generate a CCM cycle fault. Refer to Figure 6-8 and Figure 6-9 for CCM cycle fault behavior.

The N+1 cycle with the longer period sets up the next following cycle to have a longer allowable maximum SR on time based on t(N) – tCCMDT; if CCM operation occurs in this case the maximum allowable SR on time can conflict with the primary turn-on if the converter switching period returns to the previous time. The DRV output is disabled to prevent this potential timing conflict with the primary switch.

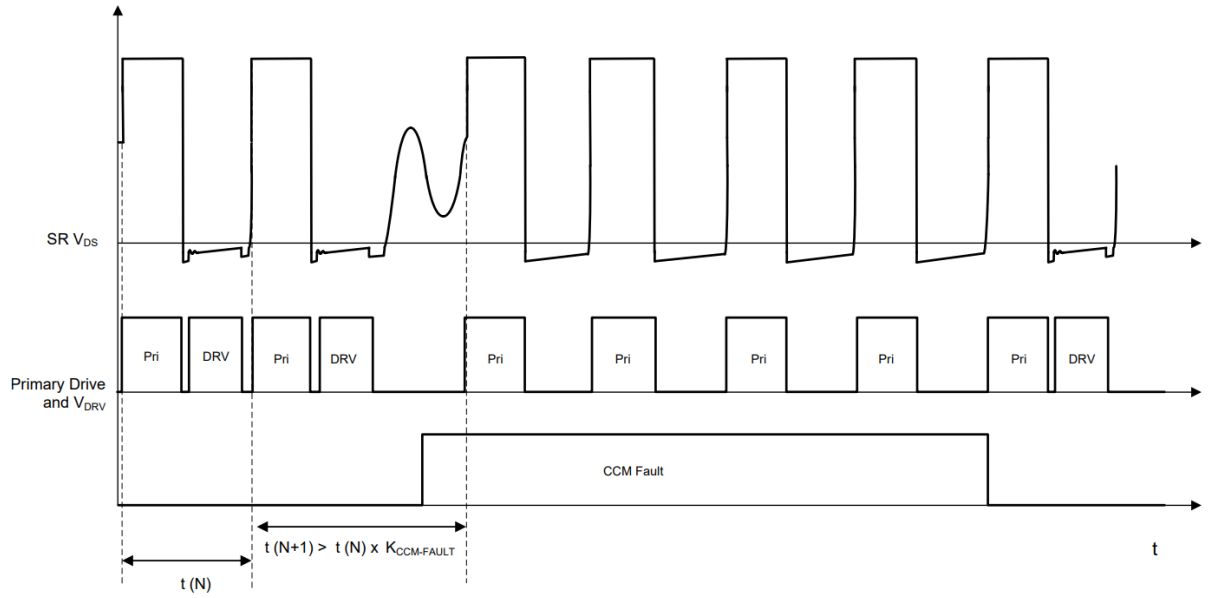


Figure 6-8. CCM Cycle-Fault Behavior, CCM Operation

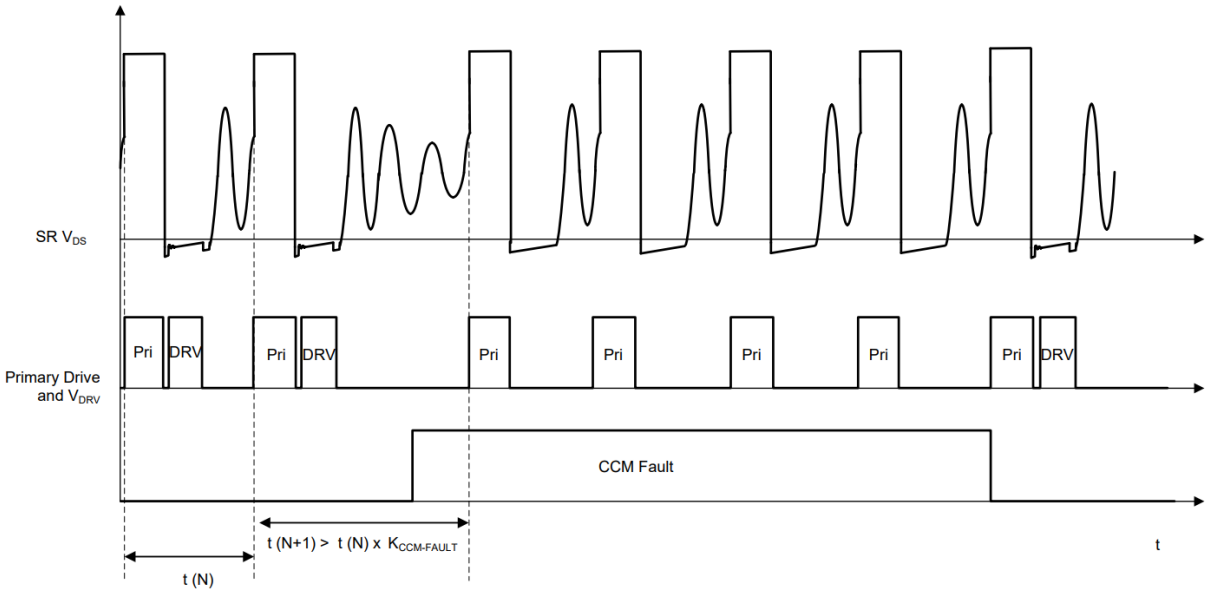


Figure 6-9. CCM Cycle-Fault Behavior, DCM Operation

6.3.4 Standby Operation

To minimize power consumption at very light load and standby conditions, the UCC24630 disables the SR DRV output and enters a low current operating state. The criteria for operating in standby mode or normal operation are determined by the average frequency detected on the VPC pin. The frequency detection is compatible with burst mode operation or continuous low frequency FM operation. At start-up, the device is in normal operation to enable DRV to the SR MOSFET. If < 64 cycles occur in tENTO, 12.8ms typical, the device disables the DRV output and enters low-current operating mode with bias current of ISTBY. In standby mode the criteria to enter normal operating mode is when > 32 cycles occur within tEN, 2.56ms typical. The device enters normal operation as soon as the 32 cycles occur to reduce the response time exiting standby operation. The average frequency of entering standby mode is 5kHz typical, and the average frequency of exiting standby mode is 12.5kHz typical. Refer to Figure 6-10 for an illustration of standby mode timing.

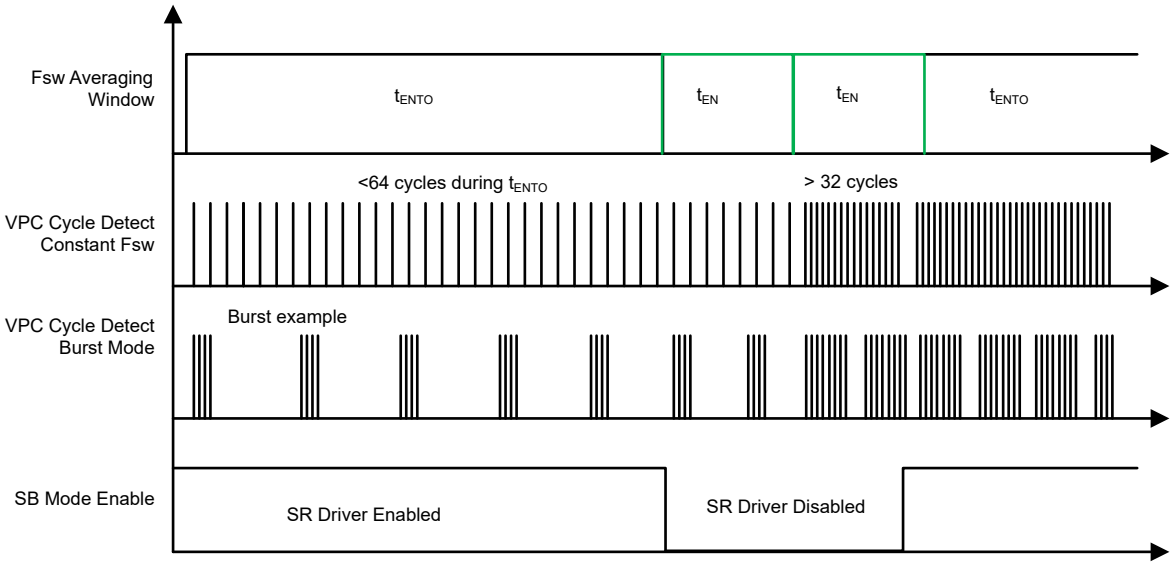


Figure 6-10. Standby Mode Operation

6.3.5 Pin Fault Protection

The UCC24630 controller includes fault protection in the event of open pin, shorted pin to ground and abnormal out of range operation.

6.3.5.1 VPC Pin Overvoltage

In the event that there is an abnormal high level on the VPC pin for a period beyond expected transformer leakage spike duration, the DRV output is disabled on a cycle-to-cycle basis. If the voltage on the VPC pin exceeds V_{VPCDIS}, 2.6V minimum, for 500ns the SR is not enabled until the next valid cycle.

6.3.5.2 VPC Pin Open

In the event of an open-circuit VPC pin, the device defaults to a no VPC input signal condition which results in disabling DRV operation.

6.3.5.3 VSC Pin Open

In the event of an open-circuit VSC pin, the device defaults to a zero VSC input signal condition which results in disabling DRV operation.

6.3.5.4 TBLK Pin Open

In the event of an open circuit TBLK pin, the device disables DRV operation.

6.3.5.5 VPC and VSC Short to Ground

Since the VPC and VSC enable thresholds must be satisfied for DRV operation, DRV is inherently disabled.

6.3.5.6 TBLK Pin Short to Ground

A shorted TBLK pin results in a minimum setting for $t_{VPC-BLK}$ blanking time.

6.4 Device Functional Modes

According to VDD voltage, VSC voltage, and VPC voltage and frequency the device can operate in different modes.

6.4.1 Start-Up

During start-up when VDD is less than $V_{VDD(on)}$ the device is disabled. When VDD exceeds the $V_{VDD(on)}$ UVLO threshold the I_{DD} goes to I_{RUN} and the device begins the start sequence detailed in Start Up and UVLO.

6.4.2 Normal Operation

When VDD exceeds $V_{VDD(on)}$, the VPC voltage exceeds V_{VPCEN} and V_{VPC-TH}, and the VSC voltage exceeds V_{VSCEN} the DRV output is active. If the switching frequency is above the standby criteria of > 5kHz the device is in normal operation determining the DRV time based on volt-sec control, or CCM dead time control. I_{DD} will be I_{RUN}.

1. The device operates in volt-sec control when the primary on-time plus the DRV on-time is less than the previous cycle minus t_{CCMDT}. This is the mode of operation most the time.
2. The device operates in CCM dead-time control when the primary on-time plus DRV on time would be greater, as determine by the volt-sec control ramps, than the previous cycle minus t_{CCMDT}. This occurs only in CCM converters, during the transition of DCM into CCM operation

6.4.3 Standby Operation

If the number of VPC pulses is less than n_{ENTO}, 64, during t_{ENTO} the device enters standby mode. DRV operation stops and most device functions are shut down. I_{DD} is I_{STBY} during standby operation. To exit standby mode the number of VPC pulses must exceed n_{EN}, 32, during t_{EN}. I_{DD} returns to I_{RUN} and the DRV output starts after 4 VPC cycles.

6.4.4 Conditions to Stop Operation

The following conditions can disable DRV operation, I_{DD} is I_{RUN} during these conditions.

1. VPC overvoltage: When V_{VPC} > V_{VPCDIS} for >500ns the DRV output is disabled for the cycle.
2. CCM Fault: If the current cycle period is greater than the previous cycle times K_{CCM_FAULT}, the DRV output is disabled for 4 cycles. The 4-cycle count can be reset, and extended if another CCM fault occurs during the 4-cycle DRV disable counter.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

7.1 Application Information

The UCC24630 is a high performance controller driver for N-channel MOSFET power devices used for secondary-side synchronous rectification. The UCC24630 is designed to operate as a companion device to a primary-side controller to help achieve efficient synchronous rectification in switching power supplies. The controller features a high-speed driver and provides appropriately timed logic circuitry that seamlessly generates an efficient synchronous rectification system. With its current emulator architecture, the UCC24630 has enough versatility for application in DCM, TM, and CCM modes. The UCC24630 SR on-time adjustability allows optimizing for PSR and SSR applications. Additional features such as pin fault protection, dynamic VPC threshold sensing, and voltage sense blanking time and make the UCC24630a robust synchronous controller. CCM dead-time protection shuts off the DRV signal in the event of an unstable switching frequency.

7.2 Typical Application

7.2.1 AC-to-DC Adapter, 19.5V, 65W

This design example describes the design of a 65W off-line fly back converter providing 19.5V at 3.33A maximum load and operating from a universal AC input. The design uses the LM5023 AC-to-DC quasi-resonant primary-side controller in a DCM type fly back converter and achieves over 92% full-load efficiency with the use of the secondary side UCC24630 synchronous rectifier controller.

- The design requirements are detailed in Section 7.2.2
- The design procedure for selecting the component circuitry for use with the UCC24630 is detailed in Section 7.2.3.
- Test results shown in Section 7.2.4 highlight the unique advantages of using the UCC24630.

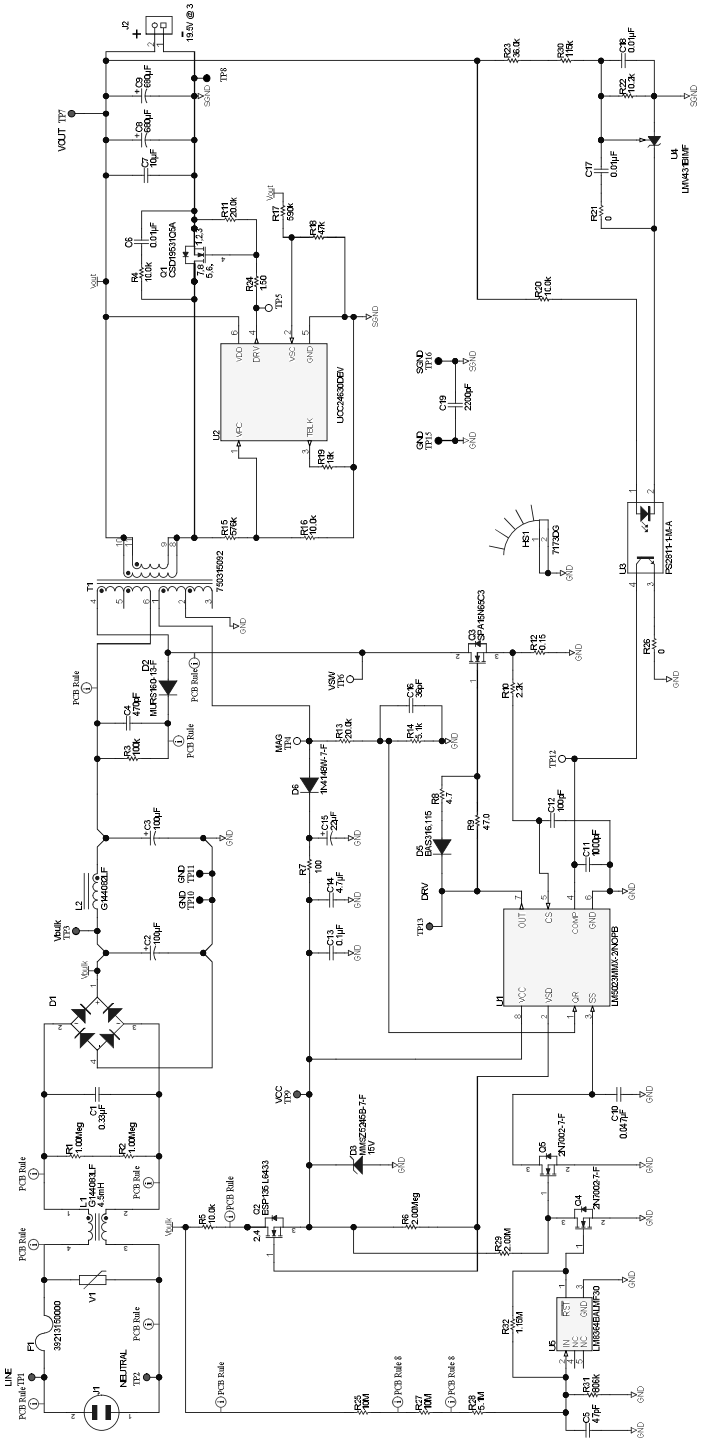


Figure 7-1. AC-to-DC Adapter 19V, 65W

7.2.2 Design Requirements

For this design example, use the parameters listed in Table 7-1.

Table 7-1. Performance Specifications AC-to-DC Adapter 19V, 65W

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
Input Characteristics						
V_{ACIN}	Input voltage		90	115/230	265	V
f_{LINE}	Frequency		47	50/60	64	Hz
$V_{AC(uvlo)}$	Brownout voltage	$I_{OUT} = I_{OUT(nom)}$		80		VRMS
$V_{AC(run)}$	Brownout recovery voltage			90		VRMS
I_{IN}	Input current	$V_{ACIN} = V_{ACIN(min)}$, $I_{OUT} = I_{OUT(nom)}$		1.65		A
Output Characteristics						
V_{OUT}	Output voltage	$V_{ACIN} = V_{ACIN(min)}$ to $V_{ACIN(max)}$, $I_{OUT} = 0$ to $I_{OUT(nom)}$	18.5	19.5	20.5	V
$I_{OUT(nom)}$	Nominal output current	$V_{ACIN} = V_{ACIN(min)}$ to $V_{ACIN(max)}$		3.33		A
$I_{OUT(min)}$	Minimum output current	$V_{ACIN} = V_{ACIN(min)}$ to $V_{ACIN(max)}$		0		A
ΔV_{OUT}	Output voltage ripple	$V_{ACIN} = V_{ACIN(min)}$ to $V_{ACIN(max)}$, $I_{OUT} = 0$ to $I_{OUT(nom)}$		500		mV
P_{OUT}	Output power	$V_{ACIN} = V_{ACIN(min)}$ to $V_{ACIN(max)}$		65		
System Characteristics						
η_{avg}	Average efficiency	$V_{ACIN} = V_{ACIN(nom)}$, I_{OUT} = 25%, 50%, 75%, 100% of $I_{OUT(nom)}$	89%	90%		
$\eta_{10\%}$	10% Load efficiency	$V_{ACIN} = V_{ACIN(nom)}$, I_{OUT} = 10% of $I_{OUT(nom)}$	79%	82%		
P_{NL}	No load power	$V_{ACIN} = V_{ACIN(nom)}$, $I_{OUT} = 0$		60	120	mW

7.2.3 Calculation of Component Values

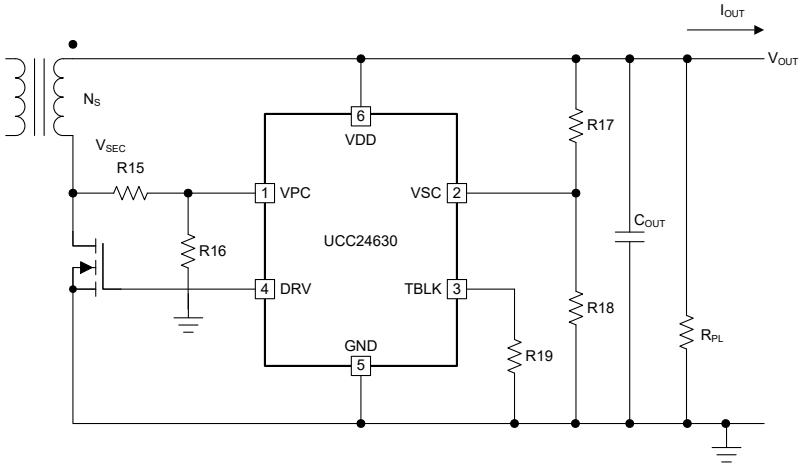


Figure 7-2. UCC24630 Circuit Design

For ease of understanding, Figure 7-2 is a modified version of Figure 6-5 where the component reference designators are the same as the schematic drawing of Figure 7-1.

7.2.3.1 VPC Input

For minimal power dissipation:

- R16 = 10kΩ

- $$R15 = \frac{\left(\left[\frac{V_{IN(min)}}{N_{PS}} + V_{OUT(min)} - V_{VPC\_EN} \times 1.1\right]\right) \times R16}{V_{VPC\_EN}} \quad (8)$$

- $V_{OUT(min)}$ = 18V
- N_{PS} = 5.5
- $V_{IN(min)}$ = 60V
- R15 = 574kΩ

With **R15 = 576kΩ**

- $$V_{VPC(max)} = \frac{\left[\frac{V_{IN(max)}}{N_{PS}} + V_{OUT(max)}\right] \times R16}{R15 + R16} \quad (9)$$

- $V_{PC(max)}$ = 1.50V

- $$V_{VPC(min)} = \frac{\left[\frac{V_{IN(min)}}{N_{PS}} + V_{OUT(min)}\right] \times R16}{R15 + R16} \quad (10)$$

- $V_{PC(min)}$ = 0.49V

Therefore, V_{VPC} is within the recommended range from 0.45V to 2V.

7.2.3.2 VSC Input

The value of R18 is recommended to be with the range from 25kΩ to 50kΩ.

- R18 = 47kΩ

- $$R17 = \left[\left(\frac{\frac{R15 + R16}{R16}}{Ratio_{VPC\_VSC} \times 1.1}\right) - 1\right] \times R18 \quad (11)$$

- R17 = 554kΩ

With R17 = 590kΩ the operating range of the VSC pin is:

- $$V_{VSC(min)} = \left(\frac{R18}{R17 + R18}\right) \times V_{OUT(min)} \quad (12)$$

- $V_{SC(min)}$ = 1.32V

- $$V_{VSC(max)} = \left(\frac{R18}{R17 + R18}\right) \times V_{OUT(max)} \quad (13)$$

- $V_{SC(max)}$ = 1.55V

Therefore, V_{VSC} is within the recommended range from 0.3V to 2V.

7.2.3.3 TBLK Input

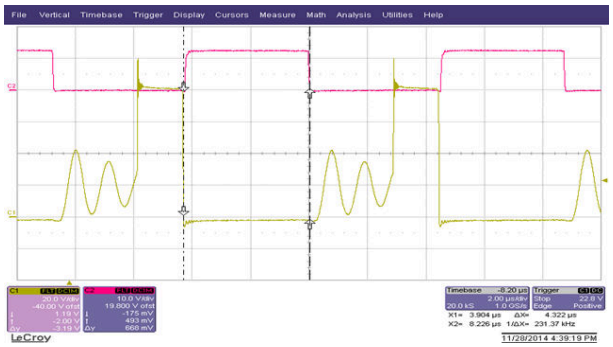
The blanking time is set with resistor R19.

Select the blanking time to meet the following criteria based on minimum primary on-time at high line, Equation 6.

$$R19 = \frac{t_{VPC-BLK} - 100ns}{18pF} \quad (14)$$

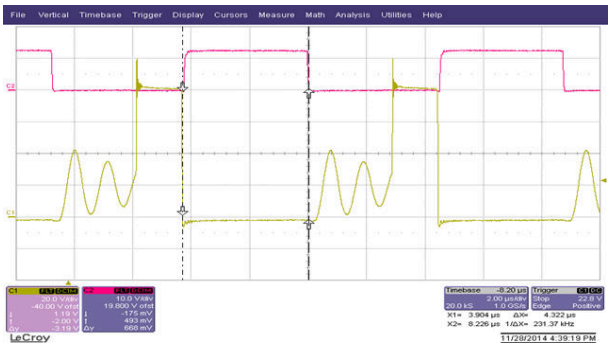
A value of **R19 = 18kΩ** results in a blanking time of approximately 420ns.

7.2.4 Application Curves



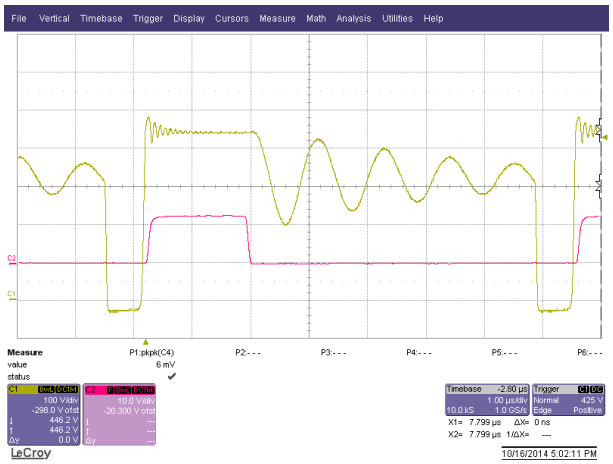
C2(RED): DRV signal to synchronous rectifier Q1
C1(YELLOW): Drain of synchronous rectifier Q1

Figure 7-3. DRV Timing at 230V_{AC}, 65W



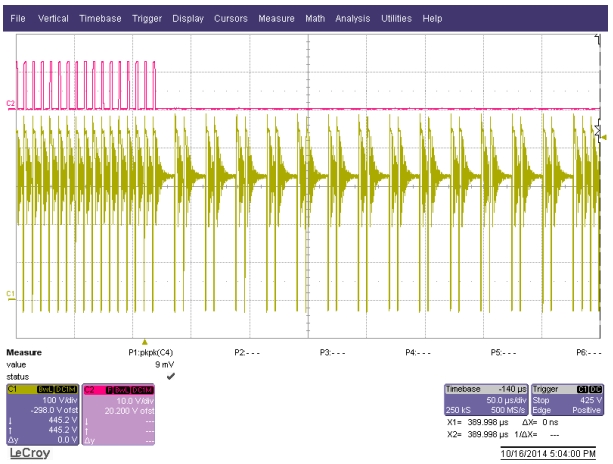
C2(RED): DRV signal to synchronous rectifier Q1
C1(YELLOW): Drain of synchronous rectifier Q1

Figure 7-4. DRV Timing at 115V_{AC}, 65W



C2(RED): DRV signal to synchronous rectifier Q1
C1(YELLOW): Drain of primary-side MOSFET Q3

Figure 7-5. DRV Timing at 230V_{AC}, 12W



C2(RED): DRV signal to synchronous rectifier Q1
C1(YELLOW): Drain of primary-side MOSFET Q3

Figure 7-6. Light-Load Behavior (230V_{AC}, 8W)

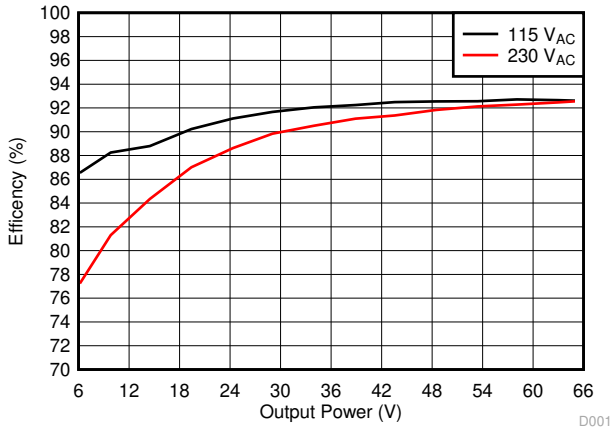


Figure 7-7. Efficiency vs Output Power

7.3 Best Design Practices

- Do operate the device within the recommended operating maximum parameters. Consider output overvoltage conditions when determining stress.
- Do consider the guideline for setting the blanking time resistor value illustrated in Figure 6-6.
- Do not use the UCC24630 with converters that operate in constant skip cycle mode at high-power levels. The skip cycle behavior results in numerous CCM faults and missing DRV pulses.
- Do not use the UCC24630 in CCM designs that are operating in CCM while the fly-back controller is operating in variable frequency, FM, modulation. The CCM dead-time function is compatible with CCM operation during fixed-frequency, PWM operation.
- Do not use the UCC24630 in hysteretic control CCM flyback converters. Constant skip-cycle operation at high-power levels results in numerous CCM cycle faults resulting in efficiency loss.
- Do not use the UCC24630 in LLC converters.

7.4 Power Supply Recommendations

The UCC24630 is recommended as a synchronous rectifier controller in a wide variety of flyback power supplies. It is compatible with Discontinuous Conduction Mode (DCM) and Transition Mode (TM) controllers in fixed frequency or variable frequency applications. It is compatible with Continuous Conduction Mode (CCM) controllers in fixed frequency applications.

It is an excellent choice as a synchronous rectifier for flyback power supplies with an input from $85V_{AC}$ to $265V_{AC}$ and an output from 5V to 24V. It can also be used in other flyback applications with different input and/or output voltages. But be sure all voltages and currents are within the recommended operating conditions and absolute ratings of the device.

It is compatible with flyback converters operating at the transition mode limit, at low line, with switching frequencies as low as 40kHz. It can also be used in switching speeds up to 200kHz.

The VDD operating range allows direct connection to converter outputs from 5V to 24V. Since the driver and control share the same VDD and ground, place a good quality ceramic capacitor as close as possible to VDD and GND pins. To reduce VDD noise and eliminate high-frequency ripple current injected from the converter output, it is recommended to place a small resistance from 2.2Ω to 10Ω between the converter output and VDD. The device can tolerate VDD rise times from 100µs to very long rise times typical of constant current chargers. The start-up sequence always is as shown in Figure 6-1. VDD can connect to an external bias to extend the device's operating range below 3.5V or above 24V converter outputs.

7.5 Layout

7.5.1 Layout Guidelines

In general, try to keep all high current loops as short as possible. Keep all high-current/high-frequency traces away from other traces in the design. If necessary, high-frequency/high-current traces must be perpendicular to signal traces, not parallel to them. Shielding signal traces with ground traces can help reduce noise pick up. Always consider appropriate clearances between the high-voltage connections and any low-voltage nets.

7.5.1.1 VDD Pin

The VDD pin must decouple to GND with good quality, low ESR, low ESL ceramic bypass capacitors with short traces to the VDD and GND pins. The value of the required capacitance on VDD is determined as shown in Recommended Operating Conditions. To eliminate high-frequency ripple current in the SR control circuit, it is recommended to place a small value resistance from 2.2Ω to 10Ω between VDD and the converter output voltage.

7.5.1.2 VPC Pin

The trace between the resistor divider and the VPC pin must be as short as possible to reduce/eliminate possible noise coupling. The lower resistor of the resistor divider network connected to the VPC pin must return to GND with short traces. Avoid adding any significant external capacitance to the VPC pin so that there is no delay of signal. If filtering is necessary a recommended maximum capacitance is 10pF with a lower resistor

divider network value of 10kΩ. Avoid high dV/dt traces close to the VPC pin and connection trace such as the SR MOSFET drain and DRV output.

7.5.1.3 VSC Pin

The trace between the resistor divider and the VSC pin must be as short as possible to reduce/eliminate possible noise coupling. The lower resistor of the resistor divider network connected to the VSC pin must return to GND with short traces. Avoid adding any external capacitance to the VPC pin so that there is no delay of signal. If filtering is necessary a recommended maximum capacitance is 47pF with a lower resistor divider network value of 50kΩ. Avoid high dV/dt traces close to the VSC pin and connection trace such as the SR MOSFET drain and DRV output.

7.5.1.4 GND Pin

The GND pin is the power and signal ground connection for the controller. The effectiveness of the filter capacitors on the signal pins depends upon the integrity of the ground return. Place all decoupling capacitors as close as possible to the device pins with short traces. The device ground and power ground should meet at the output bulk capacitor's return. Try to verify that high frequency/high current from the power stage does not go through the signal ground.

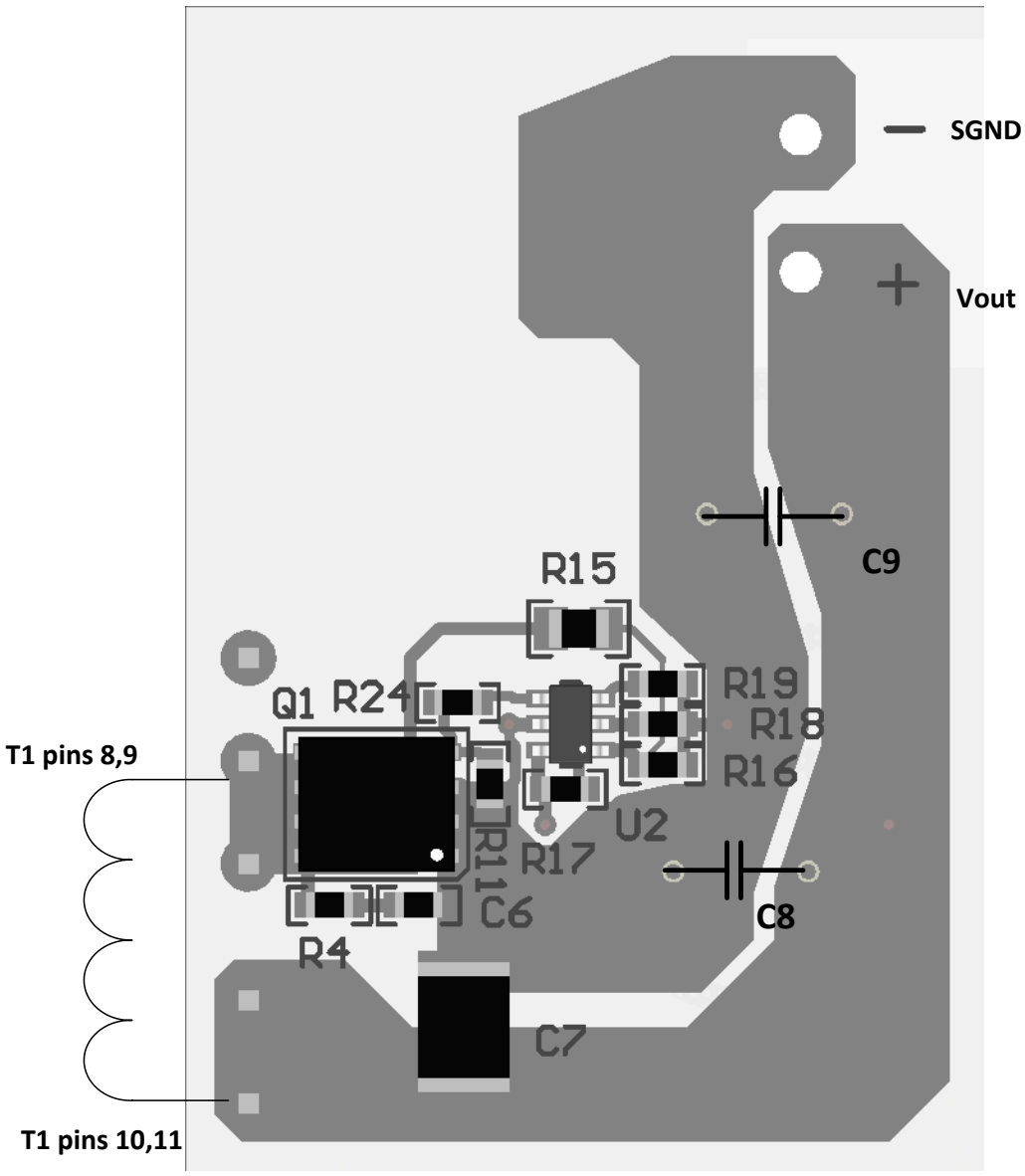
7.5.1.5 TBLK Pin

The programming resistor is placed on TBLK to GND, with short traces. Adjust the value based on the time delay required. Avoid high dV/dt traces close to the TBLK pin and connection trace such as the SR MOSFET drain and DRV output.

7.5.1.6 DRV Pin

The track connected to DRV carries high dv/dt signals. Minimize noise pickup by routing the trace to this pin as far away as possible from tracks connected to the device signal inputs, VPC, VSC, and TBLK.

7.5.2 Layout Example



8 Device and Documentation Support

8.1 Device Support

8.1.1 Device Nomenclature

8.1.1.1 Definition of Terms

- $V_{IN(min)}$ = 60V: converter minimum primary bulk capacitor voltage
- $V_{IN(max)}$ = 370V: converter maximum primary bulk capacitor voltage
- $V_{OUT(min)}$ = 18V: minimum converter output operating voltage of the UCC24630
- $V_{OUT(max)}$ = 21V: maximum converter output operating voltage of the UCC24630
- V_{VPC_EN} = 0.45V: synchronous rectifier enable voltage
- $V_{VPC(max)}$ = 2.0V: maximum operating level of VPC
- N_{PS} = 5.5: transformer primary to secondary turns ratio
- $Ratio_{VPC\_VSC}$ = 4.15: current emulator gain K_{VPC}/K_{VSC}
- t_{VPC_BLK}: minimum VPC pulse for synchronous rectifier operation

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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8.4 Trademarks

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8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (March 2015) to Revision B (July 2026)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Changed minimum secondary current conduction time for the minimum SR on time ($t_{SR(min)}$) of 350ns from larger to less than	10

Changes from Revision * (March 2015) to Revision A (March 2015)	Page
• Changed Applications section typo.	1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UCC24630DBVR	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	U630
UCC24630DBVR.B	Active	Production	null (null) |	3000 | LARGE T&R	-	NIPDAU	Level-1-260C-UNLIM	See UCC24630DBVR	U630
UCC24630DBVT	Active	Production	SOT-23 (DBV) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	U630
UCC24630DBVT.B	Active	Production	null (null) |	250 | SMALL T&R	-	NIPDAU	Level-1-260C-UNLIM	See UCC24630DBVT	U630

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

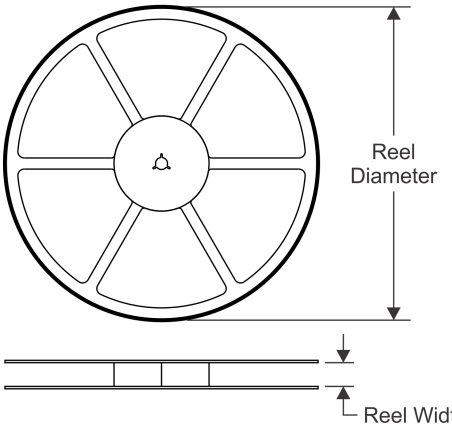
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

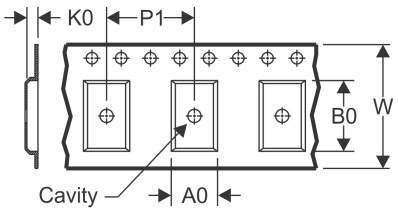
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

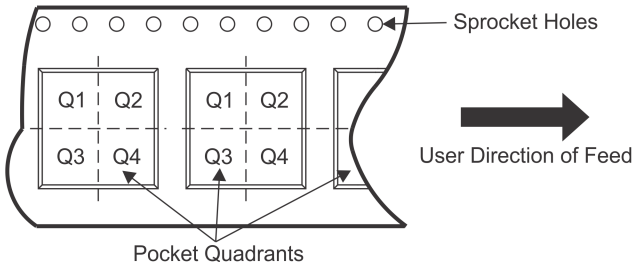


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

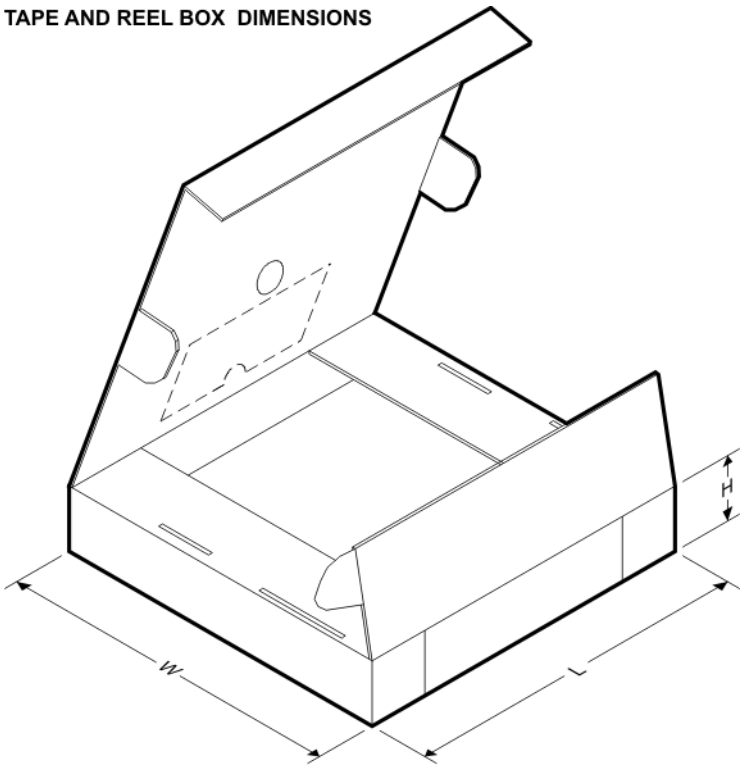
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC24630DBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
UCC24630DBVT	SOT-23	DBV	6	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

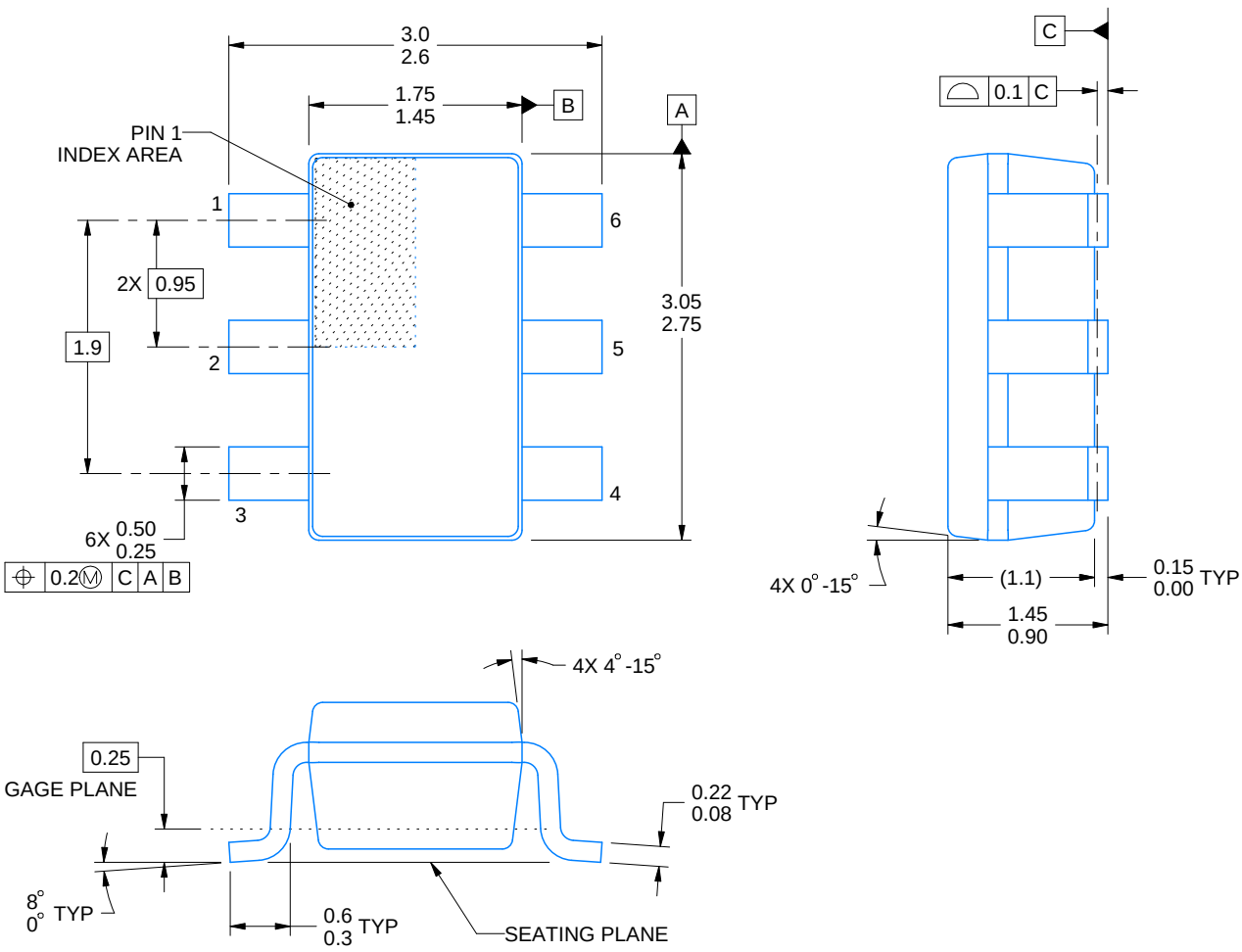
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC24630DBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
UCC24630DBVT	SOT-23	DBV	6	250	180.0	180.0	18.0

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



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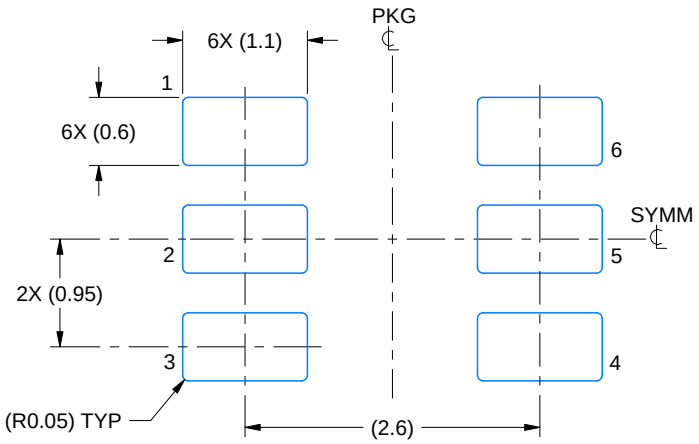
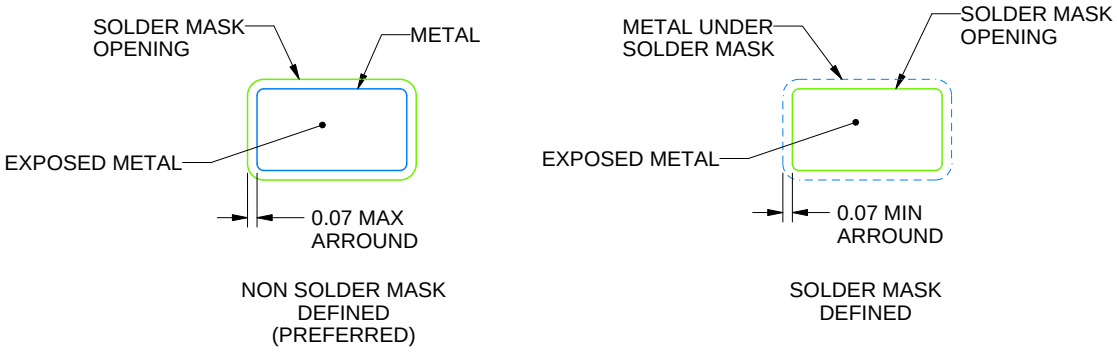
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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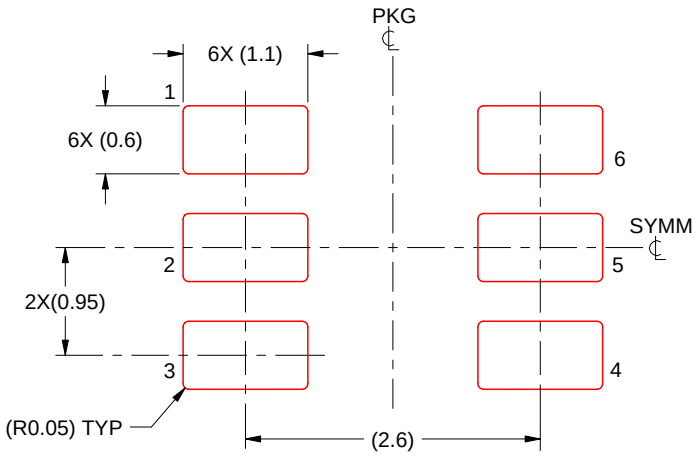
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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