

UCC25640x LLC Resonant Controller with Ultra-Low Audible Noise and Standby Power

1 Features

- Optimized low-power mode and burst mode algorithm
 - Burst mode with Soft-ON and Soft-OFF periods
 - Minimized audible noise at no load and standby
 - User option to disable burst mode
 - Opto-coupler low-power operation
 - Efficiency performance exceeds DoE Level VI and EU CoC Tier-2 External Power Supply Standards
- Hybrid hysteretic control (HHC)
 - Best-in-class transient response
 - Fast exit from burst mode
- Robust adaptive dead-time control
- Integrated high-voltage gate driver with 0.6A source and 1.2A sink capability
- Robust capacitive region (ZCS) avoidance scheme
- Over temperature, output over voltage, input undervoltage protection, three levels of overcurrent protection
- Integrated high voltage startup function
- Active X-capacitor discharge function

2 Applications

- SMPS power supply for TV
- Lighting
- AC-DC adapter
- Power tools
- Medical power supply
- Multi-functional printer
- Enterprise and cinema projector
- PC power supply
- Gaming console power supply

3 Description

The UCC25640x is a fully featured LLC controller with integrated high-voltage gate driver. UCC25640x is designed to pair with a PFC controller to provide a complete power system using a minimum of external components. The resulting power system is designed to meet the most stringent requirements for standby power without the need for a separate standby power converter.

UCC25640x provides a highly efficient burst mode with soft-on and soft-off periods to minimize audible noise at standby operation. The burst power level and hysteresis are programmable, simplifying the optimization of efficiency and burst mode operation. Disable burst mode through the pin configuration. UCC25640x uses hybrid hysteretic control to provide best in class line and load transient response.

UCC25640x includes a range of features designed to make LLC converter operation well controlled and protected. Use UCC25640x with UCC28056 or UCC28064A PFC controllers, along with a UCC24624 synchronous rectifier controller to offer a complete power supply option.

Package Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾
UCC256402	SOIC	9.9mm × 3.9mm
UCC256403		
UCC256404		

(1) For all available packages, see the orderable addendum at the end of the datasheet.

(2) The package size (length × width) is a nominal value and includes pins, where applicable.





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4 Device Comparison Table

Device	Integrated High Voltage Startup	Integrated X-Capacitor Discharge	Requires External Bias Supply	Burst Soft On and Soft Off	BLK OVP	BW OVP Mode
UCC256402	Yes	No	No	No	No	Restart
UCC256402A	Yes	No	No	No	Yes	Restart
UCC256403	No	No	Yes	Yes	No	Restart
UCC256403A	No	No	Yes	No	No	Latch
UCC256404	Yes	Yes	No	Yes	No	Restart
UCC256404A	Yes	Yes	No	No	No	Latch
UCC256404B ⁽¹⁾	Yes	Yes	No	Yes	No	Restart

- (1) The X capacitor discharge feature of this device is not tested by a certification agency and is qualified by similarity under the existing UCC25640x certification

5 Pin Configuration and Functions

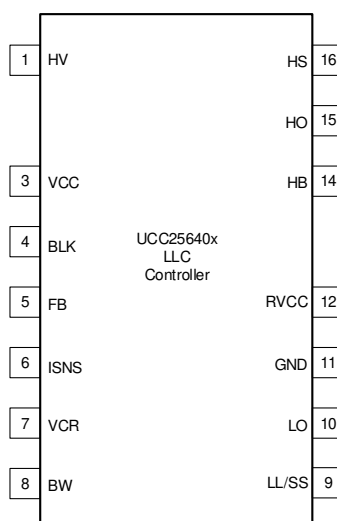


Figure 5-1. DDB Package 16-Pin SOIC (Pins 2, 13 removed) Top View

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
BLK	4	I	This pin is used to sense the LLC stage input voltage level. A resistor divider should be used to attenuate the signal before it is applied to this pin. The voltage level on this pin will determine when the LLC converter starts/stops switching.
BW	8	I	This pin is used to sense the output voltage through the bias winding. The sensed voltage is used for output over voltage protection. During startup, the pin is also used to program the ratio between the two burst mode thresholds (BMT_L and BMT_H).
FB	5	I	LLC stage control feedback input. The amount of current sourced from this pin will determine the LLC input power level.
GND	11	G	Ground reference for all signals.
HB	14	I	High-side gate-drive floating supply voltage. The bootstrap capacitor is connected between this pin and HS pin. A high voltage, high speed diode should be connected from RVCC to this pin to supply power to the high-side gate-driver during the period when the low-side MOSFET is conducting.
HO	15	O	High-side floating gate-drive output.
HS	16	I	High-side gate-drive floating ground. Current return for the high-side gate-drive current.
HV	1	I	Connects to internal HV startup JFET. For UCC256402 and UCC256404, this pin provides start up power for both PFC and LLC stage. This pin also monitors the AC line voltage for x-capacitor discharge function. For UCC256403, this pin needs to be connected to ground.
ISNS	6	I	Resonant current sense. The resonant capacitor voltage is differentiated with a first order filter to measure the resonant current.
LL/SS	9	I	The capacitance value connected from this pin to ground will impact the duration of the soft-start period. The resistor divider connected to the pin will define the initial voltage applied on the pin for startup. After system startup, this pin is used to program the burst mode threshold.
LO	10	O	Low-side gate-drive output.
Removed	2	N/A	Functional creepage and clearance
Removed	13	N/A	Functional creepage and clearance
RVCC	12	P	Regulated 13V supply. This pin is used to supply the gate driver and PFC controller.
VCC	3	P	Supply input.
VCR	7	I	Resonant capacitor voltage sense.

(1) I = input, O = output, P = power, G = ground

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted), all voltages are with respect to GND, currents are positive into and negative out of the specified terminal.⁽¹⁾

		MIN	MAX	UNIT
Input voltage	HV, HB	-0.3	700	V
	BLK, LL/SS	-0.55	7.2	V
	VCR	-0.8 Internally Clamped		V
	VCC	-0.55	30	V
	BW, ISNS	-5	7.2	V
	HB - HS (For UCC256402, UCC256402A, UCC256403, UCC256403A, UCC256404, UCC256404A)	-0.3	17	V
	HB - HS (For UCC256404B)	-0.3	25	V
RVCC output voltage	DC	-0.3	17	V
HO output voltage	DC	HS – 0.3	HB + 0.3	V
	Transient, less than 100ns	HS – 2	HB + 0.3	
LO output voltage	DC	-0.3	RVCC + 0.3	V
	Transient, less than 100ns	-2	RVCC + 0.3	
Floating ground slew rate	dV _{HS} /dt	-50	50	V/ns
HO, LO pulsed current	I _{OUT_PULSED}	-0.6	1.2	A
Junction temperature range	T _J	-40	150	°C
Storage temperature range, T _{stg}	T _{stg}	-65	150	
Lead temperature	Soldering, 10 second		300	
	Reflow		260	

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, HV, HO, HS, HB pins ⁽¹⁾	±1000	V
		Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all other pins ⁽¹⁾	±2000	
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	±500	

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

All voltages are with respect to GND, $-40^{\circ}\text{C} < T_J = T_A < 125^{\circ}\text{C}$, currents are positive into and negative out of the specified terminal, unless otherwise noted.

		MIN	NOM	MAX	UNIT
HV, HS	Input voltage			600	V
V _{CC}	Supply voltage	13	15	26	V
HB - HS	Driver bootstrap voltage	10	12	16	V
C _B	Ceramic bypass capacitor from HB to HS	0.1		5	μF
C _{SS}	Soft start pin capacitor	4.7		470	nF
C _{RVCC}	RVCC pin decoupling capacitor	4.7			μF
I _{RVCCMAX}	Maximum output current of RVCC ⁽¹⁾			100	mA
T _A	Operating ambient temperature	-40		125	°C

(1) Not tested in production. Established by characterization

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		UCC25640x	UNIT
		D (SOIC)	
		14 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	74.7	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	30.7	°C/W
R _{θJB}	Junction-to-board thermal resistance	31.8	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	4.4	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	31.4	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics application note](#).

6.5 Electrical Characteristics

All voltages are with respect to GND, $-40^{\circ}\text{C} < T_J = T_A < 125^{\circ}\text{C}$, V_{CC} = 15V, currents are positive into and negative out of the specified terminal, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE						
V _{CCShort}	Below this threshold, use reduced start up current	For UCC256402, UCC256402A, UCC256404, UCC256404A, UCC256404B	0.3	0.5	0.8	V
V _{CCReStartJfet}	Below this threshold, re-enable JFET.	For UCC256402, UCC256402A, UCC256404, UCC256404A, UCC256404B	9.35	9.65	9.95	V
V _{CCStartSelf}	Startup when VCC is above this level	For UCC256402, UCC256402A, UCC256404, UCC256404A, UCC256404B	25	26	28	V
V _{CCStartSwitching}	Startup when VCC is above this level	For UCC256403, UCC256403A		10.9		V
V _{CCUVLOrising}	VCC under voltage lockout voltage (rising)		7.85	8.25	8.70	V
V _{CCUVLOHYS}	VCC under voltage lockout voltage hysteresis		0.15	0.25	0.35	V
SUPPLY CURRENT						
I _{CCSleep}	Current drawn from VCC rail during burst off period		650	780	950	μA

6.5 Electrical Characteristics (continued)

All voltages are with respect to GND, $-40^{\circ}\text{C} < T_J = T_A < 125^{\circ}\text{C}$, $V_{CC} = 15\text{V}$, currents are positive into and negative out of the specified terminal, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{CCR_{\text{Run}}}$	Current drawn from VCC Pin while gate is switching. Excluding Gate Current	Dead time = 1 μs maximum dead time	1.8	2.2	2.7	mA
REGULATED SUPPLY						
V_{RVCC}	Regulated supply voltage	$V_{CC} = 15\text{V}$, no load	12.7	13	13.45	V
	Regulated supply voltage	$V_{CC} = 15\text{V}$, 100mA load	12.4	13	13.45	V
	Regulated supply voltage	$V_{CC} = 13\text{V}$, no load	12.7	12.98		V
	Regulated supply voltage	$V_{CC} = 13\text{V}$, 30mA load	12.4	12.6		V
$V_{RVCCUVLO}$	RVCC under voltage lock out voltage		6.5	7	7.5	V
HIGH VOLTAGE STARTUP						
$I_{HVL_{\text{Low}}}$	Reduced startup pin current	$V_{HV} = 20\text{V}$, $V_{CC} = 0\text{V}$	0.3	0.5	0.65	mA
$I_{HV_{\text{High}}}$	Full startup pin current	$V_{HV} = 20\text{V}$, $V_{CC} = 4\text{V}$	7.6	10.20	13.5	mA
$I_{HV_{\text{Leak}}}$	HV current source leakage current	$V_{HV} = 600\text{V}$		1	4	μA
I_{HVZCD}	Highest AC zero crossing detection test current	For UCC256404B	1.0	1.3	1.6	mA
		For UCC256404, UCC256404A	1.4	1.7	2.1	mA
$I_{HVZCD_{\text{Step}}}$	AC zero crossing detection test current steps			0.38		mA
$I_{XCAPD_{\text{Discharge}}}$	X-cap discharge current		8.9	11.5	13.5	mA
$V_{\text{zero-crossing}}$	HV pin voltage threshold that zero-crossing is detected		8	9	11	V
$t_{XCAPZCD}$	AC zero crossing detection window length for first three test current stage (1)		10	12	14	ms
$t_{XCAPZCD_{\text{Last}}}$	AC zero crossing detection window length for final test current stage (1)		43	46	52	ms
$t_{XCAP_{\text{Idle}}}$	AC zero crossing detection idle period length (1)		635	700	772	ms
$t_{XCAPD_{\text{Discharge}}}$	Time for X-cap discharge current active (1)		327	360	390	ms
$t_{XCAP_{\text{JFETON}}}$	Time of first X-cap detection after JFETON (1)			12		ms
BULK VOLTAGE SENSE						
$V_{BLK_{\text{Start}}}$	BLK voltage that allows LLC to start switching	For UCC256402, UCC256402A, UCC256403, UCC256403A	2.94	3	3.06	V
		For UCC256404, UCC256404A, UCC256404B	0.98	1	1.02	V
$V_{BLK_{\text{Stop}}}$	BLK voltage that forces LLC operation to stop	For UCC256402, UCC256402A, UCC256403, UCC256403A	2.15	2.2	2.25	V
		For UCC256404, UCC256404A, UCC256404B	0.88	0.9	0.925	V
$V_{BLKOVPR_{\text{Rise}}}$	BLK over voltage protection rising threshold	For UCC256402A	3.92	4.0	4.08	V
$V_{BLKOVPF_{\text{Fall}}}$	BLK over voltage protection falling threshold	For UCC256402A	3.72	3.8	3.88	V
FEEDBACK PIN						
$R_{FB_{\text{Internal}}}$	Internal pull down resistor value		90	100	110	k Ω

6.5 Electrical Characteristics (continued)

All voltages are with respect to GND, $-40^{\circ}\text{C} < T_J = T_A < 125^{\circ}\text{C}$, $V_{CC} = 15\text{V}$, currents are positive into and negative out of the specified terminal, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{FB}	FB internal current source	For UCC256402, UCC256402A, UCC256404, UCC256404A, UCC256404B	73	82	91	μA
		For UCC256403, UCC256403A	147	164	182	μA
V_{FB}	FB pin voltage when FB pin sink current is at $(I_{FB} - 50\mu\text{A})$			5.6		V
ΔV_{FB}	FB pin voltage variation when FB pin sink current ranges from $(I_{FB} - 50\mu\text{A})$ to $(I_{FB} - 5\mu\text{A})$			0.28		V
ΔV_{clamp}	FB pin voltage variation when FB pin sink current ranges from $(I_{FB} - 5\mu\text{A})$ to $(I_{FB} + 5\mu\text{A})$			0.4		V
$I_{FB\text{clamp}}$	Maximum FB internal current source when FB is clamped			82		μA
$\Delta V_{FB\text{clamp}}$	FB pin voltage variation when FB pin sink current ranges from $(I_{FB} + 5\mu\text{A})$ to $(I_{FB} + I_{FB\text{clamp}} - 5\mu\text{A})$			0.25		V
$f_{-3\text{dB}}$	Feedback chain -3dB cut off frequency (2)		1			MHz
RESONANT CURRENT SENSE						
$V_{\text{ISNS_OCP1}}$	OCP1 threshold		3.9	4	4.1	V
$V_{\text{ISNS_OCP1_S}}$	OCP1 threshold during soft start		4.85	5	5.15	V
$V_{\text{ISNS_OCP2}}$	OCP2 threshold		0.57	0.6	0.63	V
$V_{\text{ISNS_OCP3}}$	OCP3 threshold		0.40	0.43	0.46	V
$t_{\text{ISNS_OCP2}}$	The time the average input current needs to stay above OCP2 threshold before OCP2 is triggered (1)			2		ms
$t_{\text{ISNS_OCP3}}$	The time the average input current needs to stay above OCP3 threshold before OCP3 is triggered (1)			50		ms
$V_{\text{IpolarityHyst}}$	Resonant current polarity detection hysteresis		16	30	44	mV
n_{OCP1}	Number of OCP1 cycles before OCP1 fault is tripped (1)			4		
RESONANT CAPACITOR VOLTAGE SENSE						
V_{CM}	Internal common mode voltage		2.90	3	3.14	V
I_{RAMP}	Frequency compensation ramp current source value		1.84	2	2.16	mA
I_{Mismatch}	Pull up and pull down ramp current source mismatch (3)		-1.25		1.25	%
GATE DRIVER						
V_{LOL}	LO output low voltage	$I_{\text{sink}} = 20\text{mA}$	0.02	0.05	0.12	V
$V_{\text{RVCC}} - V_{\text{LOH}}$	LO output high voltage	$I_{\text{source}} = 20\text{mA}$	0.10	0.18	0.3	V
$V_{\text{HOL}} - V_{\text{HS}}$	HO output low voltage	$I_{\text{sink}} = 20\text{mA}$	0.02	0.05	0.12	V
$V_{\text{HB}} - V_{\text{HOH}}$	HO output high voltage	$I_{\text{source}} = 20\text{mA}$	0.10	0.18	0.3	V
$V_{\text{HB-}} - V_{\text{HSUVLOFall}}$	High side gate driver UVLO falling threshold		6.6	7.25	7.75	V
$V_{\text{HB-}} - V_{\text{HSUVLOHys}}$	High side gate driver UVLO threshold hysteresis		0.78	0.9	1.05	V

6.5 Electrical Characteristics (continued)

All voltages are with respect to GND, $-40^{\circ}\text{C} < T_J = T_A < 125^{\circ}\text{C}$, $V_{CC} = 15\text{V}$, currents are positive into and negative out of the specified terminal, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{\text{source_pk_HO}}$	HO peak source current ⁽²⁾			-0.6		A
$I_{\text{source_pk_LO}}$	LO peak source current ⁽²⁾			-0.6		A
$I_{\text{sink_pk_HO}}$	HO peak sink current ⁽²⁾			1.2		A
$I_{\text{sink_pk_LO}}$	LO peak sink current ⁽²⁾			1.2		A
BOOTSTRAP						
$I_{\text{BOOT_QUIESC}}^{\text{ENT}}$	(HB - HS) quiescent current	HB - HS = 12V	42	62	80	μA
$I_{\text{BOOT_LEAK}}$	HB to GND leakage current	$V_{\text{HB}} = 600\text{V}$		0.40	5.40	μA
$t_{\text{ChargeBoot}}$	Length of charge boot state		230	265	300	μs
SOFT START AND BURST MODE						
I_{SSup}	Current output from SS pin to charge up the soft start capacitor		26	36	45	μA
R_{SSDown}	SS pin pull down resistance	ZCS or OCP1	300	370	450	Ω
$t_{\text{SSInitVolPrgm}}$	SS initial voltage programming time ⁽¹⁾		720	776	830	μs
R_{LL}	LL/SS voltage scaling resistor value		92	98	106	k Ω
N_{burst}	Minimum number of pulses in each burst packet (including burst soft on/off pulses)	For UCC256402, UCC256402A, UCC256403A, UCC256404A		16		
		For UCC256403, UCC256404, UCC256404B		40		
N_{softmax}	Maximum number of pulses for burst soft on/off			7		
K_{soft}	Minimal ratio of $V_{\text{comp}}/V_{\text{FBreplica}}$ during burst soft on/off			0.33		
$V_{\text{LLVolPrgm}}$	LL pin voltage during the burst mode exit threshold (BMT_H) programming			3.5		V
$\text{BMT}_{H\text{min}}$	Minimal burst mode exit threshold			0.2		V
$\text{BMT}_{L\text{min}}$	Minimal burst mode entry threshold			0.2		V
BIAS WINDING						
V_{BWOPPos}	Output voltage OVP - Positive Threshold		3.86	4	4.12	V
V_{BWOPNeg}	Output voltage OVP - Negative Threshold		-4.12	-4	-3.86	V
n_{BWOP}	Number of BW OVP cycles before BW OVP fault is tripped ⁽¹⁾			5		
I_{BWPrgm}	BW pin sourcing current for $\text{BMT}_L/\text{BMT}_H$ programming		51	54	57	μA
t_{BWPrgm}	$\text{BMT}_L/\text{BMT}_H$ programming time			2		ms
$K_{\text{BMTL/BMTH1}}$	Ratio of $\text{BMT}_L/\text{BMT}_H$ Option 1			0.95		
$K_{\text{BMTL/BMTH2}}$	Ratio of $\text{BMT}_L/\text{BMT}_H$ Option 2			1		
$K_{\text{BMTL/BMTH3}}$	Ratio of $\text{BMT}_L/\text{BMT}_H$ Option 3			0.9		
$K_{\text{BMTL/BMTH4}}$	Ratio of $\text{BMT}_L/\text{BMT}_H$ Option 4			0.8		
$K_{\text{BMTL/BMTH5}}$	Ratio of $\text{BMT}_L/\text{BMT}_H$ Option 5			0.6		
$K_{\text{BMTL/BMTH6}}$	Ratio of $\text{BMT}_L/\text{BMT}_H$ Option 6			0.6		
$K_{\text{BMTL/BMTH7}}$	Ratio of $\text{BMT}_L/\text{BMT}_H$ Option 7 (Burst mode disable)			0.4		
R_{BWPrgm1}	BW pin equivalent resistance to select $\text{BMT}_L/\text{BMT}_H$ ratio option 1 ⁽²⁾		24730			Ω

6.5 Electrical Characteristics (continued)

All voltages are with respect to GND, $-40^{\circ}\text{C} < T_J = T_A < 125^{\circ}\text{C}$, $V_{CC} = 15\text{V}$, currents are positive into and negative out of the specified terminal, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{BWPrgm2}$	BW pin equivalent resistance to select BMT _L /BMT _H ratio option 2 ⁽²⁾		17125		19976	Ω
$R_{BWPrgm3}$	BW pin equivalent resistance to select BMT _L /BMT _H ratio option 3 ⁽²⁾		12562		13624	Ω
$R_{BWPrgm4}$	BW pin equivalent resistance to select BMT _L /BMT _H ratio option 4 ⁽²⁾		9018		9813	Ω
$R_{BWPrgm5}$	BW pin equivalent resistance to select BMT _L /BMT _H ratio option 5 ⁽²⁾		6478		6849	Ω
$R_{BWPrgm6}$	BW pin equivalent resistance to select BMT _L /BMT _H ratio option 6 ⁽²⁾		4450		4732	Ω
$R_{BWPrgm7}$	BW pin equivalent resistance to select BMT _L /BMT _H ratio option 7 (Burst mode disable) ⁽²⁾		2422		3038	Ω
ADAPTIVE DEADTIME						
dV_{HS}/dt	Detectable slew rate ⁽¹⁾		-0.1		-50	V/ns
FAULT RECOVERY						
$t_{PauseTimeOut}$	Paused timer ⁽¹⁾			1		s
THERMAL SHUTDOWN						
T_{J_r}	Thermal shutdown temperature ⁽¹⁾	Temperature rising	125	145		$^{\circ}\text{C}$
T_{J_H}	Thermal shutdown hysteresis ⁽¹⁾			10		$^{\circ}\text{C}$

(1) Not tested in production. Established by characterization

(2) Not tested in production. Established by design

(3) $I_{Mismatch}$ calculated as

$$[I_{PU} - (I_{PD} + I_{PU})/2] / [(I_{PD} + I_{PU})/2] \quad (1)$$

6.6 Switching Characteristics

All voltages are with respect to GND, $-40^{\circ}\text{C} < T_J = T_A < 125^{\circ}\text{C}$, $V_{CC} = 15\text{V}$, currents are positive into and negative out of the specified terminal, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{r(LO)}$	Rise time	10% to 90%, 1nF load		30	50	ns
$t_{f(LO)}$	Fall time	10% to 90%, 1nF load		20	50	ns
$t_{r(HO)}$	Rise time	10% to 90%, 1nF load		30	50	ns
$t_{f(HO)}$	Fall time	10% to 90%, 1nF load		20	50	ns
$t_{DT(min)}$	Minimum dead time ⁽¹⁾			100		ns
$t_{DT(max)}$	Maximum dead time (dead time fault) ⁽¹⁾	ZCS event is not detected		1.1		μs
$t_{DT(max_ZCS)}$	Maximum dead time (dead time fault) ⁽¹⁾	ZCS event is detected		150		μs
$t_{ON(min)}$	Minimum gate on time ⁽¹⁾			250		ns
$t_{ON(max)}$	Maximum gate on time ⁽¹⁾			16		μs

(1) Not tested in production. Established by design

6.7 Typical Characteristics

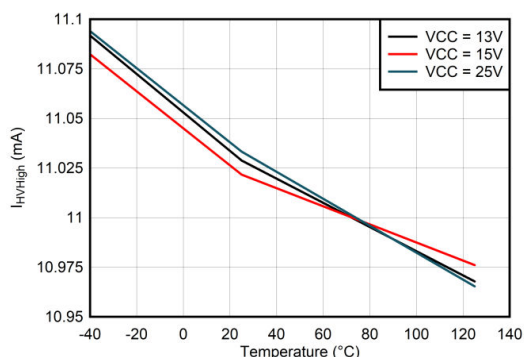


Figure 6-1. I_{HVHigh} vs Temperature

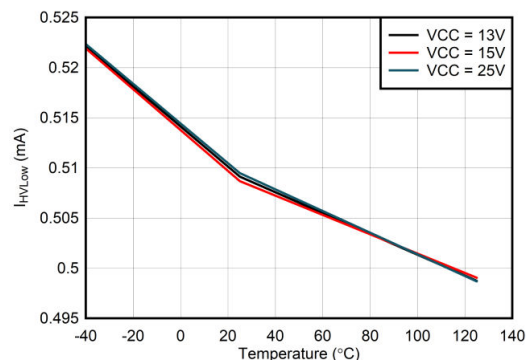


Figure 6-2. I_{HVLow} vs Temperature

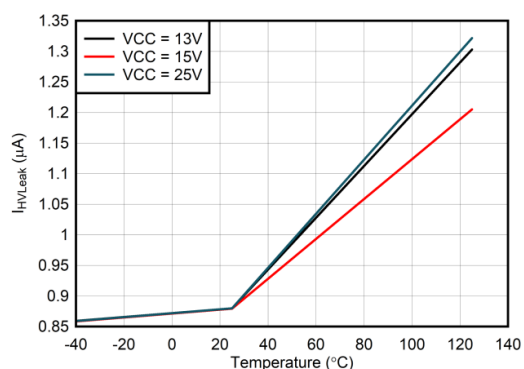


Figure 6-3. I_{HVLeak} vs Temperature

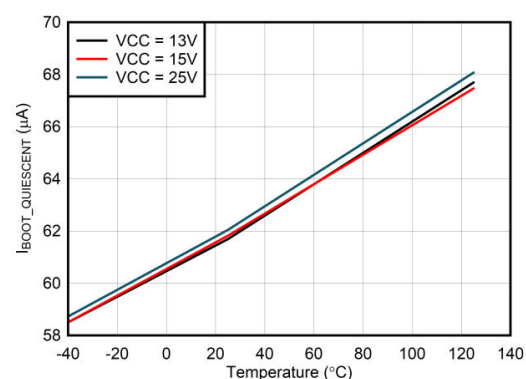


Figure 6-4. $I_{BOOT_QUIESCENT}$ vs Temperature

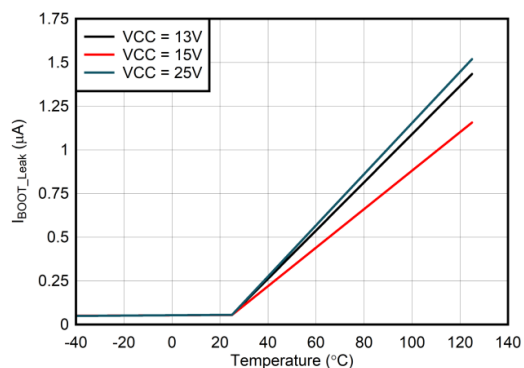


Figure 6-5. I_{BOOT_LEAK} vs Temperature

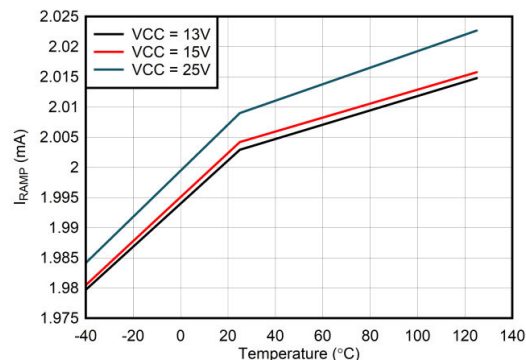


Figure 6-6. I_{RAMP} vs Temperature

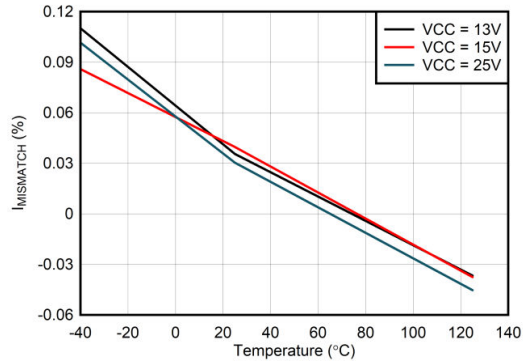


Figure 6-7. I_{MISMATCH} vs Temperature

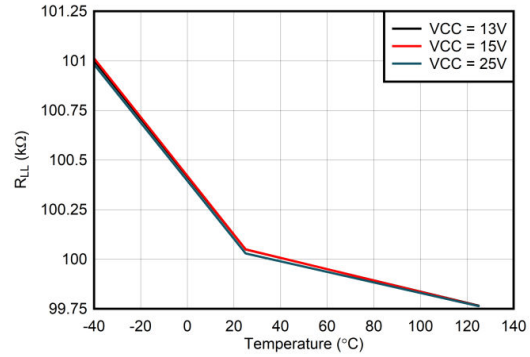


Figure 6-8. R_{LL} vs Temperature

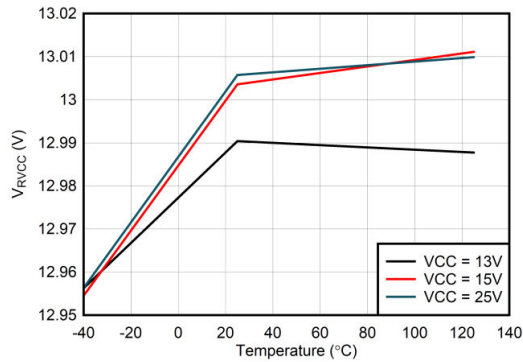


Figure 6-9. V_{RVCC} (no load) vs Temperature

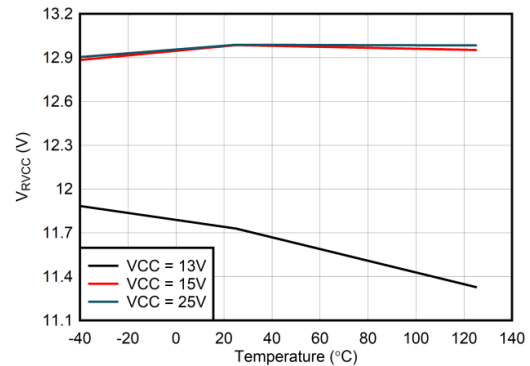


Figure 6-10. V_{RVCC} (100mA load) vs Temperature

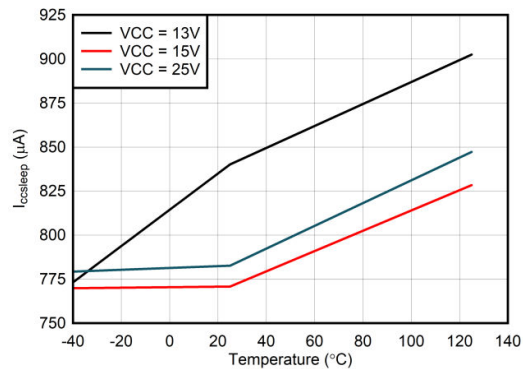


Figure 6-11. I_{CCSleep} vs Temperature

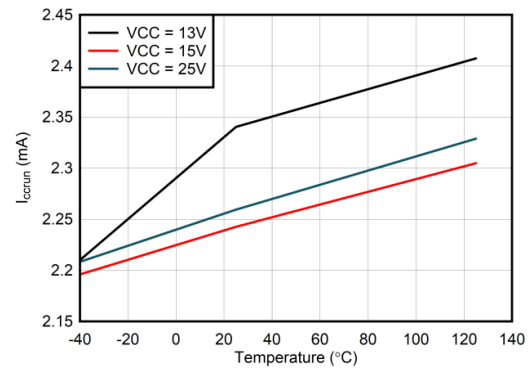


Figure 6-12. I_{CCRun} vs Temperature

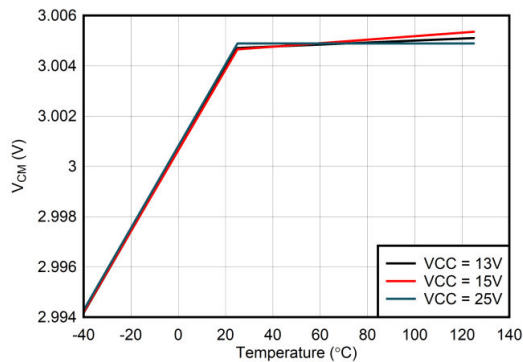


Figure 6-13. V_{CM} vs Temperature

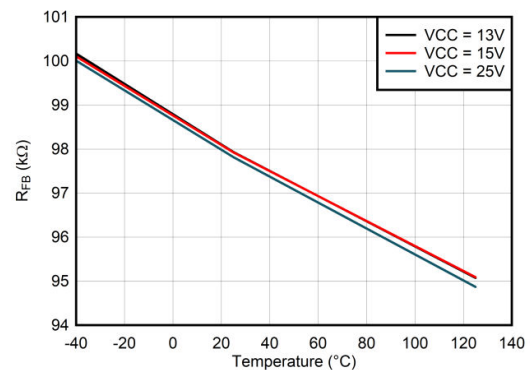


Figure 6-14. R_{FB} vs Temperature

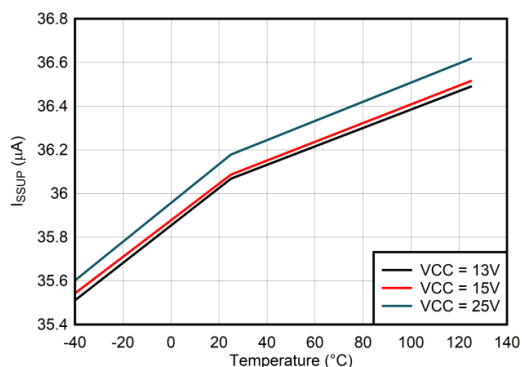


Figure 6-15. I_{SSUP} vs Temperature

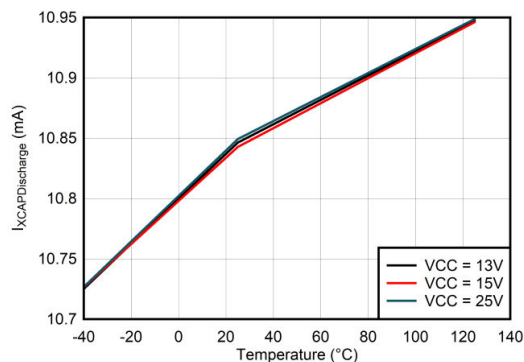


Figure 6-16. $I_{XCAPDischarge}$ vs Temperature

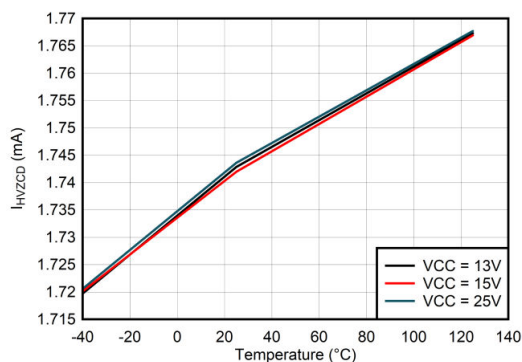


Figure 6-17. I_{HVZCD} vs Temperature

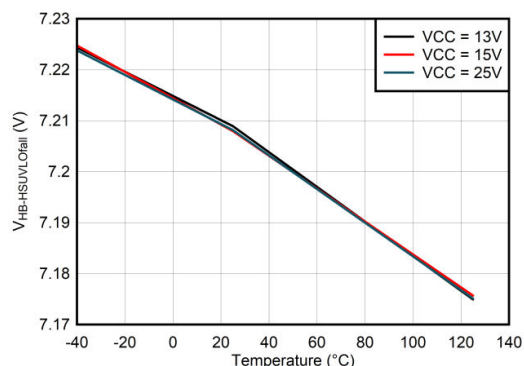


Figure 6-18. $V_{HB-HSUVLOFall}$ vs Temperature

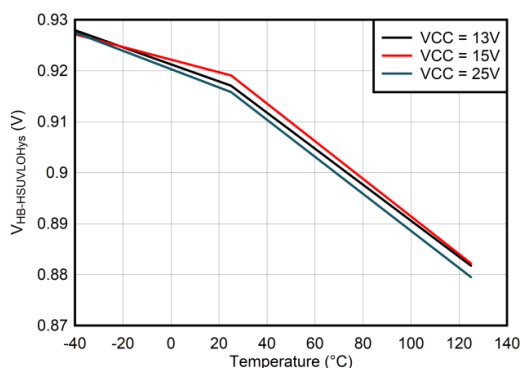


Figure 6-19. $V_{HB-HSUVLOHys}$ vs Temperature

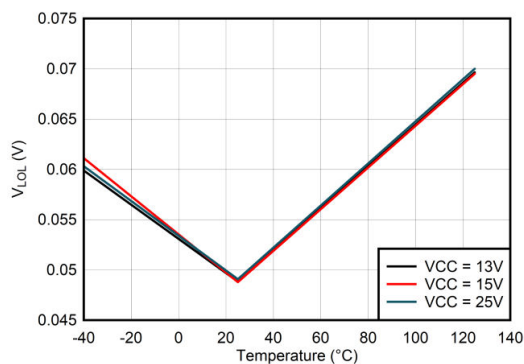


Figure 6-20. V_{LOL} vs Temperature

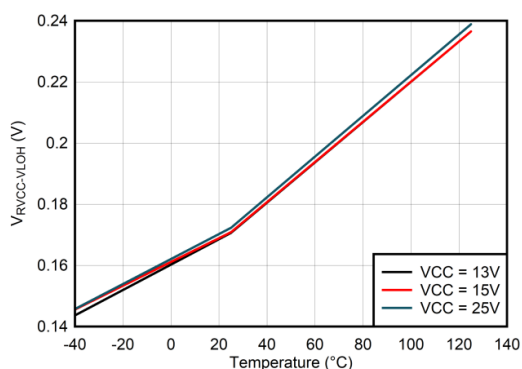


Figure 6-21. $V_{RVCC-VLOH}$ vs Temperature

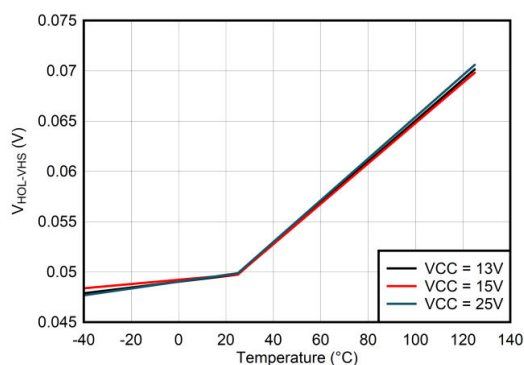


Figure 6-22. $V_{HOL-V_{HS}}$ vs Temperature

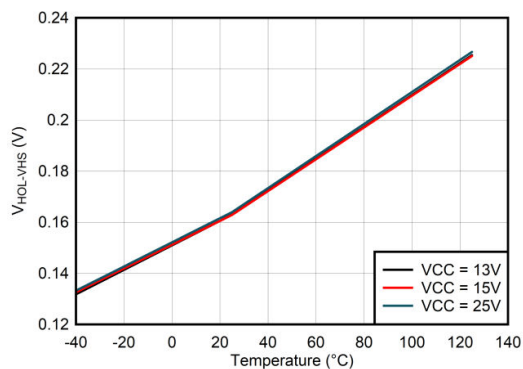


Figure 6-23. $V_{HB} - V_{HOH}$ vs Temperature

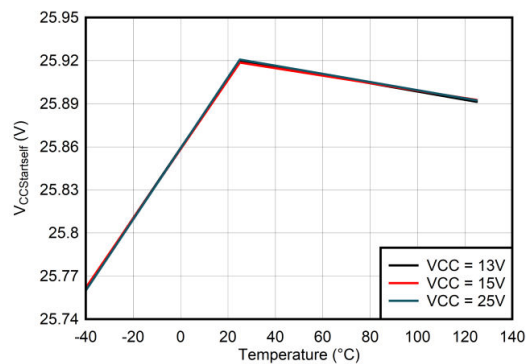


Figure 6-24. $V_{CCStartSelf}$ vs Temperature

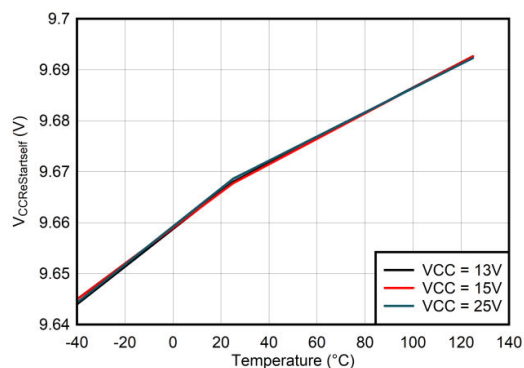


Figure 6-25. $V_{CCReStartJfet}$ vs Temperature

7 Detailed Description

7.1 Overview

The UCC25640x is a fully featured LLC resonant controller for AC/DC power supplies. The high level of integration of UCC25640x enables significant reduction of component count and option size without compromising functionality. UCC25640x achieves very low standby power and low audible noise standby operation using an optimized burst mode. The novel control scheme of the device offers excellent transient performance.

Many consumer application use PFC + LLC power supplies, including large screen televisions, AC-DC adapters, industrial power supplies, and LED drivers. This topology is preferred over a PFC and flyback design because it offers improved efficiency and a smaller size. A disadvantage of the PFC and LLC power supply system is that it has poor light load efficiency and high no-load power consumption because the LLC stage requires a minimum amount of circulating current to maintain regulation. To meet light load efficiency and standby power consumption requirements, traditionally an auxiliary flyback converter is used. The auxiliary flyback converter runs continuously to allow the main PFC + LLC power system to shut down when the system enters low-power or standby mode. UCC25640x contains several novel features that enable it to offer excellent light load efficiency and low no-load power. This allows power supply designers to create systems that meet the stringent no-load power target without needing an auxiliary flyback converter.

UCC25640x uses a novel control algorithm, Hybrid Hysteretic Control (HHC), to achieve regulation. In this control algorithm, the resonant capacitor voltage defines the switching frequency, which carries accurate input current information. This allows the controller to monitor and correct the input current directly. Compared with traditional Direct Frequency Control (DFC), HHC makes the system close to a first order system if the frequency control portion is small. This enables excellent load and line transient response.

UCC25640x adopts an advanced burst mode to meet the stringent requirements on standby power consumption and audible noise level. At low output power levels UCC25640x automatically transitions into light-load burst mode. In burst mode, UCC25640x repetitively delivers a burst packet with a fixed number of switching pulses and a shut-off period. The secondary regulator loop based on the FB pin current terminates the shut-off time period between burst packets. The LLC equivalent load current level during the burst on period is a programmable value. For each burst packet, the switching frequency slowly ramps down at the first few switching periods and ramps up at the last few switching periods, to slowly ramp-up and ramp-down the resonant current during burst operation. This burst soft-on and soft-off can effectively help to minimize the audible noise during burst mode operation. In addition, UCC25640x operates in a low-power mode during burst mode with a very low quiescent current and biased optocoupler operation with low current.

UCC25640x monitors the half-bridge switch node to determine the required dead-time for the gate signals. In this way the dead-time is automatically adjusted to provide optimum efficiency and robust operation. UCC25640x includes a slew rate detector with improved sensitivity of the switch node voltage for adaptive dead-time that makes its operation inherently robust compared with alternative parts.

UCC25640x includes high and low-side drivers that can directly drive N-channel MOSFETs in an LLC power stage. This allows complete and fully featured power systems to be realized with minimum component count.

UCC256402 and UCC256404 includes a high-voltage startup JFET to initially charge the VCC capacitor to provide the energy needed to start the PFC and LLC power system. Once running, power for the PFC and LLC controllers derive from a bias winding on the LLC transformer. UCC256404 also includes the active X-capacitor discharge feature to discharge the remaining voltage on the X-capacitor of the EMC filters after unplugging the AC input. UCC256403 does not include the high voltage startup and active X-capacitor discharge features. It requires an auxiliary supply to power the VCC.

UCC25640x includes robust algorithms for avoiding the zero-current switching (ZCS) operation region. When ZCS operation is detected, UCC25640x overrides the feedback signal and ramps up the switching frequency until non-capacitive operation is restored. After, the switching frequency ramps back down at a rate the soft-start capacitor determines until control is handed back to the voltage control loop.

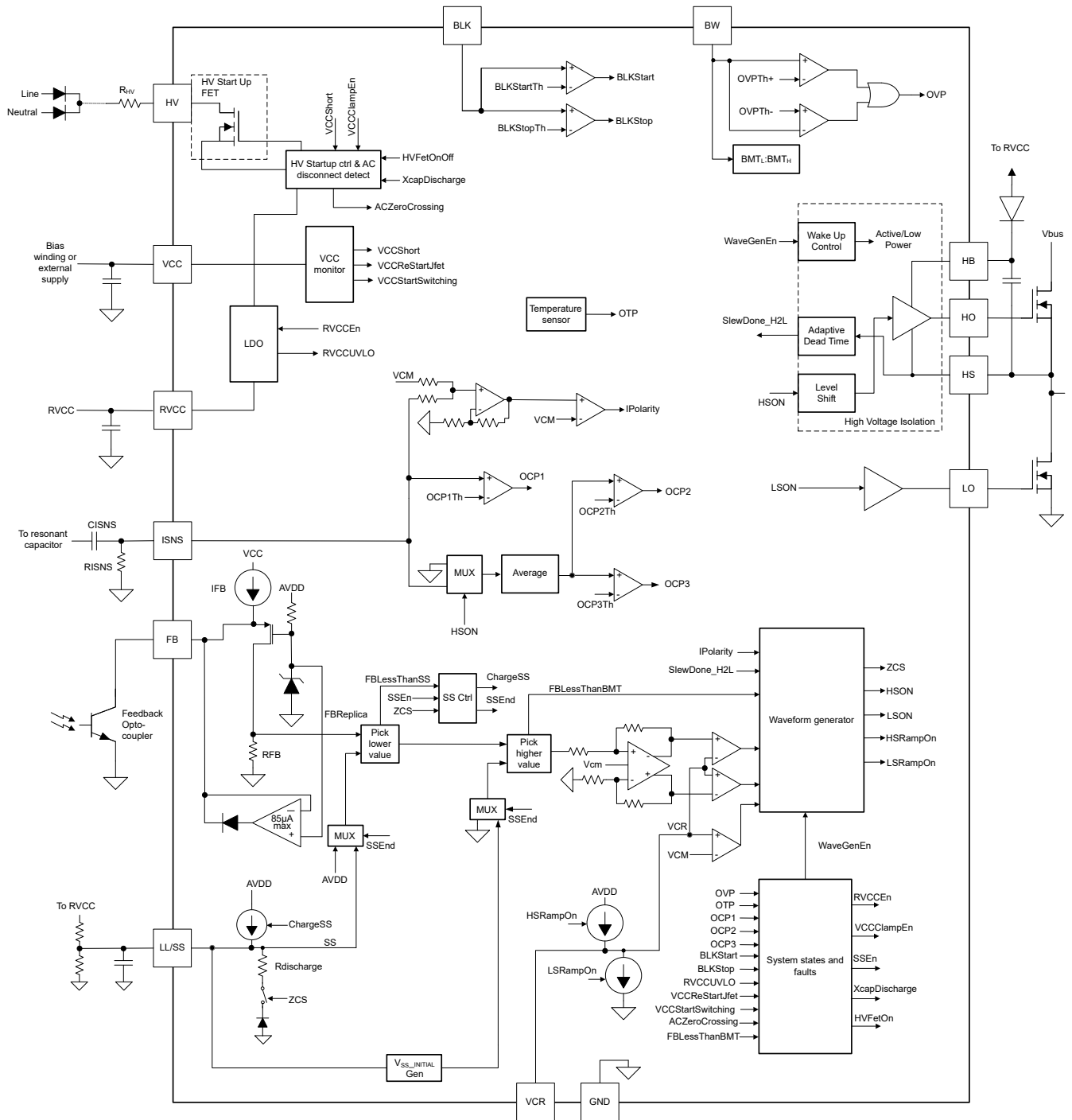
Additional protection features of UCC25640x include

- Three-level overcurrent protection (OCP)
- Output overvoltage protection (OVP)
- Input voltage undervoltage protection (UVP)
- Gate driver undervoltage lock-out (UVLO) protection
- Over temperature protection (OTP)

A summary of the key features of UCC25640x follows:

- Hybrid Hysteretic Control helps achieve best-in-class load and line transient response
- Optimized light load burst mode enables less than 150mW standby power designs
- Burst soft-on and soft-off enables ultra-quiet standby operation
- Robust adaptive dead time control
- Integrated high-voltage gate driver
- Integrated high-voltage startup for UCC256402 and UCC256404
- Active X-capacitor discharge for UCC256404
- Improved capacitive region operation prevention scheme
- Comprehensive protection feature set

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Hybrid Hysteretic Control

UCC25640x uses a novel control scheme, Hybrid Hysteretic Control (HHC), to achieve best-in-class line and load transient performance. The control method makes the compensator easier to design. The control method also makes light load management easier and more efficient. Improved line transient enables lower bulk capacitor and output capacitor values, reducing system cost.

HHC is a control method which combines traditional frequency control and charge control. It is a charge control with an added frequency compensation ramp. Compared with traditional frequency control, it changes the power stage transfer function from a second order system to a first order system, so that it makes the compensation network design easier. The control effort is directly related to input current, so superior line and load transients can be achieved. Compared with charge control, Hybrid Hysteretic Control avoids instability by adding in a frequency compensation ramp. The frequency compensation establishes system stability, and makes the output impedance lower as well. Lower output impedance makes the transient performance better than charge control. The frequency compensation also makes the implementation of burst mode soft-on and soft-off much easier, as changing the control effort can directly impact the switching frequency. For burst mode soft-on and soft-off, the converter switching frequency self-adjusts to achieve a reduced resonant current.

In summary, HHC solves the following problems:

- Help LLC converters achieve superior load transient and line transient
- Changes the small-signal transfer function to a first order system to easily achieve very high bandwidth
- Inherently stable via frequency compensation
- Makes burst mode control easier to optimize light load efficiency
- Makes the implementation of burst mode soft-on and soft-off much easier, to achieve lower audible noise

Figure 7-1 shows the HHC implementation in UCC25640x: a capacitor divider (C1 and C2) and two well matched controlled current sources. The resonant capacitor voltage is divided down by the capacitor divider formed by C1 and C2. The current sources are controlled by the gate drive signals. When the high-side switch is on, the upper current source injects a constant current into the capacitor divider; when the low-side switch is on, the lower current source pulls the same amount of constant current out of the capacitor divider. The two current sources add a triangular compensation ramp to the VCR node. The current sources are supplied by a reference voltage AVDD. AVDD must be equal to or larger than twice the common mode voltage V_{CM} . The divided resonant capacitor voltage and the compensation ramp voltage are then added together to get the VCR node voltage. If the frequency compensation ramp dominates, the VCR node voltage looks like a triangular waveform, and the control is similar to direct frequency control. If the resonant capacitor voltage dominates, the shape of the VCR node voltage will look like the actual resonant capacitor voltage, and the control will be similar to charge control. This is why the control method is called “hybrid” and the compensation ramp is called frequency compensation.

This set up has an inherent negative feedback to keep the high-side and low-side on-time balanced, and also to keep the common mode voltage at the VCR node at V_{CM} .

There are two input signals needed for the new control scheme: VCR and V_{COMP} . VCR is the sum of the scaled down version of the resonant capacitor voltage and the frequency compensation ramp. V_{COMP} is the voltage loop compensator output. The waveform below shows how the high-side and low-side switches are controlled based on VCR and V_{COMP} . The common mode voltage of VCR is V_{CM} .

Based on V_{COMP} and V_{CM} (3V), two thresholds: V_{TH} and V_{TL} are created.

$$V_{TH} = V_{CM} + \frac{V_{comp}}{2} \quad (2)$$

$$V_{TL} = V_{CM} + \frac{V_{comp}}{2} \quad (3)$$

The VCR voltage is compared with the two thresholds. When $VCR > V_{TH}$, the high-side switch is turned off; when $VCR < V_{TL}$, low-side switch is turned off. HO and LO turn on edges are controlled by the adaptive dead time circuit.

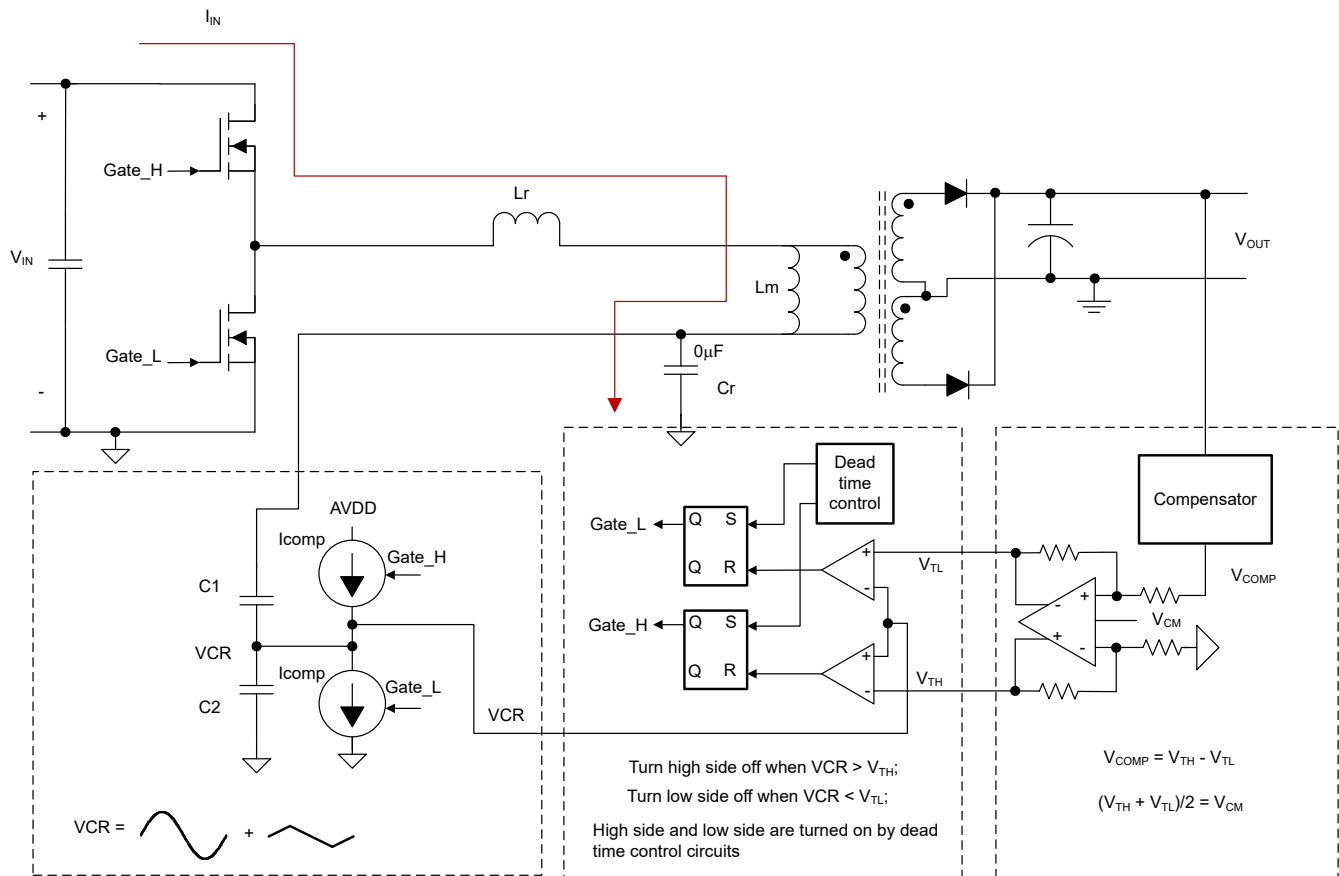


Figure 7-1. UCC25640x HHC Implementation

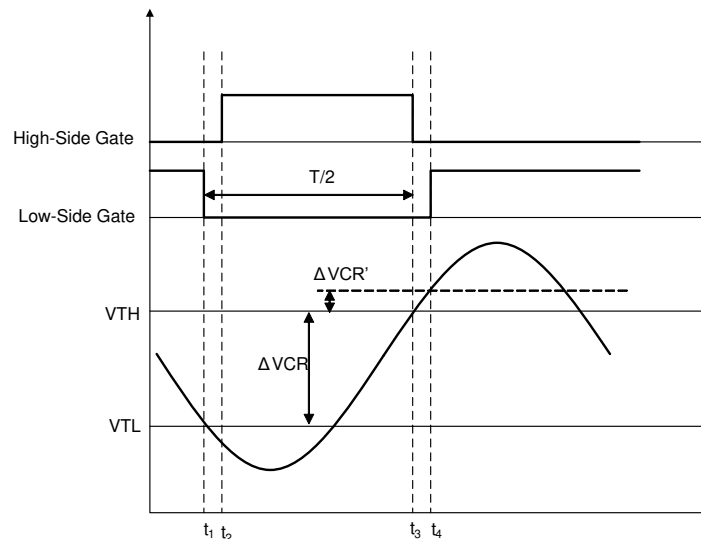


Figure 7-2. HHC Gate On/Off Control Principle

7.3.2 Regulated 13V Supply

RVCC pin is the regulated 13V supply. This regulated rail is used to supply the PFC and LLC as a bias. RVCC has under voltage lock out (UVLO) function. During normal operation, if the RVCC voltage is less than $RVCC_{UVLO}$ threshold, the system enters FAULT state. The [Section 7.3.9](#) section includes details about the FAULT handling.

7.3.3 Feedback Chain

Control of the output voltage is provided by a voltage regulator circuit located on the secondary side of the isolation barrier. The demand signal from the secondary regulator circuit is transferred across the isolation barrier using an optocoupler and is fed into the FB pin on UCC25640x. This section describes the whole feedback chain. [Figure 7-3](#) shows the block diagram of the FB chain, and [Figure 7-4](#) shows the typical timing diagram with a normal soft start, followed by a ZCS event, and load step into burst mode, and then exiting burst mode.

The feedback chain has the following functions:

- Optocoupler feedback signal input and bias
- FB voltage clamp
- Soft start function selection by a "pick lower value" block
- Burst mode selection by a "pick higher value" block
- Convert single ended feedback demand into two thresholds V_{TH} and V_{TL} ; and VCR comparison with the thresholds and the common mode voltage V_{CM}

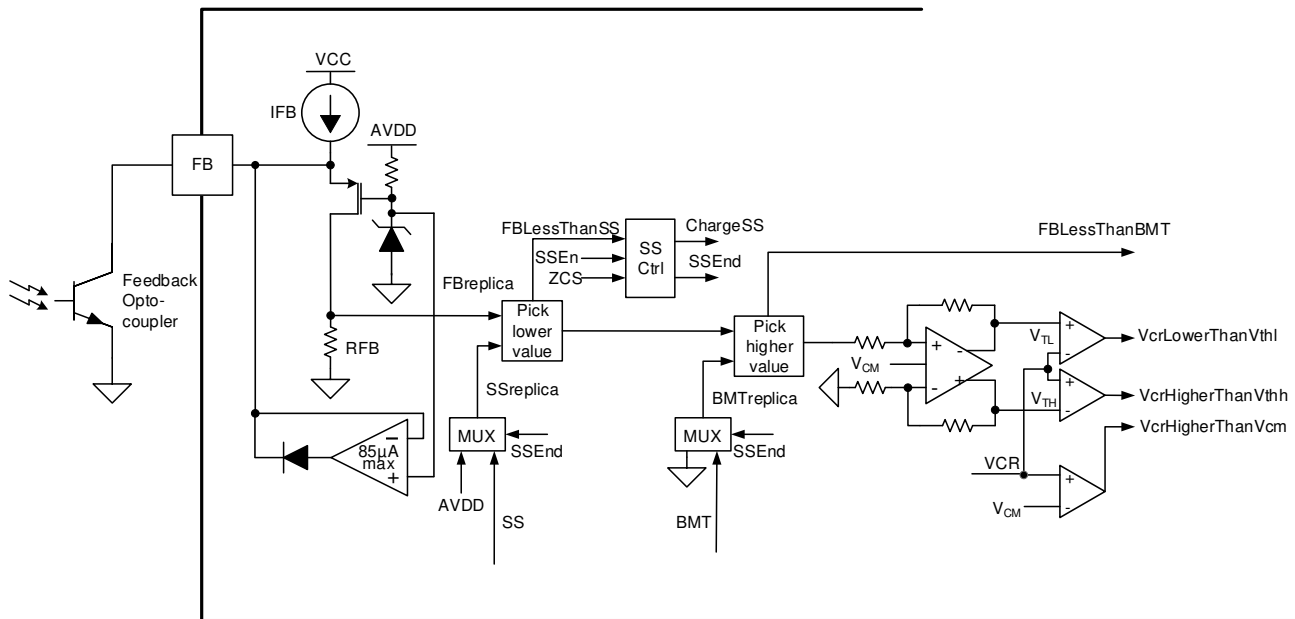


Figure 7-3. Feedback Chain Block Diagram

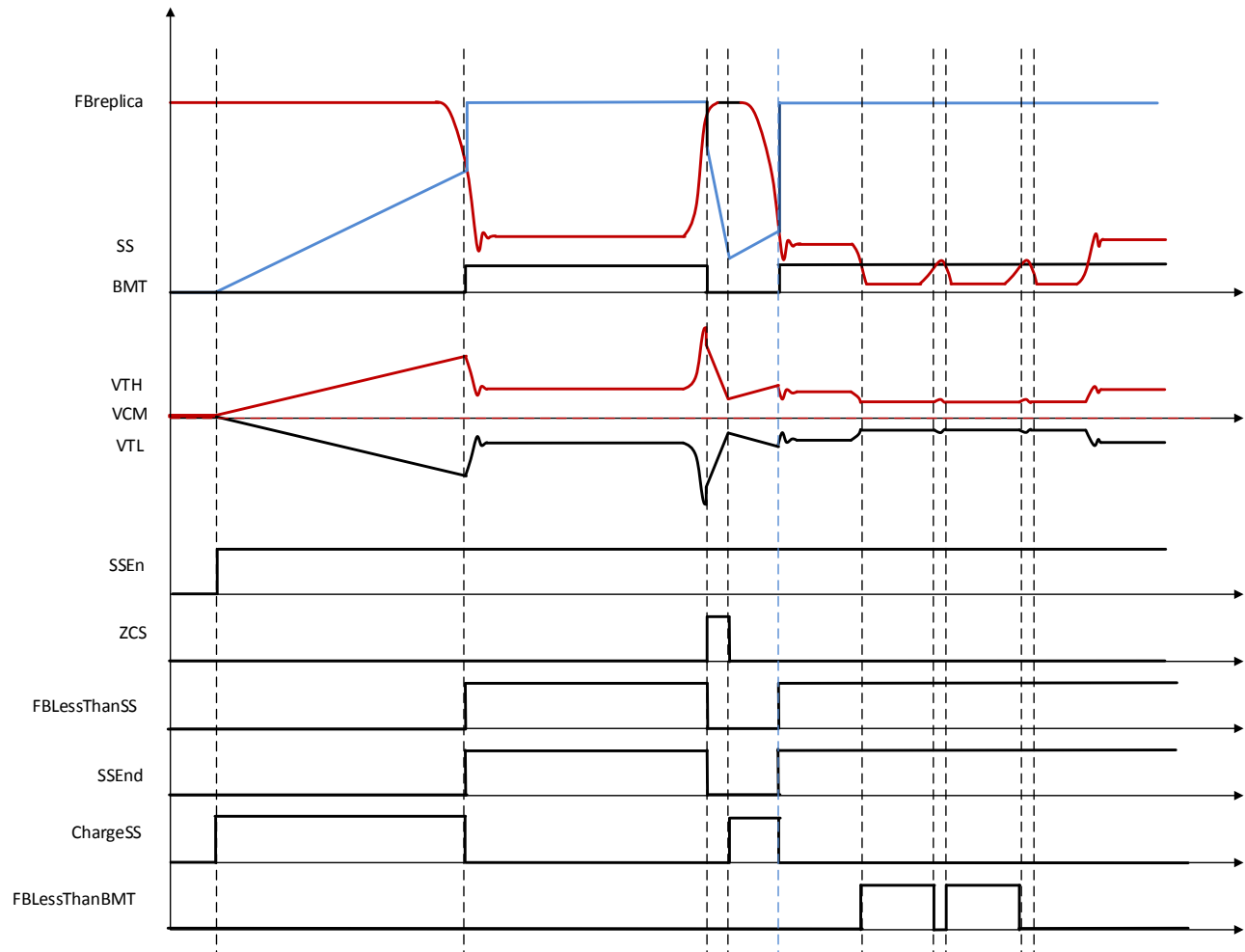


Figure 7-4. Feedback Chain Timing Diagram

7.3.3.1 Optocoupler Feedback Signal Input and Bias

The secondary regulator circuit and optocoupler feedback circuit all add directly to the standby power the system consumes. To achieve very low standby power, to drive the optocoupler in a low current mode.

As shown in [Figure 7-3](#), a constant current source I_{FB} is generated from VCC voltage and connected to FB pin. A resistor R_{FB} is also connected to this current source with a PMOS in series. During normal operation, the PMOS is always on, so that the FB pin voltage is equal to the zener diode reference voltage plus the voltage drop on the PMOS source to gate.

$$I_{FB} = I_{opto} + I_{RFB} \quad (4)$$

From this equation, when I_{opto} increases, I_{RFB} decreases, making $FB_{replica}$ decrease. In this way, the control effort is inverted. A conventional way to bias the optocoupler is using a pull up resistor on the collector of the optocoupler output. To reduce the power consumption, the pullup resistor must be big, which limits the loop bandwidth. For the bias current method used in UCC25640x, the FB pin voltage is maintained constant so that the parasitic capacitor of the optocoupler does not introduce an extra pole to the system, and subsequently limit the loop bandwidth.

7.3.3.2 FB Pin Voltage Clamp

As shown in the [Section 7.3.3.1](#) section, the $FB_{replica}$ decreases while I_{opto} increases. When I_{opto} reaches the value of I_{FB} , the FB pin voltage starts to drop because there is no current flow through the PMOS. FB pin pulled

low impacts the system transient response, due to the extra delay introduced by charging the parasitic capacitor of the optocoupler to pull up the FB pin voltage. A FB pin voltage clamp circuit is used to prevent this scenario. When FB pin voltage drops below the FB pin clamp voltage threshold, an extra current source is turned on to clamp the FB voltage. The clamp strength is $I_{FBclamp}$. The FB pin clamp circuit improves the system transient performance from light load to heavy load.

7.3.3.3 "Pick Lower Value" Block and Soft Start Multiplexer

This part of the circuit consists of 3 elements:

- A pick lower block
- A MUX which selects AVDD or SS signal as the second input to the pick lower block
- An SS control block which handles the charge and discharge of the SS capacitor in the case of a ZCS fault

The pick lower block has two inputs. The first input is FBreplica. The second input is selected between AVDD and LL/SS pin voltage. The output of the block is the lower of the two inputs.

The MUX selects between SS and AVDD. The selection is based on SSEnd (soft start end) signal, which is an output of the SS Ctrl block. SSEnd is high when SS is higher than FBreplica, and the soft start process has been initiated by the state machine, and there is no ZCS condition. Switching to AVDD after soft start has ended helps make sure that during non-soft start or non-ZCS fault condition, FBreplica signal is always sent through the pick lower block. It also releases the LL/SS pin to perform the light load threshold programming.

The SS control block handles the charge and discharge of the SS capacitor in the case of a ZCS fault. It resets the SSEnd signal when ZCS occurs, so the effect of pulling down on LL/SS pin to increase the switching frequency can pass through the pick lower block.

7.3.3.4 Pick Higher Block and Burst Mode Multiplexer

The output of the pick lower block goes into a pick higher block, which selects the higher of the pick lower block output and the burst mode threshold setting.

The burst mode multiplexer selects between burst mode threshold (BMT) and ground. During soft start, the multiplexer selects ground. The startup process is open loop and controlled by the soft start ramp. Burst mode is not enabled during soft start phase.

After soft start, the higher of the two inputs are sent to the differential amplifier. The output of the block is FBLessThanBMT. This output is sent to the waveform generator state machine to control burst mode and system external shut down.

7.3.3.5 VCR Comparators

The output of the pick higher block is sent to a differential amplifier to convert the signal into two thresholds symmetrical to V_{CM} . The difference between the two thresholds V_{TH} and V_{TL} equals the input amplitude. The VCR pin voltage is then compared with V_{TH} , V_{TL} , and V_{CM} . The results are sent to the waveform generator.

7.3.4 Resonant Capacitor Voltage Sensing

The resonant capacitor voltage sense pin senses the resonant capacitor voltage through a capacitor divider. Inside the device, two well matched, controlled current sources are connected to the VCR pin to generate the frequency compensation ramp. The on/off control signals of the two current sources come from the waveform generator block.

During waveform generator IDLE state or before startup, the VCR node clamp to V_{CM} . This action helps reduce the startup peak current, and help the VCR voltage to settle down quickly during burst mode.

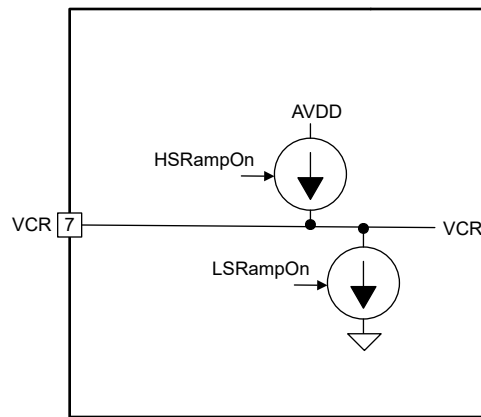


Figure 7-5. VCR Block Diagram

Figure 7-6 shows the ramp current on/off sequence. The ramp current is on all the time. It changes direction at the falling edge of the high-side on or low-side on signal.

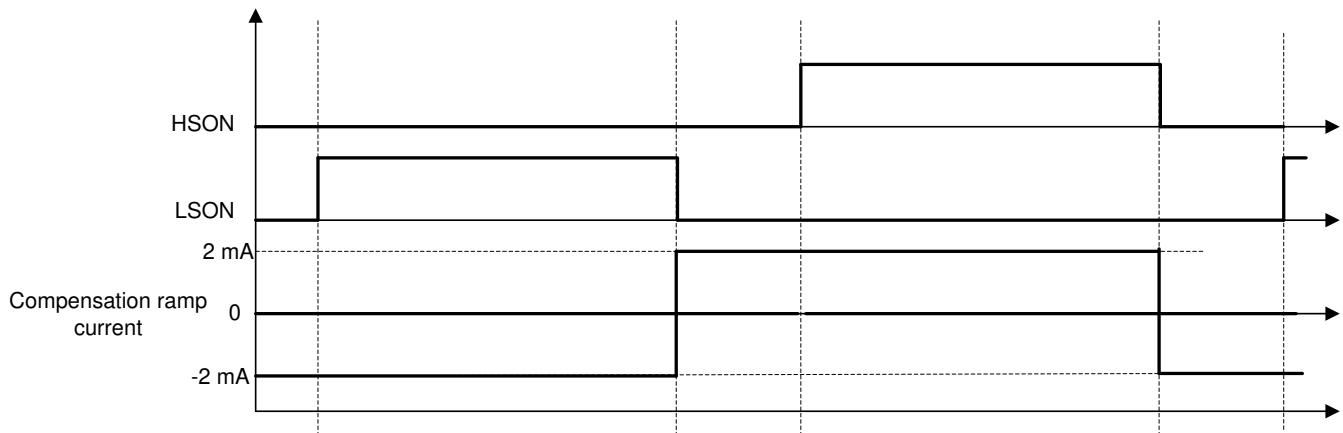


Figure 7-6. VCR Compensation Ramp Current On/Off

On the VCR pin, a capacitor divider is used to combine the resonant capacitor waveform and the compensation ramp waveform. Adjusting the size of the external capacitors can change the contribution of charge control and direct frequency control. Assuming the divided down version of the resonant capacitor voltage by the capacitor divider is V_{div} , the compensation ramp current resultant voltage on the VCR pin is V_{ramp} . If V_{div} is much larger than V_{ramp} , the control method is similar to charge control, in which the control effort is proportional to the input charge of one switching cycle. If V_{ramp} is much larger than V_{div} , the control method is similar to direct frequency control, in which the control effort is proportional to the switching frequency. Adjust the ratio between V_{div} and V_{ramp} to achieve the best transient response.

7.3.5 Resonant Current Sensing

The ISNS pin is connected to the resonant capacitor using a high voltage capacitor. The capacitor CISNS and the resistor RISNS form a differentiator. The resonant capacitor voltage is differentiated to get the resonant current. The differentiated signal is AC and goes both positive and negative. To sense the zero crossing, the signal is level shifted using an op amp adder. The IPolarity comparator detects the direction of the resonant current. IPolarity is checked at LSON and HSON falling edges for ZCS protection, with more details described in Section 7.3.9.1 section. The digital state machine implements a blanking time on IPolarity. The IPolarity edges during the first 400ns of dead time are ignored considering the noise on ISNS pin introduced by the switching node transition.

OCP2 and OCP3 thresholds are based on average input current. To get the average input current, the differentiator output is multiplexed with the high-side switch on signal HSON. When HSON is on, the MUX

output is the differentiator output; when HSON is off, the MUX output is 0. The MUX output is then averaged using a low pass filter. The output of the filter is the sensed average input current. Note that the MUX must pass through both positive and negative voltages. OCP2 and OCP3 faults have a 2ms and 50ms timer respectively. Only when the OCP2/OCP3 comparators output high for continuous 2ms or 50ms, the faults activate.

OCP1 threshold is set on the peak resonant current. The voltage on the ISNS pin gets compared to OCP1 threshold OCP1Th directly. The peak resonant current is checked once per cycle on the positive half cycle. OCP1 fault is only activated when there are 4 consecutive cycles of OCP1 event detected. During start up, the OCP1 comparator output of the first 15 cycles are ignored.

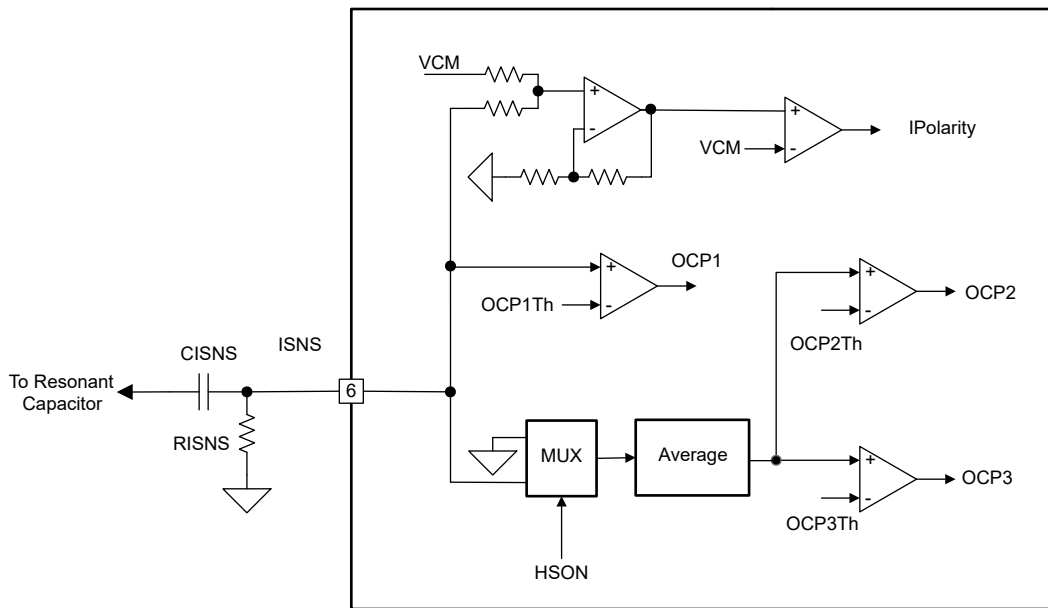


Figure 7-7. ISNS Block Diagram

7.3.6 Bulk Voltage Sensing

The BLK pin is used to sense the LLC DC input voltage (bulk voltage) level. The comparators on BLK pin have the following two thresholds:

- Bulk voltage level when LLC starts switching – $V_{BLKStart}$
- Bulk voltage level when LLC stops switching – $V_{BLKStop}$

A resistor divider is connected to the pin to achieve the desired system input range. A fault is triggered if BLK pin voltage drops lower than $V_{BLKStop}$ during operation. The detailed action of Input Under Voltage Protection is described in [Section 7.3.9.4](#) section.

[Figure 7-8](#) shows the block diagram of the BLK pin.

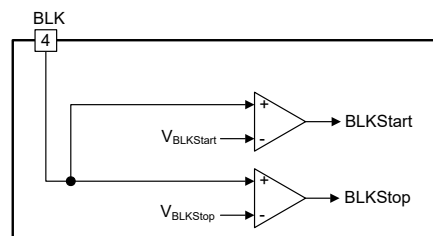


Figure 7-8. BLK Pin Block Diagram

BLK voltage is also used to monitor the input over voltage fault for some device versions as listed in [Section 4](#). There are two thresholds:

- Bulk voltage level when BLK over voltage protection (OVP) rising threshold - $V_{BLKOVPRise}$
- Bulk voltage level when BLK over voltage protection (OVP) falling threshold - $V_{BLKOVPFall}$

When BLK voltage is higher than $V_{BLKOVPRise}$, OVP is triggered; OVP gets cleared when BLK voltage falls below $V_{BLKOVPFall}$.

7.3.7 Output Voltage Sensing

The output voltage is sensed through the bias winding (BW) voltage sense pin. With one terminal of the bias winding connected to primary side ground, the bias winding voltage at the other terminal represents the output voltage when the secondary side rectifier diode conducts. A resistor divider is typically used to connect from the bias winding terminal to the BW pin. The BW voltage is compared with a positive and a negative threshold to generate an output OVP fault. During startup, BW pin is multiplexed for burst mode threshold programming. The details are introduced in the [Section 7.4.3.1](#) section. [Figure 7-9](#) is a block diagram of the bias winding voltage sense block.

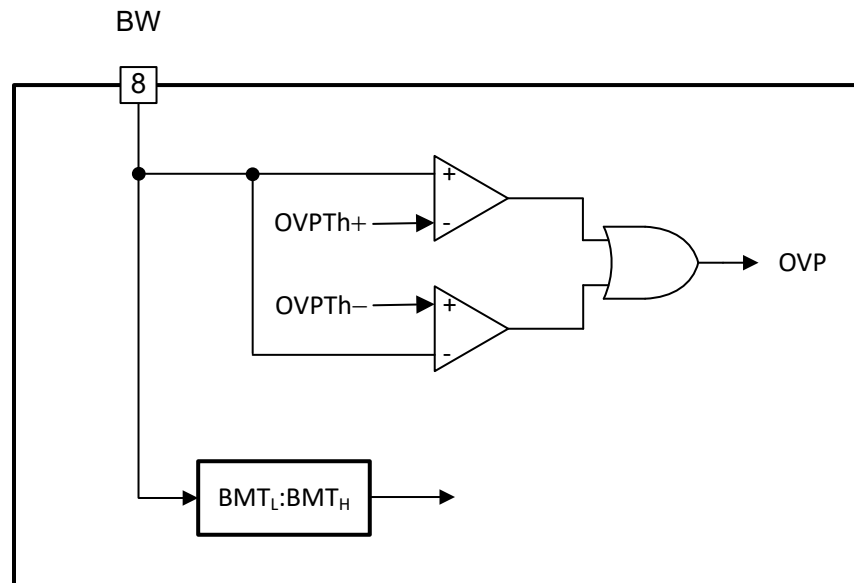


Figure 7-9. Bias Winding Sensing Block Diagram

If the OVP event is high for 5 consecutive switching cycles, the system enters FAULT state. [Section 7.3.9.3](#) describes the actions during an OVP fault.

7.3.8 High Voltage Gate Driver

LO is the low-side gate driver output. The gate driver is supplied by the 13V RVCC rail.

The high-side driver module consists of three physical device pins. HB and HS form the positive and negative bias rail, respectively, of the high-side driver, and HO connects to the gate of the upper half-bridge MOSFET.

During periods when the lower half-bridge MOSFET is conducting, HS shortens to GND through the conducting lower MOSFET. At this time power for the high-side driver is obtained from RVCC through the high voltage diode DBOOT, and capacitor CBOOT charges to RVCC, minus the forward drop on the diode.

During periods when the upper half-bridge MOSFET is conducting, HS connects to the LLC input voltage rail. At this time the HV diode is reverse biased and the high-side driver is powered by the charge stored in CBOOT.

Both the high-side and low-side gate drivers have under voltage lock out (UVLO) protection. The low-side gate driver UVLO is implemented on RVCC; the high-side gate driver UVLO is implemented on (HB - HS) voltage.

When operating at light load, UCC25640x enters burst mode. During the burst off period, the gate driver enters low-power mode to reduce power consumption.

Figure 7-10 shows the block diagram of the gate driver.

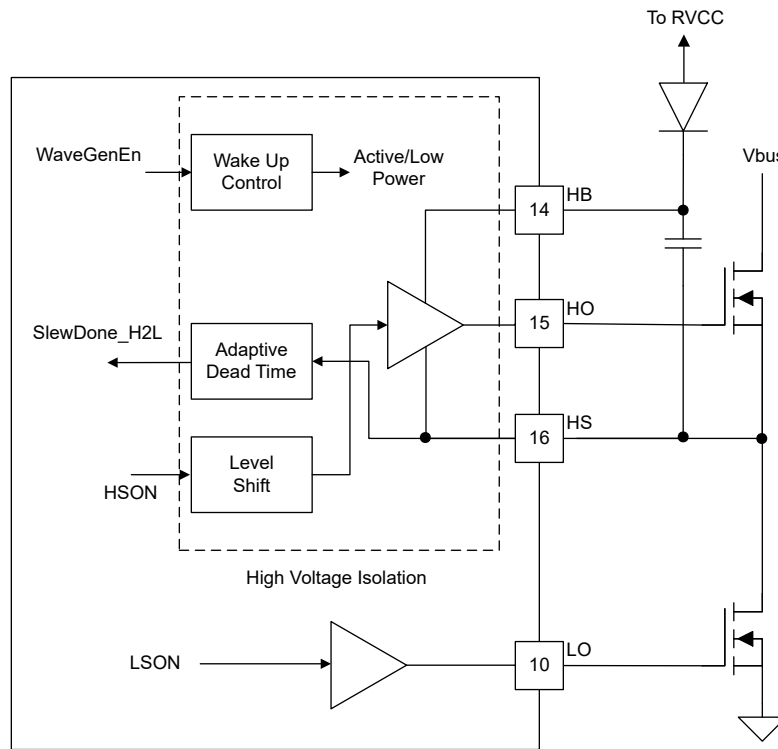


Figure 7-10. Gate Driver Block Diagram

7.3.8.1 Adaptive Dead Time Control

The Dead Time describes the time interval between an outgoing LLC MOSFET turning off and the incoming LLC MOSFET turning on. Dead time control is critical for LLC operation. A certain amount of dead time is required to prevent shoot-through. During the dead time, the HS node slews from one input rail to the other due to the inductive resonant current. To achieve zero voltage switching (ZVS) turn on, the dead time must be long enough for the resonant current to fully charge or discharge the HS node. After the body diode starts conducting, the MOSFET must be quickly turned on. Too long of a turn-on delay can result in reverse resonant current and lead to the loss of ZVS. Also, the voltage drop on the body diode is higher than that on the MOSFET channel. Optimized dead time can help to minimize the power loss.

The resonant current flowing through the HS node during the dead time depends on the LLC resonant tank design and varies by operating frequency and output/input voltage ratio. Therefore, the optimized dead time varies widely with LLC operating conditions. UCC25640x includes an adaptive dead time control to automatically find the optimized dead time across the entire operating range. It detects the change of slew rate of the HS node voltage. During a switching transition, the slew rate rises up first and then drops back to zero. A slew rate detector is used to detect the moment when the slew rate drops below a pre-defined threshold. A slew done event is only detected when the slew rate during dead time crosses the threshold and then drops back below the threshold. If the slew rate is lower than the threshold (that is, minimal detectable slew rate) during the whole dead time period, no slew done is detected. This is to prevent the misdetection due to noise on the HS node voltage. If slew done is not detected, maximum dead time is used.

Because of the natural symmetric operation of LLC, only the dead time between high-side MOSFET turn off and low-side MOSFET turn on is determined by the slew rate detector. This dead time is copied and then applied to the dead time between low-side MOSFET turn off and high-side MOSFET turn on.

7.3.9 Protections

7.3.9.1 ZCS Region Prevention

The capacitive region is an LLC operating region in which the voltage gain increases when the switching frequency increases. It is also called the ZCS region. Avoid capacitive mode operation for two reasons:

- The feedback loop becomes positive feedback in the capacitive region
- The MOSFET can be damaged because of body diode reverse recovery

The capacitive region detection is done by checking the resonant current polarity at HSON or LSON falling edge. If the resonant current is positive at LSON falling edge, or negative at HSON falling edge, the ZCS signal in the waveform generator is turned high. The ZCS signal stays high until ZCS is cleared at the next HSON or LSON falling edge.

If ZCS is detected, the next gate is turned on at the next IPolarity flip event when the resonant current becomes inductive again. The IPolarity flip indicates that the capacitive operation cycle has already passed. The resonant current reverses direction and begins to discharge the switch node. In this stage, the body diode is no longer conducting and it is allowed to turn on the next gate. If there is a slew done event detected, it suggests that the opposite body diode must not be conducting and the next gate is turned on as well. If neither the IPolarity flip event or slew done event is detected, the next gate is turned on by the maximum dead time timer expiration. During a ZCS event, the maximum dead time is changed to 150µs.

ZCS typically occurs when the LLC operates at heavy load condition and the switching frequency is too low. Therefore, when ZCS is detected, the LL/SS pin is pulled low through a diode to ground and the system enters a "ZCS soft start" process. The switching frequency is forced to ramp up for the system to recover from ZCS. The details of the "ZCS soft start" are described in the [Section 7.4.3.1](#) section. As the ZCS detection relies on the resonant current polarity detection, if LLC operates at very light load condition, the magnitude of the resonant current can be very small and there can be chances that the resonant current polarity detection can be distorted by the switching noise. To prevent the nuisance ZCS detection at light load condition, ZCS is disabled at light load condition by utilizing the burst mode control. The details are described in the [Section 7.4.3](#) section.

Below is the flow chart of the capacitive region prevention algorithm and the timing diagram of a ZCS event:

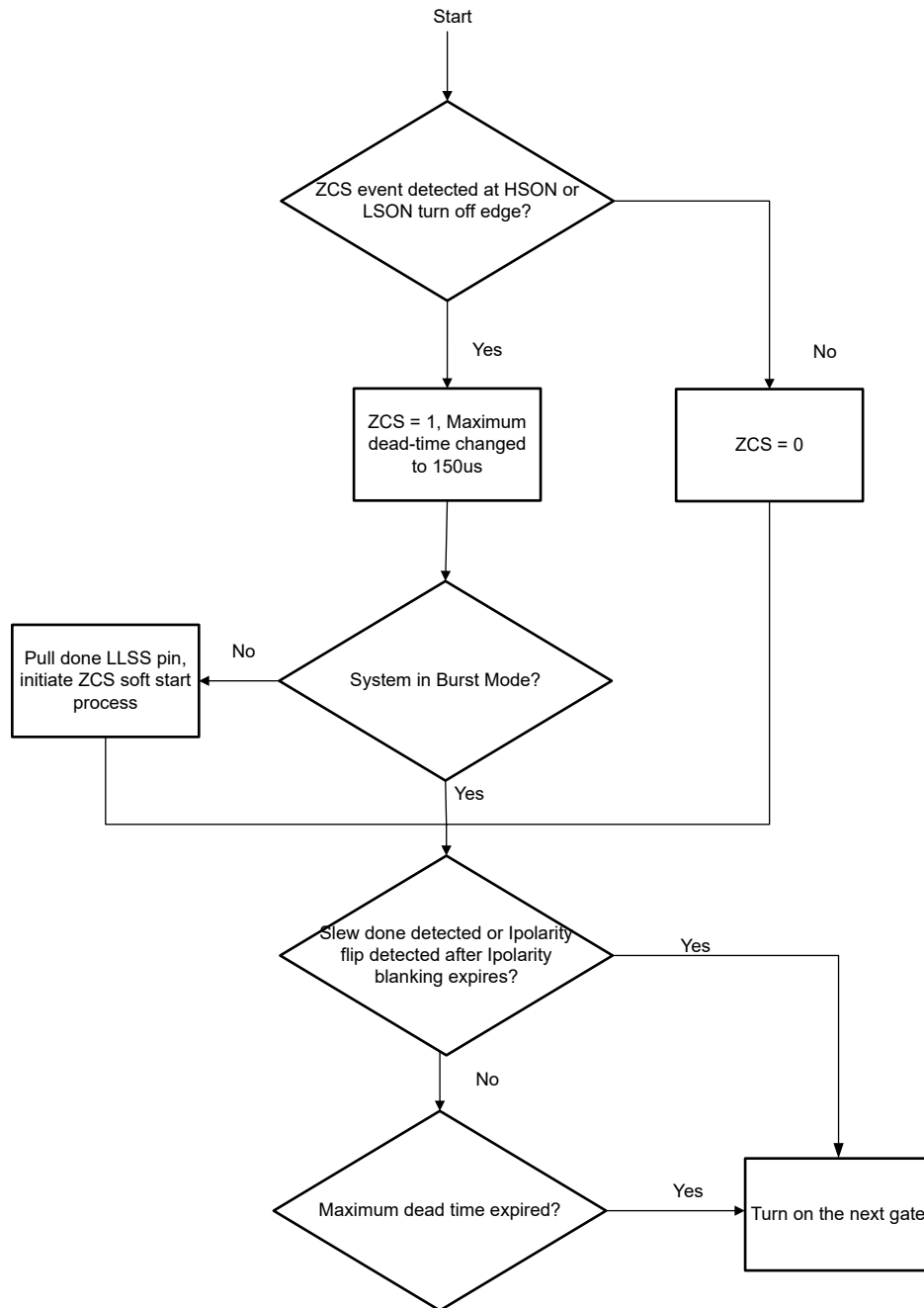


Figure 7-11. ZCS Prevention Algorithm Flow Chart

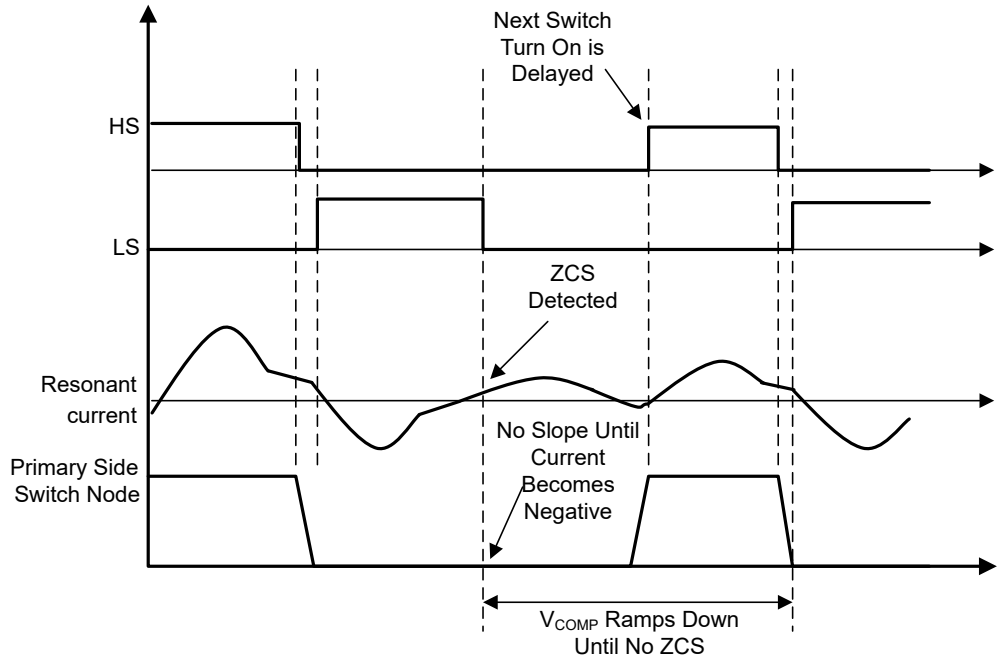


Figure 7-12. Timing Diagram of a ZCS Event

7.3.9.2 Over Current Protection (OCP)

There are three levels of OCP:

1. OCP1: peak current protection (highest threshold)
 - a. Fault action: If ISNS is higher than OCP1 threshold for 4 consecutive switching cycles, the switching stops. The system enters FAULT state, and waits for 1s and then re-enters the startup state.
2. OCP2: average input current protection (high threshold)
 - a. Fault action: If sensed ISNS average value is above the threshold for 2ms, the switching stops. The system enters FAULT state, and waits for 1s and then re-enters the startup state.
3. OCP3: average input current protection (low threshold)
 - a. Fault action: If sensed ISNS average value is above the threshold for 50ms, the switching stops. The system enters FAULT state, and waits for 1s and then re-enters the startup state.

Section 7.3.5 provides information regarding the circuit block diagram.

7.3.9.3 Bias Winding Over Voltage Protection (BWOVP)

This is typically used for output over voltage protection when the transformer has a bias winding. The output over voltage trip point can be set by configuring the voltage divider on the BW pin. When the BW OVP comparator is high for 5 consecutive switching cycles, the switching stops. The system enters fault state, and waits for 1s and then re-enters the startup state.

7.3.9.4 Input Under Voltage Protection (VINUVP)

This is the input under voltage protection. The trip point can be set by configuring the voltage divider on the BLK pin. If the BLK voltage drops below BLKStop, switching stops immediately. The system enters FAULT state, and waits for 1s and then re-enters the startup state.

7.3.9.5 Input Over Voltage Protection (VINOVP)

This is the input over voltage protection. This feature only exists in some device versions. If the BLK voltage rises above $V_{BLKOVPRise}$, switching will stop immediately. The system enters FAULT state, and waits for 1s and then re-enters the startup state if BLK voltage falls below $V_{BLKOVPRise}$.

7.3.9.6 Boot UVLO

This is the high-side gate driver UVLO. When (HB – HS) voltage is less than the threshold, the high-side gate output shuts down. The system does not enter FAULT state.

7.3.9.7 RVCC UVLO

This is the regulated 13V UVLO. When RVCC voltage is less than the threshold, both the high-side gate output and the low-side gate output turns off immediately. The system enters FAULT state, and waits for 1s and then re-enters the startup state.

7.3.9.8 Over Temperature Protection (OTP)

This is the device over temperature protection. When OTP threshold is exceeded, the switching stops. The system enters FAULT state, and waits for 1s and then re-enters the startup state if the temperature is back below the OTP threshold.

7.4 Device Functional Modes

7.4.1 High Voltage Start-Up

UCC256402 and UCC256404 uses a self bias start-up scheme, thus eliminating the need for a separate auxiliary supply. When AC power is first plugged in, the PFC and LLC are both off. The internal JFET on the HV pin is enabled and starts to deliver current from a source connected from the HV pin to the VCC capacitor. The charge current is small when VCC pin voltage is below $V_{CCShort}$, and then becomes larger when VCC pin voltage is above $V_{CCShort}$. Once the VCC pin voltage exceeds its $V_{CCStartSwitching}$ threshold, the current source is turned off and RVCC is enabled to turn on the PFC. When the PFC output voltage reaches a certain level, the LLC is turned on. When the LLC is operating and the output voltage is established, the bias winding supplies current for both the PFC and the LLC controller devices.

UCC256403 does not include a high voltage start-up feature and requires an external auxiliary supply to power on the IC. Ground the HV pin when using the UCC256403.

7.4.2 X-Capacitor Discharge

X-capacitors used in EMC filters on the AC side of the diode bridge rectifier must have a method to allow them to discharge down to a reasonable voltage within a specific amount of time. This is to confirm that voltage does not remain present on the pins of the AC plug indefinitely after it is physically removed from the AC power.

Typically, discharge resistors are provided in parallel with the X-capacitors to provide this discharge path, but these resistors then lead to fixed standing power loss as long as the power supply is connected to AC power, and can be significant in the context of achieving very low standby power.

For every 100nF of capacitance, add a maximum bleed resistor of 10MΩ in parallel. For a typical 60W to 100W power supply with a typical capacitance of 330nF, this requires 3MΩ of discharge resistance. At nominal high line 230V, these resistors dissipate 17.63mW of standing power loss. Thus it is necessary to find alternative ways to discharge the X-capacitors using switched discharge paths to avoid the static standing loss.

There are several standards for X-capacitor discharge. IEC60950 and IEC60065 requires that the discharge time constant is less than 1s. IEC62368 requires that after 2 seconds of AC unplug, the remaining voltage on the X-capacitor is less than 60V (for 300nF or more capacitance). UCC25640x uses an active discharge scheme to support the fast discharge of up to 5μF X-capacitance, for device variants that has X-capacitor discharge.

To meet the requirements of the standards, AC disconnect events must be detected. UCC25640x detects AC disconnect by monitoring the AC zero crossings through the HV pin. When AC is present, there is two AC zero crossings in one line cycle. When AC is disconnected, there is no zero crossings for an extended period of time. [Figure 7-13](#) shows the rectified AC waveform. In the figure, the AC is disconnected at the peak of the last half AC cycle. In reality, it can be disconnected anywhere within a switching cycle.

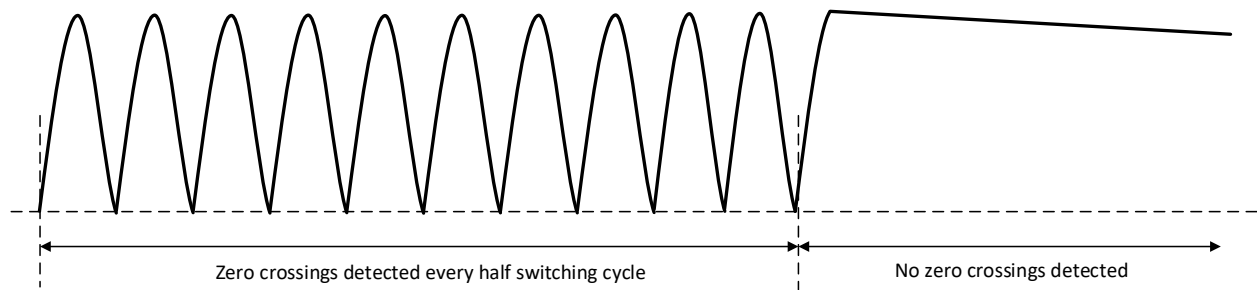


Figure 7-13. AC Disconnect Waveform

To detect the zero crossings reliably as well as save power consumption, a staircase test current generates every 700ms. When there are 4 zero crossings missing in a row at the highest test current setting, AC disconnect is confirmed and the $I_{XCapDischarge}$ current source enables. The waveform below shows the staircase current waveform:

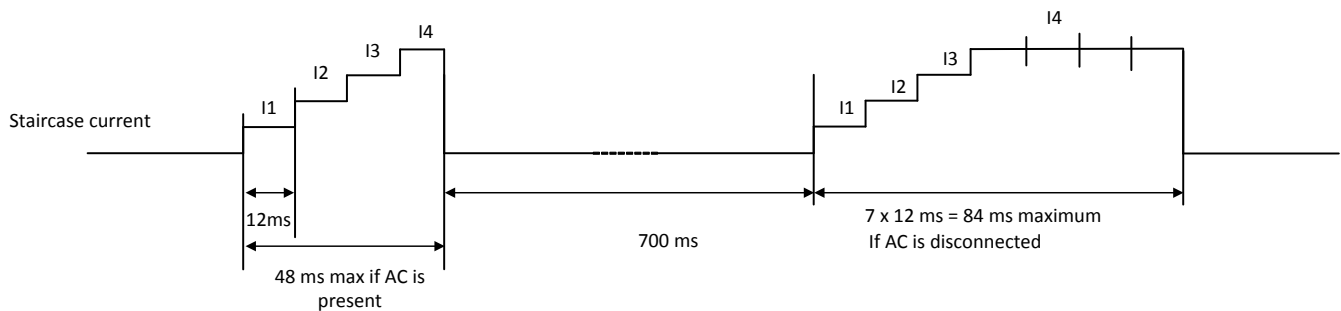


Figure 7-14. Staircase Test Current for X-Capacitor Discharge

The test current is required for reliable AC zero-crossing sensing. In short, this is because the leakage current in the AC bridge rectifier diodes affects the zero-crossing detection at very light load. The added test current on the HV pin overcomes the leakage current and make sure that AC zero-crossing is detected on the HV pin. If one zero-crossing is detected during any test current stage, it means that AC is not disconnected. The test current shuts off immediately and the system goes to the 700ms no test current stage.

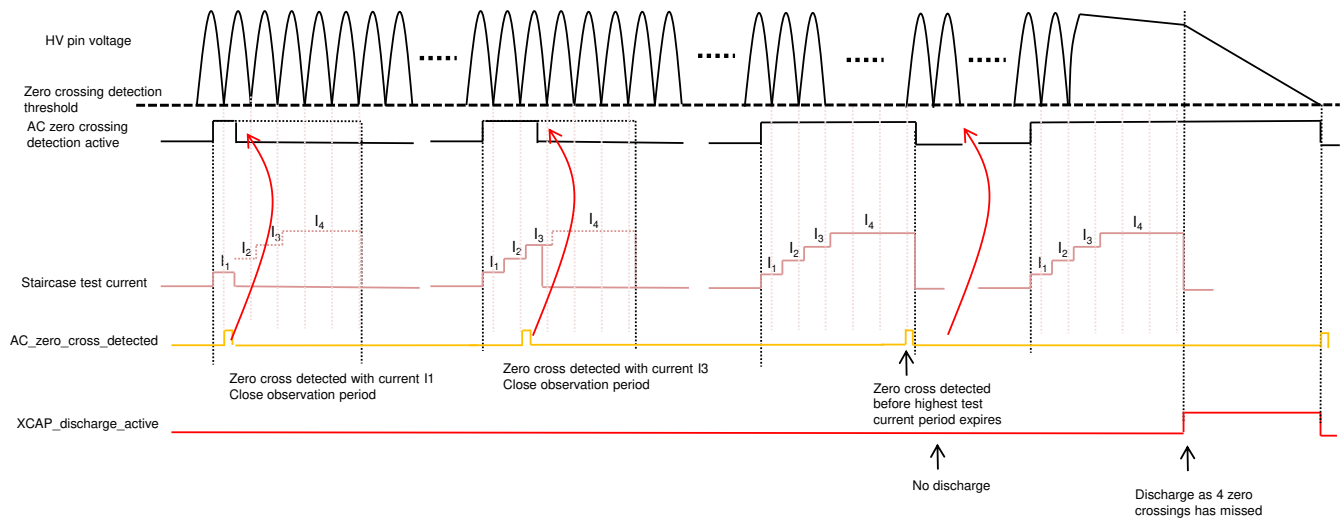


Figure 7-15. Different Staircase Current Waveforms

Figure 7-15 shows different staircase current waveforms. The last waveform shows the AC disconnect is detected and X-capacitor discharge current is enabled. The X-capacitor discharge current is enabled for 350ms.

AC zero-crossing function is available in all operation modes and available all the time. Figure 7-16 shows the flow chart of AC zero-crossing detection and X-capacitor discharge. The zero-crossing test starts 12ms after HV startup is completed. The discharge current $I_{XCapDischarge}$ is created by turning on the JFET and enabling a current source from JFET source to GND. During a fault restart process, HV startup is higher priority, so that the JFET is connected to VCC. A zero-crossing test current is sent out 12ms after HV startup is completed, regardless of whether the detection idle timer has expired.

In some of the device variants, the X-capacitor discharge feature is disabled.

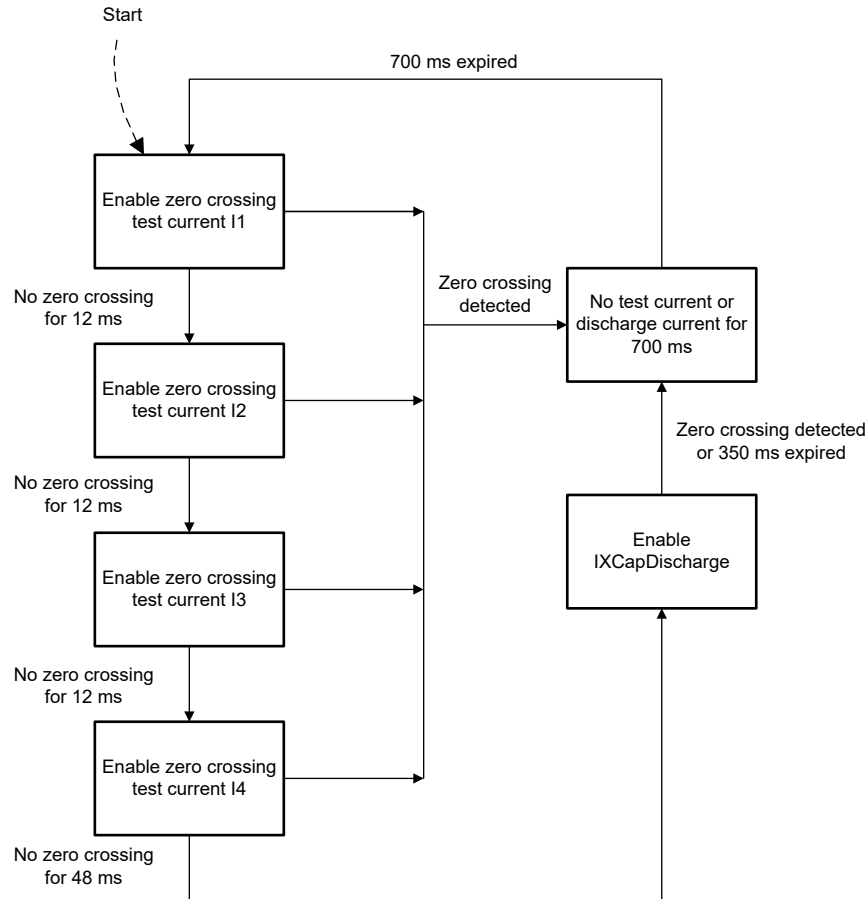


Figure 7-16. AC ZCD and X-Capacitor Discharge Flow Chart

7.4.3 Burst Mode Control

The efficiency of an LLC converter power stage drops rapidly with falling output power. To maintain reasonable light load efficiency it is necessary to operate the LLC converter in burst mode. In this mode the LLC converter operates at relatively high power for a short burst period and then switching is stopped for a time period. During the burst period excess charge is transferred to and stored in the output capacitor. During the burst off period this stored charge is used to supply the load current. The burst mode operation is critical to meet strict standby power consumption requirements. A challenge with burst mode operation is the audible noise performance. Due to the need to stop switching for certain time, there is a pattern of switching pulses with frequencies that fall within the audible frequency range from 20Hz to 20kHz. Some device variants of UCC25640x includes a burst mode with soft on and soft off periods at the first few and last few switching pulses, minimizing the audible noise during standby operation.

Figure 7-17 describes the timing diagram of the burst mode operation. Two burst mode thresholds are used (BMT_H for burst mode exit and BMT_L for burst mode entry). The details of how to program these two thresholds

are described in [Section 7.4.3.1](#) section. The FBreplica from the FB chain is compared with the two thresholds, and determines the burst mode operation.

- At t_1 , FBreplica is below BMT_L . The system enters burst mode and stops switching immediately. During the burst off period, UCC25640x disables some internal blocks to save power consumption.
- At t_2 , FBreplica is above BMT_H . The system starts to switch again, and this period is referred to as the burst on period. During burst on period, the control effort V_{comp} sent to the VCR comparator is the higher value of FBreplica and BMT_L . For the first switching pattern after the system enters burst mode, there is no burst soft on.
- At t_3 , FBreplica falls below BMT_L again. Switching does not stop until it reaches the predefined number (N_{burst}) of a burst packet. The V_{comp} still selects the higher value of FBreplica and BMT_L . For the last 7 switching cycles, soft off applies (only 3 soft on/off steps are in [Figure 7-17](#) for conceptual introduction). The V_{comp} is a fraction of the higher value between FBreplica and BMT_L . The number of fractions for different switching cycles are described in [Table 7-1](#). For burst soft off, it starts from step 7 and ramps down. After it reaches step 1, soft off steps are completed and the system enters burst off period. This helps to achieve slow ramping down of the LLC transformer current. For burst soft on, it reverses the direction by starting from step 1 and ends at step 7. If FBreplica becomes greater than BMT_L before the soft off steps are completed, the burst soft off ends immediately and the system transitions to burst soft on. In this condition, the soft on step starts from the step where soft off ends at, to confirm a smooth transition between soft off and soft on.
- At t_4 , FBreplica is greater than BMT_L . The system enters burst on period, and since this is not the first burst on period, there is soft on period at the first 7 switching cycles. The fraction of V_{comp} to the higher value of FBreplica and BMT_L is also described in [Table 7-1](#). After burst soft on steps are completed, V_{comp} uses the higher value of FBreplica and BMT_L until it reaches burst soft off periods.
- At t_5 , FBreplica is greater than BMT_L again after another burst off period. This time the difference is that FBreplica is greater than BMT_H at t_6 , when the burst soft on steps are not completed yet. The burst soft on immediately terminates, so that V_{comp} can follow the FBreplica to confirm a quick system response during a load transient from burst mode operation to out-of-burst mode operation.

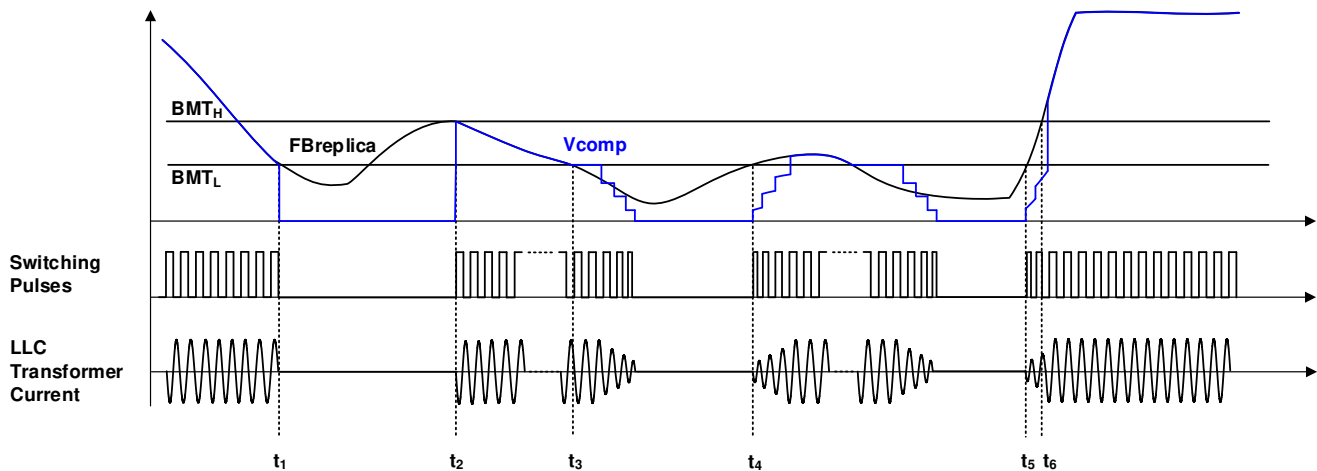


Figure 7-17. Burst Mode Switching Pattern

Table 7-1. Burst Mode Soft On and Soft Off V_{comp} Control

BURST SOFT ON AND SOFT OFF STEP	FRACTION USED FOR REDUCED V_{comp} DURING SOFT ON
1	1/3
2	9/21
3	11/21
4	13/21
5	15/21
6	17/21

Table 7-1. Burst Mode Soft On and Soft Off V_{comp} Control (continued)

BURST SOFT ON AND SOFT OFF STEP	FRACTION USED FOR REDUCED V_{comp} DURING SOFT ON
7	19/21

The HHC control makes the implementation of the burst soft on and soft off very straight forward. Due to the frequency control portion in HHC, changing the V_{comp} can directly impact the LLC switching frequency to control the resonant current magnitude within switching cycles. Also the last pulse of each burst on period is turned off when the VCR node voltage equals the common mode voltage VCM. In HHC control, this is approximately equivalent to resonant capacitor voltage equal to $V_{IN}/2$. This operation keeps the resonant capacitor voltage to approximate $V_{IN}/2$ for each burst off period, thus enabling the burst pattern to settle as soon as possible during the burst on period.

As described in [Section 7.3.9.1](#), to avoid nuisance ZCS detection at light load condition, ZCS is disabled at light load condition. This is achieved by using the BMT_H threshold. When FBreplica is below BMT_H , indicating a light load operating condition, ZCS detection is disabled. When FBreplica is above BMT_H , ZCS detection resumes.

Some device variants disables the burst soft on and soft off feature, for applications that have less concern about audible noise, but want smaller output ripple during burst mode. A smaller burst packet size is also used. The timing diagram of the burst mode operation for when burst soft on and soft off is disabled is described in [Figure 7-18](#).

- At t_1 , FBreplica is below BMT_L . The system enters burst mode and stops switching immediately.
- At t_2 , FBreplica is above BMT_H . The system starts to switch again, and enters burst on period. The control effort V_{comp} sent to the VCR comparator is the higher value of FBreplica and BMT_L .
- At t_3 , FBreplica falls below BMT_L again. Switching does not stop until it reaches the predefined number (N_{burst}) of a burst packet. If switching reaches the N_{burst} before FBreplica falls below BMT_L again, system continues to deliver burst packet until FBreplica is below BMT_L .
- At t_4 , FBreplica is greater than BMT_L . The system enters burst on period without soft on. So the control effort V_{comp} is the higher value of FBreplica and BMT_L .
- At t_5 , FBreplica is greater than BMT_L again after another burst off period. The control effort V_{comp} follows FBreplica. At t_6 , FBreplica becomes above BMT_H , V_{comp} still follows FBreplica. If FBreplica remains above BMT_H more than N_{burst} switching cycles, system exits burst mode.

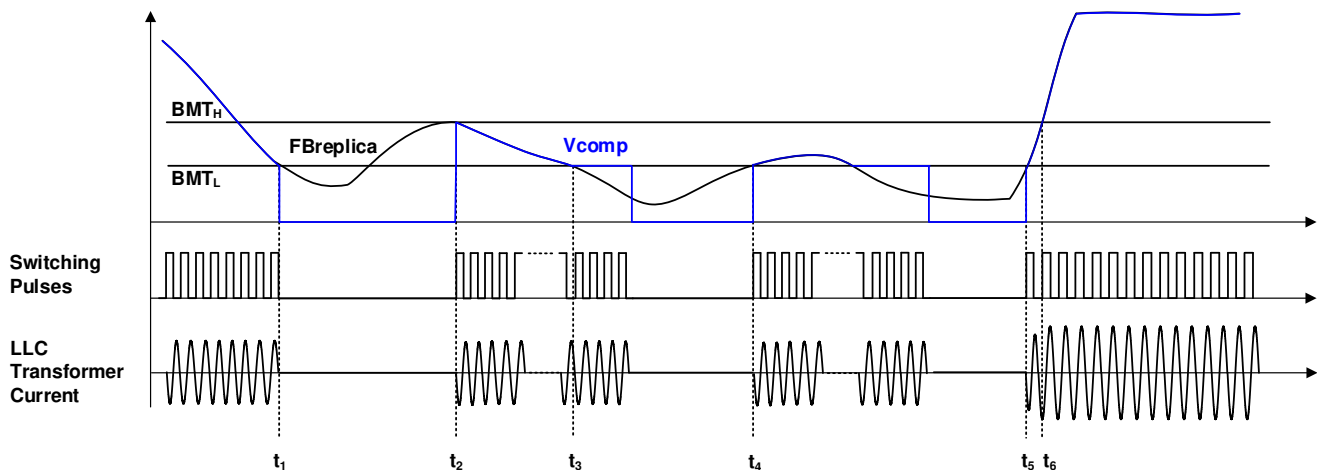


Figure 7-18. Burst Mode Switching Pattern when Soft On and Soft Off is Disabled

UCC25640x can also disable the burst mode by changing the BW pin resistance, as described in [Section 7.4.3.2](#). When burst mode is disabled, the switching does not stop even when FBreplica becomes lower than BMT_L . The pick higher block still works by picking the higher value of BMT_L and FBreplica for the control effort V_{comp} . In this case, BMT_L limits the maximum switching frequency of LLC.

When burst mode is disabled, FB_{replica} must be higher than BMT_L at steady state. Otherwise, LLC output voltage loses regulation as it continues deliver more energy than what is demanded from the feedback. For a transient period, it is ok for FB_{replica} to be lower than BMT_L.

7.4.3.1 Soft-Start and Burst-Mode Threshold

The soft-start programming and burst mode threshold programming are multiplexed on the pin LL/SS. In addition, when ZCS region operation occurs, this pin pulls down to ground through a diode to increase the switching frequency. Figure 7-19 shows the pin block diagram.

Figure 7-20 shows the timing diagram of the LL/SS pin programming and includes five phases:

- SS pull low phase - LL/SS pin is internally pulled low with a typical 1.2kΩ resistor to ground.
- SS initial voltage program phase - The internal pull low is released. As shown in Figure 7-19, LL/SS pin is typically connected with a resistor divider from RVCC and a capacitor to ground. When the internal pull low circuit is released, LL/SS pin voltage can be charged up depending on the external resistor and capacitor. This phase ends when charge boot stage is completed and it has a fixed time of $t_{SSInitVolPrgm}$.
- Soft start phase - An internal constant current source charges the soft-start capacitor right after the charge boot stage, and ends when FB_{replica} becomes lower than the LL/SS pin voltage. During this phase, LL/SS pin voltage is used as the control effort V_{comp} . The slow ramp up of LL/SS pin helps the LLC operate at a higher switching frequency when the output voltage is not established yet during startup. This can avoid the large inrush current during startup.
- BMT_L settling phase - When the soft-start phase is completed, LL/SS pin is used for burst mode threshold programming. As described in Section 7.4.3, two burst mode thresholds are used. During this phase, BMT_H is fixed at either 0.6V or 1.2V, if BW option 7 is selected. BMT_L is also fixed which is determined by the programmed ratio of BMT_L/BMT_H. The typical duration of this phase is 600us.
- BMT_L and BMT_H programming/setting phase - LL/SS pin is buffered at 3.5V during this phase. Depending on the resistors connected to the pin, LL/SS pin can either sink or source current. If LL/SS pin sinks current, the current is internally mirrored to flow through R_{LL}, and the voltage on R_{FB} is the programmed voltage of BMT_H. If LL/SS pin sources current, the programmed voltage of BMT_H is set to minimal. If the programmed voltage of BMT_H is different from the initial voltage, BMT_H ramps to the target value at a refresh frequency of every 200us. The slow refresh frequency makes sure that BMT_H does not change due to the noise on LL/SS pin. BMT_L follows the change of BMT_H based on the programmed ratio of BMT_L/BMT_H.

The programmability of the SS initial voltage provides a freedom to limit the maximum switching frequency during startup. This helps to prevent hard switching due to excessively high switching frequency. For applications that require very high switching frequency during startup, an option is also provided to disable the SS initial voltage programming through BW pin, as described in Section 7.4.3.2. If selecting this option, the LL/SS pin continues pull low with the internal 1.2kΩ resistor during the SS initial voltage program phase.

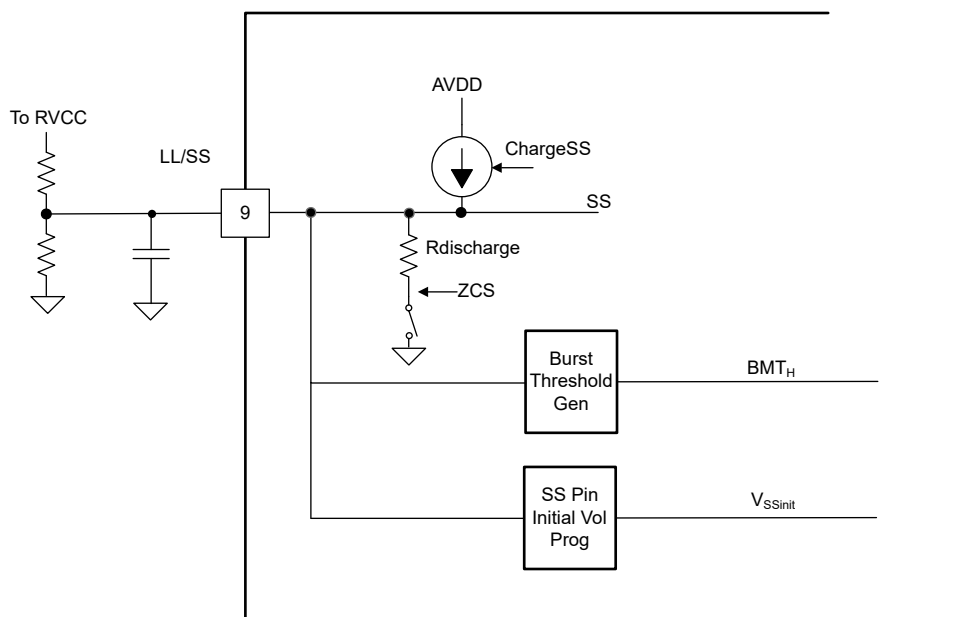


Figure 7-19. LL/SS Block Diagram

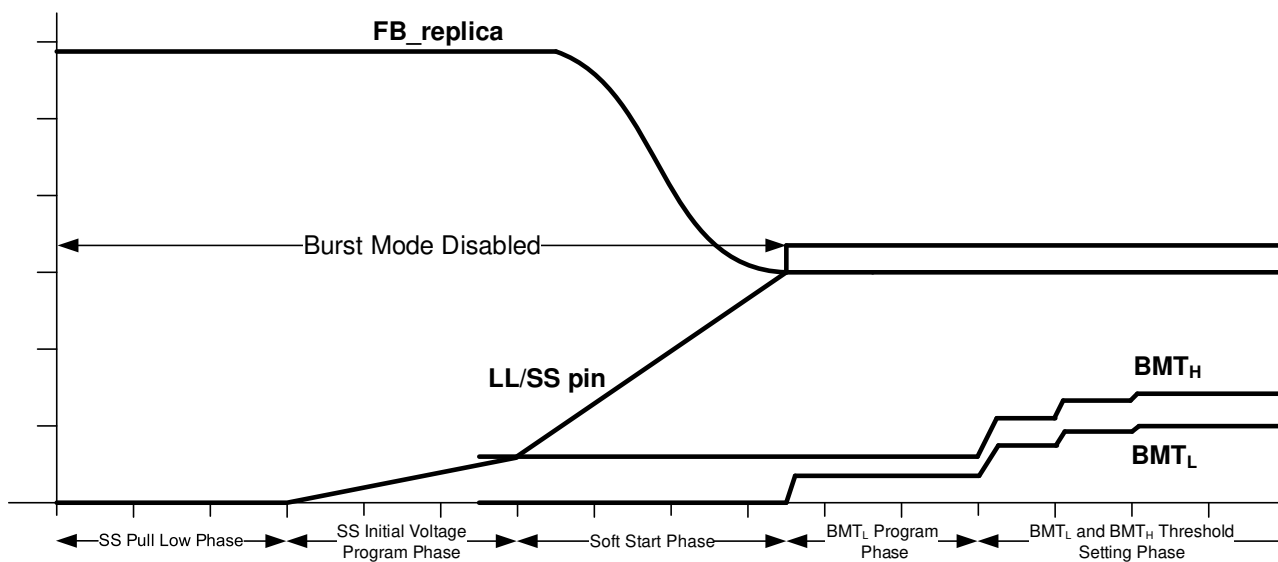


Figure 7-20. Timing Diagram of LL/SS Pin Programming

7.4.3.2 BMT_L/BMT_H Ratio Programming

As described in [Section 7.3.7](#), BW pin is multiplex for BMT_L/BMT_H ratio programming. The programming phase occurs only once before startup. After that, the BMT_L/BMT_H ratio is then fixed, until system restarts after a fault or power recycle. The programming phase occurs right before soft start begins. It sources a constant current and measures the voltage on the pin. Depending on the measured pin voltage, different ratio of BMT_L/BMT_H is selected as listed in [Table 7-2](#). [Section 6.5](#) lists the required BW equivalent resistance.

Other than selecting different BMT_L/BMT_H ratios, the option 5 also disables the LL/SS pin initial voltage program phase during startup, and the option 7 disables the burst mode.

Table 7-2. BMT_L/BMT_H Ratio Programming

OPTION	BMT _L /BMT _H
1	0.95

Table 7-2. BMT_L/BMT_H Ratio Programming (continued)

OPTION	BMT _L /BMT _H
2	1
3	0.9
4	0.8
5	0.6 (LL/SS pin initial voltage programming disabled)
6	0.6
7	0.4 (Burst Mode Disabled)

7.4.4 System State Machine

Below is an overview of the system states sequence:

The state transition diagram starts from the un-powered condition of UCC25640x. For device variants that has HV startup, as soon as the AC input is plugged in, the internal JFET of the HV pin is enabled and starts to deliver current from a source connected from the HV pin to the VCC capacitor. Once the VCC pin voltage exceeds its VCC_{StartSwitching} threshold, the system state changes to JFETOFF. For device variants which does not have HV startup feature, there is no JFETon state. Once VCC exceeds its VCC_{StartSwitching} threshold, the system state changes to JFETOFF. When the PFC output voltage reaches a certain level, the LLC is turned on. Before the LLC starts running, the LO pin is kept high to pull the HS node of the LLC bridge low, thus allowing the capacitor between the HB and HS pins to be charged from VCC through the bootstrap diode. UCC25640x remains in the CHARGE_BOOT state for a certain time to establish the boot capacitor is fully charged. When the LLC output voltage reaches a certain level, both PFC and LLC controllers get power from the LLC transformer bias winding. When the load drops below a certain level, the LLC operates in burst mode.

Fault conditions encountered by UCC25640x causes normal operation to stop, or pause for a certain period of time followed by an automatic re-start. This is to confirm that while a persistent fault condition is present, it is not possible for the temperature of UCC25640x controller or the power converter to rise as a result of the repeated re-start attempts.

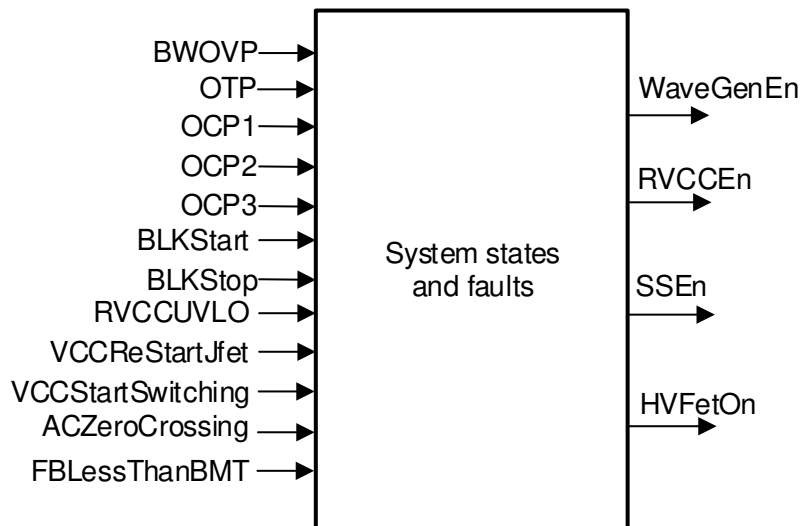


Figure 7-21. Block Diagram of System State Machine

Table 7-3 summarizes the inputs and outputs of Figure 7-21.

Table 7-3. System State Machine Block Inputs and Outputs

SIGNAL NAME	I/O	DESCRIPTION
BWOVP	I	Output over voltage fault
OTP	I	Over temperature fault
OCP1	I	Peak current fault

Table 7-3. System State Machine Block Inputs and Outputs (continued)

SIGNAL NAME	I/O	DESCRIPTION
OCP2	I	Average current fault with 2ms timer
OCP3	I	Average current fault with 50ms timer
BLKStart	I	Bulk voltage is above start threshold
BLKStop	I	Bulk voltage is below stop threshold
RVCCUVLO	I	RVCC UVLO fault
VCCReStartJfet	I	VCC is below restart threshold
VCCStartSwitching	I	VCC is above start switching threshold
ACZeroCrossing	I	AC zero crossing is detected
WaveGenEn	O	Waveform generator enable
RVCCEn	O	RVCC enable
SSEn	O	Soft start enable
HVFetOn	O	Turn on or off JFET

Figure 7-22 shows the state machine and the description of the states and state transition conditions are in the tables below.

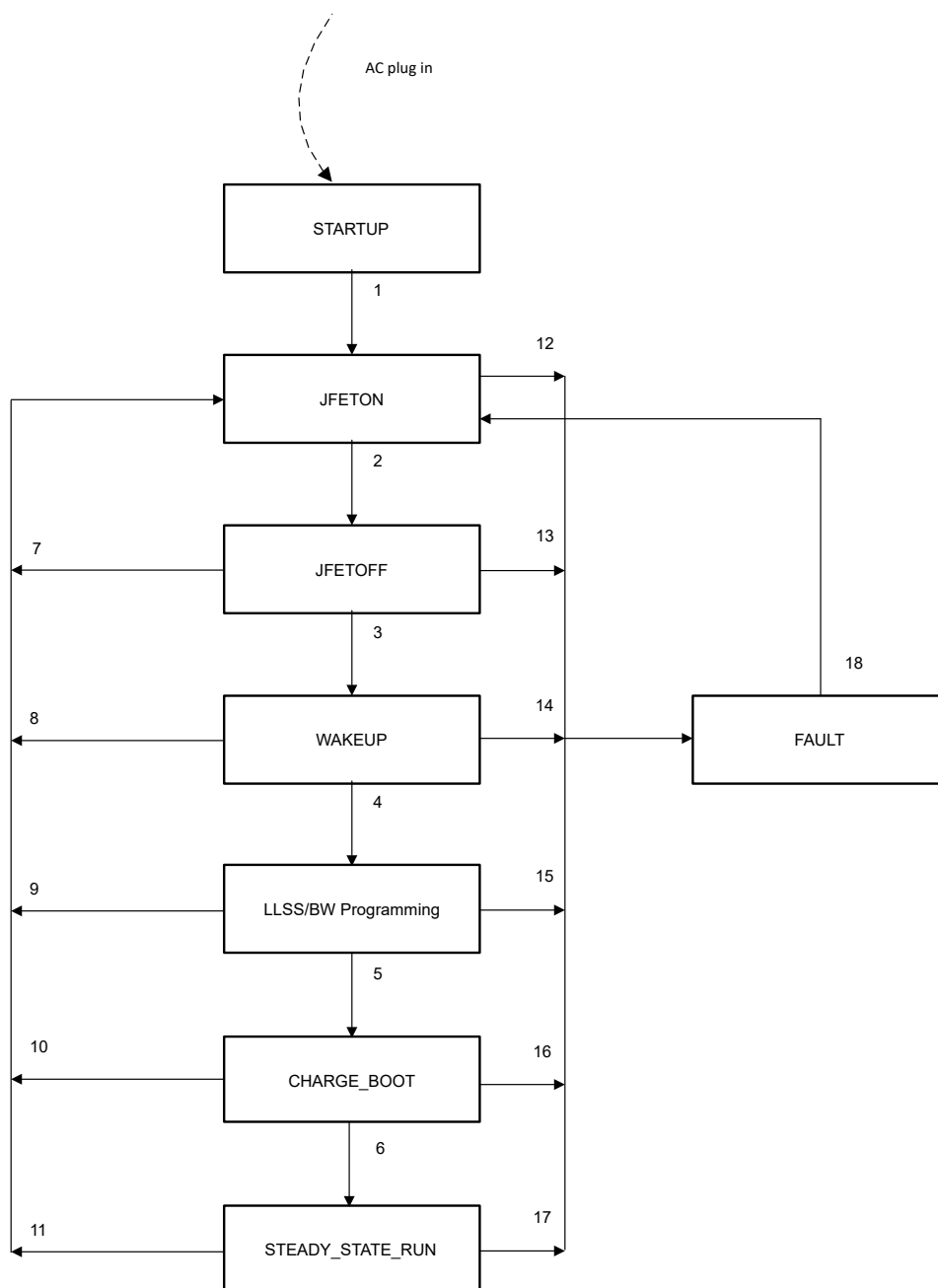


Figure 7-22. System State Machine Transition

Table 7-4. States in System State Machine

STATE	OUTPUT STATUS	DESCRIPTION
STARTUP	WaveGenEn = 0 RVCCEn = 0 SSEn = 0 HVFetOn = 0	This is the first state after AC input is plugged-in for the system to load trim.
JFETON	WaveGenEn = 0 RVCCEn = 0 SSEn = 0 HVFetOn = 1	In this state, the JFET is on. VCC is charged with a current source connected from HV pin. For device variants that does not have HV startup feature, this state does not exist.

Table 7-4. States in System State Machine (continued)

STATE	OUTPUT STATUS	DESCRIPTION
JFETOFF	WaveGenEn = 0 RVCCEn = 1 SSEn = 0 HVFetOn = 0	When VCC is higher than VCCStartSwitching threshold, the JFET is turned off and the system enters JFETOFF state. The regulated RVCC is turned on. If RVCC is supplied to PFC voltage supply pin, PFC soft start begins.
WAKEUP	WaveGenEn = 0 RVCCEn = 1 SSEn = 0 HVFetOn = 0	When BLK voltage reaches BLKStart level, the system enters WAKEUP state and stays in WAKEUP state for a short time for the analog circuits to wake up.
LLSS/BW Programming	WaveGenEn = 0 RVCCEn = 1 SSEn = 0 HVFetOn = 0	In this state, the system goes through the LL/SS pin and BW pin programming phase.
CHARGE_BOOT	WaveGenEn = 0 RVCCEn = 1 SSEn = 0 HVFetOn = 0	In this state, the BOOT capacitor is charged by turning on the low-side switch for a certain period of time. The programmed initial voltage is buffered to LL/SS pin.
STEADY_STATE_RUN	WaveGenEn = 1 RVCCEn = 1 SSEn = 1 HVFetOn = 0	In this state, the waveform generator is enabled. Soft start module is enabled. The LLC starts to soft start. When soft start is done, the system enters normal operation.
FAULT	WaveGenEn = 0 RVCCEn = 0 SSEn = 0 HVFetOn = 0	In fault state, the waveform generator is disabled to stop switching. The system will stay in FAULT state for 1s before re-start. The 1s timer allows the system to cool down and prevents frequent repetitive start ups in case of a persistent fault.

Table 7-5. System State Machine Transition Conditions

STATE TRANSITION CONDITION	DESCRIPTION
1	System ready (trim load done)
2	VCCStartSwitching = 1 VCCReStartJfet = 0
3	BLKStart = 1 BLKStop = 0 RVCCUVLO = 0
4	BLKStart = 1 BLKStop = 0 RVCCUVLO = 0 FBLessThanBMT = 0
5	LLSS/BW programming done
6	Charge boot done
7	VCCReStartJfet = 1
8	VCCReStartJfet = 1
9	VCCReStartJfet = 1
10	VCCReStartJfet = 1
11	VCCReStartJfet = 1
12	OTP = 1
13	OTP = 1
14	OTP = 1
15	OTP = 1
16	OTP = 1
17	OTP = 1 or BLKStop = 1 or BWOVP = 1 or OCP1 = 1 or OCP 2 = 1 or OCP3 = 1 or RVCCUVLO = 1
18	1s pause time out

Figure 7-23 and Figure 7-24 show the most commonly used state transition (assuming no faults during start up states so all the states are captured in the timing diagram). Many different ways of state transitions can happen according to the state machine, but are not captured in this section.

In Figure 7-24, a normal start up procedure is shown. The system enters normal operation and then a fault (OCP, OVP, or OTP) happens.

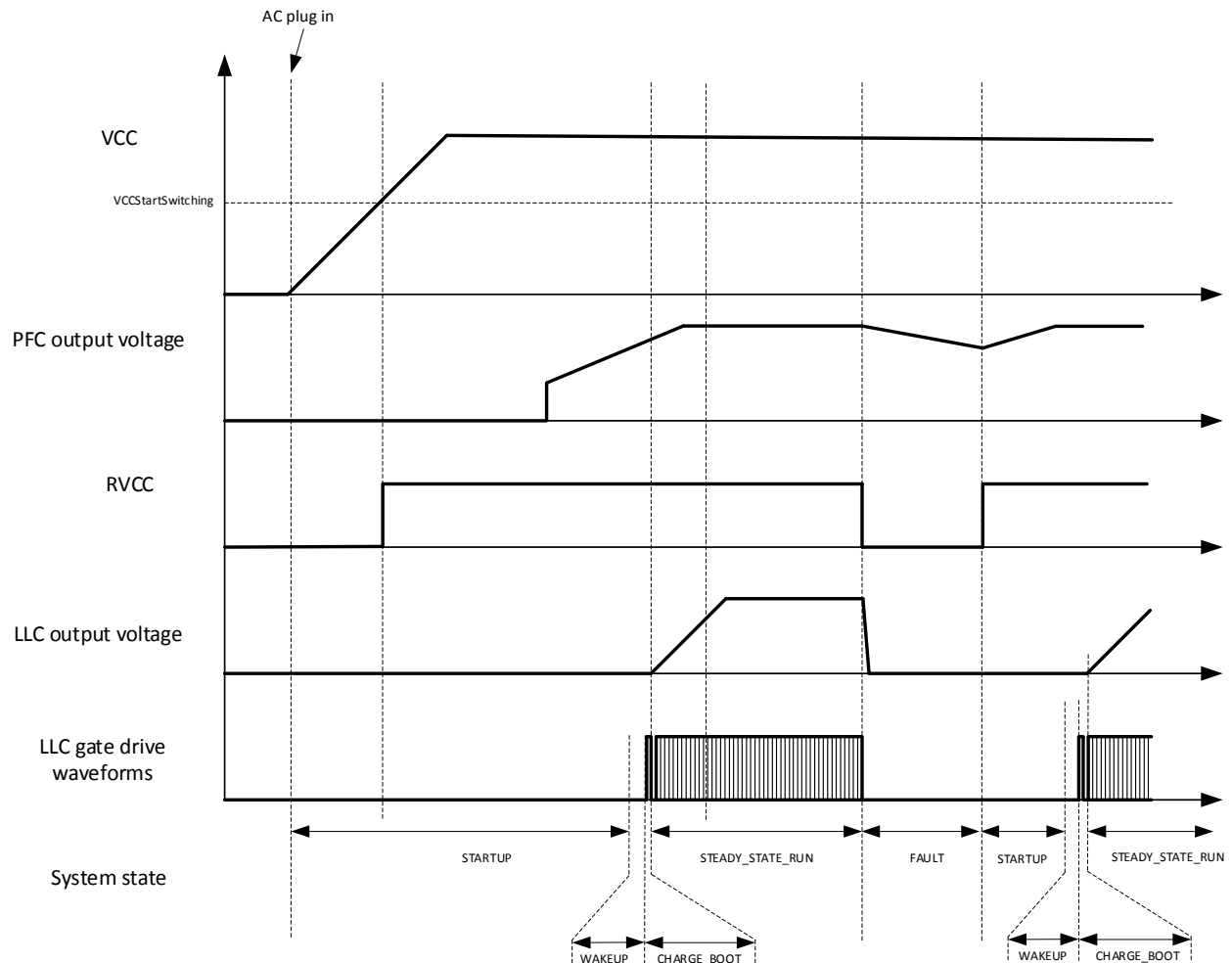


Figure 7-23. Timing Diagram of System State Machine for UCC256403

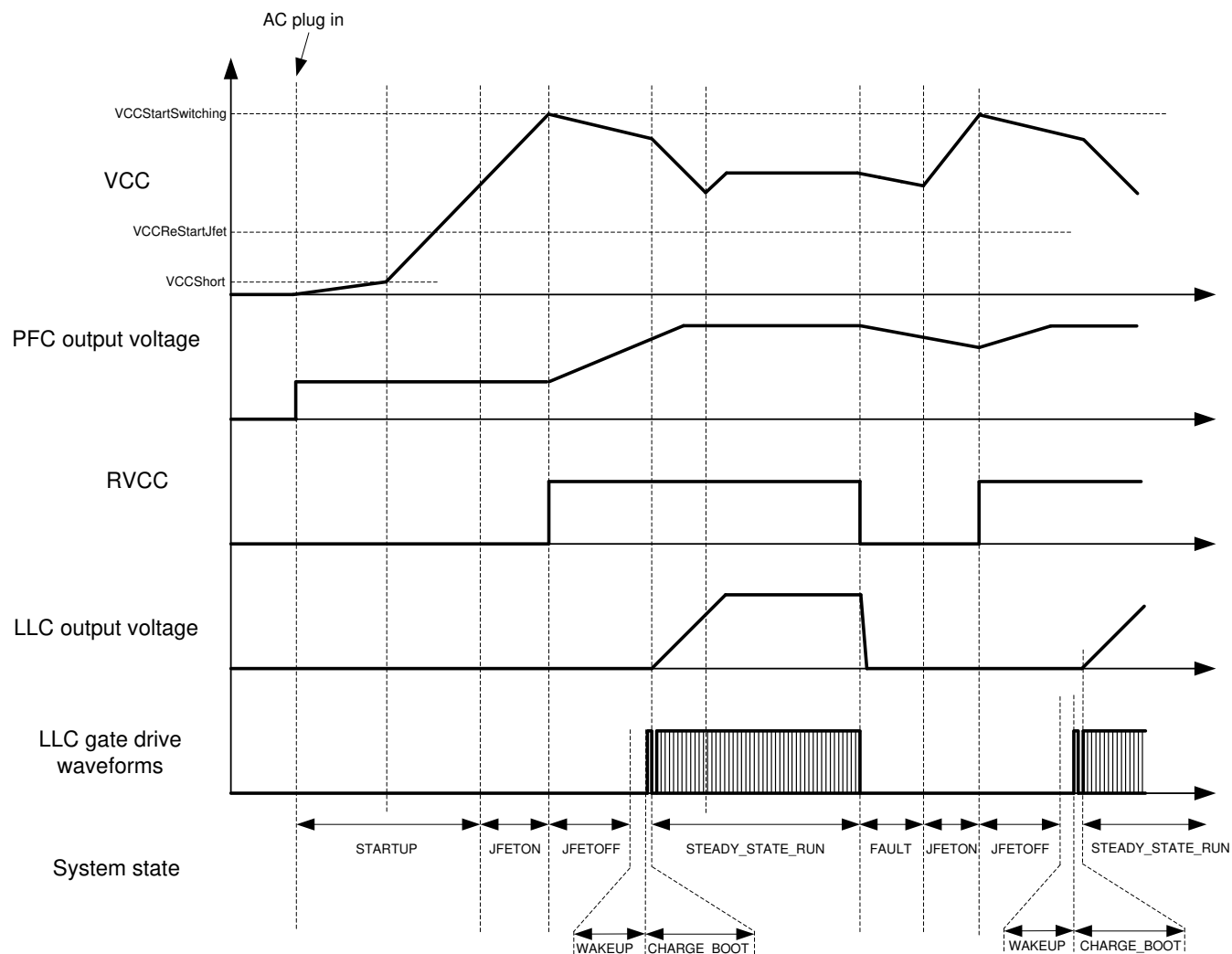


Figure 7-24. Timing Diagram of System State Machine for UCC256402 and UCC256404

8.2.1 Design Requirements

Table 8-1 lists the design specifications.

Table 8-1. System Design Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS					
DC Voltage range		365	390	410	VDC
AC Voltage range		85		264	VAC
AC Voltage frequency		47		63	Hz
Input DC UVLO On			365		VDC
Input DC UVLO Off			315		VDC
OUTPUT CHARACTERISTICS					
Output voltage, VOUT	No load to full load		12		VDC
Output load current, IOUT	360VDC to 410VDC			15	A
Output voltage ripple	390VDC and full load = 10A		120		mVpp
SYSTEMS CHARACTERISTICS					
Resonant Frequency			100		kHz
Peak efficiency	390VDC		92		
Operating temperature	Natural convection		25		°C

8.2.2 Detailed Design Procedure

8.2.2.1 LLC Power Stage Requirements

Start the design by deciding the LLC power stage component values. The LLC power stage design procedure outlined here follows the one given in the TI technical article [Power Tips: Designing an LLC resonant half-bridge power converter](#). The technical article contains a full explanation of the origin of each of the equations used. The equations given below are based on the First Harmonic Approximation (FHA) method commonly used to analyze the LLC topology. This method gives a good starting point for any design, but a final design requires an iterative approach combining the FHA results, circuit simulation, and hardware testing. The TI application note [LLC Design for UCC29950](#) includes an alternative design approach.

8.2.2.2 LLC Gain Range

First, determine the transformer turns ratio by the nominal input and output voltages.

$$N_{PS} = \frac{V_{IN(nom)}/2}{V_{OUT(nom)}} = \frac{390/2}{12} = 16.25 \approx 16.5 \quad (5)$$

Then determine the LLC gain range $M_{G(min)}$ and $M_{G(max)}$. Assume there is a 0.5V drop in the rectifier diodes (V_f) and an additional 0.5V due to other losses (V_{loss}).

$$M_{G(min)} = N_{PS} \times \frac{V_{OUT(min)} + V_f}{V_{IN(max)}/2} = 16.5 \times \frac{12 + 0.5}{410/2} = 1.006 \quad (6)$$

$$M_{G(max)} = N_{PS} \times \frac{V_{OUT(max)} + V_f + V_{loss}}{V_{IN(min)}/2} = 16.5 \times \frac{12 + 0.5 + 0.5}{365/2} = 1.175 \quad (7)$$

8.2.2.3 Select L_n and Q_e

L_N is the ratio between the magnetizing inductance and the resonant inductance.

$$L_N = \frac{L_M}{L_R} \quad (8)$$

$$(9)$$

Q_E is the quality factor of the resonant tank.

$$Q_E = \frac{\sqrt{L_R/C_R}}{R_E} \quad (10)$$

In this equation, R_E is the equivalent load resistance.

Selecting L_N and Q_E values must result in an LLC gain curve, that intersects with $M_{G(\min)}$ and $M_{G(\max)}$ traces. The peak gain of the resulting curve must be larger than $M_{G(\max)}$. Details of how to select L_N and Q_E are not discussed here. They are available in the [UCC25640x Design Calculator](#).

In this case, the selected L_N and Q_E values are:

$$L_N = 6 \quad (11)$$

$$Q_E = 0.3 \quad (12)$$

8.2.2.4 Determine Equivalent Load Resistance

Determine the equivalent load resistance by [Equation 13](#).

$$R_E = \frac{8 \times N_{PS}^2}{\pi^2} \times \frac{V_{OUT(nom)}}{I_{OUT(nom)}} = \frac{8 \times 16.5^2}{\pi^2} \times \frac{12}{15} = 176.5\Omega \quad (13)$$

8.2.2.5 Determine Component Parameters for LLC Resonant Circuit

Before determining the resonant tank component parameters, select a nominal switching frequency (resonant frequency). In this design, 100kHz is the resonant frequency.

$$f_0 = 100\text{kHz} \quad (14)$$

Calculate the resonant tank parameters as the following:

$$C_R = \frac{1}{2\pi \times Q_E \times f_0 \times R_E} = \frac{1}{2\pi \times 0.3 \times 100\text{kHz} \times 176.5\Omega} = 30.0\text{nF} \quad (15)$$

$$L_R = \frac{1}{(2\pi \times f_0)^2 \times C_R} = \frac{1}{(2\pi \times 100\text{kHz})^2 \times 30.0\text{nF}} = 84.4\mu\text{H} \quad (16)$$

$$L_M = L_N \times L_R = 6 \times 84.4\mu\text{H} = 506.4\mu\text{H} \quad (17)$$

After the preliminary parameters are selected, find the closest actual component value that is available, re-check the gain curve with the selected parameters, and then run time domain simulation to verify the circuit operation.

The following resonant tank parameters are:

$$C_R = 30\text{nF} \quad (18)$$

$$L_R = 85\mu\text{H} \quad (19)$$

$$L_M = 510\mu\text{H} \quad (20)$$

Based on the final resonant tank parameters, the resonant frequency can be calculated:

$$f_0 = \frac{1}{2\pi\sqrt{L_R C_R}} = \frac{1}{2\pi\sqrt{85\mu\text{H} \times 30\text{nF}}} = 99.7\text{kHz} \quad (21)$$

Based on the new LLC gain curve, the normalized switching frequency at maximum and minimum gain are given by:

$$f_{N(Mgmax)} = 0.7 \quad (22)$$

$$f_{N(Mgmin)} = 1.0 \quad (23)$$

The maximum and minimum switching frequencies are:

$$f_{SW(Mgmax)} = 69.8\text{kHz} \quad (24)$$

$$f_{SW(Mgmin)} = 99.7\text{kHz} \quad (25)$$

8.2.2.6 LLC Primary-Side Currents

The primary-side currents are calculated for component selection purposes. The currents are calculated based on a 110% overload condition.

The primary side RMS load current is:

$$I_{OE} = \frac{\pi}{2\sqrt{2}} \times \frac{I_o}{n} = \frac{\pi}{2\sqrt{2}} \times \frac{1.1 \times 15\text{A}}{16.5} = 1.111\text{A} \quad (26)$$

The RMS magnetizing current at minimum switching frequency is:

$$I_M = \frac{2\sqrt{2}}{\pi} \times \frac{N_{PS}V_{OUT}}{\omega L_M} = \frac{2\sqrt{2}}{\pi} \times \frac{16.5 \times 12}{2\pi \times 64.8\text{kHz} \times 510\mu\text{H}} = 0.797\text{A} \quad (27)$$

The total current in resonant tank is:

$$I_R = \sqrt{I_M^2 + I_{OE}^2} = \sqrt{(1.111\text{A})^2 + (0.797\text{A})^2} = 1.367\text{A} \quad (28)$$

8.2.2.7 LLC Secondary-Side Currents

The total secondary side RMS load current is the current referred from the primary side current (I_{OE}) to the secondary side.

$$I_{OES} = N_{PS} \times I_{OE} = 16.5 \times 1.111\text{A} = 18.327\text{A} \quad (29)$$

In this design, the secondary side of the transformer has a center-tapped configuration. Calculate the current of each secondary transformer winding using:

$$I_{WS} = \frac{\sqrt{2} \times I_{OES}}{2} = \frac{\sqrt{2} \times 18.327\text{A}}{2} = 12.959\text{A} \quad (30)$$

The corresponding half-wave average current is:

$$I_{SAV} = \frac{\sqrt{2} \times I_{OES}}{\pi} = \frac{\sqrt{2} \times 18.327\text{A}}{\pi} = 8.250\text{A} \quad (31)$$

8.2.2.8 LLC Transformer

Use a bias winding is needed to use the HV self start-up function. It is recommended to design the bias winding so that the VCC voltage is greater than 13V.

The transformer can be built or purchased according to these specifications:

- Turns ratio: Primary : Secondary : Bias = 33 : 2 : 3
- Primary terminal voltage: 450V_{ac}
- Primary magnetizing inductance: $L_M = 510 \mu\text{H}$
- Primary side winding rated current: $I_R = 1.367\text{A}$
- Secondary terminal voltage: 36V_{ac}

- Secondary winding rated current: $I_{WS} = 12.959A$
- Minimum switching frequency: 69.8kHz
- Maximum switching frequency: 99.7kHz
- Insulation between primary and secondary sides: IEC60950 reinforced insulation

The minimum operating frequency during normal operation is calculated above. Please note that for some applications that operate as a wide input LLC where the PFC can be shut off in standby mode, the operating frequency can be much lower during heavy load shutdown and the LLC can operate at just above the ZCS boundary which is a lower frequency. The magnetic components in the resonant circuit, the transformer and resonant inductor, must be rated to operate at this lower frequency.

8.2.2.9 LLC Resonant Inductor

The AC voltage across the resonant inductor is the impedance multiplied by the current:

$$V_{LR} = \omega L_R I_R = 2\pi \times 69.8\text{kHz} \times 85\mu\text{H} \times 1.367A = 50.946V \quad (32)$$

The inductor can be built or purchased according to the following specifications:

- Inductance: $L_R = 85\mu\text{H}$
- Rated current: $I_R = 1.367A$
- Terminal AC voltage: 50.946V
- Frequency range: 69.8kHz to 99.7kHz

Please note some designs can use the leakage inductance of the transformer as the resonant inductance and do not require an external resonant inductor.

8.2.2.10 LLC Resonant Capacitor

This capacitor carries the full-primary current at the switching frequency. Use a low dissipation factor capacitor to prevent overheating.

The AC voltage across the resonant capacitor is the impedance multiplied by the current.

$$V_{CR} = \frac{I_R}{\omega C_R} = \frac{1}{2\pi \times 69.8\text{kHz} \times 30\text{nF}} = 104.0V \quad (33)$$

$$V_{CR(\text{rms})} = \sqrt{\left[\frac{V_{IN(\text{max})}}{2}\right]^2 + V_{CR}^2} = \sqrt{\left[\frac{410}{2}\right]^2 + 104.0^2} = 229.9V \quad (34)$$

Peak voltage:

$$V_{CR(\text{peak})} = \frac{V_{IN(\text{max})}}{2} + \sqrt{2}V_{CR} = \frac{410}{2} + \sqrt{2} \times 104.0 = 352.0V \quad (35)$$

Valley voltage:

$$V_{CR(\text{valley})} = \frac{V_{IN(\text{max})}}{2} - \sqrt{2}V_{CR} = \frac{410}{2} - \sqrt{2} \times 104.0 = 58.0V \quad (36)$$

Rated current:

$$I_R = 1.367A \quad (37)$$

8.2.2.11 LLC Primary-Side MOSFETs

Each MOSFET sees the input voltage as its maximum applied voltage. Select the MOSFET voltage rating to be 1.5 times of the maximum bulk voltage:

$$V_{QLLC(\text{peak})} = 1.5 \times V_{IN(\text{max})} = 615V \quad (38)$$

Select the MOSFET current rating to be 1.1 times of the maximum primary side RMS current:

$$I_{QLLC} = 1.1 \times I_R = 1.504A \quad (39)$$

8.2.2.12 LLC Rectifier Diodes

The voltage rating of the output diodes is:

$$V_{DB} = 1.2 \times \frac{V_{IN(max)}}{N_{PS}} = 1.2 \times \frac{410}{16.5} = 29.82V \quad (40)$$

The current rating of the output diodes is:

$$I_{SAV} = \frac{\sqrt{2} \times I_{OES}}{\pi} = \frac{\sqrt{2} \times 18.329}{\pi} = 8.250A \quad (41)$$

8.2.2.13 LLC Output Capacitors

The LLC converter topology does not require an output filter although a small second stage filter inductor can be useful in reducing peak-to-peak output noise. Assuming that the output capacitors carry the full wave output current of the rectifier then the capacitor ripple current rating is:

$$I_{RECT} = \frac{\pi}{2\sqrt{2}} I_{OUT} = \frac{\pi}{2\sqrt{2}} \times 15 = 16.66A \quad (42)$$

Use 20V rating for 12V output voltage:

$$V_{LLCcap} = 20V \quad (43)$$

The RMS current rating of the capacitor is:

$$I_{C(out)} = \sqrt{\left(\frac{\pi}{2\sqrt{2}} \times I_{OUT}\right)^2 - I_{OUT}^2} = \sqrt{\left(\frac{\pi}{2\sqrt{2}} \times 15\right)^2 - 15^2} = 7.251A \quad (44)$$

$$(45)$$

Solid Aluminum capacitors with conductive polymer technology have high ripple-current ratings and are a good choice, especially if the design is required to operate at colder temperatures. The ripple-current rating for a single capacitor may not be sufficient so multiple capacitors are often connected in parallel.

The ripple voltage at the output of the LLC stage is a function of the amount of AC current that flows in the capacitors. To estimate this voltage, assume that all the current, including the DC current in the load, flows in the filter capacitors.

$$ESR_{max} = \frac{V_{OUT(pk-pk)}}{I_{RECT(pk)}} = \frac{0.12V}{2\frac{\pi}{4} \times 15A} = 5.1m\Omega \quad (46)$$

The capacitor specifications are:

- Voltage Rating: 20V
- Ripple Current Rating: 7.251A
- ESR: < 5.1mΩ

8.2.2.14 HV Pin Series Resistors

Multiple resistors are connected in series with HV pin to limit the power dissipation of the UCC25640x device. The recommended series resistor with HV pin is 5kΩ.

8.2.2.15 BLK Pin Voltage Divider

BLK pin senses the LLC input voltage and determines when to turn on and off the LLC converter. Different versions of UCC25640x have different BLK thresholds.

Select bulk startup voltage at 365V, calculate the BLK resistor divider ratio as below:

$$k_{BLK} = \frac{365V}{1V} = 365 \quad (47)$$

The desired power consumption of the BLK pin resistor divider is $P_{BLKsns} = 10mW$. The BLK sense resistor total value is:

$$R_{BLKsns} = \frac{V_{IN(nom)}^2}{P_{BLKsns}} = \frac{390^2}{0.01} = 15.21M\Omega \quad (48)$$

The lower BLK divider resistor value is:

$$R_{BLKlower} = \frac{R_{BLKsns}}{k_{BLK}} = \frac{15.21M\Omega}{365} = 41.67k\Omega \quad (49)$$

A standard value of 41.2kΩ is selected for $R_{BLKlower}$. The higher BLK divider resistor value is:

$$R_{BLKupper} = R_{BLKsns} - R_{BLKlower} = 15.17M\Omega \quad (50)$$

A standard value of 3x 4.99MΩ in series is selected for $R_{BLKupper}$. Calculate the actual bulk voltage thresholds as:

$$V_{BulkStart} = 365V \quad (51)$$

$$V_{BulkStart} = 365V \times \frac{0.9}{1} - 328.5V \quad (52)$$

8.2.2.16 ISNS Pin Differentiator

ISNS pin sets the overcurrent protection level. OCP1 is peak current protection level; OCP2 and OCP3 are average current protection levels. The typical threshold voltages are 4.0V, 0.6V, and 0.43V, respectively.

Set OCP3 level at 130% of full load. Thus, the sensed average input current level at full load is:

$$V_{ISNSfullload} = \frac{0.43V}{130\%} = 0.331V \quad (53)$$

Calculate the current sense ratio:

$$k_{ISNS} = \frac{V_{ISNSfullload}}{\left(\frac{P_{OUT}}{\eta} \times \frac{1}{V_{bulknom}}\right)} = \frac{0.331V}{\left(\frac{180W}{0.92} \times \frac{1}{390V}\right)} = 0.66\Omega \quad (54)$$

Select a current sense capacitor first, since there are less high voltage capacitor choices than resistors:

$$C_{ISNS} = 150pF \quad (55)$$

Then calculate the required ISNS resistor value:

$$R_{ISNS} = \frac{k_{ISNS}C_r}{C_{ISNS}} = \frac{0.66\Omega \times 30nF}{150pF} = 132\Omega \quad (56)$$

After determining the current sense ratio, calculate the peak ISNS pin voltage at full load:

$$V_{ISNSpeak} = \sqrt{2}I_r \times k_{ISNS} = \sqrt{2} \times 1.367A \times 0.66\Omega = 1.29V \quad (57)$$

The peak resonant current at OCP1 level is:

$$I_{respeakOCP1} = \frac{4V \times C_R}{R_{ISNS} \times C_{ISNS}} = \frac{4V \times 30nF}{133\Omega \times 150pF} = 6.02A \quad (58)$$

The peak secondary-side current at OCP1 level is:

$$I_{secpeakOCP1} = I_{respeakOCP1} \times N_{PS} = 6.02A \times 16.5 = 99.33A \quad (59)$$

8.2.2.17 VCR Pin Capacitor Divider

The capacitor divider on the VCR pin sets two parameters: (1) the divider ratio of the resonant capacitor voltage; (2) the amount of frequency compensation to be added. The first criteria the capacitor divider must meet is that under over load condition, the peak-to-peak voltage on the VCR pin is within 6V. It is recommended to size the VCR capacitance to give a total peak-to-peak voltage from 3V to 4.5V at full load with the frequency compensation ramp contributing from 1V to 2V to the total VCR peak-to-peak voltage. For this design, the VCR pin capacitance is selected to give a maximum peak-to-peak voltage of approximately 4.25V at full load with the internal ramp contributing 1.75V to the total VCR waveform.

Calculate the required VCR capacitance directly from the resonant capacitor peak-to-peak voltage and the minimum expected switching frequency.

$$V_{CR(pk-pk)} = V_{CR(peak)} - V_{CR(valley)} = 352V - 58V = 294V \quad (60)$$

Based on the expected peak-to-peak resonant capacitor voltage, derive the required capacitor divider ratio:

$$k_{CapDiv} = \frac{V_{CR(pk-pk)}}{V_{VCRpin(pk-pk)} - V_{Ramp(pk-pk)}} = \frac{294V}{4.25V - 1.75V} = 117.6 \quad (61)$$

From the expected minimum switching frequency, derive the lower VCR capacitance:

$$C_{VCRlower} = \frac{1}{V_{Ramp(pk-pk)}} \times \frac{I_{Ramp}}{2 \times f_{SW_min}} = \frac{1}{1.75V} \times \frac{2mA}{2 \times 69.8kHz} = 8.2nF \quad (62)$$

A standard value of 8.2nF is selected for the lower VCR capacitor. From the selected lower VCR capacitor and calculated capacitor divider ratio, the upper VCR capacitance is:

$$C_{VCRupper} = \frac{C_{VCRlower}}{k_{CapDiv} - 1} = \frac{8.2nF}{117.6 - 1} = 70.6pF \quad (63)$$

A standard value of 68pF is selected for the upper VCR capacitor. From the selected upper and lower VCR capacitors, calculate the actual peak-to-peak voltage on the VCR pin:

$$k_{CapDiv} = \frac{C_{VCRlower}}{C_{VCRupper}} + 1 = \frac{8.2nF}{68pF} + 1 = 121.59 \quad (64)$$

$$\begin{aligned} V_{VCRpin(pk-pk)} &= \frac{1}{C_{VCRlower}} \times \frac{I_{Ramp}}{2 \times f_{SW(Mgmin)}} + \frac{V_{CR(pk-pk)}}{k_{CapDiv}} \\ &= \frac{1}{8.2nF} \times \frac{2mA}{2 \times 69.8kHz} + \frac{294V}{121.59} = 4.17V \end{aligned} \quad (65)$$

8.2.2.18 BW Pin Voltage Divider

The BW pin programs the ratio between burst mode entry and exit thresholds as well as senses the output voltage through the bias winding and protects the power stage from overvoltage. The nominal output voltage is 12V. The bias winding has 3 turns, and the secondary side winding has 2 turns. Assuming there is a 0.5V drop

in the rectifier diodes (V_f) and a further 0.5V drop due to other losses (V_{loss}), the nominal voltage of the bias winding is given by:

$$V_{BiasWindingNom} = (12V + 0.5V + 0.5V) \times \frac{3}{2} = 19.5 \quad (66)$$

The desired OVP threshold in this design is 140% of the nominal value. The OVP threshold level in UCC25640x device is 4V, so the nominal BW pin voltage is given by:

$$V_{BWnom} = \frac{4V}{140\%} = 2.86V \quad (67)$$

The required BW divider ratio is then given by:

$$k_{BW} = \frac{V_{BiasWindingNom} \times \eta_{OVP}}{V_{BW OVP}} = \frac{19.5V \times 140\%}{4V} = 6.825 \quad (68)$$

In this design, the burst mode threshold ratio is selected to be 0.6 (Option 6). The target programming resistance is then:

$$R_{BMT_Program} = 4.59k\Omega \quad (69)$$

The lower BW resistor can be calculated by:

$$R_{BWLower} = R_{BMT_Program} \times \left(1 + \frac{1}{k_{BW} - 1}\right) = 4.59k\Omega \times \left(1 + \frac{1}{6.825 - 1}\right) = 5.38k\Omega \quad (70)$$

A standard value of 5.36k Ω is selected for the lower BW resistor.

Calculate the upper resistor:

$$\begin{aligned} R_{BWUpper} &= R_{BMTLower} \times \left(\frac{V_{BiasWindingNom} - V_{BWNom}}{V_{BWNom}}\right) \\ &= 5.36k\Omega \times \left(\frac{19.5V - 2.86V}{2.86V}\right) = 31.32k\Omega \end{aligned} \quad (71)$$

A standard value of 30.9k Ω is selected for the upper BW resistor.

8.2.2.19 Soft Start and Burst Mode Programming

The LL/SS and BW pins allow the designer to select a burst mode threshold as well as program hysteresis for entering and exiting burst mode. The resistor divider of connected to the LL/SS pin sets the BMT_H threshold while the BW pin sets the ratio between BMT_L and BMT_H . In addition to programming the burst mode threshold, the LL/SS pin provides the capability to program an initial voltage onto the LL/SS pin to limit the maximum switching frequency during startup. For initial selection of LL/SS components, it is recommended to select an initial LL/SS pin voltage from 0V to 1V and to select burst mode threshold from 1V to 2V. The LL/SS pin parameters can be fine tuned later based on bench measurement.

In this design, an initial LL/SS pin voltage of 0.3V and a BMT_H threshold of 0.6V are selected. The soft start capacitor sets how quickly the voltage on the soft start capacitor rises. The soft start time varies with load condition. At full load or over load condition, the soft start time is the longest. It is not easy to calculate the exact soft start time value. However, it can be estimated that under full load condition, the longest possible soft start time is determined by how quickly the soft start pin voltage rises to the maximum VCR peak-to-peak voltage. For a start up time of 7.5ms, the soft start capacitor is sized to be the following:

$$C_{LL/SS} = I_{SS} \times \frac{T_{SS_Max}}{V_{VCR(pk-pk)} - V_{LL/SS_precharge}} = 37.5\mu A \times \frac{7.5ms}{4.17V - 0.3V} = 72.7nF \quad (72)$$

A standard value of 68nF is selected for the soft start capacitor. To properly select the resistors on LL/SS, first define R_{TH} as the equivalent resistance on the LL/SS pin and V_{TH} as the equivalent voltage source on the LL/SS pin.

$$R_{TH} = R_{LL/SS_Upper} \parallel R_{LL/SS_Lower} \quad (73)$$

$$V_{TH} = \frac{R_{TH} \times RVCC}{R_{LL/SS_Upper}} \quad (74)$$

During the SS pull low phase, the voltage on the LL/SS pin is internally pulled down through a 1.2kΩ resistor. During the SS initial program phase, the internal pulldown is released and the soft start capacitor is allowed to naturally charge up from RVCC. Calculate the total voltage offset on the LL/SS soft start capacitor using the equation below.

$$V_{ssinit} = \frac{1.2k\Omega \times RVCC}{R_{LL/SS_Upper}} + V_{TH} \left[1 - e^{\left(\frac{-t_{SSInitPrgm}}{C_{SS}} \right)} \right] \quad (75)$$

Substituting for $RVCC/R_{LL/SS_Upper}$ and using a linear approximation for the exponential term, the equation can be simplified to the following.

$$V_{ssinit} = \frac{1.2k\Omega \times V_{TH}}{R_{TH}} + \frac{V_{TH} \times t_{SSInitVolPrgm}}{R_{TH} \times C_{SS}} \quad (76)$$

The current used by the LL/SS pin to program BMT_H , I_{BMT} , has the following relationships. I_{BMT} can be directly solved for based on the desired BMT_H threshold.

$$I_{BMT} = \frac{BMT_H}{R_{LL}} = \frac{0.6V}{98k\Omega} = 6.12\mu A \quad (77)$$

$$I_{BMT} = \frac{V_{TH} - 3.5V}{R_{TH}} \quad (78)$$

Rearranging Equation 76, calculate V_{TH} and R_{TH} .

$$\begin{aligned} V_{TH} &= \frac{3.5V}{1 - \frac{I_{BMT}}{V_{ssinit}} \left(1.2k\Omega + \frac{t_{SSInitVolPrgm}}{C_{SS}} \right)} \\ &= \frac{3.5V}{1 - \frac{6.12\mu A}{0.3V} \left(1.2k\Omega + \frac{776\mu s}{68nF} \right)} = 4.71V \end{aligned} \quad (79)$$

$$R_{TH} = \frac{4.71V - 3.5V}{I_{BMT}} = 197k\Omega \quad (80)$$

Determine values for R_{LL/SS_Upper} and R_{LL/SS_Lower} from V_{TH} and R_{TH} .

$$R_{LL/SS_Upper} = \frac{R_{TH} \times RVCC}{V_{TH}} = \frac{197k\Omega \times 13V}{4.71V} = 544k\Omega \quad (81)$$

A standard value of 549kΩ is selected for R_{LL/SS_Upper} .

$$R_{LL/SS_Lower} = \frac{R_{TH} \times R_{LL/SS_Upper}}{R_{LL/SS_Upper} - R_{TH}} = \frac{197k\Omega \times 549k\Omega}{549k\Omega - 197k\Omega} = 307k\Omega \quad (82)$$

A standard value of 316kΩ is selected for R_{LL/SS_Lower} .

8.2.3 Application Curves

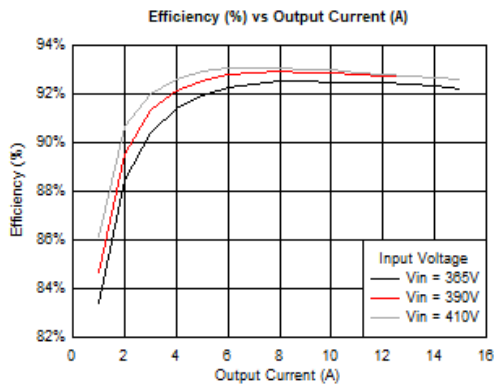


Figure 8-2. Efficiency

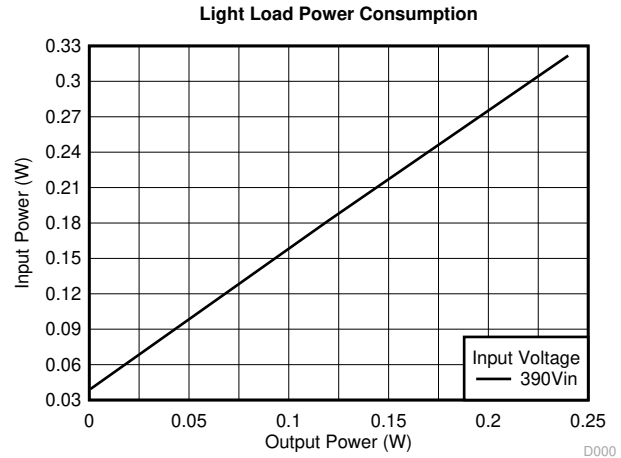


Figure 8-3. Light Load Power Consumption

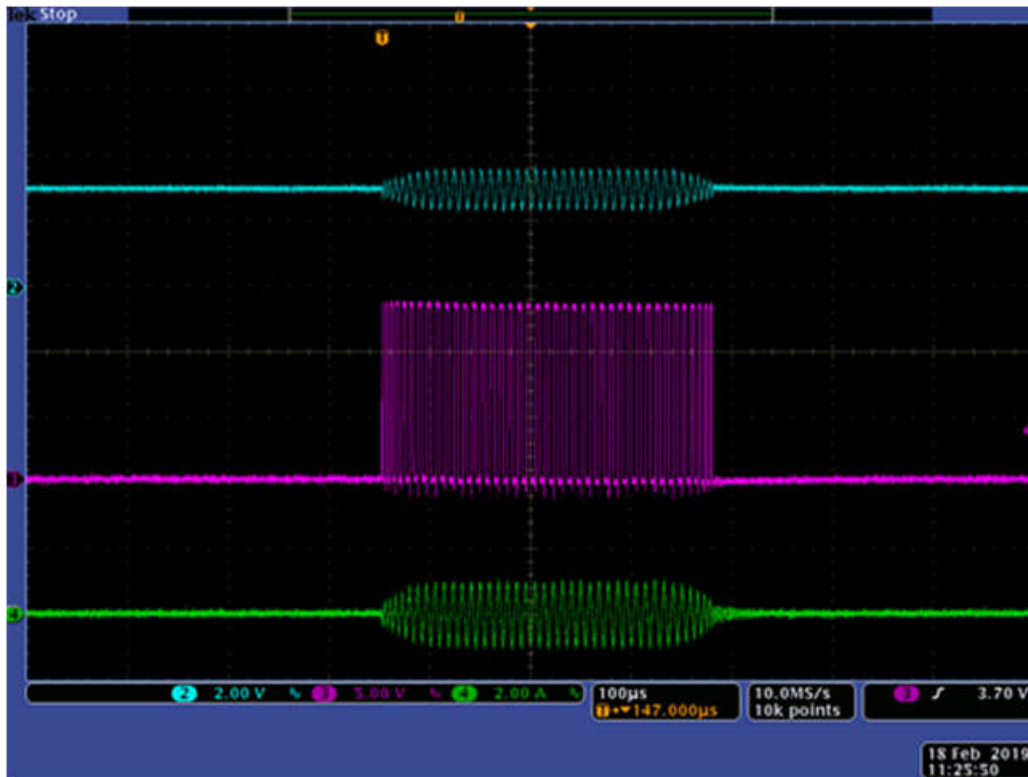


Figure 8-4. Burst Mode with Soft On/Off (Ch2 = VCR, Ch3 = LO, Ch4 = Resonant Current)

8.3 Power Supply Recommendations

8.3.1 VCC Pin Capacitor

Size the VCC capacitor based on the total start-up charge the system requires. The start-up charge is mostly consumed by the gate driver circuit. Thus, estimate the total start-up charge by the start-up switching frequency, MOSFET gate charge, and the soft-start time.

Assume the total start-up charge the system requires is in [Equation 83](#)

$$Q_{\text{tot}} = 1.6\text{mC} \quad (83)$$

During PFC and LLC startup phase, the maximum VCC voltage drop allowed is

$$V_{\text{ccd} \text{dropmax}} = 26\text{V} - 9.65\text{V} = 16.35\text{V} \quad (84)$$

The minimum VCC capacitor needed:

$$C_{\text{VCC}} = \frac{Q_{\text{tot}}}{V_{\text{ccd} \text{dropmax}}} = 97.86\mu\text{F} \quad (85)$$

Select at least a 100 μF capacitor, or combination of capacitors.

8.3.2 Boot Capacitor

During burst off period, power consumed by the high-side gate driver from the HB pin must be drawn from C_{BOOT} and causes the voltage to decay. At the start of the next burst period there must be sufficient voltage remaining on C_{BOOT} to power the high-side gate driver until the conduction period of LO allows it to replenish from C_{RVCC} . The power consumed by the high-side driver during this burst off period will therefore have a direct impact on the size and cost of capacitors that must be connected to HB and RVCC.

Assume the system has a maximum burst off period of 150ms and the bootstrap diode has a forward voltage drop of 1V. Target a minimum bootstrap voltage of 8V to avoid UVLO fault. The maximum allowable voltage drop on the boot capacitor is:

$$V_{\text{bootmaxdrop}} = V_{\text{RVCC}} - V_{\text{bootforwarddrop}} - 8\text{V} = 13\text{V} - 1\text{V} - 8\text{V} = 4\text{V} \quad (86)$$

Size the boot capacitor:

$$C_{\text{boot}} = \frac{I_{\text{BOOT_QUIESCENT}} \times t_{\text{maxoff}}}{V_{\text{bootforwarddrop}}} = \frac{62\mu\text{A} \times 150\text{ms}}{4\text{V}} = 2.32\mu\text{F} \quad (87)$$

8.3.3 RVCC Pin Capacitor

The RVCC capacitor must be at least five times greater than boot capacitor. In addition, sizing of the RVCC capacitor depends on the stability of the RVCC LDO. If the load is light on RVCC, smaller capacitors can be used. The larger the load, the larger the capacitor is needed. In a typical system, the RVCC LDO powers the PFC and LLC gate drivers.

8.4 Layout

8.4.1 Layout Guidelines

- Put a 2.2 μF ceramic capacitor on VCC pin in addition to the energy storage electrolytic capacitor. Place the 2.2 μF ceramic capacitor as close as possible to the VCC pin.
- RVCC pin must have a bypass capacitor of 4.7 μF or more. It is recommended to add a 0.1 μF ceramic capacitor in addition to the 4.7 μF . Place the capacitors as close as possible to the RVCC pin. RVCC cap is recommended to be size at least five times of boot capacitor.
- Minimum recommended boot capacitor, C_{BOOT} , is 0.1 μF . The minimum value of the boot capacitor must be determined by the minimum burst frequency. The boot capacitor must be large enough to hold the bootstrap voltage during the lowest burst frequency. See the boot leakage current in the electrical table.
- Signal ground and power ground must be single-point connected. Power ground is recommended to connect to the negative terminal of the LLC input bulk capacitor.
- Place the filtering capacitors for ISNS and BLK as close as possible to the pins.
- Place the bottom capacitor on VCR as close as possible to the VCR pin.
- FB trace must be as short as possible
- Place the soft-start capacitor as close as possible to LL/SS pin
- Use film capacitors or C0G, NP0 ceramic capacitors for the VCR divider and ISNS capacitor for low distortion

- Add necessary filtering capacitors on the BW pin to filter out the high spikes on the bias winding waveform. It is critical to filter out the high spikes because internally the signal is peak detected and then sampled at the low-side turn off edge.
- Keep necessary high voltage clearance and creepage.
- If 2kV HBM ESD rating is needed on HV pin, place a 100pF capacitor from the HV pin to ground to pass up to 2kV HBM ESD.

8.4.2 Layout Example

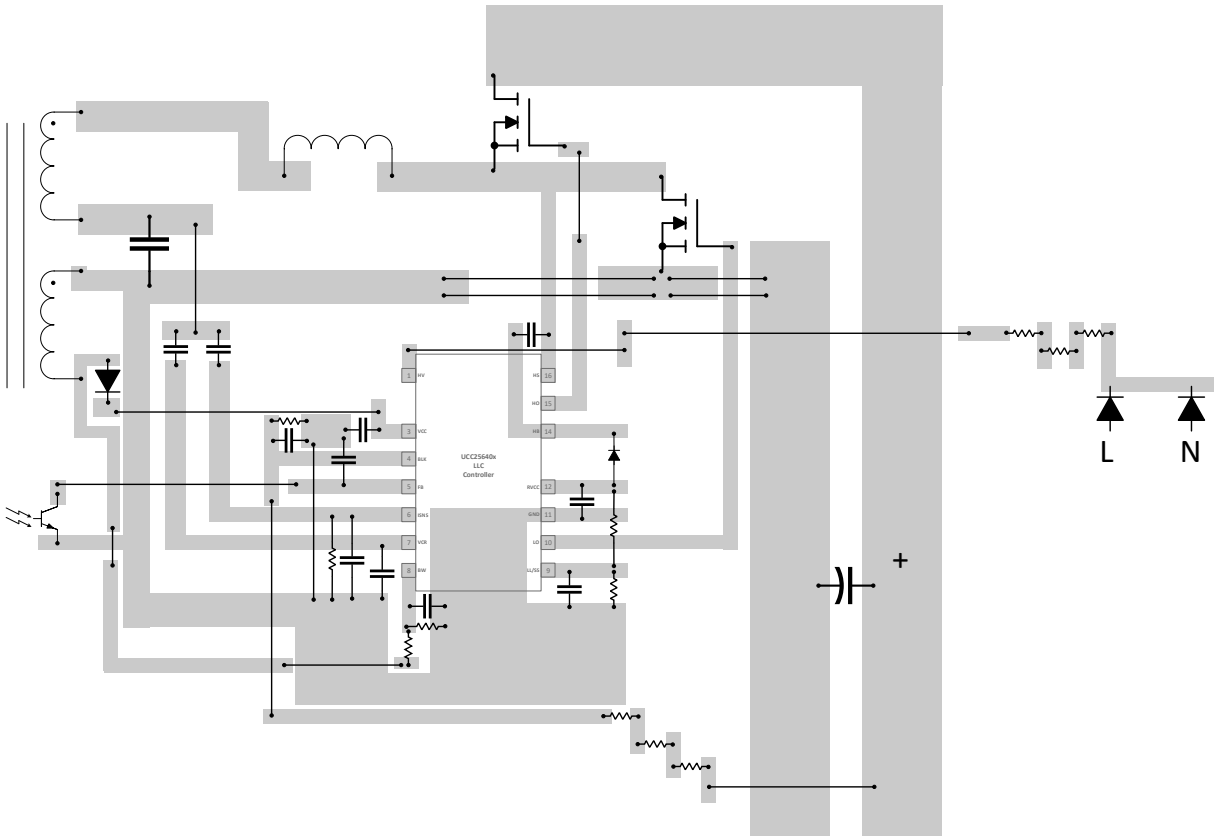


Figure 8-5. Layout Example for Single-Layer PCB

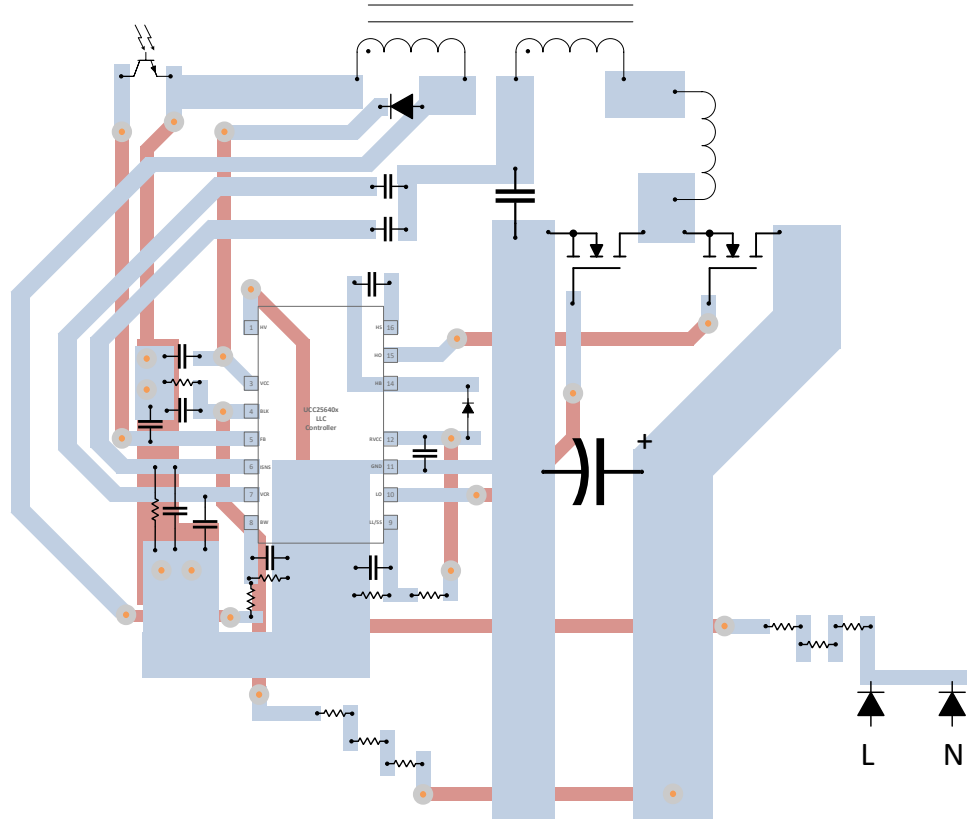


Figure 8-6. Layout Example for Double-Layer PCB

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation see the following:

- Design Spreadsheet, [UCC25640x Design Calculator](#)
- User Guide, [Using UCC25640EVM-020](#)

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (February 2021) to Revision F (August 2026)	Page
---	------

- | | |
|---|---|
| • Updated the numbering format for tables, figures, and cross-references throughout the document..... | 1 |
|---|---|

Changes from Revision D (September 2020) to Revision E (February 2021)	Page
--	------

- | | |
|--|---|
| • Updated Absolute Maximum Ratings HV, HB Input Voltage from 640V to 700V maximum..... | 6 |
|--|---|

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this datasheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UCC256402ADDBR	Active	Production	SOIC (DDB) 14	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	UCC256402A
UCC256402ADDBR.B	Active	Production	SOIC (DDB) 14	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	UCC256402A
UCC256402ADDBT	Active	Production	SOIC (DDB) 14	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	UCC256402A
UCC256402ADDBT.B	Active	Production	SOIC (DDB) 14	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	UCC256402A
UCC256402DDBR	Active	Production	SOIC (DDB) 14	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	UCC256402
UCC256402DDBR.B	Active	Production	SOIC (DDB) 14	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	UCC256402
UCC256402DDBT	Active	Production	SOIC (DDB) 14	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	UCC256402
UCC256402DDBT.B	Active	Production	SOIC (DDB) 14	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	UCC256402
UCC256403ADDBR	Active	Production	SOIC (DDB) 14	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	UCC256403A
UCC256403ADDBR.B	Active	Production	SOIC (DDB) 14	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	UCC256403A
UCC256403DDBR	Active	Production	SOIC (DDB) 14	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	UCC256403
UCC256403DDBR.B	Active	Production	SOIC (DDB) 14	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	UCC256403
UCC256403DDBT	Active	Production	SOIC (DDB) 14	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	UCC256403
UCC256403DDBT.B	Active	Production	SOIC (DDB) 14	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	UCC256403
UCC256404ADDBR	Active	Production	SOIC (DDB) 14	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	UCC256404A
UCC256404ADDBR.B	Active	Production	SOIC (DDB) 14	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	UCC256404A
UCC256404ADDBT	Active	Production	SOIC (DDB) 14	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	UCC256404A
UCC256404ADDBT.B	Active	Production	SOIC (DDB) 14	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	UCC256404A
UCC256404BDBR	Active	Production	SOIC (DDB) 14	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	UCC256404B
UCC256404BDBR.B	Active	Production	SOIC (DDB) 14	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	UCC256404B
UCC256404DDBR	Active	Production	SOIC (DDB) 14	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	UCC256404
UCC256404DDBR.B	Active	Production	SOIC (DDB) 14	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	UCC256404
UCC256404DDBT	Active	Production	SOIC (DDB) 14	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	UCC256404
UCC256404DDBT.B	Active	Production	SOIC (DDB) 14	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	UCC256404

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

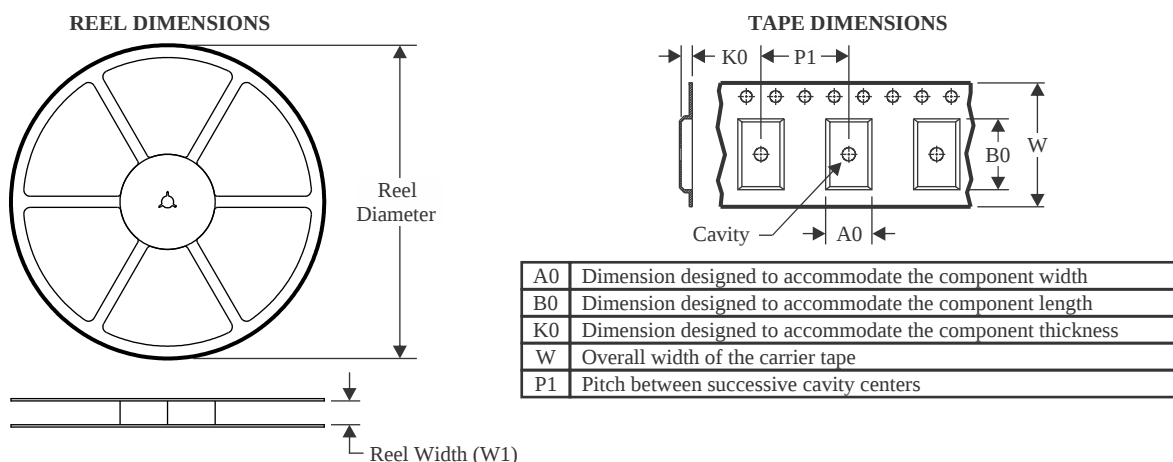
⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

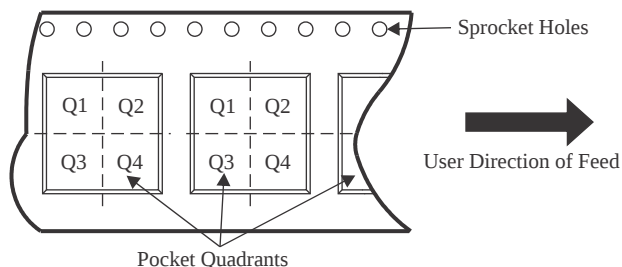
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TAPE AND REEL INFORMATION



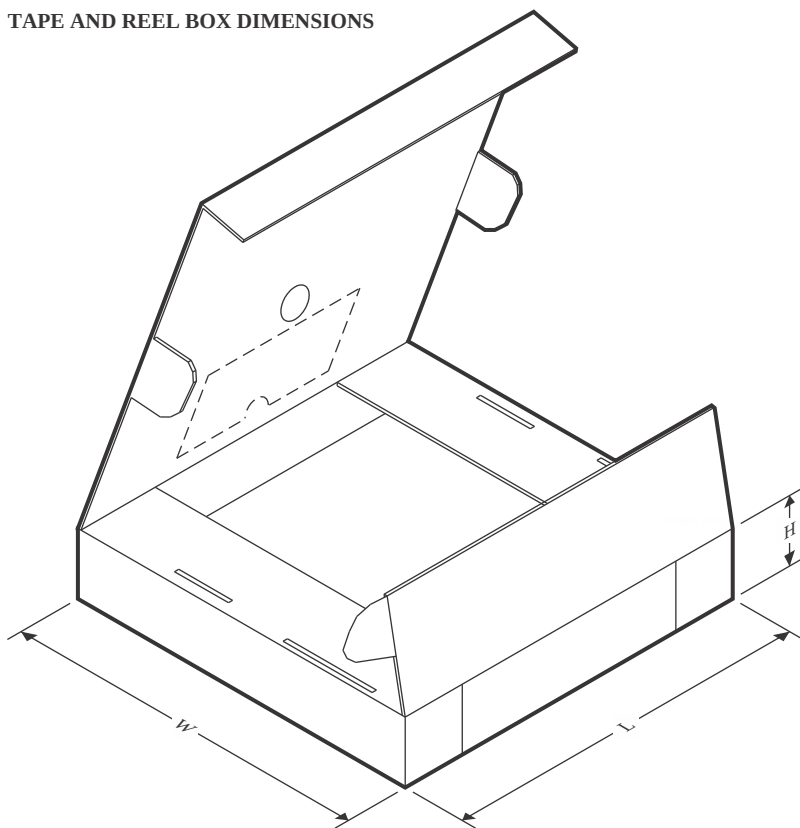
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

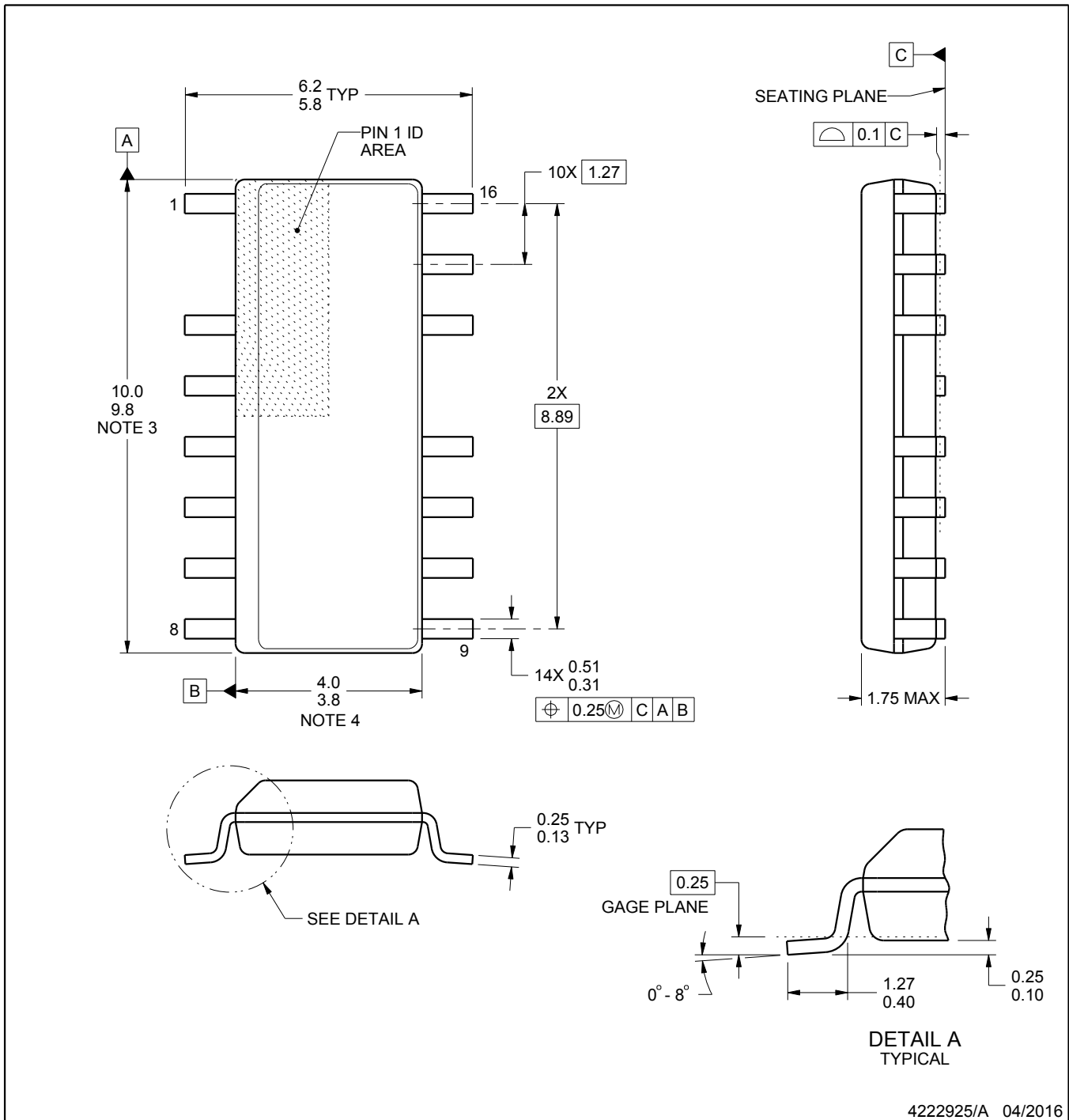
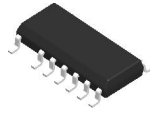
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC256402ADDBR	SOIC	DDB	14	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
UCC256402ADDBT	SOIC	DDB	14	250	180.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
UCC256402DDBR	SOIC	DDB	14	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
UCC256402DDBT	SOIC	DDB	14	250	180.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
UCC256403ADDBR	SOIC	DDB	14	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
UCC256403DDBR	SOIC	DDB	14	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
UCC256403DDBT	SOIC	DDB	14	250	180.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
UCC256404ADDBR	SOIC	DDB	14	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
UCC256404ADDBT	SOIC	DDB	14	250	180.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
UCC256404BDDBR	SOIC	DDB	14	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
UCC256404DDBR	SOIC	DDB	14	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
UCC256404DDBT	SOIC	DDB	14	250	180.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC256402ADDBR	SOIC	DDB	14	2500	353.0	353.0	32.0
UCC256402ADDBT	SOIC	DDB	14	250	213.0	191.0	35.0
UCC256402DDBR	SOIC	DDB	14	2500	353.0	353.0	32.0
UCC256402DDBT	SOIC	DDB	14	250	213.0	191.0	35.0
UCC256403ADDBR	SOIC	DDB	14	2500	353.0	353.0	32.0
UCC256403DDBR	SOIC	DDB	14	2500	353.0	353.0	32.0
UCC256403DDBT	SOIC	DDB	14	250	213.0	191.0	35.0
UCC256404ADDBR	SOIC	DDB	14	2500	353.0	353.0	32.0
UCC256404ADDBT	SOIC	DDB	14	250	213.0	191.0	35.0
UCC256404BDDBR	SOIC	DDB	14	2500	353.0	353.0	32.0
UCC256404DDBR	SOIC	DDB	14	2500	353.0	353.0	32.0
UCC256404DDBT	SOIC	DDB	14	250	213.0	191.0	35.0



NOTES:

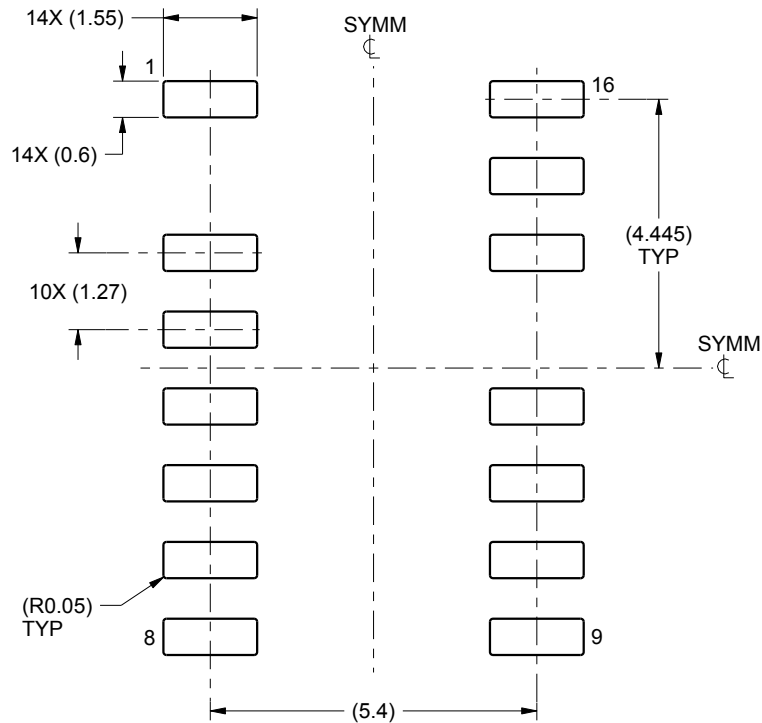
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-012, variation AC.

EXAMPLE BOARD LAYOUT

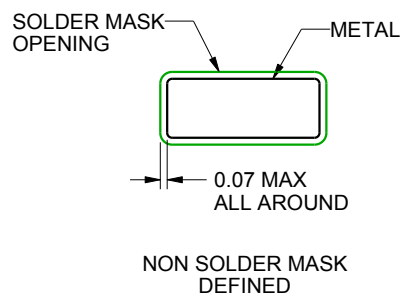
DDB0014A

SOIC - 1.75 mm max height

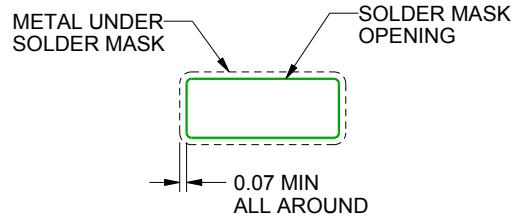
SOIC



LAND PATTERN EXAMPLE
SCALE:8X



NON SOLDER MASK
DEFINED



SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4222925/A 04/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

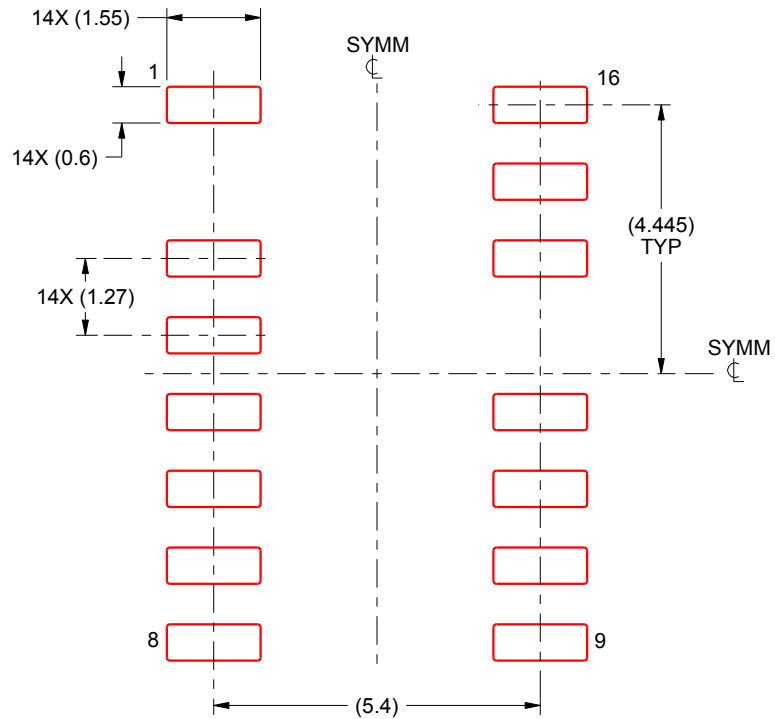
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DDB0014A

SOIC - 1.75 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4222925/A 04/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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