



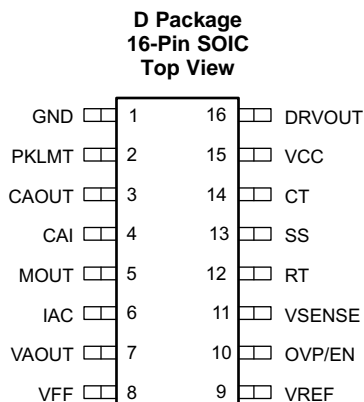
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## 4 Revision History

Changes from Original (February 2010) to Revision A	Page
• Added the <i>Applications</i> section, <i>Feature Description</i> section, <i>Application and Implementation</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section .....	<b>1</b>
• Updated the <i>Pin Functions</i> table to match the pin out configuration image .....	<b>3</b>

## 5 Pin Configuration and Functions



### Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	GND	—	Ground
2	PKLMT	I	PFC peak current limit
3	CAOUT	O	Current amplifier output
4	CAI	I	Current amplifier noninverting input
5	MOUT	I/O	Multiplier output and current amplifier inverting input
6	IAC	I	Current proportional to input voltage
7	VAOUT	O	Voltage amplifier output
8	VFF	I	Feed-forward voltage
9	VREF	O	Voltage reference output
10	OVP/EN	I	Overvoltage/enable
11	VSENSE	I	Voltage amplifier inverting input
12	RT	I	Oscillator charging current
13	SS	I	Soft-start
14	CT	I	Oscillator timing capacitor
15	VCC	I	Positive supply voltage
16	DRVOUT	O	Gate drive

## 6 Specifications

### 6.1 Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage		18	V
I <sub>CC</sub>	Supply current		20	mA
	Gate drive current, continuous		0.2	A
	Gate drive current		1.2	A
Input voltage	CAI, MOUT, SS		8	V
	PKLMT		5	
	VSENSE, OVP/EN		10	
Input current	RT, IAC, PKLMT		10	mA
	V <sub>CC</sub> (no switching)		20	
Maximum negative voltage	DRVOUT, PKLMT, MOUT		−0.5	V
Power dissipation			1	W
θ <sub>JA</sub>	Package thermal impedance <sup>(2)</sup>		73.1	°C/W
T <sub>J</sub>	Junction temperature	−40	150	°C
T <sub>stg</sub>	Storage temperature range	−65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The package thermal impedance is calculated in accordance with JESD 51-5.

### 6.2 ESD Ratings

		VALUE	UNIT	
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 <sup>(1)</sup>	±1000	V

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 6.3 Thermal Information

THERMAL METRIC <sup>(1)</sup>		D 16 PINS	UNIT
θ <sub>JA</sub>	Package thermal impedance <sup>(2)</sup>	73.1	°C/W

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).
- (2) The package thermal impedance is calculated in accordance with JESD 51-5.

## 6.4 Electrical Characteristics

$T_J = T_A = -40^\circ\text{C}$  to  $125^\circ\text{C}$ ,  $V_{CC} = 12\text{ V}$ ,  $R_T = 22\text{ k}\Omega$ ,  $C_T = 270\text{ pF}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
<b>SUPPLY CURRENT</b>						
Supply current, off	$V_{CC} = (V_{CC} \text{ turn-on threshold} - 0.3\text{ V})$		150	300	$\mu\text{A}$	
Supply current, on	$V_{CC} = 12\text{ V}$ , No load on DRVOUT	2	4	6	$\text{mA}$	
<b>UVLO</b>						
VCC turn-on threshold		9.7	10.2	10.9	V	
VCC turn-off threshold		9.4	9.7		V	
UVLO hysteresis		0.3	0.5		V	
<b>VOLTAGE AMPLIFIER</b>						
Input voltage		7.369	7.5	7.631	V	
VSENSE bias current	$V_{SENSE} = V_{REF}$ , $V_{AOUT} = 2.5\text{ V}$		50	200	$\text{nA}$	
Open-loop gain	$V_{AOUT} = 2\text{ V}$ to $5\text{ V}$	50	90		$\text{dB}$	
High-level output voltage	$I_L = -150\ \mu\text{A}$	5.3	5.5	5.6	V	
Low-level output voltage	$I_L = 150\ \mu\text{A}$	0	50	150	$\text{mV}$	
<b>OVERVOLTAGE PROTECTION AND ENABLE</b>						
Overvoltage reference		VREF + 0.48	VREF + 0.5	VREF + 0.52	V	
Hysteresis		300	500	600	$\text{mV}$	
Enable threshold		1.7	1.9	2.1	V	
Enable hysteresis		0.1	0.2	0.3	V	
<b>CURRENT AMPLIFIER</b>						
Input offset voltage	$V_{CM} = 0\text{ V}$ , $V_{CAOUT} = 3\text{ V}$	$T_A = 25^\circ\text{C}$	-3.5	0	3	$\text{mV}$
		$T_A = -40^\circ\text{C}$ to $125^\circ\text{C}$	-5		5	
Input bias current	$V_{CM} = 0\text{ V}$ , $V_{CAOUT} = 3\text{ V}$		-50	-100	$\text{nA}$	
Input offset current	$V_{CM} = 0\text{ V}$ , $V_{CAOUT} = 3\text{ V}$		25	100	$\text{nA}$	
Open-loop gain	$V_{CM} = 0\text{ V}$ , $V_{CAOUT} = 2\text{ V}$ to $5\text{ V}$	90			$\text{dB}$	
Common-mode rejection ratio	$V_{CM} = 0\text{ V}$ to $1.5\text{ V}$ , $V_{CAOUT} = 3\text{ V}$	60	80		$\text{dB}$	
High-level output voltage	$I_L = -120\text{ mA}$	5.6	6.5	6.9	V	
Low-level output voltage	$I_L = 1\text{ mA}$	0.1	0.2	0.5	V	
Gain bandwidth product <sup>(1)</sup>			2.5		$\text{MHz}$	
<b>VOLTAGE REFERENCE</b>						
Input voltage		7.313 to 7.687	7.5	7.631	V	
Load regulation	$I_{REF} = 1\text{ mA}$ to $2\text{ mA}$	0		10	$\text{mV}$	
Line regulation	$V_{CC} = 10.8\text{ V}$ to $15\text{ V}$ <sup>(2)</sup>	0		10	$\text{mV}$	
Short-circuit current	$V_{REF} = 0\text{ V}$	-20	-25	-50	$\text{mA}$	
<b>OSCILLATOR</b>						
Initial accuracy	$T_A = 25^\circ\text{C}$	85	100	115	$\text{kHz}$	
Voltage stability	$V_{CC} = 10.8\text{ V}$ to $15\text{ V}$	-1		+1	%	
Total variation	Over line and temperature	80		120	$\text{kHz}$	
Ramp peak voltage		4.5	5	5.5	V	
Ramp amplitude voltage (peak to peak)		3.5	4	4.5	V	
<b>PEAK CURRENT LIMIT</b>						
PKLMT reference voltage		-15		15	$\text{mV}$	
PKLMT propagation delay		150	350	550	$\text{ns}$	

(1) Ensured by design, not production tested

(2) Reference variation for  $V_{CC} < 10.8\text{ V}$  is shown in [Figure 8](#).

## Electrical Characteristics (continued)

$T_J = T_A = -40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ ,  $V_{CC} = 12\text{ V}$ ,  $R_T = 22\text{ k}\Omega$ ,  $C_T = 270\text{ pF}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>MULTIPLIER</b>						
$I_{MOUT}$	High line, low power output current	$I_{AC} = 500\text{ }\mu\text{A}$ , $V_{FF} = 4.7\text{ V}$ , $VAOUT = 1.25\text{ V}$	0	-6	-23	$\mu\text{A}$
	High-line, high-power output current	$I_{AC} = 500\text{ }\mu\text{A}$ , $V_{FF} = 4.7\text{ V}$ , $VAOUT = 5\text{ V}$	-70	-90	-105	
	Low-line, low-power output current	$I_{AC} = 150\text{ }\mu\text{A}$ , $V_{FF} = 1.4\text{ V}$ , $VAOUT = 1.25\text{ V}$	-10	-19	-50	
	Low-line, high-power output current	$I_{AC} = 150\text{ }\mu\text{A}$ , $V_{FF} = 1.4\text{ V}$ , $VAOUT = 5\text{ V}$	-268	-300	-345	
	IAC limited output current	$I_{AC} = 150\text{ }\mu\text{A}$ , $V_{FF} = 1.3\text{ V}$ , $VAOUT = 5\text{ V}$	-250	-300	-400	
Gain constant (K)		$I_{AC} = 200\text{ }\mu\text{A}$ , $V_{FF} = 3\text{ V}$ , $VAOUT = 2.5\text{ V}$	0.5	1	1.6	1/V
$I_{MOUT}$	Zero current	$I_{AC} = 150\text{ }\mu\text{A}$ , $V_{FF} = 1.4\text{ V}$ , $VAOUT = 0.25\text{ V}$		0	-2	$\mu\text{A}$
		$I_{AC} = 500\text{ }\mu\text{A}$ , $V_{FF} = 4.7\text{ V}$ , $VAOUT = 0.25\text{ V}$		0	-2	
		$I_{AC} = 500\text{ }\mu\text{A}$ , $V_{FF} = 4.7\text{ V}$ , $VAOUT = 0.5\text{ V}$		0	-3.5	
Power limit ( $I_{MOUT} \times V_{FF}$ )		$I_{AC} = 150\text{ }\mu\text{A}$ , $V_{FF} = 1.4\text{ V}$ , $VAOUT = 5\text{ V}$	-375	-420	-490	$\mu\text{W}$
<b>FEED FORWARD</b>						
VFF output current		$I_{AC} = 300\text{ }\mu\text{A}$	-140	-150	-160	$\mu\text{A}$
<b>SOFT START</b>						
Softstart charge current			-6	-10	-17	$\mu\text{A}$
<b>GATE DRIVER</b>						
Pullup resistance		$I_O = -100\text{ mA}$ to $-200\text{ mA}$		9	12	$\Omega$
Pulldown resistance		$I_O = 100\text{ mA}$		4	10	$\Omega$
Output rise time		$C_L = 1\text{ nF}$ , $R_L = 10\text{ }\Omega$ , $V_{DRVOUT} = 0.7\text{ V}$ to $9\text{ V}$		25	50	ns
Output fall time		$C_L = 1\text{ nF}$ , $R_L = 10\text{ }\Omega$ , $V_{DRVOUT} = 9\text{ V}$ to $0.7\text{ V}$		10	50	ns
Maximum duty cycle			93	95	99	%
Minimum controlled duty cycle <sup>(1)</sup>		At 100 kHz			2	%
<b>ZERO POWER</b>						
Zero-power comparator threshold		Measured on VAOUT	0.2	0.33	0.5	V



## Feature Description (continued)

### 7.2.5 Ground, GND

All voltages measured with respect to ground.  $V_{CC}$  and REF should be bypassed directly to GND with a 0.1- $\mu$ F or larger ceramic capacitor.

### 7.2.6 Current Proportional to Input Voltage, IAC

This input to the analog multiplier is a current proportional to instantaneous line voltage. The multiplier is tailored for very low distortion from this current input ( $I_{IAC}$ ) to multiplier output. The recommended maximum  $I_{IAC}$  is 500  $\mu$ A.

### 7.2.7 Multiplier Output and Current Amplifier Inverting Input, MOUT

The output of the analog multiplier and the inverting input of the current amplifier are connected together at MOUT. As the multiplier output is a current, this is a high-impedance input so the amplifier can be configured as a differential amplifier. This configuration improves noise immunity and allows for the leading-edge modulation operation. The multiplier output current is limited to ( $2 \times I_{IAC}$ ). The multiplier output current is given by [Equation 2](#).

$$I_{MOUT} = \frac{I_{IAC} \times (V_{VAOUT} - 1)}{V_{VFF}^2 \times K}$$

where

- $K = 1/V$  is the multiplier gain constant (2)

### 7.2.8 Overvoltage and Enable, OVP/EN

A window comparator input that disables the output driver if the boost output voltage is a programmed level above the nominal, or disables both the PFC output driver and resets SS if pulled below 1.9 V (typ).

### 7.2.9 PFC Peak Current-Limit, PKLMT

The threshold for peak limit is 0 V. Use a resistor divider from the negative side of the current sense resistor to  $V_{REF}$  to level shift this signal to a voltage level defined by the value of the sense resistor and the peak current limit. Peak current limit is reached when PKLMT voltage falls below 0 V.

### 7.2.10 Oscillator Charging Current, RT

A resistor from RT to GND is used to program oscillator charging current. A resistor between 10 k $\Omega$  and 100 k $\Omega$  is recommended. Nominal voltage on this pin is 3 V.

### 7.2.11 Soft Start, SS

The  $V_{SS}$  supply is discharged for  $V_{VCC}$  low conditions. When enabled, SS charges an external capacitor with a current source. This voltage is used as the voltage error signal during start-up, enabling the PWM duty cycle to increase slowly. In the event of a  $V_{VCC}$  dropout, the OVP/EN is forced below 1.9 V (typical), SS quickly discharges to disable the PWM.

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#### NOTE

In an open-loop test circuit, grounding the SS pin does not ensure 0% duty cycle. See the [Application and Implementation](#) section for details.

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### 7.2.12 Voltage amplifier output, VAOUT

This is the output of the operational amplifier that regulates output voltage. The voltage amplifier output is internally limited to approximately 5.5 V to prevent overshoot.

## Feature Description (continued)

### 7.2.13 Positive Supply Voltage, VCC

Connect to a stable source of at least 20 mA between 10 V and 17 V for normal operation. Bypass  $V_{CC}$  directly to GND to absorb supply current spikes required to charge external MOSFET gate capacitances. To prevent inadequate gate drive signals, the output devices are inhibited unless  $V_{VCC}$  exceeds the upper under-voltage lockout voltage threshold and remains above the lower threshold.

### 7.2.14 Feed-Forward Voltage, VFF

The RMS voltage signal generated at this pin by mirroring 1/2 of the  $I_{IAC}$  into a single pole external filter. At low line, the VFF voltage should be 1.4 V.

### 7.2.15 Voltage Amplifier Inverting Input, VSENSE

The VSENSE pin is normally connected to a compensation network and to the boost converter output through a divider network.

### 7.2.16 Voltage Reference Output, VREF

$V_{REF}$  is the output of an accurate 7.5-V voltage reference. This output is capable of delivering 20 mA to peripheral circuitry and is internally short-circuit current limited. VREF is disabled and remains at 0 V when  $V_{CC}$  is below the UVLO threshold. Bypass VREF to GND with a 0.1- $\mu$ F or larger ceramic capacitor for best stability. See [Figure 8](#) and [Figure 9](#) for VREF line and load regulation characteristics.

## 8 Application and Implementation

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### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

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### 8.1 Application Information

The UCC2818A-Q1 is a BiCMOS average current mode boost controller for high-power-factor high-efficiency preregulator power supplies. [Figure 1](#) shows the UCC2818A-Q1 in a 250-W PFC preregulator circuit. Off-line switching power converters normally have an input current that is not sinusoidal. The input current waveform has a high harmonic content because current is drawn in pulses at the peaks of the input voltage waveform. An active power-factor correction circuit programs the input current to follow the line voltage, forcing the converter to look like a resistive load to the line. A resistive load has 0° phase displacement between the current and voltage waveforms. Power factor (PF) can be defined in terms of the phase angle between two sinusoidal waveforms of the same frequency:

$$PF = \cos \theta \quad (3)$$

Therefore, a purely resistive load would have a power factor of 1. In practice, power factors of 0.999 with total harmonic distortion (THD) of less than 3% are possible with a well-designed circuit. Following guidelines are provided to design PFC boost converters using the UCC2818A-Q1.

### NOTE

Schottky diodes, D5 and D6, are required to protect the PFC controller from electrical over stress during system power up.

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## 8.2 Typical Application

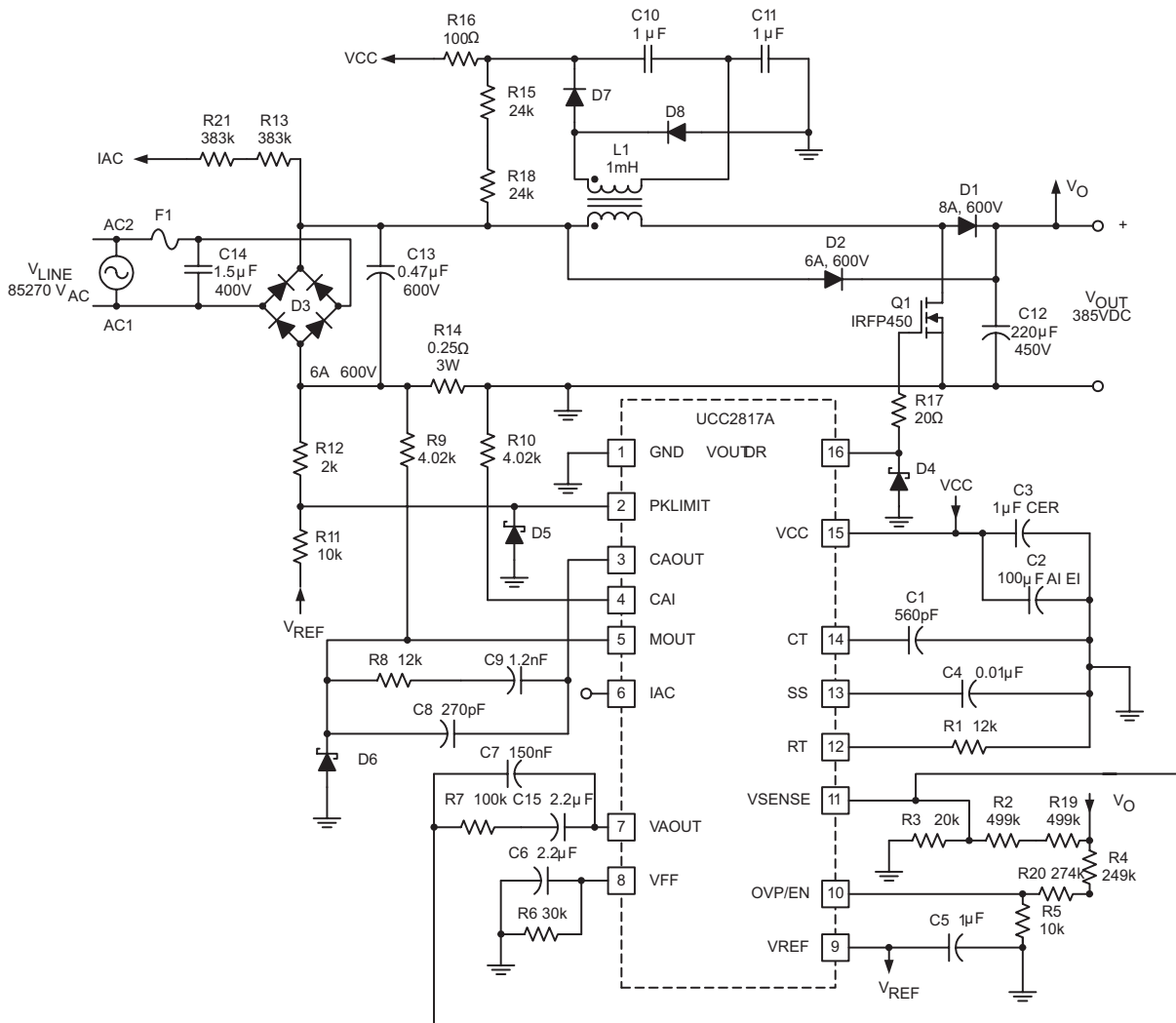


Figure 1. Typical Application Circuit

### 8.2.1 Detailed Design Procedure

#### 8.2.1.1 Power Stage

##### 8.2.1.1.1 L<sub>BOOST</sub>

The boost inductor value is determined by Equation 4:

$$L_{\text{BOOST}} = \frac{(V_{\text{IN}(\text{min})} \times D)}{(\Delta I \times f_s)}$$

where

- D = Duty cycle
- $\Delta I$  = Inductor ripple current
- $f_s$  = Switching frequency

(4)

For the example circuit, a switching frequency of 100 kHz, a ripple current of 875 mA, a maximum duty cycle of 0.688, and a minimum input voltage of 85 V<sub>RMS</sub> produces a boost inductor value of about 1 mH. The values used in this equation are at the peak of low line, where the inductor current and its ripple are at a maximum.

## Typical Application (continued)

### 8.2.1.1.2 C<sub>OUT</sub>

Two main criteria, the capacitance and the voltage rating, dictate the selection of the output capacitor. The value of capacitance is determined by the holdup time required for supporting the load after input ac voltage is removed. Holdup is the amount of time that the output stays in regulation after the input has been removed. For this circuit, the desired holdup time is approximately 16 ms. Expressing the capacitor value in terms of output power, output voltage, and holdup time gives Equation 5:

$$C_{OUT} = \frac{(2 \times P_{OUT} \times \Delta t)}{(V_{OUT}^2 - V_{OUT(min)}^2)} \quad (5)$$

In practice, the calculated minimum capacitor value may be inadequate because output ripple voltage specifications limit the amount of allowable output capacitor ESR. Attaining a sufficiently low value of ESR often necessitates the use of a much larger capacitor value than calculated. The amount of output capacitor ESR allowed can be determined by dividing the maximum specified output ripple voltage by the inductor ripple current. In this design holdup time was the dominant determining factor and a 220- $\mu$ F, 450-V capacitor was chosen for the output voltage level of 385 VDC at 250 W.

### 8.2.1.1.3 Power Switch Selection

As in any power-supply design, tradeoffs between performance, cost, and size have to be made. When selecting a power switch, it can be useful to calculate the total power dissipation in the switch for several different devices at the switching frequencies being considered for the converter. Total power dissipation in the switch is the sum of switching loss and conduction loss. Switching losses are the combination of the gate charge loss, C<sub>OSS</sub> loss, and turnon and turnoff losses:

$$P_{GATE} = Q_{GATE} \times V_{GATE} \times f_s$$

where

- Q<sub>GATE</sub> = Total gate charge
- V<sub>GATE</sub> = Gate drive voltage
- f<sub>s</sub> = Clock frequency

$$P_{COSS} = \frac{1}{2} \times C_{OSS} \times V_{OFF}^2 \times f_s$$

where

- C<sub>OSS</sub> = Drain source capacitance of the MOSFET
- V<sub>OFF</sub> = Voltage across the switch during the off time (in this case V<sub>OFF</sub> = V<sub>OUT</sub>)

$$P_{ON} + P_{OFF} = \frac{1}{2} \times V_{OFF} \times I_L \times (t_{ON} + t_{OFF}) \times f_s$$

where

- I<sub>L</sub> = Peak inductor current
- t<sub>ON</sub> and t<sub>OFF</sub> = Switching times (estimated using device parameters R<sub>GATE</sub>, Q<sub>GD</sub> and V<sub>TH</sub>)

Conduction loss is calculated as the product of the R<sub>DS(on)</sub> of the switch (at the worst-case junction temperature) and the square of RMS current:

$$P_{COND} = R_{DS(on)} \times K \times I_{RMS}^2$$

where

- K = temperature factor found in the manufacturer's R<sub>DS(on)</sub> vs junction temperature curves

## Typical Application (continued)

Calculating these losses and plotting against frequency gives a curve that enables the designer to determine which manufacturer's device has the best performance at the desired switching frequency, or which switching frequency has the least total loss for a particular power switch. For this design example, an IRFP450 HEXFET™ from International Rectifier was chosen because of its low  $R_{DS(on)}$  and its  $V_{DSS}$  rating. The IRFP450  $R_{DS(on)}$  of 0.4  $\Omega$  and the maximum  $V_{DSS}$  of 500 V made it an ideal choice. A review of this procedure can be found in the Unitrode™ Power-Supply Design Seminar SEM1200, Topic 6, Design Review: 140 W (*Multiple Output High Density DC/DC Converter*).

### 8.2.1.2 Soft Start

The soft-start circuitry is used to prevent overshoot of the output voltage during start up. This is accomplished by slowly bringing up the voltage amplifier output ( $V_{VAOUT}$ ), which allows for the PWM duty cycle to slowly increase. Use Equation 9 to select a capacitor for the soft-start pin.

In this example,  $t_{DELAY} = 7.5$  ms, which yields a  $C_{SS}$  of 10 nF.

$$C_{SS} = \frac{10 \mu A \times t_{DELAY}}{7.5 V} \quad (9)$$

In an open-loop test circuit, shorting the soft-start pin to ground does not ensure 0% duty cycle. This is due to the current amplifiers input offset voltage, which could force the current amplifier output high or low depending on the polarity of the offset voltage. However, in the typical application, there is sufficient amount of inrush and bias current to overcome the current amplifier offset voltage.

### 8.2.1.3 Multiplier

The output of the multiplier of the UCC2818A-Q1 is a signal representing the desired input line current. It is an input to the current amplifier, which programs the current loop to control the input current to give high power factor operation. As such, the proper functioning of the multiplier is key to the success of the design. The inputs to the multiplier are VAOUT, the voltage amplifier error signal,  $I_{IAC}$ , a representation of the input rectified ac line voltage, and an input voltage feed-forward signal,  $V_{VFF}$ . The output of the multiplier,  $I_{MOUT}$ , can be expressed as:

$$I_{MOUT} = I_{IAC} \times \frac{(V_{VAOUT} - 1)}{K \times V_{VFF}^2}$$

where

- $K =$  Constant typically equal to 1/V (10)

The *Electrical Characteristics* table covers all the required operating conditions for designing with the multiplier. Additionally, curves in Figure 10, Figure 11, and Figure 12 provide typical multiplier characteristics over its entire operating range.

The  $I_{IAC}$  signal is obtained through a high-value resistor connected between the rectified ac line and the IAC pin of the UCC2818A-Q1. This resistor  $R_{IAC}$  is sized to give the maximum  $I_{IAC}$  current at high line. For the UCC2818A-Q1, the maximum  $I_{IAC}$  current is about 500  $\mu A$ . A higher current than this can drive the multiplier out of its linear range. A smaller current level is functional, but noise can become an issue, especially at low input line. Assuming a universal line operation of 85  $V_{RMS}$  to 265  $V_{RMS}$  gives a  $R_{IAC}$  value of 750 k $\Omega$ , because of voltage-rating constraints of a standard 1/4-W resistor, use a combination of lower-value resistors connected in series to give the required resistance and distribute the high voltage amongst the resistors. For this design example, two 383-k $\Omega$  resistors were used in series.

The current into the IAC pin is mirrored internally to the VFF pin where it is filtered to produce a voltage feed-forward signal proportional to line voltage. The VFF voltage is used to keep the power-stage gain constant, and to provide input power limiting. See the TI application report [SLUA196](#) for detailed explanation on how the VFF pin provides power limiting. The following equation can be used to size the VFF resistor  $R_{VFF}$  to provide power limiting where  $V_{IN(min)}$  is the minimum RMS input voltage, and  $R_{IAC}$  is the total resistance connected between the IAC pin and the rectified line voltage.

### Typical Application (continued)

$$R_{VFF} = \frac{1.4 \text{ V}}{\frac{V_{IN(\min)} \times 0.9}{2 \times R_{IAC}}} \approx 30 \text{ k}\Omega \quad (11)$$

Because the VFF voltage is generated from line voltage, it needs to be adequately filtered to reduce THD caused by the 120-Hz rectified line voltage. Refer to Unitrode Power-Supply Design Seminar, SEM-700 Topic 7 (*Optimizing the Design of a High Power Factor Preregulator*). A single pole filter was adequate for this design. Assuming that an allocation of 1.5% total harmonic distortion from this input is allowed, and that the second harmonic ripple is 66% of the input ac line voltage, the amount of attenuation required by this filter is:

$$\frac{1.5 \%}{66 \%} = 0.022 \quad (12)$$

A ripple frequency ( $f_R$ ) of 120 Hz and an attenuation of 0.022 requires that the pole of the filter ( $f_P$ ) be placed at:

$$f_P = 120 \text{ Hz} \times 0.022 \approx 2.6 \text{ Hz} \quad (13)$$

The following equation can be used to select the filter capacitor  $C_{VFF}$  required to produce the desired low-pass filter.

$$C_{VFF} = \frac{1}{2 \times \pi \times R_{VFF} \times f_P} \approx 2.2 \mu\text{F} \quad (14)$$

The  $R_{MOUT}$  resistor is sized to match the maximum current through the sense resistor to the maximum multiplier current. The maximum multiplier current, or  $I_{MOUT(\max)}$ , can be determined by the equation:

$$I_{MOUT(\max)} = \frac{I_{IAC@V_{IN(\min)}} \times (V_{VAOUT(\max)} - 1 \text{ V})}{K \times V_{VFF(\min)}^2} \quad (15)$$

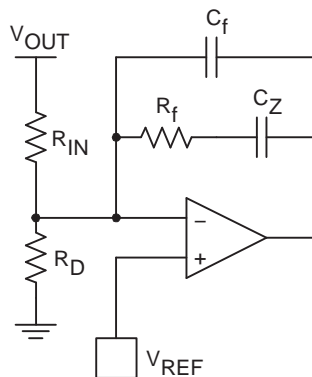
$I_{MOUT(\max)}$  for this design is approximately 315  $\mu\text{A}$ . The  $R_{MOUT}$  resistor can then be determined by:

$$R_{MOUT} = \frac{V_{RSENSE}}{I_{MOUT(\max)}} \quad (16)$$

In this example,  $V_{RSENSE}$  was selected to give a dynamic operating range of 1.25 V, which gives an  $R_{MOUT}$  of roughly 3.91 k $\Omega$ .

#### 8.2.1.4 Voltage Loop

The second major source of harmonic distortion is the ripple on the output capacitor at the second harmonic of the line frequency. This ripple is fed back through the error amplifier and appears as a third harmonic ripple at the input to the multiplier. The voltage loop must be compensated not just for stability but also to attenuate the contribution of this ripple to the total harmonic distortion of the system (see [Figure 2](#)).



**Figure 2. Voltage Amplifier Configuration**

### Typical Application (continued)

The gain of the voltage amplifier,  $G_{VA}$ , can be determined by first calculating the amount of ripple present on the output capacitor. The peak value of the second harmonic voltage is given by the equation:

$$V_{OPK} = \frac{P_{IN}}{2\pi \times f_R \times C_{OUT} \times V_{OUT}} \quad (17)$$

In this example,  $V_{OPK} = 3.91$  V. Assuming an allowable contribution of 0.75% (1.5% peak to peak) from the voltage loop to the THD budget, set the gain equal to:

$$G_{VA} = \frac{(\Delta V_{VAOUT})^{0.015}}{2 \times V_{OPK}}$$

where

- $\Delta V_{VAOUT}$  = Effective output voltage range of the error amplifier (5 V for the UCC2818A-Q1) (18)

The network needed to realize this filter is comprised of an input resistor,  $R_{IN}$ , and feedback components  $C_f$ ,  $C_Z$ , and  $R_f$ . The value of  $R_{IN}$  is already determined because of its function as one-half of a resistor divider from  $V_{OUT}$  feeding back to the voltage amplifier for output voltage regulation. In this case, the value was chosen to be 1 M $\Omega$ . This high value was chosen to reduce power dissipation in the resistor. In practice, the resistor value would be realized by the use of two 500-k $\Omega$  resistors in series because of the voltage rating constraints of most standard 1/4-W resistors. The value of  $C_f$  is determined by the equation:

$$C_f = \frac{1}{2\pi \times f_R \times G_{VA} \times R_{IN}} \quad (19)$$

In this example,  $C_f = 150$  nF. Resistor  $R_f$  sets the dc gain of the error amplifier and, thus, determines the frequency of the pole of the error amplifier. The location of the pole can be found by setting the gain of the loop equation to one and solving for the crossover frequency. The frequency, expressed in terms of input power, can be calculated by the equation:

$$f_{VI}^2 = \frac{P_{IN}}{(2\pi)^2 \times \Delta V_{VAOUT} \times V_{OUT} \times R_{IN} \times C_{OUT} \times C_f} \quad (20)$$

The  $f_{VI}$  value for this converter is 10 Hz. A derivation of this equation can be found in the Unitrode Power Supply Design Seminar SEM1000, Topic 1 (*A 250-kHz, 500-W Power Factor Correction Circuit Employing Zero Voltage Transitions*).

Solving for  $R_f$  becomes:

$$R_f = \frac{1}{2\pi \times f_{VI} \times C_f} \quad (21)$$

or  $R_f = 100$  k $\Omega$ .

Because of the low output impedance of the voltage amplifier, capacitor  $C_Z$  was added in series with  $R_f$  to reduce loading on the voltage divider. To ensure the voltage loop crossed over at  $f_{VI}$ ,  $C_Z$  was selected to add a zero at 1/10th of  $f_{VI}$ . For this design, a 2.2- $\mu$ F capacitor was chosen for  $C_Z$ . The following equation can be used to calculate  $C_Z$ :

$$C_Z = \frac{1}{2 \times \pi \times \frac{f_{VI}}{10} \times R_f} \quad (22)$$

#### 8.2.1.5 Current Loop

The gain of the power stage is:

$$G_{ID}(s) = \frac{V_{OUT} \times R_{SENSE}}{s \times L_{BOOST} \times V_P} \quad (23)$$

### Typical Application (continued)

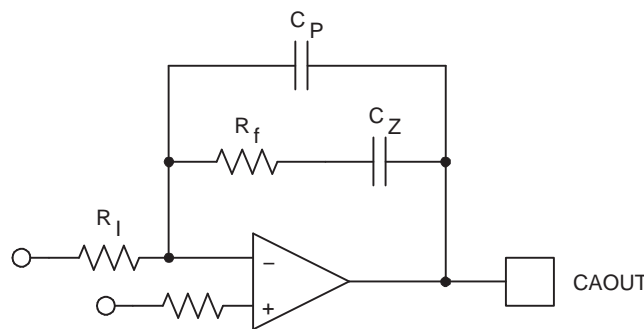
The value of  $R_{SENSE}$  was selected to provide the desired differential voltage for the current sense amplifier at the desired current limit point. In this example, a current limit of 4 A and a reasonable differential voltage to the current amplifier of 1 V gives a  $R_{SENSE}$  value of 0.25  $\Omega$ .  $V_P$  in this equation is the voltage swing of the oscillator ramp, 4 V for the UCC2818A-Q1. Setting the crossover frequency of the system to 1/10th of the switching frequency, or 10 kHz, requires a power-stage gain at that frequency of 0.383. In order for the system to have a gain of 1 at the crossover frequency, the current amplifier must have a gain of  $1/G_{ID}$  at that frequency.  $G_{EA}$ , the current amplifier gain is then:

$$G_{EA} = \frac{1}{G_{ID}} = \frac{1}{0.383} = 2.611 \quad (24)$$

$R_I$  is the  $R_{MOUT}$  resistor, previously calculated to be 3.9 k $\Omega$  (see [Figure 3](#)). The gain of the current amplifier is  $R_f/R_I$ , so multiplying  $R_I$  by  $G_{EA}$  gives the value of  $R_f$ , in this case approximately 12 k $\Omega$ . Setting a zero at the crossover frequency and a pole at one-half the switching frequency completes the current loop compensation.

$$C_Z = \frac{1}{2 \times \pi \times R_f \times f_C} \quad (25)$$

$$C_P = \frac{1}{2 \times \pi \times R_f \times \frac{f_S}{2}} \quad (26)$$



**Figure 3. Current Loop Compensation**

The UCC2818A-Q1 current amplifier has the input from the multiplier applied to the inverting input. This change in architecture from previous TI PFC controllers improves noise immunity in the current amplifier. It also adds a phase inversion into the control loop. The UCC2818A-Q1 takes advantage of this phase inversion to implement leading-edge duty cycle modulation. Synchronizing a boost PFC controller to a downstream dc-to-dc controller reduces the ripple current seen by the bulk capacitor between stages, reducing capacitor size and cost and reducing EMI. This is explained in greater detail in a following section. The UCC2818A-Q1 current amplifier configuration is shown in [Figure 4](#).

## Typical Application (continued)

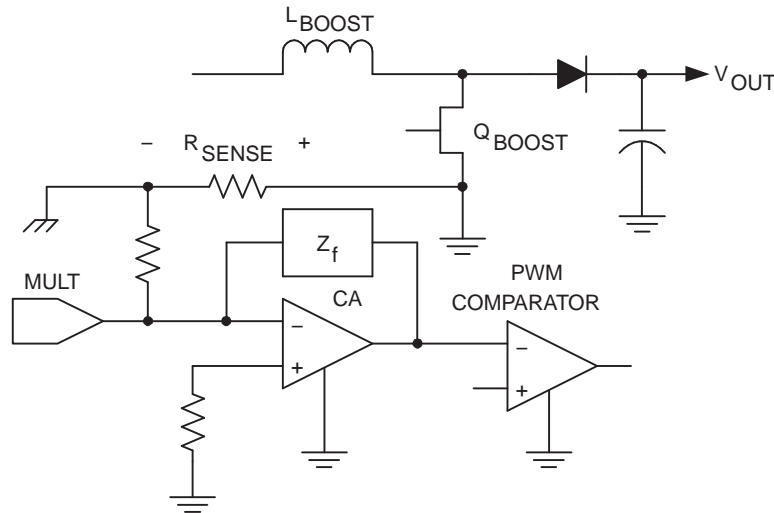


Figure 4. Current Amplifier Configuration

### 8.2.1.5.1 Start Up

The UCC2818 version of the device is intended to have  $V_{CC}$  connected to a 12-V supply voltage. The UCC2817A has an internal shunt regulator enabling the device to be powered from bootstrap circuitry, as shown in the typical application circuit of Figure 1. The current drawn by the UCC2818A-Q1 during undervoltage lockout, or start-up current, is typically 150  $\mu$ A. Once  $V_{CC}$  is above the UVLO threshold, the device is enabled and draws 4 mA typically. A resistor connected between the rectified ac line voltage and the  $V_{CC}$  pin provides current to the shunt regulator during power up. Once the circuit is operational, the bootstrap winding of the inductor provides the  $V_{CC}$  voltage. Sizing of the start-up resistor is determined by the start-up time requirement of the system design.

$$I_C = C \frac{\Delta V}{\Delta t}$$

where

- $I_C$  = Charge current
- $C$  = Total capacitance at the  $V_{CC}$  pin
- $\Delta V$  = UVLO threshold
- $\Delta t$  = Allowed start-up time

(27)

$$R = \frac{V_{RMS} \times 0.9}{I_C}$$

(28)

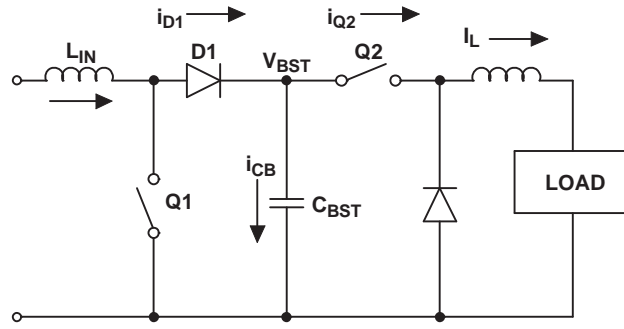
Assuming a 1-s allowed start-up time, a 16-V UVLO threshold, and a total  $V_{CC}$  capacitance of 100  $\mu$ F, a resistor value of 51 k $\Omega$  is required at a low line input voltage of 85  $V_{RMS}$ . The IC start-up current is sufficiently small as to be ignored in sizing the start-up resistor.

### 8.2.1.5.2 Capacitor Ripple Reduction

For a power system where the PFC boost converter is followed by a dc-to-dc converter stage, there are benefits to synchronizing the two converters. In addition to the usual advantages, such as noise reduction and stability, proper synchronization can significantly reduce the ripple currents in the boost circuit output capacitor. Figure 5 shows the impact of proper synchronization by showing a PFC boost converter together with the simplified input stage of a forward converter. The capacitor current during a single switching cycle depends on the status of the switches Q1 and Q2 and is shown in Figure 6. With a synchronization scheme that maintains conventional trailing-edge modulation on both converters, the capacitor current ripple is highest. The greatest ripple current cancellation is attained when the overlap of Q1 offtime and Q2 ontime is maximized. One method of achieving this is to synchronize the turnon of the boost diode (D1) with the turnon of Q2. This approach implies that the

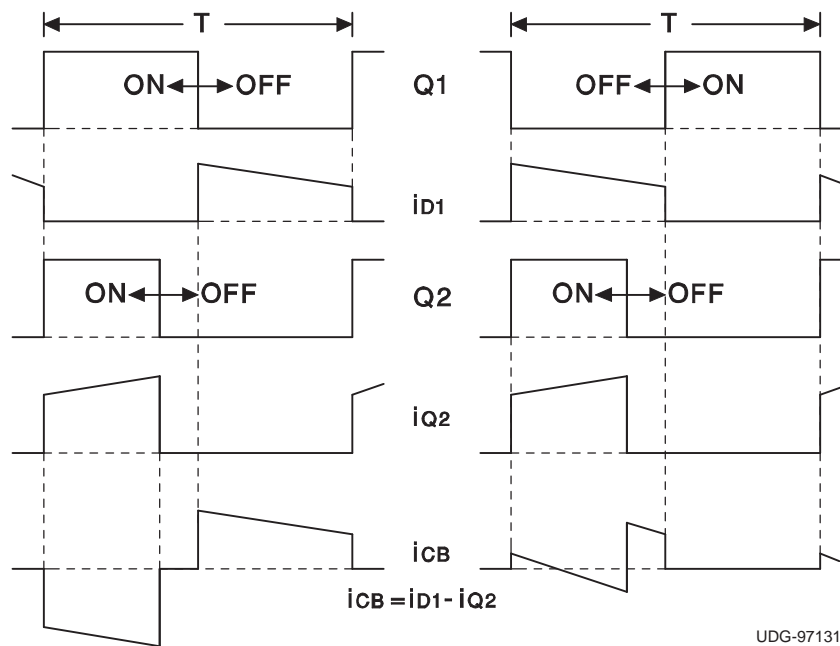
**Typical Application (continued)**

boost converter leading edge is pulse width modulated, while the forward converter is modulated with traditional trailing-edge PWM. The UCC2818A-Q1 is designed as a leading edge modulator with easy synchronization to the downstream converter to facilitate this advantage. Table 1 compares the  $I_{CB(rms)}$  for D1/Q2 synchronization as offered by UCC2818A-Q1, versus the  $I_{CB(rms)}$  for the other extreme of synchronizing the turnon of Q1 and Q2 for a 200-W power system with a  $V_{BST}$  of 385 V.



UDG-97130-1

**Figure 5. Simplified Representation of a Two-Stage PFC Power Supply**



UDG-97131

**Figure 6. Timing Waveforms for Synchronization Scheme**

**Table 1. Effects of Synchronization on Boost Capacitor Current**

	$V_{IN} = 85\text{ V}$		$V_{IN} = 120\text{ V}$		$V_{IN} = 240\text{ V}$	
	Q1/Q2	D1/Q2	Q1/Q2	D1/Q2	Q1/Q2	D1/Q2
D(Q2)	Q1/Q2	D1/Q2	Q1/Q2	D1/Q2	Q1/Q2	D1/Q2
0.35	1.491 A	0.835 A	1.341 A	0.663 A	1.024 A	0.731 A
0.45	1.432 A	0.93 A	1.276 A	0.664 A	0.897 A	0.614 A

Table 1 shows that the boost capacitor ripple current can be reduced by about 50% at nominal line and about 30% at high line with the synchronization scheme facilitated by the UCC2818A-Q1. Figure 7 shows the suggested technique for synchronizing the UCC2818A-Q1 to the downstream converter. With this technique, maximum ripple reduction as shown in Figure 6 is achievable. The output capacitance value can be significantly reduced if its choice is dictated by ripple current or the capacitor life can be increased as a result. In cost-sensitive designs where holdup time is not critical, this is a significant advantage.

An alternative method of synchronization to achieve the same ripple reduction is possible. In this method, the turnon of Q1 is synchronized to the turnoff of Q2. While this method yields almost identical ripple reduction and maintains trailing edge modulation on both converters, the synchronization is much more difficult to achieve and the circuit can become susceptible to noise as the synchronizing edge itself is being modulated.

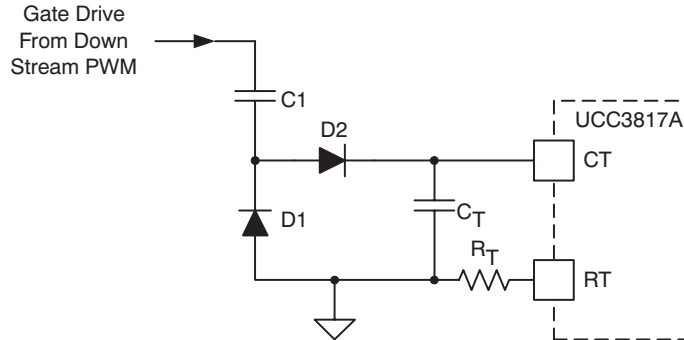
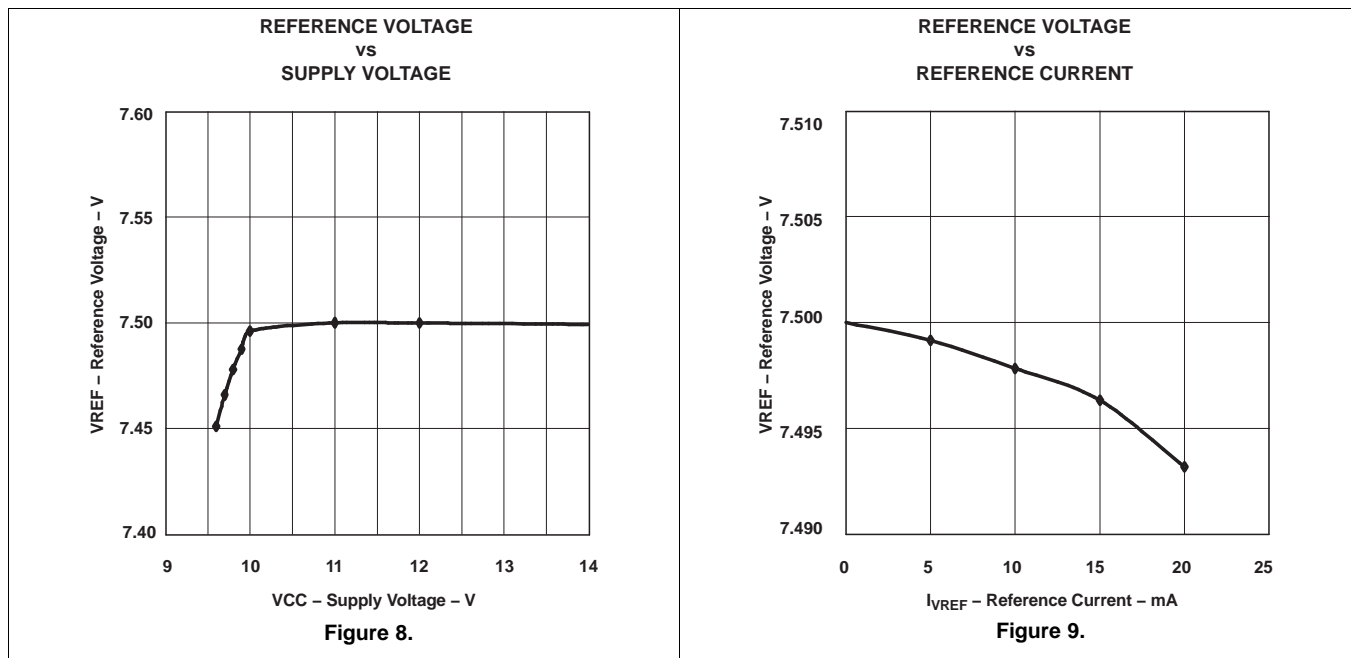
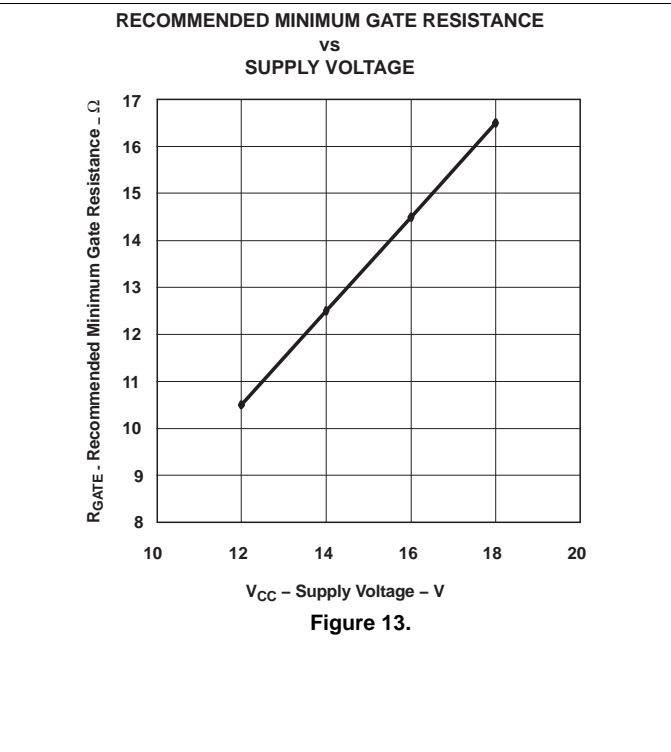
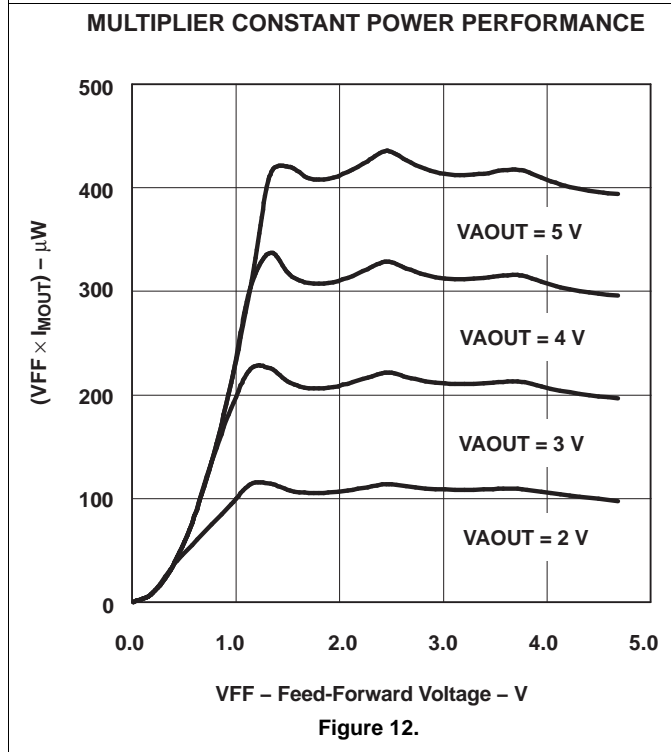
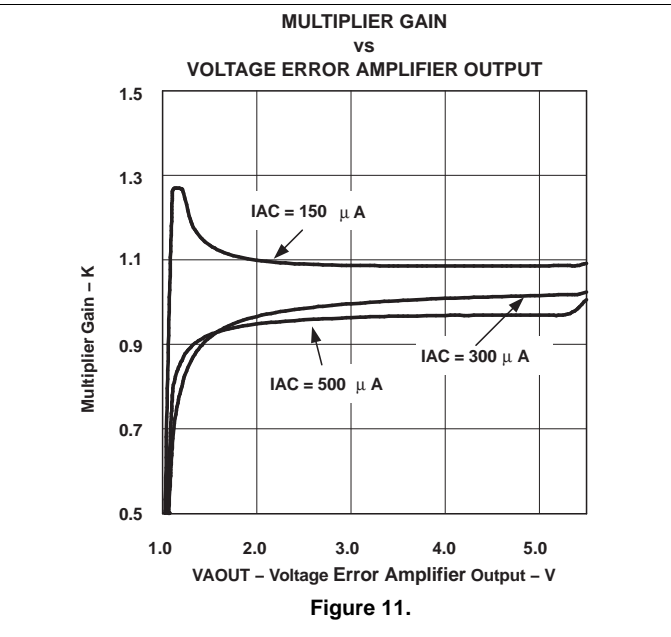
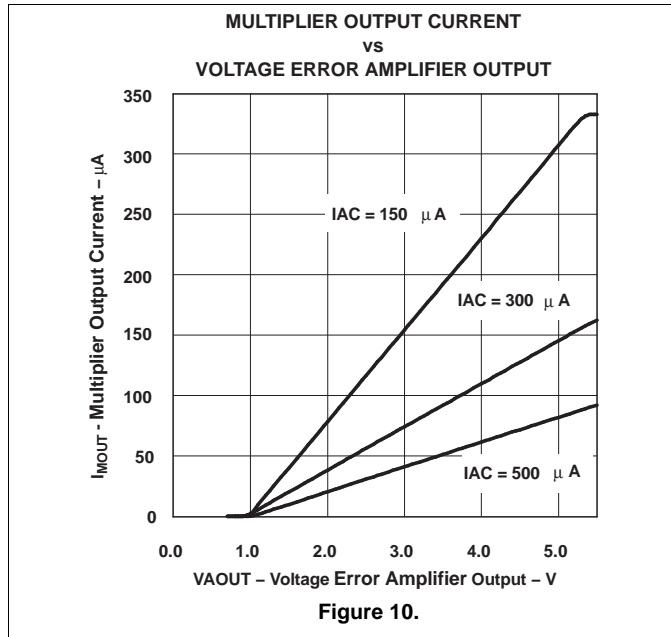


Figure 7. Synchronizing to a Downstream Converter

### 8.2.2 Application Curves





## 9 Device and Documentation Support

### 9.1 Device Support

#### 9.1.1 Development Support

Evaluation Module, UCC3817EVM, 385V, 250W PFC Boost Converter, <http://www.ti.com/tool/UCC3817EVM>

## 9.2 Documentation Support

### 9.2.1 Related Documentation

For related documentation see the following:

- *Differences Between UCC3817A/18A/19A and UCC3817/18/19*, [SLUA294](#)
- *Using the UCC3817EVM*, [SLUU077](#)
- *Synchronizing a PFC Controller from a Downstream Converter's Gate Drive*, [SLUA245](#)
- Seminar topic, High Power Factor Switching Preregulator Design Optimization, L.H. Dixon, SEM-700, 1990.
- Seminar topic, High Power Factor Preregulator for Off-line Supplies, L.H. Dixon, SEM-600, 1988.

## 9.3 Trademarks

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## 9.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## 9.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">UCC2818AQDRQ1</a>	NRND	Production	SOIC (D)   16	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2818AQ
UCC2818AQDRQ1.A	NRND	Production	SOIC (D)   16	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2818AQ

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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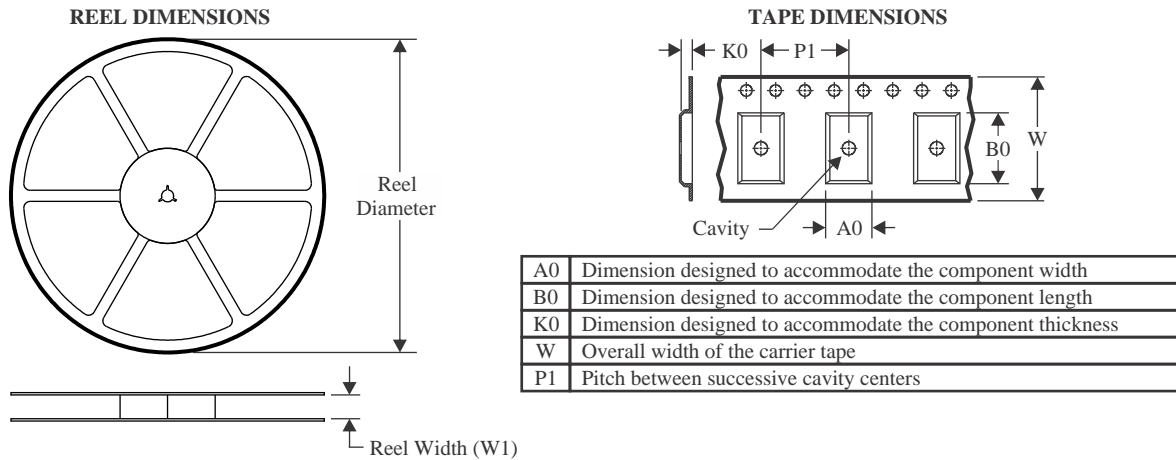
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF UCC2818A-Q1 :**

- Catalog : [UCC2818A](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC2818AQDRQ1	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC2818AQDRQ1	SOIC	D	16	2500	353.0	353.0	32.0

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040047-6/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  -  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.

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