Buck PFC Controller

Check for Samples: UCC29910A

FEATURES

- **Buck Power Factor Correction for High Efficiency Across Line**
- **Low Off-Line Startup Current, With SmartStart Algorithm for Fast Startup With Soft-Start**
- **Compatible With Resistive or Pass Transistor Fed Startup from the AC Line**
- **Low Power SmartBurst Mode for Standby and Light-Load Conditions**
- **Current Sense Inputs for PFC control and Overload Protection**
- **Line Sense UVLO**
- **Sense and Drive Control for External Startup Depletion Mode FET**
- **Latching Fault Input Pin**

APPLICATIONS

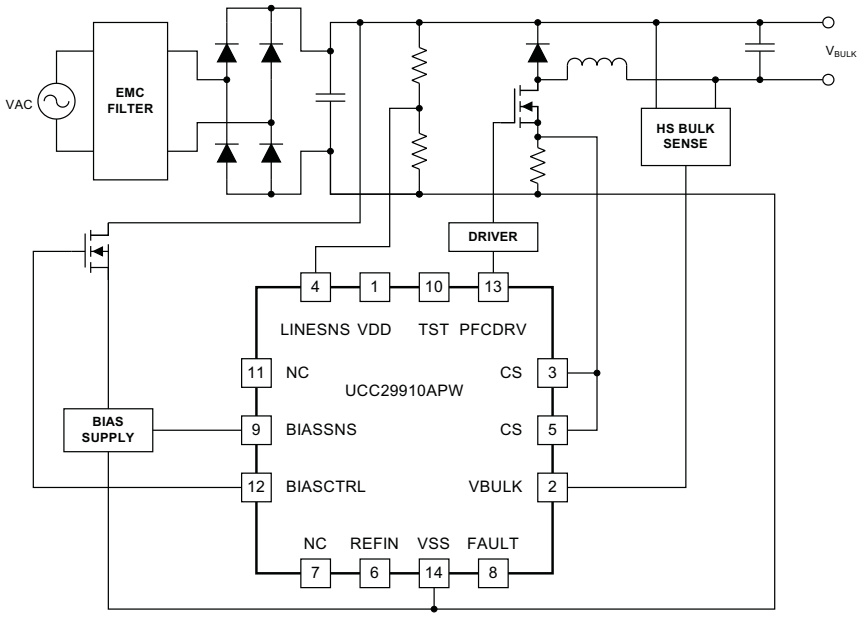
- **High Efficiency AC-DC Adapters**
- **Low Profile and High Density Adapters**

DESCRIPTION

The UCC29910A Buck Power Factor Correction (PFC) controller provides a relatively flat high-efficiency performance across universal line for designers requiring a high power factor (>0.9) and wishing to meet the requirements of IEC 61000-3-2. Based on a buck topology, inherent inrush current limiting eliminates the need for additional components. With a typical bus voltage of 84 V, the topology is ideally suited for use with low voltage stress downstream regulation/isolation power trains, such as half-bridge stages controlled by the UCC29900, (Texas Instruments Literature Number, SLUS923). This combination offers low common-mode noise generation allowing reduced filtering and exceptionally high conversion efficiency.

The UCC29910A incorporates AC line UVLO and controlled soft start for fast start-up. Enhanced light-load efficiency is achieved through advanced management algorithms for best-in-class no-load and light-load performance.

SIMPLIFIED APPLICATION DIAGRAM



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

PART NUMBER	PACKAGE	PACKING
UCC29910APW	Plastic, 14-Pin TSSOP (PW)	90-Pc. Tube
UCC29910APWR	Plastic, 14-Pin TSSOP (PW)	2000-Pc. Tape and Reel

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)(2)(3)

		VALUE	UNIT
V_{DD}	Supply Voltage	4.1	V
		-0.3	
	Voltage: All pins	−0.3 to VDD + 0.3	
T_A	Operating free air temperature, (4)	−40 to 105	°C
T_J	Operational junction temperature, (4)		
T_{STG}	Storage temperature (4)	−40 to 105	
	Lead temperature (10 seconds)	260	

(1) These are stress limits. Stress beyond these limits may cause permanent damage to the device. Functional operation of the device at these or any conditions beyond those indicated under RECOMMENDED OPERATING CONDITIONS is not implied. Exposure to absolute maximum rated conditions for extended periods of time may affect device reliability.
(2) All voltages are with respect to VSS.
(3) All currents are positive into the terminal, negative out of the terminal.
(4) Higher temperature may be applied during board soldering process according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.

THERMAL INFORMATION

THERMAL METRIC(1)		PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance(2)		°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)		
θ_{JB}	Junction-to-board thermal resistance(4)		
ψ_{JT}	Junction-to-top characterization parameter(5)		
ψ_{JB}	Junction-to-board characterization parameter(6)		
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(7)		

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range, all the voltages refer to the VSS pin (unless otherwise noted)

		MIN	NOM	MAX	UNIT
T_A	Operating free air temperature	−40		105	°C
	VDD Input Voltage	3.0		3.6	V
	All Inputs	0		VDD	

ELECTRICAL CHARACTERISTICS

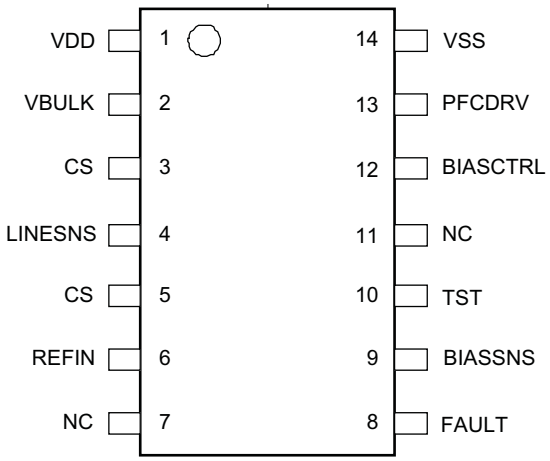
over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Current						
I_{VDD}	Operating current	V_{DD} = 3.3 V		5	8	mA
Voltage Monitoring (1)						
V_{NM}	VBULK nominal	Normal mode(2) PFCDRV = 100 kHz	1.042	1.048	1.054	V
V_{BH}	VLINESNS start-up	VB(min) < VBIASSNS < $V_{B(max)}$	258	264	270	mVRMS
V_{BL}	VLINESNS brownout	Normal mode(2)	243	249	255	
V_{LM}	VLINESNS max	Normal mode(2)	925	931	937	
$V_{B(max)}$	VBIASSNS max	VLINESNS > V_{BH}	907	913	919	mV
$V_{B(min)}$	VBIASSNS min	VLINESNS > V_{BH}	451	457	463	
FAULT Input						
t_f	Latch Time(3)	Normal mode(2), FAULT pin goes < 0.8 V		100		µs
V_{IT+}	Positive going input threshold voltage		1.45		2.5	V
V_{IT-}	Negative going input threshold voltage		0.8		1.85	
V_{HYS}	Input voltage hysteresis VIT+ - VIT-		0.3		1	
PFCDRV section						
f_{SW}	Switching frequency	Normal mode(2)	94	100	106	kHz
D_{MAX}	Max duty cycle	At PFCDRV pin, normal mode(2), VLINESNS = V_{BH}, VBULK = 1.025 V	89%	90%	91%	
V_{OH}	High level output voltage at PFCDRV pin	I_O = -1.5 mA	VDD-0.25V		VDD	V
		I_O = -6 mA	VDD-0.6V		VDD	
V_{OL}	Low Level Output Voltage at PFCDRV pin	I_O = 1.5 mA	0		0.25	
		I_O = 6 mA	0		0.6	
BIASCTRL Output						
V_{BC}	Low level output voltage at BIASCTRL pin	Start-up mode(4), VBIASSNS increasing and < $V_{B(max)}$, I_O = 1.5 mA	0		0.25	V
	High level output voltage at BIASCTRL pin	Start-up mode(4), VBIASSNS decreasing and > $V_{B(min)}$, I_O = -1.5mA	VDD-0.25V		VDD	

(1) VBULK, VLINESNS and VBIASSNS voltage thresholds are based on VREFIN = 1.500 V. These will change proportionally as VREFIN changes. Input bias current at these pins is ±50 nA max.
(2) Normal mode entered when VDD present, V_{REFIN} = 1.500 V, VLINESNS increased from 0 to V_{BH} < VLINESNS < V_{LM}, VBIASSNS increased from 0 to $V_{B(max)}$ < VBIASSNS < 1.025 V then reduced to $V_{B(min)}$ < VBIASSNS < $V_{B(max)}$, V_{CS} = 150 mV, VBULK increased to V_{NM} then reduced to 1.025 V. There is a 600-ms timeout on this process.
(3) FAULT inputs shorter than t_f cause a non-latched shutdown. FAULT inputs longer than t_f cause a latched shutdown.
(4) Start-up mode entered when VDD present, VLINESNS increased from 0 to V_{BH} < VLINESNS < V_{LM} , VBIASSNS increased from 0 to $V_{B(max)}$ < VBIASSNS < 1.025 V then reduced to $V_{B(min)}$ < VBIASSNS < $V_{B(max)}$, VBULK = 0 V. There is a 600 ms timeout on this process.

DEVICE INFORMATION

UCC29910A 14- Pin TSSOP (PW)



TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
VDD	1	-	Provides power to the device; should be decoupled with ceramic capacitor (1 µF), connected directly across pins 1-14.
VBULK	2	I	Voltage sensing of the bulk capacitor.
CS	3	I	Current sense input for PFC stage.
LINESNS	4	I	Rectified AC line sense input.
CS	5	I	Current sense input for PFC stage.
REFIN	6	I	Reference input for internal comparators/error amplifier.
NC	7	-	NC, this pin is not used, and should be left open.
FAULT	8	I	Fault input for over-voltage or over-load protection.
BIASSNS	9	I	Sense input for the bias rail for startup control.
TST	10	I	This pin should be connected directly to VDD.
NC	11	-	No connection should be made to this pin.
BIASCTRL	12	O	Control output for the external startup FET for startup control.
PFCDRV	13	O	Drive for PFC FET.
VSS	14	-	Ground for internal circuitry.

Detailed Pin Description

Pin 1 – VDD: This pin supplies power to the device. A minimum supply voltage level of 3.0 V and maximum of 3.6 V is recommended.

Pin 2 – VBULK: The output voltage level, V_{BULK} is sensed on this pin. The HV bulk sensing network should be scaled so that the desired output voltage produces V_{NM} at this pin. The Thevenin impedance at this pin should be below 20 kΩ, with appropriate capacitance provided for noise filtering.

NOTE

The V_{BULK} scaling and LINESNS scaling must maintain a ratio of close to 4:1 to ensure optimum operation of the SmartStart algorithm.

Pin 3 – CS: This pin senses the current in the PFC stage. Both CS pins must be connected to the current sense signal and it is not permissible to leave one floating. The CS pins are intended to sense average low side PFC FET current directly. A 150-mΩ current sense resistor value is optimal for powers of 90 W, with appropriate scaling for higher power levels. The recommended feed impedance level is approximately 100 Ω, and a capacitor of 1 µF is also recommended to act as a filter on the input current and to minimise noise pickup. A smaller value capacitor may result in possible current loop instability. A larger cap value may result in poor Power Factor (PF) due to excessive current signal phase shift. UCC29910A does not provide cycle-by-cycle inductor current limiting. An external circuit is needed if this type of protection is required.

Pin 4 – LINESNS: This pin senses the rectified line voltage. The internal reference for this pin is internally scaled to ¼ of the VBULK reference.

NOTE

The LINESNS scaling and VBULK scaling must maintain a ratio of close to 1:4 to ensure optimum operation of the SmartStart algorithm.

A peak of high-line voltage (typically 373-V for 264-VAC input) should be scaled to correspond to 1.158 V_{DC} at this pin. A pin feed impedance of less than 20 kΩ is recommended along with a filter capacitor of at least 2.2 nF for noise filtering. The RMS voltage at this pin must be greater than VBH before PFCDRV can start switching. The PFCDRV will go low if the RMS voltage drops below the brownout level V_{BL} (21 ms timeout). The controller will not start if VLINESNS exceeds VLM, (VBULK = 0 V).

Pin 5 – CS: See pin 3 description above. This pin senses the current in the PFC stage, pins 3 and 5 must be connected together.

Pin 6 – REFIN: This pin must be connected to an external accurate 1.500 V reference source, e.g. using a suitable shunt regulator with voltage setting resistors such as TLVH431A. The reference voltage must be established within 100 ms after VDD reaches 3.0 V.

Pin 7 – NC: This pin is not used, and should be left open.

Pin 8 – **FAULT:** This pin when pulled low causes PFCDRV and BIASCTRL to go low, typically within 10 us. After a 100 us delay the FAULT input is sampled again. If the FAULT has cleared high, the UCC29910A goes into SmartStart mode. If the FAULT input is still low the device enters a latched shutdown state.

Pin 9 – **BIASSNS:** This pin is used to sense the PFC stage bias rail (normally in the 8 V to 12 V range to drive the PFC power MOSFET) during start-up to allow control of the external start-up FET. The voltage at this pin must be greater than $V_{B(max)}$ before PFCDRV switching commences. If the voltage drops below $V_{B(min)}$ the BIASCTRL output goes low, which can enable an external start-up FET.

Pin 10 – **TST:** This pin provides no user function. It must be connected to VDD.

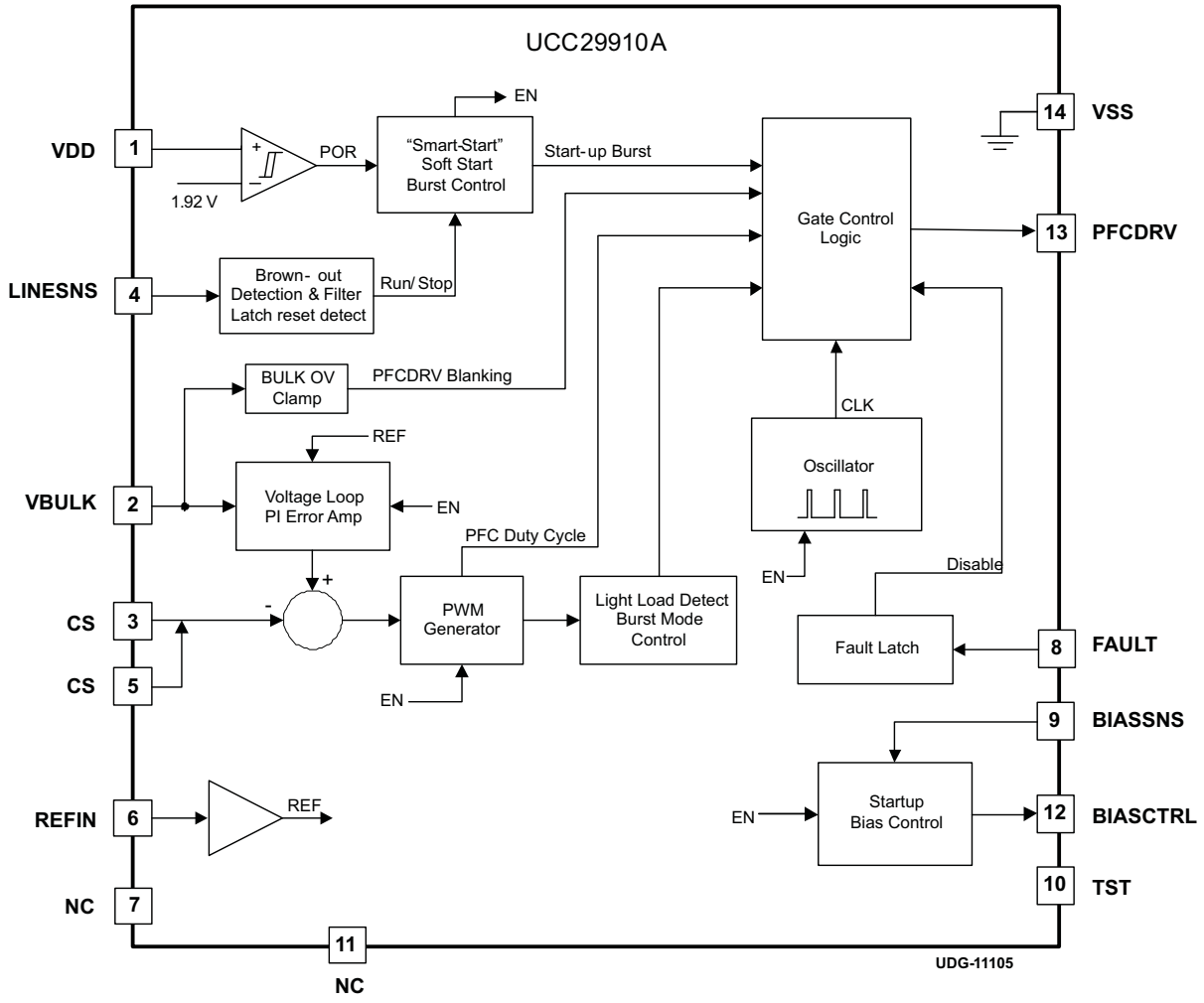
Pin 11 – **NC:** This pin is for internal use only, and must be normally left open.

Pin 12 – **BIASCTRL:** This pin allows control of an external start-up FET.

Pin 13 – **PFCDRV:** This pin is used to drive the low-side PFC FET indirectly. This pin should be connected to a level-shifting gate driver to provide the required drive signal amplitude for typical high voltage power FETs. For this drive signal, D_{MAX} is limited to 90% duty cycle.

Pin 14 – **VSS:** This pin is the common ground connection for the device.

UCC29910A Functional Block Diagram



APPLICATION INFORMATION

The UCC29910A controls a Buck PFC stage and is particularly suited to AC/DC applications in the power range from 65 W to 130 W. A fully characterised reference design using the UCC29910A PFC controller and the UCC29900 Integral Cycle Controller is available on request. The design is for a 90 W PSU intended for laptop adapter applications. It comprises a Buck PFC front end using the UCC29910A to convert line power to a nominal 84 VDC. A UCC29900 controls the conversion of this bulk voltage to a nominal 19.25 V output using a half bridge output power stage. The paragraphs following give some details on how the UCC29910A has been used in this application. Additional guidelines for both the UCC29910A and UCC29900 are available on request.

POR

A Power On Reset function operates at turn-on.

Start Up Bias Control

This block controls the BIASCTRL output which may be used to control an external depletion mode start-up FET during the start-up phase and also while the UCC29910A is operating in SmartBurst Light Load mode (explained below). After POR the BIASCTRL output is held low until the voltage at the BIASSNS pin reaches $V_{B(max)}$ at which point BIASCTRL is driven high which turns the external FET off and the start-up phase is initiated. The UCC29910A continues to monitor the voltage at the BIASSNS pin and if it drops below $V_{B(min)}$ BIASCTRL goes low again, turning the start-up FET on again. At the end of the start-up phase the UCC29910A enters normal mode operation and BIASCTRL pin is held high. In normal mode, auxiliary windings maintain the V_{CCA} rail (see Figure 5). When the UCC29910A is operating in SmartBurst light-load mode there is a possibility that these auxiliary windings can no longer supply enough current to support the bias supply within acceptable limits. The start-up bias control block prevents the bias rail from collapsing by setting the BIASCTRL pin low if VBIASSNS drops below $V_{B(min)}$. This signal may be used to turn on the external start-up FET on, thereby supplying added current to the bias rail. If VBIASSNS increases above V_{BLO} (495 mV approx.) BIASCTRL is set low again. The bias rail is therefore controlled between acceptable limits.

Brown_Out Detection and Filter, Latch Reset Detect

If the RMS voltage at the LINESNS pin drops below V_{BL} for more than 21 ms (approx) the controller latches off. In this condition, the PFCDRV pin is low. The UCC29910A recovers from this state if the RMS voltage at the LINESNS pin falls below the reset level (V_{RS} = 218-mV RMS) for at least 120 ms and then increases to at least V_{BH}. When this happens the UCC29910A enters its start-up mode after a 10-s timeout. Power cycling is not needed for recovery after a brown_out event.

Smart Start, Soft Start, Burst Control

This module controls the gate control logic during the start-up phase.

Oscillator

The internal oscillator runs at a fixed 100 kHz.

Control system

The UCC29910A uses an average current mode control loop to regulate the output voltage, this eliminates the need for slope compensation. The two inputs to this control loop are the voltages at the VBULK and CS (Current Sense) pins.

Voltage Loop – PI Error Amp

The output of the PI (Proportional Integral) Error Amplifier is proportional to the difference between the voltages at the VBULK pin and the REFIN pins. The integral term in the amplifier drives the steady state error to zero but, in common with virtually all PFC controllers the control loop bandwidth is very low – approximately 10 Hz in this case.

Current Sense

The CS pins allow the UCC29910A to sense the average current in the power stage. The current sense signal is subtracted from the demand signal from the error amplifier and the result is used to set the PFCDRV duty cycle.

PWM Generator

The PWM Generator generates a duty cycle signal which is fed into the gate control logic. The duty cycle commanded is proportional to the demand signal from the control loop.

Light Load Detect / Burst Mode Control

As the load on the power stage decreases the standing losses due to, for example, the drive power needed to effect switching of the main power MOSFET, becomes an increasingly important proportion of the whole. The UCC29910A includes a SmartBurst light-load mode which significantly reduces these standing losses. In Normal Mode operation the UCC29910A continuously switches the power MOSFET, in light load the power MOSFET is switched in a burst mode. Power losses are reduced very significantly between bursts because there is no switching activity in the power train. During the burst, the power train is efficiently operated at close to full power. The average power transferred from input to output is controlled by modulating the interval between bursts.

Gate Control Logic

The Gate Control Logic block takes the inputs from a number of sources and outputs the PFCDRV signal.

The fault latch output disables the gate control logic and sets the PFCDRV to low.

The BULK OV clamp forces the PFCDRV output low if the voltage at the VBULK pin exceeds 107% of V_{NM}.

The Start-up burst signal determines the PFCDRV on and off times during the start-up phase before the PWM generator becomes active.

The PFC duty cycle signal sets the PFCDRV output duty cycle demand in normal mode. A line dependent D_{MIN} and a 90% D_{MAX} limit are applied.

The light load detect burst mode control block controls operation during light load mode and entry to and exit from this mode.

BULK OV Clamp

The low bandwidth of the normal control loop prevents it from controlling an increase in VBULK due for example, to a large step reduction in the load on the VBULK output. This clamp activates within 120 µs if the voltage at the VBULK pin exceeds 107% of V_{NM}. When activated, it blanks the gate control logic output and the PFCDRV pin is held low. This clamp is non-latching so it releases once VBULK falls below trip level, i.e., 107% of VNM. For a short duration BULK OV clamp event, recovery will be back to the operating mode in place at the beginning of the event (usually normal mode). If VBULK stays above the clamp level for long enough, the conditions for entry into light load mode may be satisfied and recovery will be into light load mode.

Reference

All of the measurement functions within the UCC29910A use the REFIN pin for their reference voltage, these include (V_{NM}, V_{BH}, V_{BL}, V_{LM}, $V_{B(max)}$, $V_{B(min)}$ and V_{CS}). The specifications are written on the assumption that the reference voltage is 1.500 V and variations in this will proportionally affect the accuracy of measurements. The REFIN pin should be bypassed to V_{SS} to reduce noise. A 100-nF capacitor connected between pin 6 and pin 14 is recommended, this part should be placed as close as possible to the controller and connected with minimum length tracks.

Fault Latch

This latch is activated by pulling the FAULT pin to V_{SS}. When activated the current PWM cycle is terminated, PFCDRV is held Low and BIASCTRL is set low. The controller enters SmartStart mode if the FAULT input clears high in less than t_f (100 µs). If the FAULT input persists for longer than t_f the controller enters a latched shutdown mode The latched state is cleared if the LINESNS pin is held below 215 mV_{RMS} for 120 ms. The controller will re-start after a 10-s delay, providing LINESNS has recovered to at least V_{BH}. Alternatively cycling chip power off then on will also clear the latched state. Connecting a 1-nF capacitor between the FAULT pin and VSS is recommended to reduce the risk of nuisance tripping.

PFC Drive

A power MOSFET driver, such as an NPN and PNP transistor or a UCC27324 will normally be required to convert the PFCDRV output from the UCC29910A to the current and voltage levels typically needed to ensure correct power MOSFET operation.

Buck PFC Power Stage

The PFC stage converts the incoming rectified line voltage to a DC voltage on the output capacitors, power transfer happening during the times when the line voltage is greater than the output voltage. The resulting conduction angle is a function of both the incoming line and output voltages. In the reference design mentioned above, the output voltage is set to 84 VDC. This is low enough to allow conduction angles sufficient to achieve a PF (Power Factor) of at least 0.9 over an input voltage range from 90 VAC to 264 VAC. Other output voltage levels may be set by altering the voltage sensing network at the VBULK pin. A 4:1 ratio between the VBULK and LINESNS scaling ensures optimum operation of the SmartStart algorithm, so if the VBULK scaling is altered significantly, then the LINESNS scaling should be altered too. A high efficiency second stage, controlled by a UCC29900, can then down-convert to a nominal output of 19.25 V using a transformer with a simple 4:1 turns ratio, or to any other desired output voltage. The basic Buck PFC power stage is shown in Figure 1. This low-side switched buck stage has the same performance as the more usual high-side switched buck converter. It features easy power FET drive, at the expense of requiring output sense through a PNP level shift transistor, Q9. The incoming AC line is fed through a rectifier and filter stages, not shown here. The resulting unipolar voltage (V_{HV}) is then fed into the power stage. The MOSFET is switched at a constant 100 kHz and the freewheeling diode function is provided by D1. The output voltage (V_{BULK}) is developed across the two large capacitors, C2 and C21.

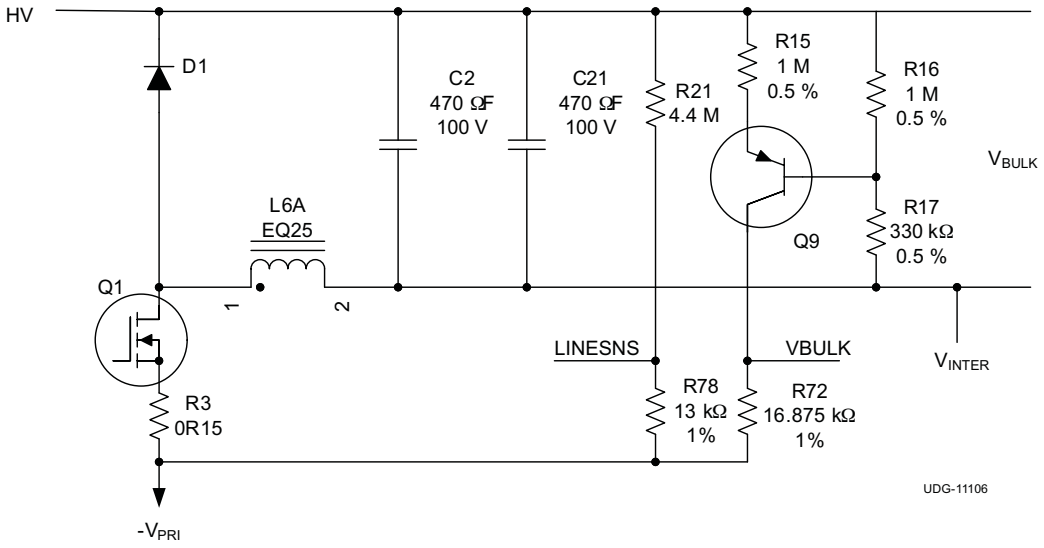


Figure 1. Buck Power Stage (simplified)

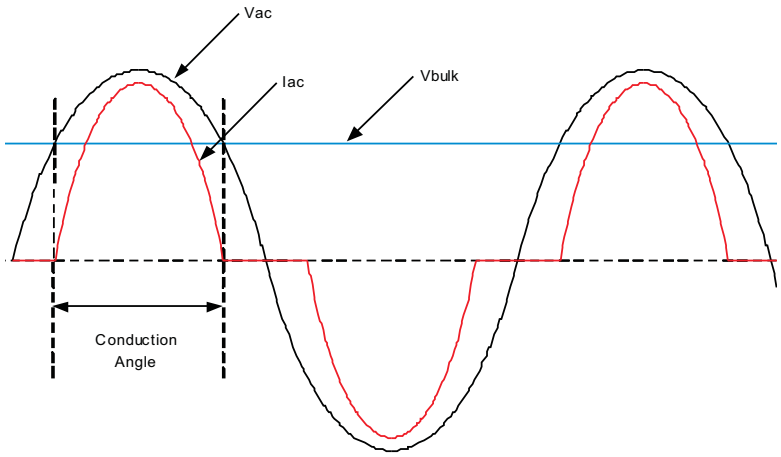


Figure 2. Illustrative Line Current and Voltage

The buck converter operates off a rectified sinusoid and there are periodic dead times when the input voltage is lower than the output. During these times no power can be transferred to the output and the input current is nominally zero. Figure 2 shows the line current, I_{AC}, falling to zero when V_{AC} is less than V_{BULK}. The associated conduction angle increases as the RMS line voltage increases and the current waveform changes from low line to high line. The input current is *skewed* a little towards the beginning of the conduction cycle because V_{BULK} is at its lowest value at this time so conduction starts at a lower voltage than it finishes. This effect may be seen in Figure 3 and Figure 4. These waveforms are taken from a 90-W buck PFC reference design, both meet the harmonics requirements set out in EN61000-3-2 and their PF is greater than 90%.

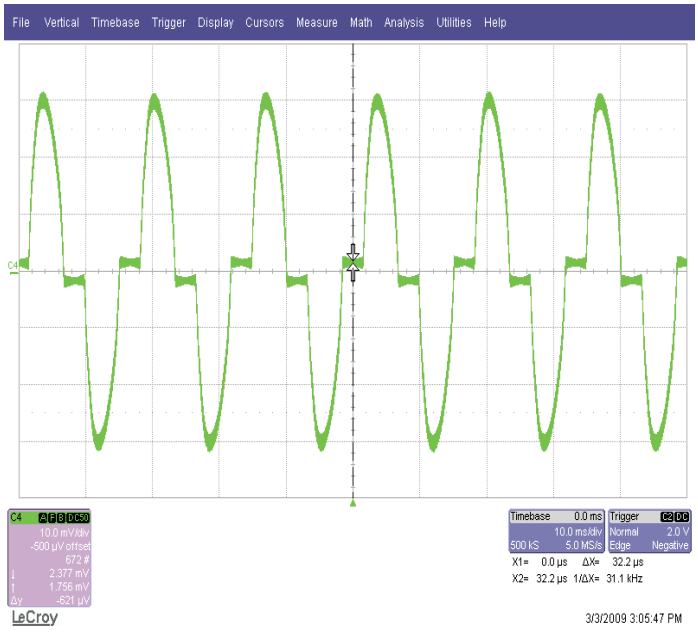


Figure 3. 115 V, 60 Hz, Full Load, 0.5 A/div

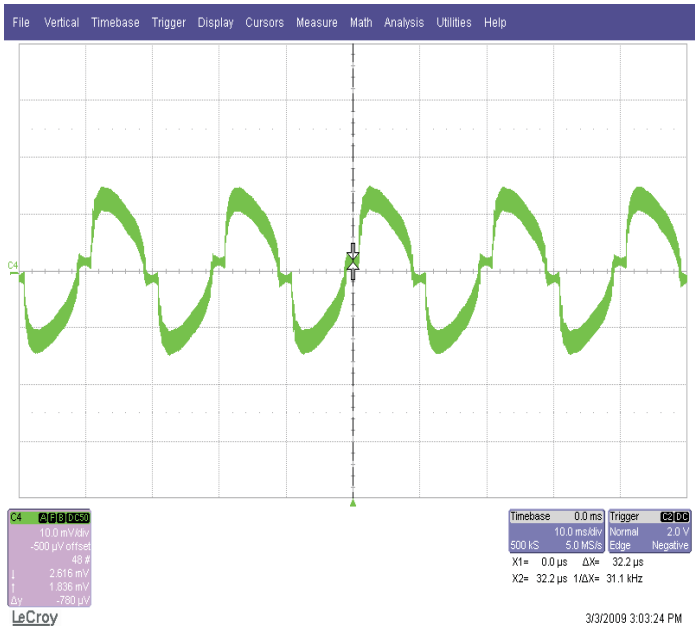


Figure 4. 230 V, 50 Hz, Full Load, 0.5 A/div

Start-Up With External FET

Conventional start-up schemes utilising either resistive or enhancement mode MOSFET feeds incur line dependant static power losses. To avoid these power losses and to obtain an optimum turn-on time an external depletion mode FET may be used Figure 5 and Figure 6. The V_{HV} node is connected to the rectified incoming line. Q12 is a depletion mode FET which will start charging C45 as soon as line power is connected. Initially U1 is inactive and BIASCTRL is low. The VDD_3V rail will begin to increase as U10 starts to conduct. The POR (Power On Reset) sequence of U1 will begin once this rail gets to about 1.7 V and will execute while the VDD_3V rail is being established. The BIASCTRL pin will go high when BIASSNS reaches the $V_{B(max)}$ level. If VLINESNS is then > V_{BH}, U1 begins to pulse the PFCDRV pin, which starts the process of charging the bulk capacitors at the output of the buck PFC power stage. The PFCDRV current is drawn from C45, which starts to discharge. If the voltage at the BIASSNS pin falls below $V_{B(min)}$ then PFC switching is disabled and Q12 is turned on to re-charge C45. With the given component values the $V_{B(max)}$ level corresponds to 12 V and a $V_{B(min)}$ level of 6 V at the V_{CCA} rail. The user sets the $V_{B(max)}$ and $V_{B(min)}$ levels depending on the characteristics of any alternative components used by adjusting R84.

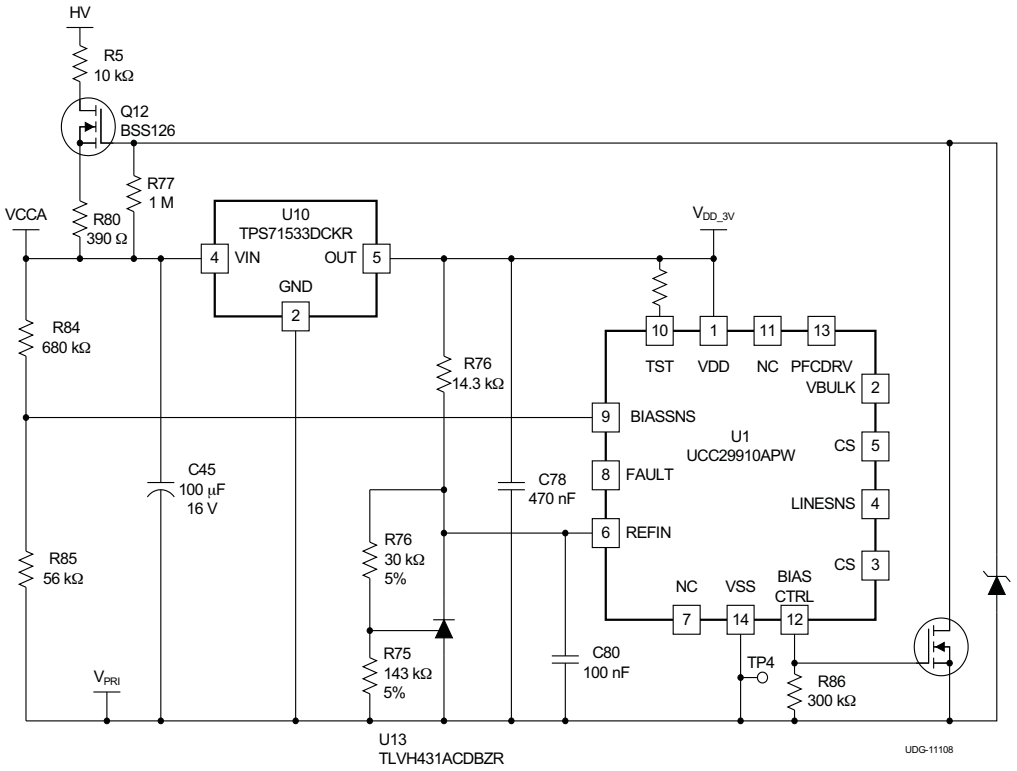


Figure 5. Simplified Schematic

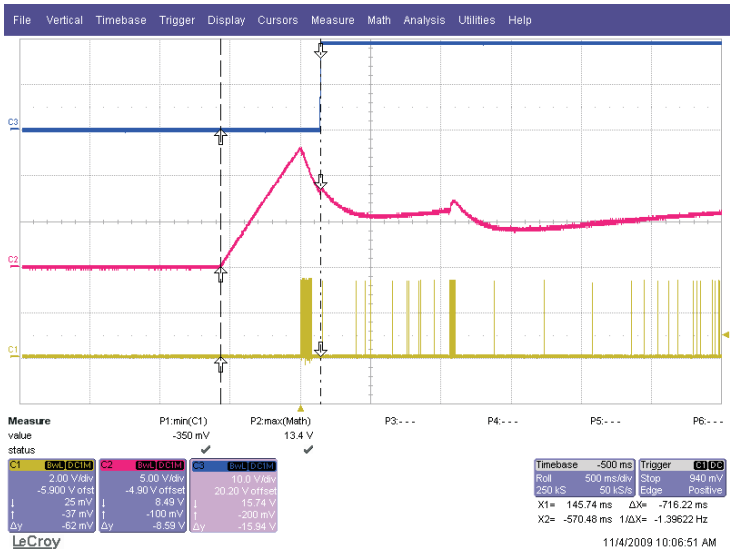


Figure 6. Start-Up Sequence Waveforms (Ch1 (Y), PFCDRV, Ch2 (R), V_{CCA}, Ch3 (B), DUT V_O)

SmartStart, V_{BULK} Ramp-Up

Once V_{CCA} has reached 12 V and Q12 has been turned off, and VLINESNS > V_{BH}, the PFCDRV output of U1 becomes active and begins driving the main power MOSFET. The SmartStart algorithm increases V_{BULK}, the voltage across C2 and C21, as rapidly as possible. This is done by transferring the maximum amount of energy possible during each pulse set. The UCC29910A requires that the inductor has a Volt-sec product withstand rating of 600 Vμs. In fact any inductor suitable for application in a buck PFC stage will already meet this requirement in order to carry the full-load currents involved without saturating, therefore the Volt-sec rating will not result in any additional constraints on the inductor design. However it is more convenient to think in terms of applied Volt-sec product rather than the peak-inductor current.

The UCC29910A's SmartStart algorithm generates a series of pulses for the switching MOSFET which apply a constant Volt-sec product to the inductor during the on and off intervals. This ensures that the inductor current is ramped up as high as possible while the MOSFET is on and then decays to zero during the off time. In fact, T_{OFF} is extended to 110% of nominal which provides margin to ensure the inductor current ramps back to zero. The UCC29910A measures the instantaneous line voltage and the output voltage (V_{HV} and V_{BULK} in Figure 1). The voltage applied to the inductor when Q1 is on is then found by subtracting these two values. It then calculates an appropriate T_{ON} corresponding to a 600 V x μs product. T_{OFF} is calculated in a similar fashion except that the inductor voltage during the off time is the voltage on the capacitors C2 and C21 (V_{BULK}) plus the forward voltage drop in D1 which is assumed to be 0.6 V. Inductor current is controlled on a cycle-by-cycle basis by constraining the T_{ON} and T_{OFF} values so that the inductor Volt-sec product is never exceeded. The initial T_{OFF} intervals are typically 1.1 ms long because the bulk capacitor voltage is still very low. As V_{BULK} increases, the current ramp-down rate increases so that the required T_{OFF} reduces, allowing the pulses to occur more frequently. In addition, as V_{BULK} rises, the voltage across the PFC inductor during T_{ON} will drop, so the on-time is adjusted to maintain a constant PFC inductor volt-secs product.

During ramp-up the UCC29910A monitors the voltage at the BIASSNS pin and if it falls below $V_{B(MIN)}$ the ramp-up operation is terminated and the BIASCTRL pin goes low. In the reference design the minimum bias voltage will be approximately 6 V. When BIASCTRL goes low, Q12 is turned on again and C45 will begin charging back up towards 12 V. The ramp-up phase is then re-started. A maximum of 10 such restarts is allowed before the UCC29910A goes into a latched shutdown mode. Line power cycling is necessary for recovery from this mode.

Typically, the capacitor voltage increases monotonically until the voltage at the VBULK pin reaches 1.024 V. This is slightly lower than V_{NM} and in the circuit of Figure 1 corresponds to a V_{BULK} across C2 and C21 of 82 V. The UCC29910A then switches to Normal Mode operation. This approach allows the fastest possible start-up time.

In order to save standby power at no load, once the start-up phase is complete, and V_{BULK} is being regulated (either by the normal mode voltage regulation loop, or the SmartBurst light-load mode), the BIASCTRL pin is driven high. This turns the start-up fet off which eliminates the power loss in the start-up current path. While in SmartBurst mode the voltage at the BIASSNS input is monitored. If the voltage at this pin drops below $V_{B(min)}$ then the start-up fet is turned back on to recharge the capacitors on the V_{CCA} rail. In this way and with the component values shown, the V_{CCA} rail is maintained above 6 V.

Normal Mode Operation

In normal mode, the VBULK pin is controlled at V_{NM}. Due to the slow voltage loop, and low gain at 100/120 Hz, the voltage loop PI error amp output will be essentially a fixed demand. If the power stage stays in Discontinuous Conduction Mode (DCM) throughout the half-cycle, then peak current will be proportional to (VHV-V_{BULK}) over the half cycle and I_{AVG} is approximately proportional to I_{PEAK}. If the power stage transitions into Continuous Conduction Mode (CCM) during the line cycle, the current loop, responding to the average current, keeps the peak current *flatter*, so the line current doesn't quite follow (V_{IN}-V_O) anymore but average line current is approx proportional to (VHV-V_{BULK}) over the half-cycle. The overall effect is shown in the current waveforms in Figure 3 and Figure 4.

The line voltage is used by the control loop to set dynamic D_{MIN} and D_{MAX} values.

Transient Response and V_{BULK} Regulation

When the UCC29910A is regulating in normal mode, the VBULK pin will be at V_{NM}. An AC ripple at twice line frequency will be superimposed on this as the PFC stage drives current into the bulk capacitors. The amplitude of this ripple will be a function of line frequency, capacitance value and load current. Due to the necessary low control loop bandwidth V_{BULK} will reduce in response to a step load increase. If the load step is large enough to cause the V_{BULK} pin to reduce to less than 0.992 V the loop response is temporarily speeded up until this voltage has been increased back up to 1.043 V at which point the original loop response is restored.

SmartBurst Mode (light load)

As load current reduces the UCC29910A will continue to regulate the voltage at the VBULK pin at V_{NM}. It will do this by reducing the PWMDRV waveform duty cycle, except that any pulses which are commanded to be less than D_{MIN} will be masked and not delivered to the PWMDRV output. The proportion of cycles thus dropped is counted over a 10-ms window and if it exceeds 10% the UCC29910A changes its operating mode to SmartBurst mode.

In SmartBurst mode the UCC29910A enters a low power consumption mode to minimize wasted power and improve light-load efficiency. Every 1 ms (approximately) it samples the voltages at the LINESNS and VBULK pins. If the voltage at VBULK is still within a target window of 1.087 V to 1.074 V no action is taken. The applied load will eventually cause the bus voltage to drop below this window and a burst of pulses are then output at the PFCDRV pin. These drive the PFC FET and thereby recharge the PFC bus capacitance. The most efficient transfer of power is achieved by minimizing the number of switching events, thus minimizing switching and gate drive losses. The line voltage sample is used to set the maximum safe duty cycle for the PFCDRV pulses while keeping the inductor current discontinuous, based on an inductor rating of 600 Vμs. The pulse duty cycle is ramped from D_{MIN} to this maximum value. At the end of the burst, the pulse duty cycle is ramped back to D_{MIN}. Ramping the duty cycle in this manner avoids the sudden application of high power pulses to the power train which may cause excessive EMI and unwanted audio noise generation. A full SmartBurst pulse will last for 2 ms – including the ramp-up time but excluding the ramp-down time.

The SmartBurst pulse train is terminated if the voltage at the VBULK pin reaches the peak value of the allowed window, 1.087 V or if it exceeds 2 ms in length. There is a 5-ms minimum time between the start of successive SmartBurst pulse trains.

The max burst length and minimum burst repetition interval ensure that as load is increased, at some point the burst rate will become insufficient to maintain V_{BULK}. Once the voltage falls below the normal mode setpoint V_{NM} at the VBULK pin the controller reverts to normal regulation mode.

PFC Inductor Value

The PFC inductor is designed for an inductance value that ensures DCM operation at high line (i.e. >160 V_{AC}), right up to full-peak load. With an appropriate value of inductance, operation at low line should then result in CCM operation over most of the conduction angle at full load. The inductance required is given by:

$$L_{PFC} = \frac{1}{2 \times f_{SW} \times I_{IN(pk)}} \left(V_{IN(pk)} - V_{BULK}\right) \left(\frac{V_{BULK}}{V_{IN(pk)}}\right)^2 \quad (1)$$

where:

$$I_{IN(pk)} = \frac{P_{IN(avg)} \times \pi}{2 \times V_{IN(pk)}} \times \frac{1 - \sin(\theta_{START})}{\frac{1}{4} \times \pi - \frac{1}{2} \times \cos(\theta_{START}) \times \sin(\theta_{START}) \times -\frac{1}{2} \times (\theta_{START})} \quad (2)$$

And π is the stage conversion efficiency, θ_{START} is the phase angle (in radians) at which conduction starts, where the instantaneous line voltage equals the bulk voltage. For a 100-W converter with an 84-V_{BULK} DC output we evaluate the equation at 160 V as follows.

$$L_{PFC} = \frac{1}{2 \times \left(100 \times 10^3\right) \text{Hz} \times 1.033\,\text{A}} \left(\sqrt{2} \times 160\,\text{V} - 84\,\text{V}\right) \left(\frac{84\,\text{V}}{\sqrt{2} \times 160\,\text{V}}\right)^2 = 94.9\,\mu\text{H} \quad (3)$$

Compared to the Boost PFC, much smaller values of PFC inductance can typically be used in the buck, because the voltage differential that needs to be supported across the inductor is lower. Practical inductance values that have been used in various designs have ranged from ~150 µH at 50 W, to ~80 µH to 100 µH at 90 W to 130 W.

Bulk Capacitor Choice

The value of bulk capacitance required is dictated by requirements on the allowable ripple voltage and hold-up time. In applications where hold-up time is not the main factor, then the capacitors should be sized for approximately 12% peak-to-peak ripple as follows:

$$C_{BUS} = \frac{P_{LOAD} \times \theta_{cond\_\%}}{V_{BUS}^{2} \times \Delta V_{BUS(\%)} \times 2 \times f_{AC}} \tag{4}$$

For a typical 90-W adapter using buck PFC, the required bus capacitance for ±6% maximum ripple at 90 VAC/50 Hz (12% total ripple) and at 84 VDC bus, assuming 96.5% efficiency of the second stage, would be:

$$C_{BUS} = \frac{\frac{90}{0.965} \times 0.57}{84^{2} \times 0.12 \times 2 \times 50} = 628\,\mu F \tag{5}$$

where:

- P_{LOAD}: load power drawn (usually by the second regulation/isolation stage)
- C_{BUS}: bus capacitance
- $\theta_{COND\_\%}$: conduction angle at AC line of interest (as decimal percentage of total cycle, e.g. 50% conduction angle expressed as 0.5)
- f_{AC}: AC line frequency

The capacitance required to achieve a specific hold up time may be calculated as follows:

$$C_{BUS} = \frac{T_{HOLDUP} \times 2 \times P_{LOAD}}{\left(V_{BUS(min)}^{2} - V_{BUS(min\_reg)}^{2}\right)} \tag{6}$$

For example, in order to achieve 3-ms holdup, with nominal bus voltage of 84 VDC, ±5% maximum bus ripple, and 70-VDC minimum bus regulation level for the second stage, the required bus capacitance would be calculated as follows for a 90-W load, assuming 96.5% second stage efficiency:

$$C_{BUS} = \frac{0.003 \times 2 \times \frac{90}{0.965}}{\left((84 \times 0.95)^{2} - 70^{2}\right)} = 381\,\mu F \tag{7}$$

References

1. 2009/10 Power Supply Design Seminar - SEM1900 Topic 4, *Power Factor Correction Using the Buck Topology – Efficiency Benefits and Practical Design Considerations*

REVISION HISTORY

Changes from Original (May 2011) to Revision A	Page
• Added New DESCRIPTION	1
• Added an updated description for the TST pin.	4
• Added an updated description for the TST pin.	6
• Changed UCC29910A Functional Block Diagram	6

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UCC29910APW	Active	Production	TSSOP (PW) | 14	90 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	29910A
UCC29910APW.A	Active	Production	TSSOP (PW) | 14	90 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	29910A
UCC29910APW.B	Active	Production	TSSOP (PW) | 14	90 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	29910A
UCC29910APWR	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	29910A
UCC29910APWR.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	29910A
UCC29910APWR.B	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	29910A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

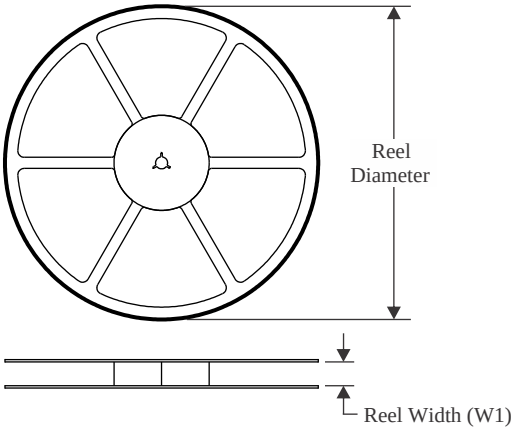
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

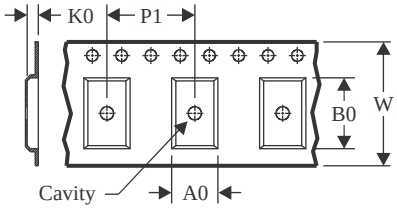
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

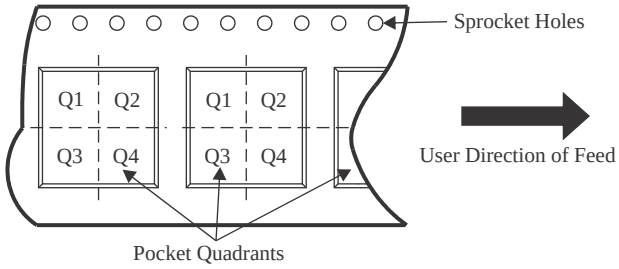


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

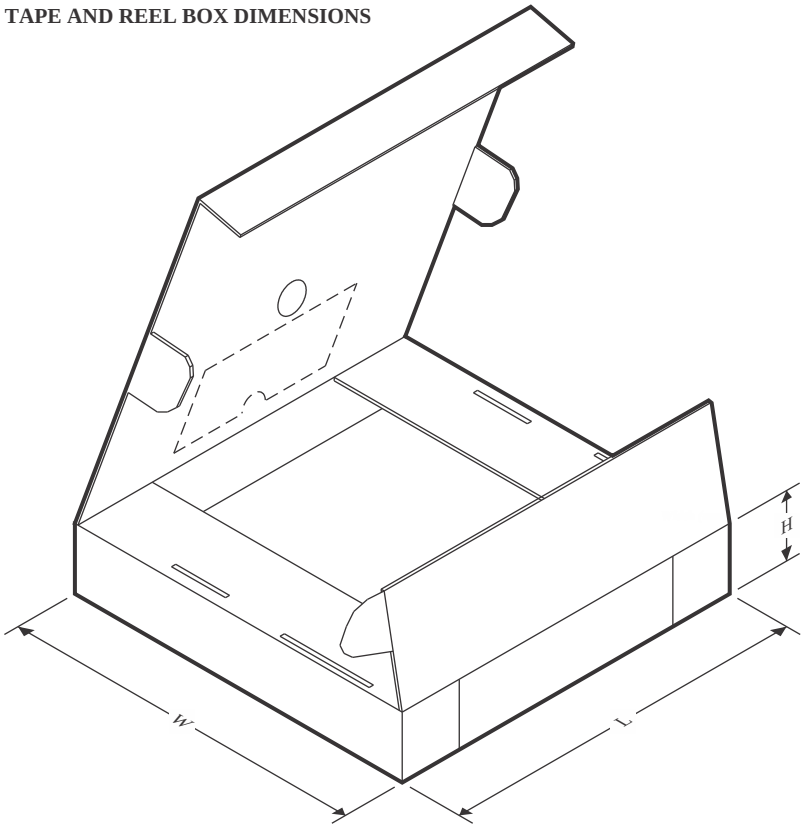
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC29910APWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

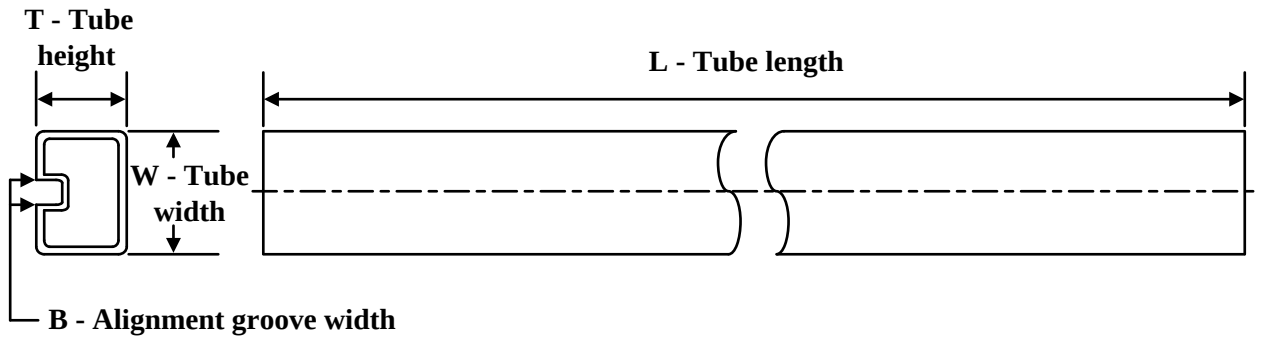
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC29910APWR	TSSOP	PW	14	2000	353.0	353.0	32.0

TUBE



*All dimensions are nominal

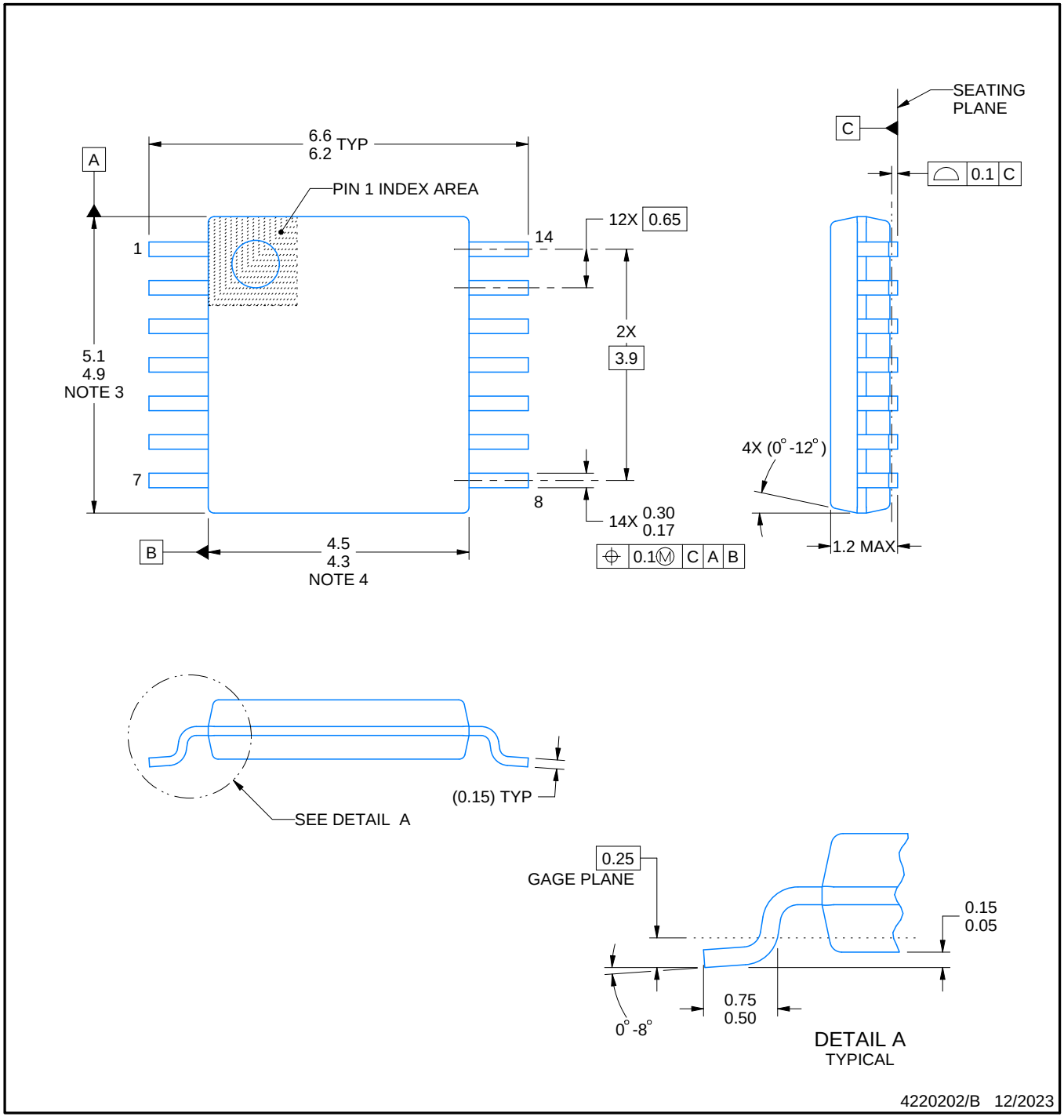
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
UCC29910APW	PW	TSSOP	14	90	530	10.2	3600	3.5
UCC29910APW.A	PW	TSSOP	14	90	530	10.2	3600	3.5
UCC29910APW.B	PW	TSSOP	14	90	530	10.2	3600	3.5

PACKAGE OUTLINE

PW0014A

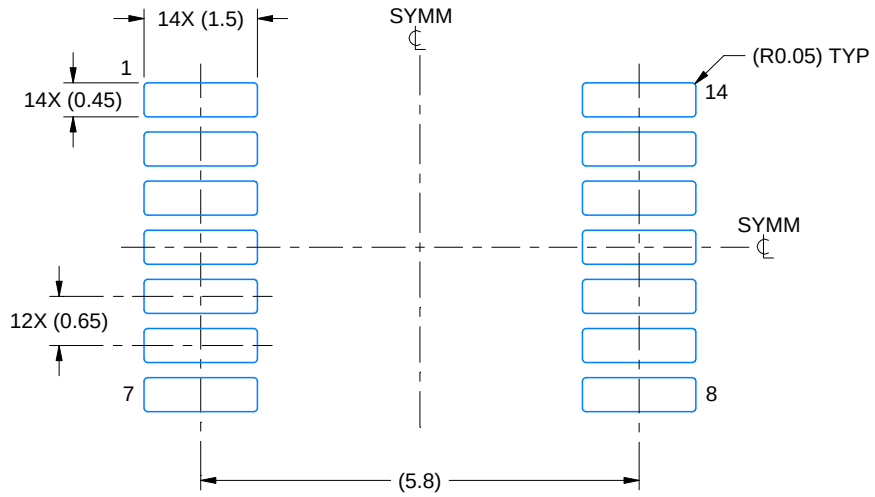
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

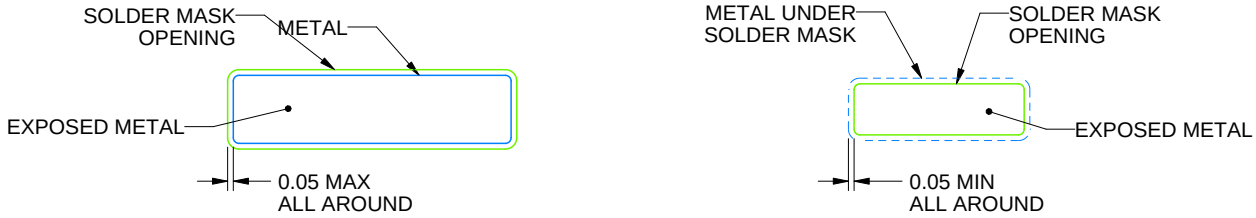


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

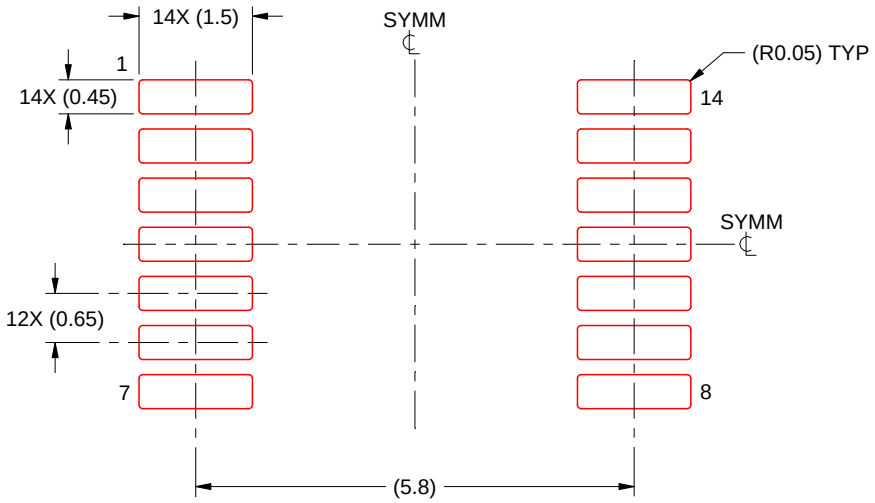


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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