

## Digital Dual Synchronous-Buck Power Driver

Check for Samples: [UCD7242-EP](#)

### FEATURES

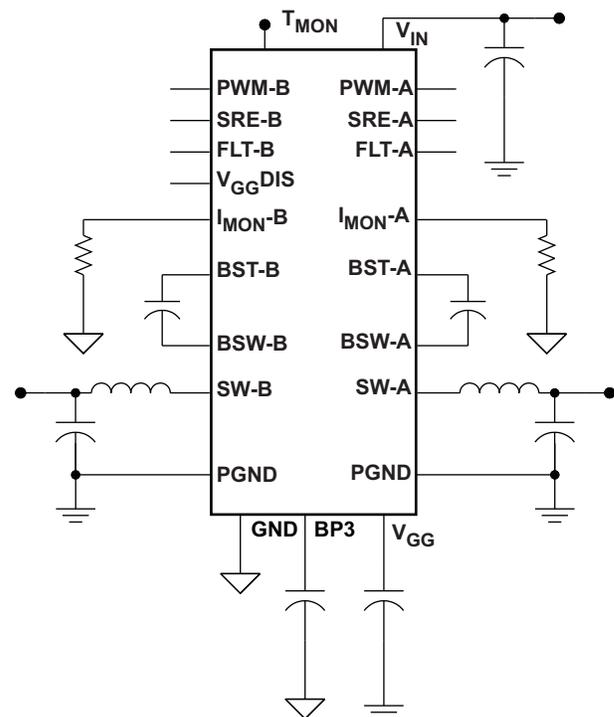
- Fully Integrated Power Switches With Drivers for Dual Synchronous Buck Converters
- Full Compatibility With TI Fusion Digital Power Supply Controllers, Such as the UCD92xx Family
- Wide Input Voltage Range: 4.75 V to 18 V Operational Down to 2.2-V Input With an External Bias Supply
- Up to 10-A Output Current per Channel
- Operational to 2-MHz Switching Frequency
- High Side Current Limit With Current Limit Flag
- Onboard Regulated 6 V Driver Supply From  $V_{IN}$
- Thermal Protection
- Temperature Sense Output – Voltage Proportional to Chip Temperature
- UVLO and OVLO Circuits Ensure Proper Drive Voltage
- RoHS Compliant
- Accurate On-Die Current Sensing ( $\pm 5\%$ )

### APPLICATIONS

- Digitally-Controlled Synchronous-Buck Power Stages
- High Current Dual-Phase VRM/EVRD Regulators for Desktop, Server, Telecom and Notebook Processors

### SUPPORTS DEFENSE, AEROSPACE, AND MEDICAL APPLICATIONS

- Controlled Baseline
- One Assembly and Test Site
- One Fabrication Site
- Available in Military ( $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ ) Temperature Range
- Extended Product Life Cycle
- Extended Product-Change Notification
- Product Traceability



### DESCRIPTION

The UCD7242 is a complete power system ready to drive two independent buck power supplies (see [Figure 1](#)). High side MOSFETs, low side MOSFETs, drivers, current sensing circuitry and necessary protection functions are all integrated into one monolithic solution to facilitate minimum size and maximum efficiency. Driver circuits provide high charge and discharge current for the high-side NMOS switch and the low-side NMOS synchronous rectifier in a synchronous buck circuit. The MOSFET gates are driven to +6.25 V by an internally regulated  $V_{GG}$  supply. The internal  $V_{GG}$  regulator can be disabled to permit the user to supply an independent gate drive voltage. This flexibility allows a wide power conversion input voltage range of 2.2 V to 18 V. Internal under voltage lockout (UVLO) logic ensures  $V_{GG}$  is good before allowing chip operation.



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## DESCRIPTION (CONTINUED)

The synchronous rectifier enable (SRE) pin controls whether or not the low-side MOSFET is turned on when the PWM signal is low. When SRE is high the part operates in continuous conduction mode for all loads. In this mode the drive logic block uses the PWM signal to control both the high-side and low-side gate drive signals. Dead time is also optimized to prevent cross conduction. When SRE is low, the part operates in discontinuous conduction mode at light loads. In this mode the low-side MOSFET is always held off.

On-board comparators monitor the current through the high side switch to safeguard the power stage from sudden high current loads. Blanking delay is set for the high side comparator to avoid false reports coincident with switching edge noise. In the event of an over-current fault, the high-side FET is turned off and the Fault Flag (FLT) is asserted to alert the controller.

MOSFET current is measured and monitored by a precision integrated current sense element. This method provides an accuracy of  $\pm 5\%$  over most of the load range. The amplified signal is available for use by the controller on the  $I_{MON}$  pin.

An on-chip temperature sense converts the die temperature to a voltage at the  $T_{MON}$  pin for the controller's use. If the die temperature exceeds  $170^{\circ}\text{C}$ , the temperature sensor initiates a thermal shutdown that halts output switching and sets the FLT flag. Normal operation resumes when the die temperature falls below the thermal hysteresis band.

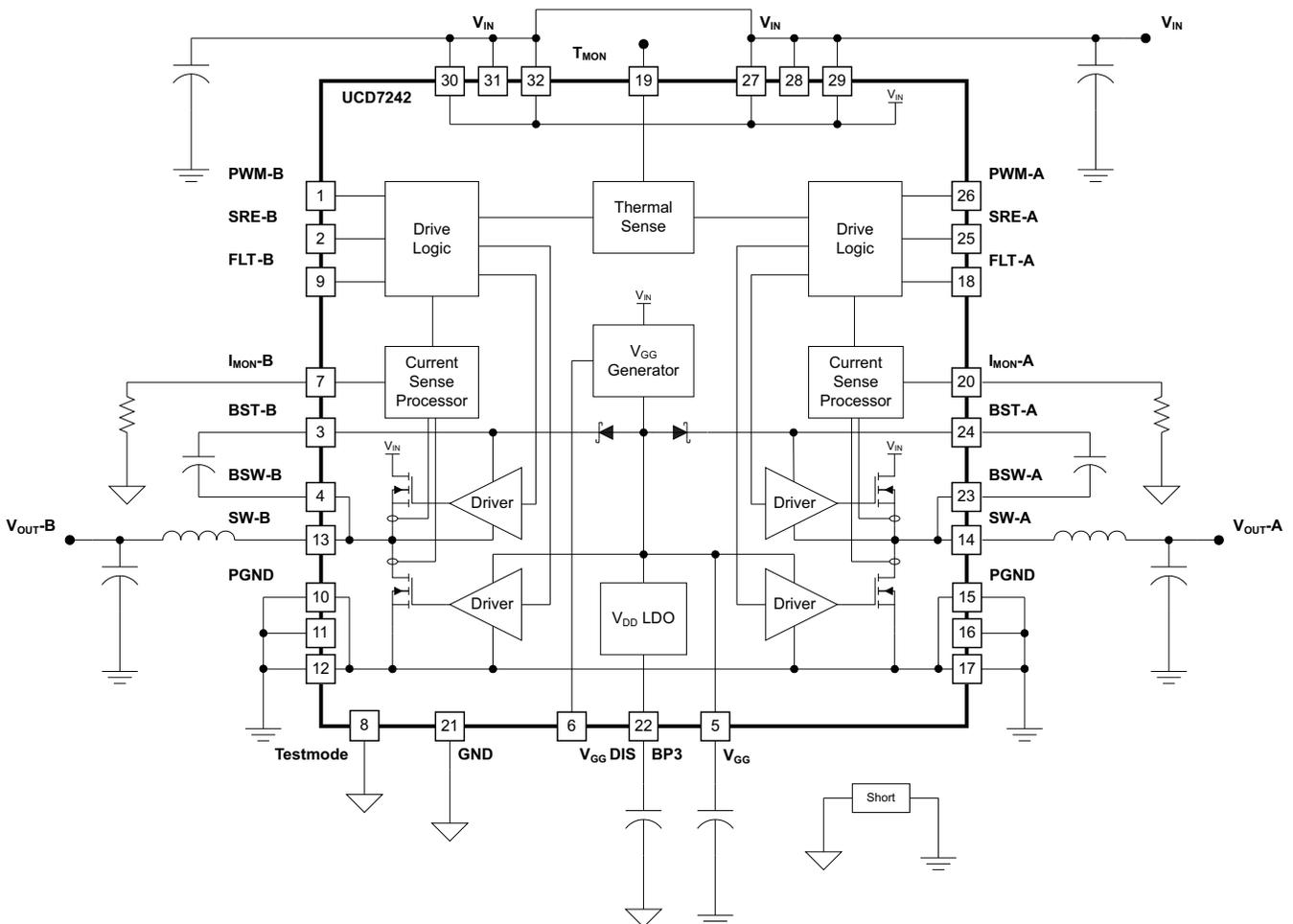


Figure 1. Typical Application Circuit and Block Diagram

**ORDERING INFORMATION**

T <sub>J</sub>	PIN COUNT	ORDERABLE PART NUMBER	SUPPLY	PACKAGE	TOP SIDE MARKING	VID NUMBER
-55°C to 125°C	32-pin	UCD7242MRSJREP	Reel of 2500	QFN	UCD7242EP	V62/14601-01XE

**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

over operating free-air temperature range (unless otherwise noted)

PARAMETER		RATING	VALUE
V <sub>IN</sub>	Supply voltage	-0.3 to 20	V
B <sub>ST</sub>	Boot voltage	DC	-0.3 to SW + 7
		AC <sup>(2)</sup>	34
V <sub>GG</sub> , V <sub>GG_DIS</sub>	Gate supply voltage	7	V
B <sub>P3</sub>	Logic supply voltage	4	V
S <sub>W</sub> , B <sub>SW</sub>	Switch voltage	DC	-2 to V <sub>IN</sub> + 1
		AC <sup>(2)</sup>	34
T <sub>MON</sub> , I <sub>MON</sub> , Testmode	Analog outputs	-0.3 to 3.6	V
P <sub>WM-A</sub> , P <sub>WM-B</sub> , S <sub>RE-A</sub> , S <sub>RE-B</sub> , F <sub>LT-A</sub> , F <sub>LT-B</sub>	Digital I/O's	-0.3 to 5.5	V
T <sub>J</sub>	Junction temperature	-55 to 150	°C
T <sub>stg</sub>	Storage temperature	-55 to 150	°C
ESD rating	HBM: Human Body model	2000	V
	CDM: Charged device model	500	V

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltages are with respect to GND. Currents are positive into, negative out of the specified terminal. Consult company packaging information for thermal limitations and considerations of packages.

(2) AC levels are limited to within 5 ns.

**THERMAL INFORMATION**

THERMAL METRIC <sup>(1)</sup>		UCD7242-EP	UNITS
		RSJ	
		32 PINS	
θ <sub>JA</sub>	Junction-to-ambient thermal resistance <sup>(2)</sup>	40.7	°C/W
θ <sub>JCtop</sub>	Junction-to-case (top) thermal resistance <sup>(3)</sup>	17.8	
θ <sub>JB</sub>	Junction-to-board thermal resistance <sup>(4)</sup>	12	
ψ <sub>JT</sub>	Junction-to-top characterization parameter <sup>(5)</sup>	0.1	
ψ <sub>JB</sub>	Junction-to-board characterization parameter <sup>(6)</sup>	11.9	
θ <sub>JCbot</sub>	Junction-to-case (bottom) thermal resistance <sup>(7)</sup>	0.3	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.

(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.

(5) The junction-to-top characterization parameter, ψ<sub>JT</sub>, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ<sub>JA</sub>, using a procedure described in JESD51-2a (sections 6 and 7).

(6) The junction-to-board characterization parameter, ψ<sub>JB</sub>, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ<sub>JA</sub>, using a procedure described in JESD51-2a (sections 6 and 7).

(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

## RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
$V_{IN}$	Power input voltage (internally generated $V_{GG}$ )	4.75	12	18	V
$V_{IN}$	Power input voltage (externally generated $V_{GG}$ )	2.2	12	18	V
$V_{GG}$	Externally supplied gate drive voltage	4.75	6.2		V
$T_J$	Operating junction temperature range	-55		125	°C
$f_s$	Switching frequency	300	750	2000	kHz

## ELECTRICAL CHARACTERISTICS

$V_{IN} = 12V$ ;  $1\mu F$  from BP3 to GND,  $0.22\mu F$  from BST to BSW,  $4.7\mu F$  from  $V_{GG}$  to PGND,  $T_A = T_J = -55^\circ C$  to  $125^\circ C$  (unless otherwise noted)

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT	
<b>SUPPLY SECTION</b>						
Supply current	Outputs not switching, $V_{IN} = 2.2 V$ , PWM(INH) = LOW, SRE(INL) = HIGH, $V_{GG\_DIS} = HIGH$ , $V_{GG} = 5V$		6		mA	
	Outputs not switching, $V_{IN} = 18 V$ , PWM(INH) = LOW, SRE(INL) = HIGH, $V_{GG\_DIS} = LOW$		6		mA	
<b>GATE DRIVE UNDER VOLTAGE LOCKOUT</b>						
$V_{GG}$	UVLO ON	BP3 Rising	4.0		V	
	UVLO OFF	BP3 Falling	3.8		V	
	UVLO hysteresis		200		mV	
<b><math>V_{GG}</math> SUPPLY GENERATOR</b>						
$V_{GG}$	$V_{IN} = 7$ to $18 V$	5.2	6.25	6.8	V	
$V_{GG}$ drop out	$V_{IN} = 4.75$ to $7 V$ , $I_{V_{GG}} < 50 mA$			850	mV	
<b>BP3 SUPPLY VOLTAGE</b>						
BP3	$I_{DD} = 0$ to $10 mA$	3.14	3.3	3.45	V	
<b>INPUT SIGNAL (PWM, SRE)</b>						
$V_{IH}$	Positive-going input threshold voltage		2.1	2.3	V	
$V_{IL}$	Negative-going input threshold voltage		1	1.2	V	
	3-state Condition		1.4	1.9	V	
$t_{HLD\_R}$	3-state hold-off time	$V_{PWM} = 1.65 V$	275		ns	
$I_{PWM}$	Input current	$V_{PWM} = 5.0 V$	133		$\mu A$	
		$V_{PWM} = 3.3 V$	66			
		$V_{PWM} = 0 V$	-66			
$I_{SRE}$	Input current	$V_{SRE} = 5.0 V$	1		$\mu A$	
		$V_{SRE} = 3.3 V$	1			
		$V_{SRE} = 0 V$	1			
<b><math>V_{GG}</math> DISABLE (<math>V_{GG\_DIS}</math>)</b>						
	Input resistance to AGND	$V_{GG\_DIS}$	45	100	150	k $\Omega$
	Threshold		1.35	1.6		V
	Hysteresis		550			mV
<b>FAULT FLAG (FLT)</b>						
	FLT Output High Level	$I_{OH} = 2 mA$	2.7			V
	FLT Output Low Level	$I_{OL} = -2 mA$		0.6		V

**ELECTRICAL CHARACTERISTICS (continued)**

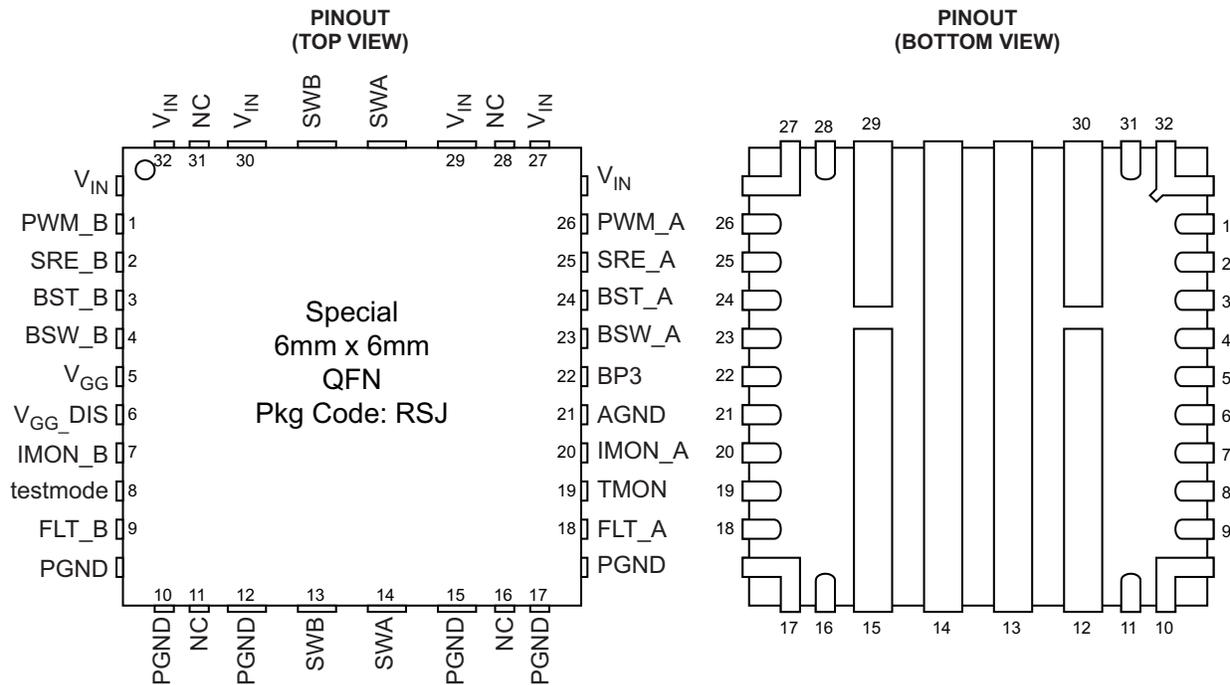
$V_{IN} = 12V$ ;  $1\mu F$  from BP3 to GND,  $0.22\mu F$  from BST to BSW,  $4.7\mu F$  from  $V_{GG}$  to PGND,  $T_A = T_J = -55^\circ C$  to  $125^\circ C$  (unless otherwise noted)

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
<b>CURRENT LIMIT</b>					
Over current threshold		12	15	18.5	A
$T_{\text{fault\_HS}}$ delay until HS FET off <sup>(1)</sup>				80	ns
$T_{\text{fault\_FF}}$ delay until FLT asserted <sup>(1)</sup>				100	ns
Propagation delay from PWM to reset FLT <sup>(1)</sup>	1 <sup>st</sup> falling edge of PWM without a fault event			100	ns
High side blanking time <sup>(1)</sup>	Over currents during this period will not be detected			60	ns
<b>CURRENT SENSE AMPLIFIER</b>					
Gain	$I_{\text{MON}}/I_{\text{OUT}}$ , (see <a href="#">Figure 14</a> )	17	20	26	$\mu A/A$
Bandwidth <sup>(1)</sup>		5			kHz
<b>THERMAL SENSE</b>					
Thermal shutdown <sup>(1)</sup>			170		$^\circ C$
Thermal shutdown hysteresis <sup>(1)</sup>			20		$^\circ C$
Temperature Sense T <sup>(1)</sup>	Gain, $T_J = -20^\circ C$ to $125^\circ C$		10		mV/ $^\circ C$
Temperature Sense T Offset <sup>(1)</sup>	$T_J = 0^\circ C$ , $-100\mu A \leq I_{\text{TMON}} \leq 100\mu A$		470		mV
<b>POWER MOSFETS</b>					
Propagation delay from PWM to switch node going high			32		ns
High side MOSFET $R_{\text{DS(ON)}}$			15.5		m $\Omega$
Low side MOSFET $R_{\text{DS(ON)}}$			6.5		m $\Omega$
High side MOSFET turn on – Dead Time <sup>(1)</sup>			5	10	ns
Low side MOSFET turn on – Dead Time <sup>(1)</sup>			6	11	ns

(1) As designed and characterized. Not 100% tested in production. These specifications apply for  $-40^\circ C \leq T_J \leq 125^\circ C$ .

## DEVICE INFORMATION

### PINOUT



### PIN FUNCTIONS

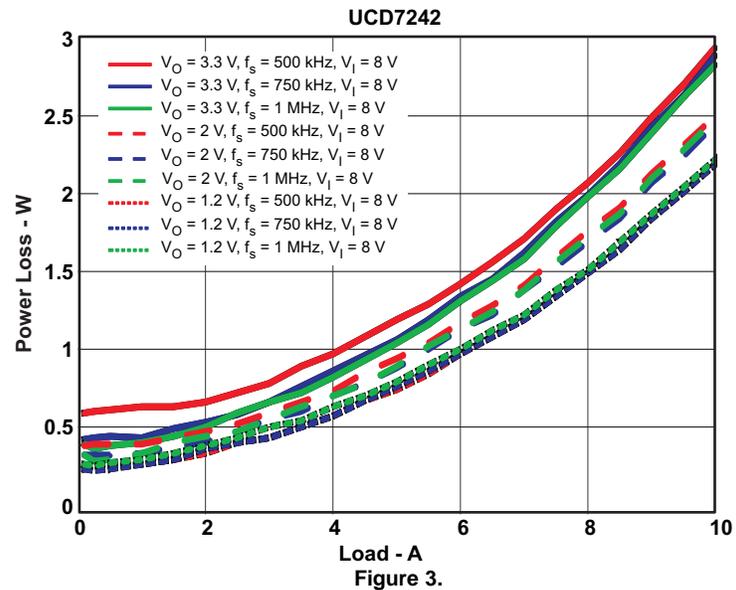
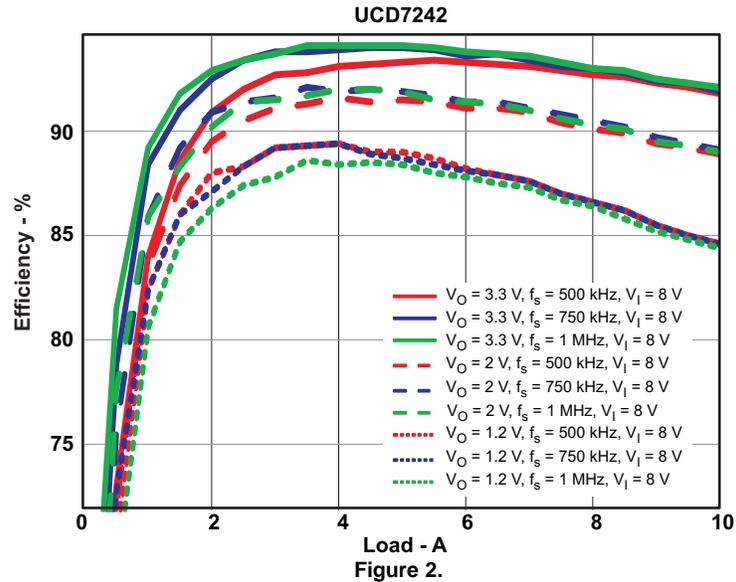
UCD7242 –BUCK POWER STAGE															
QFN	PIN NAME	I/O	FUNCTION												
1	PWM-B	I	<p>High impedance digital input capable of accepting 3.3V or 5 V logic level signals up to 2 MHz. A Schmitt trigger input comparator desensitizes this pin from external noise. This pin controls the state of the high side MOSFET and the low side MOSFET when SRE-B is high.</p> <table border="1"> <thead> <tr> <th></th> <th>PWM = high</th> <th>PWM = low</th> <th>PWM = 1.65 V</th> </tr> </thead> <tbody> <tr> <td>SRE = high</td> <td>HS = on, LS = off</td> <td>HS = off, LS = on</td> <td>HS = off, LS = off</td> </tr> <tr> <td>SRE = low</td> <td>HS = on, LS = off</td> <td>HS = off, LS = off</td> <td>HS = off, LS = off</td> </tr> </tbody> </table>		PWM = high	PWM = low	PWM = 1.65 V	SRE = high	HS = on, LS = off	HS = off, LS = on	HS = off, LS = off	SRE = low	HS = on, LS = off	HS = off, LS = off	HS = off, LS = off
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SRE = low	HS = on, LS = off	HS = off, LS = off	HS = off, LS = off												
2	SRE-B	I	Synchronous Rectifier Enable input for the B-channel. High impedance digital input capable of accepting 3.3V or 5V logic level signals used to control the synchronous rectifier switch. An appropriate anti-cross-conduction delay is used during synchronous mode.												
3	BST_B	I	Connection for the B-channel charge pump capacitor that provides a floating supply for the high side driver. Connect a 0.22µF ceramic capacitor from this pin to BSW-B (pin 4).												
4	BSW-B	I	Connection for B-channel charge pump capacitor. Internally connected to SW-B.												
5	V <sub>GG</sub>	I/O	Gate drive voltage for the power MOSFETs. For V <sub>IN</sub> ≥ 4.75V, the internal V <sub>GG</sub> generator can be used. For V <sub>IN</sub> < 4.75 V, this pin should be driven from an external bias supply. When externally driven, V <sub>GG_DIS</sub> must be tied to V <sub>GG</sub> . In all cases, bypass this pin with a 4.7µF (min), 10V (min) ceramic capacitor to PGND.												
6	V <sub>GG_DIS</sub>	I	When tied to V <sub>GG</sub> , disables the on-chip V <sub>GG</sub> generator to allow gate drive voltage to be supplied from an external source. This is required when V <sub>IN</sub> is < 4.75V. To use the internal V <sub>GG</sub> generator, tie to GND.												
7	IMON-B	O	MOSFET current sense monitor output. Provides a current source output that is proportional to the current flowing in the power MOSFETs. The gain on this pin is equal to 20µA/A. The I <sub>MON</sub> pin should be connected to a resistor to GND to produce a voltage proportional to the power-stage load current.												
8	testmode	I	Test mode only. Tie to GND.												

**PIN FUNCTIONS (continued)**

UCD7242 –BUCK POWER STAGE															
QFN	PIN NAME	I/O	FUNCTION												
9	FLT-B	O	Fault flag for the B-channel. This signal is a 3.3V digital output which is latched high when the current in the B-channel high-side FET exceeds the current limit trip point. When tripped, high-side FET drive pulses are truncated to limit output current. FLT is cleared after one complete switching cycle without a fault. Additionally, if the die temperature exceeds 170°C, the temperature sensor will initiate a thermal shutdown that halts output switching and sets the FLT flag. Normal operation resumes when the die temperature falls below the thermal hysteresis band.												
10, 12, 15, 17	PGND	–	Shared power ground return for the buck power stage												
11, 16	NC	–	No internal connection. It is recommended that these pins be tied to PGND.												
13	SW-B	–	Switching node of the B-channel buck power stage and square wave input to the buck inductor. Electrically this is the connection of the high side MOSFET source to the low side MOSFET drain.												
14	SW-A	–	Switching node of the A-channel buck power stage and square wave input to the buck inductor. Electrically this is the connection of the high side MOSFET source to the low side MOSFET drain.												
18	FLT-A	O	Fault flag for the A-channel. This signal is a 3.3V digital output which is latched high when the current in the A-channel high-side FET exceeds the current limit trip point. When tripped, high-side FET drive pulses are truncated to limit output current. FLT is cleared after one complete switching cycle without a fault. Additionally, if the die temperature exceeds 170°C, the temperature sensor initiates a thermal shutdown that halts output switching and sets the FLT flag. Normal operation resumes when the die temperature falls below the thermal hysteresis band.												
19	TMON	O	Temperature sense pin. The voltage on this pin is proportional to the die temperature. The gain is 10mV/°C. At $T_J = 0^\circ\text{C}$ , the output voltage has an offset of 0.47V. When the die temperature reaches the thermal shutdown threshold, this pin is pulled to BP3 and the power FETs are switched off. When the die temperature falls below the thermal hysteresis band, the FLT flag clears and normal operation resumes.												
20	IMON -A	O	MOSFET current sense monitor output. Provides a current source output that is proportional to the current flowing in the power MOSFETs. The gain on this pin is equal to 20 $\mu\text{A/A}$ . The IMON pin should be connected to a resistor to GND to produce a voltage proportional to the power-stage load current.												
21	GND	–	Analog ground return.												
22	BP3	O	Output of internal 3.3V LDO regulator for powering internal logic circuits. Bypass this pin with 1 $\mu\text{F}$ (min) to GND. This LDO is supplied by the $V_{GG}$ pin.												
23	BSW-A	–	Connection for A-channel charge pump capacitor. Internally connected to SW-A.												
24	BST-A	–	Connection for the A-channel charge pump capacitor that provides a floating supply for the high side driver. Connect a 0.22 $\mu\text{F}$ ceramic cap from this pin to BSW-A (pin 23).												
25	SRE-A	I	Synchronous Rectifier Enable input for the A-channel. High impedance digital input capable of accepting 3.3V or 5V logic level signals used to control the synchronous rectifier switch. An appropriate anti-cross-conduction delay is used during synchronous mode.												
26	PWM -A	I	High impedance digital input capable of accepting 3.3V or 5 V logic level signals up to 2 MHz. A Schmitt trigger input comparator desensitizes this pin from external noise. This pin controls the state of the high side MOSFET and the low side MOSFET when SRE-A is high. <table border="1" data-bbox="555 1377 1370 1482" style="margin-left: 20px;"> <thead> <tr> <th></th> <th>PWM = high</th> <th>PWM = low</th> <th>PWM = 1.65 V</th> </tr> </thead> <tbody> <tr> <td>SRE = high</td> <td>HS = on, LS = off</td> <td>HS = off, LS = on</td> <td>HS = off, LS = off</td> </tr> <tr> <td>SRE = low</td> <td>HS = on, LS = off</td> <td>HS = off, LS = off</td> <td>HS = off, LS = off</td> </tr> </tbody> </table>		PWM = high	PWM = low	PWM = 1.65 V	SRE = high	HS = on, LS = off	HS = off, LS = on	HS = off, LS = off	SRE = low	HS = on, LS = off	HS = off, LS = off	HS = off, LS = off
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SRE = low	HS = on, LS = off	HS = off, LS = off	HS = off, LS = off												
27, 29, 30, 32	VIN	–	Input Voltage to the buck power stage and driver circuit												
28, 31	NC	–	No internal connection. It is recommended that these pins be tied to VIN.												

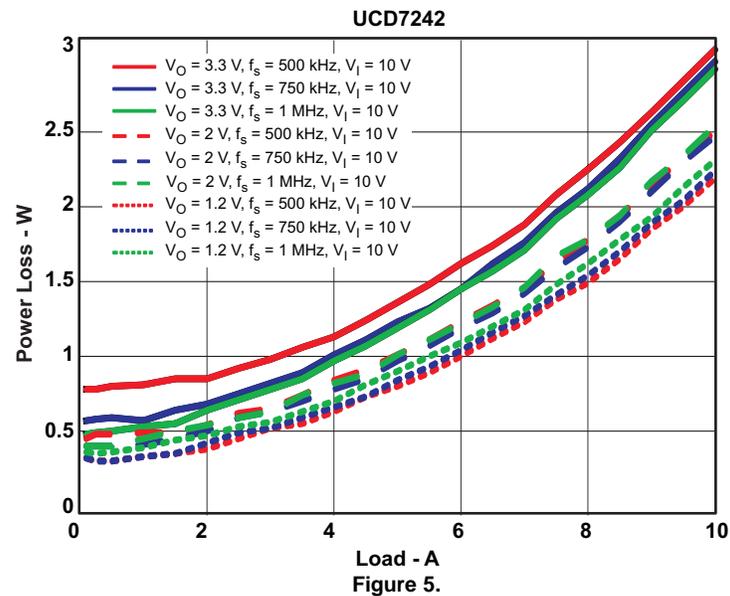
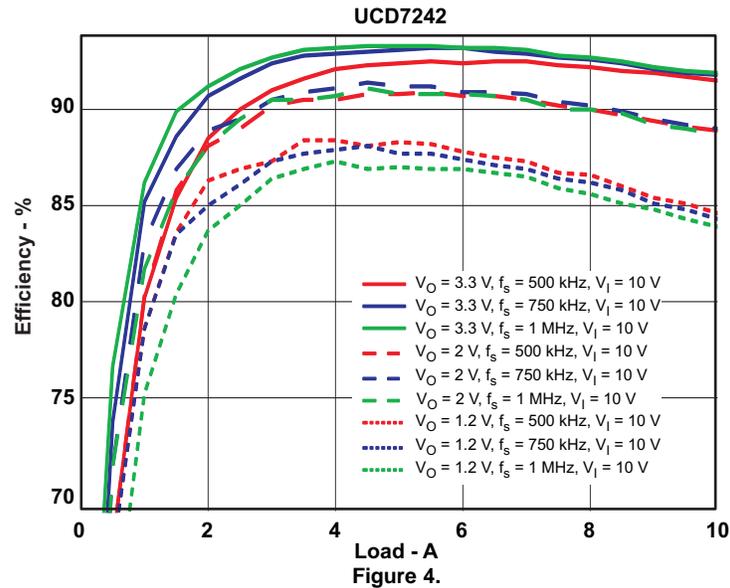
## TYPICAL CHARACTERISTICS

Inductor used in the following plots is a 0.47 $\mu$ H BI Technologies inductor (HM72A). All data taken at room ambient.



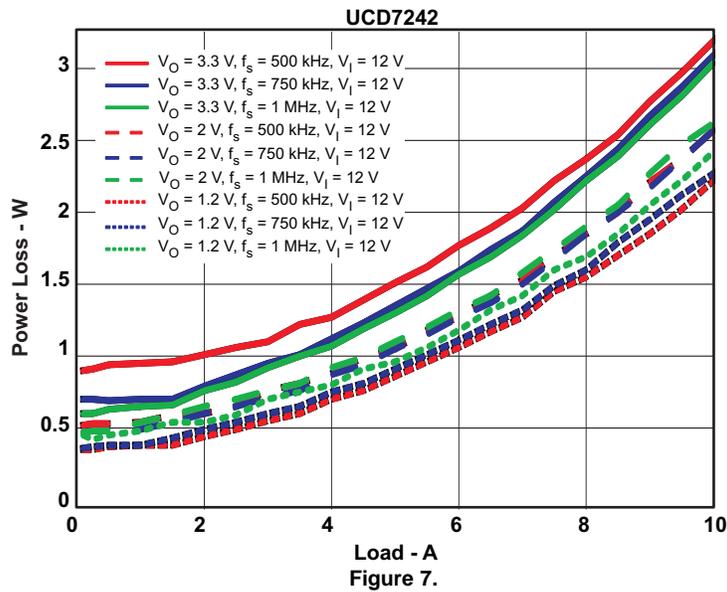
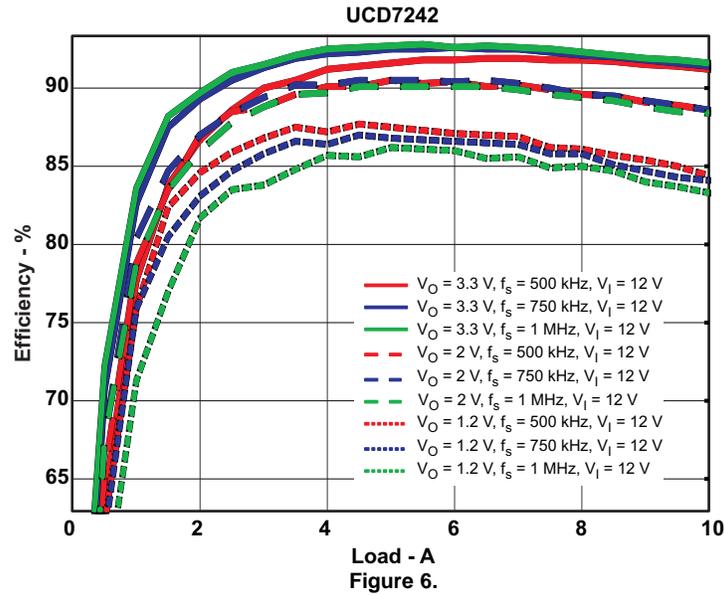
**TYPICAL CHARACTERISTICS (continued)**

Inductor used in the following plots is a 0.47µH BI Technologies inductor (HM72A). All data taken at room ambient.



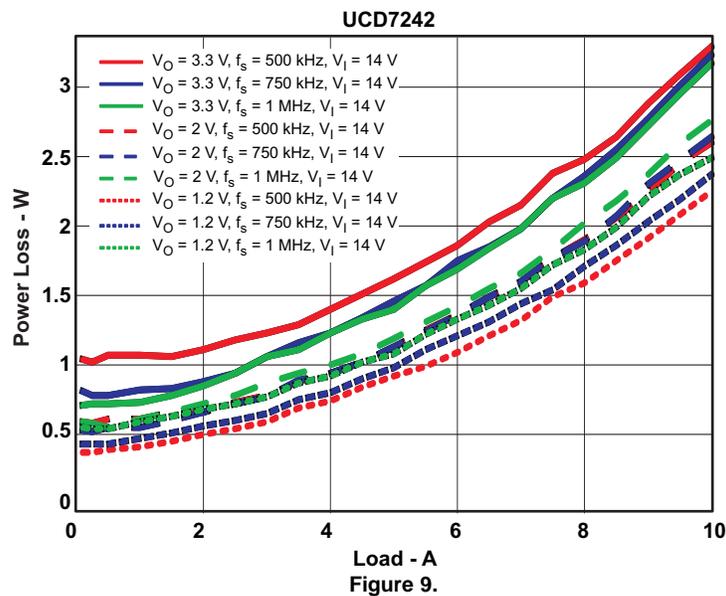
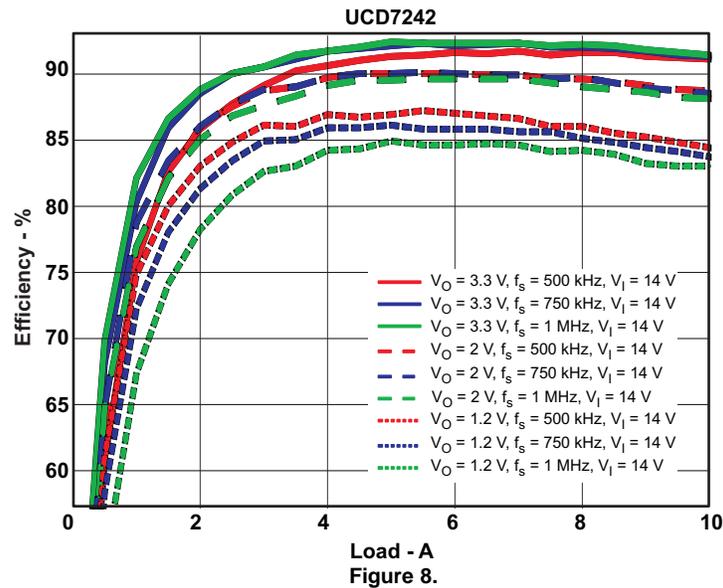
**TYPICAL CHARACTERISTICS (continued)**

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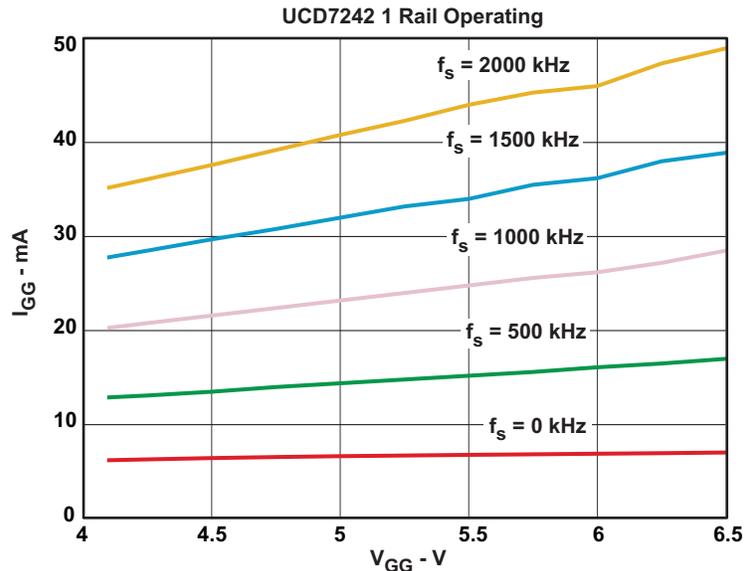


Figure 10.  $V_{GG}$  Supply Current with 1 Rail Operating and 1 Rail Off

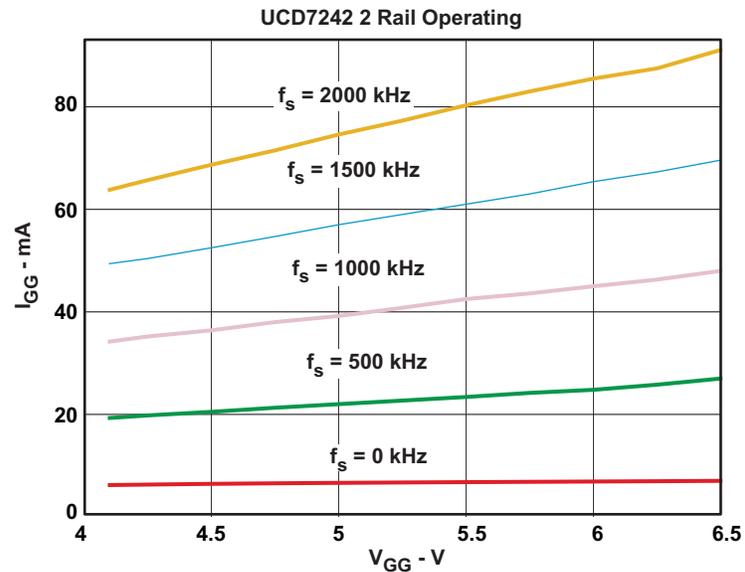


Figure 11.  $V_{GG}$  Supply Current with 2 Rails Operating

**TYPICAL CHARACTERISTICS (continued)**

Inductor used in the following plots is a 0.47µH BI Technologies inductor (HM72A). All data taken at room ambient.

Continuous Operation at  $I_{OUT} = 10A$

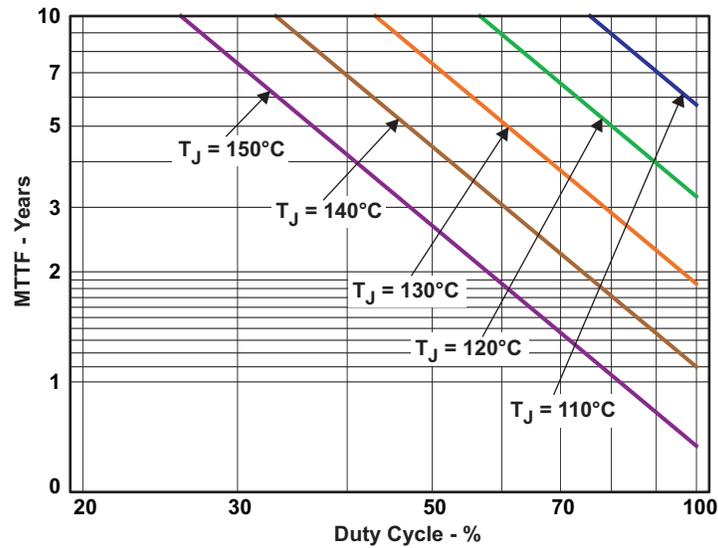


Figure 12.

Figure 12 shows the mean time to failure (MTTF) for an output load current of 10A on a single output, or an output load current of 10A on both outputs.

## DETAILED DESCRIPTION

### PWM INPUT

The PWM input pin accepts the digital signal from the controller that represents the desired high-side FET on time. This input is designed to accept 3.3V logic levels, but is also tolerant of 5V input levels. The SRE pin sets the behavior of the PWM pin. When the SRE pin is asserted high, the device is placed in synchronous mode. In this mode, the timing duration of the high-side gate drive and the low-side gate drive are both controlled by the PWM input signal. When PWM is high, the high-side MOSFET is on and the low-side MOSFET is off. When PWM is low, the high-side MOSFET is off and the low-side MOSFET is on. An optimized anti-cross-conduction delay is introduced to ensure the proper FET is turned off before the other FET is turned on. When the SRE pin is asserted low, the device is placed in non-synchronous mode. In this mode the PWM input only controls the high-side MOSFET. When PWM is high, the high-side MOSFET is on. The low side FET is always held off.

The PWM input supports a 3-state detection feature. It can detect if the PWM input signal has entered a 3-state mode. When 3-state mode is detected, both the high-side and low-side MOSFETs are held off. To support this mode, the PWM input pin has an internal pull-up resistor of approximately 50k $\Omega$  to 3.3V and a 50k $\Omega$  pull-down resistor to ground. During normal operation, the PWM input signal swings below 0.8V and above 2.5V. If the source driving the PWM pin enters a 3-state or high impedance state, the internal pull-up/pull down resistors will tend to pull the voltage on the PWM pin to 1.65V. If the voltage on the PWM pin remains within the 0.8V to 2.5V 3-state detection band for longer than  $t_{HLD\_R}$ , 3-state detection hold-off time, then the device enters 3-state mode and turns both MOSFETs off. This behavior occurs regardless of the state of the SRE pin. When exiting 3-state mode, PWM should first be asserted low and SRE High. This ensures that the bootstrap capacitor is recharged before attempting to turn on the high-side FET. The logic threshold of this pin typically exhibits 900mV of hysteresis to provide noise immunity and ensure glitch-free operation.

### SRE INPUT

The SRE (Synchronous Rectifier Enable) pin is a high impedance digital input. It is designed to accept 3.3V logic levels, but is also tolerant of 5V levels. When asserted high, the operation of the low-side synchronous rectifier FET is enabled. The state of the low-side MOSFET is governed by the PWM input. When SRE is asserted low, the low-side FET is continuously held low, keeping the FET off. While held off, current flow in the low-side FET is restricted to its intrinsic body diode. The logic threshold of this pin typically exhibits 900mV of hysteresis to provide noise immunity and ensure glitch-free operation.

### $V_{IN}$

$V_{IN}$  supplies power to the internal circuits of the device. The input power is conditioned by an internal linear regulator that provides the  $V_{GG}$  gate drive voltage. A second regulator that operates off of the  $V_{GG}$  rail produces an internal 3.3V supply that powers the internal analog and digital functional blocks. The  $V_{GG}$  regulator produces a nominal 6.2V. The output of the  $V_{GG}$  regulator is monitored by the Under-Voltage Lock Out (UVLO) circuitry. The device will not attempt to produce gate drive pulses until the  $V_{GG}$  voltage is above the UVLO threshold. This ensures that there is sufficient voltage available to drive the power FETs into saturation when switching activity begins. To use the internal  $V_{GG}$  regulator,  $V_{IN}$  should be at least 4.7V. When performing power conversion with  $V_{IN}$  values less than 4.7V, the gate drive voltage must be supplied externally. (See  $V_{GG}$  and VGG DIS sections for details.)

### $V_{GG}$

The  $V_{GG}$  pin is the gate drive voltage for the high current gate driver stages. For  $V_{IN} \geq 4.75V$ , the internal  $V_{GG}$  generator can be used. For  $V_{IN} < 4.75V$ , this pin should be driven from an external bias supply. When using the internal regulator, the VGG\_DIS pin should be tied low. When using an external  $V_{GG}$ , VGG\_DIS must be tied to  $V_{GG}$ . Current is drawn from the  $V_{GG}$  supply in fast, high-current pulses. A 4.7 $\mu F$  ceramic capacitor (10V minimum) should be connected from the  $V_{GG}$  pin to the PGND pin as close as possible to the package. Whether internally or externally supplied, the voltage on the  $V_{GG}$  pin is monitored by the ULVO circuitry. The voltage must be higher than the UVLO threshold before power conversion can occur. The average current drawn from the  $V_{GG}$  supply is dependant on the switching frequency, the absolute value of  $V_{GG}$  and the total gate charge of the power FETs inside the device.

## V<sub>GG</sub>\_DIS

This pin, when asserted high, disables the on-chip V<sub>GG</sub> linear regulator. When tied low, the V<sub>GG</sub> linear regulator is used to derive V<sub>GG</sub> from V<sub>IN</sub>. This pin is designed to be permanently tied high or low depending on the power architecture being implemented. It is not intended to be switched dynamically while the device is in operation.

## SW

The SW pin is the switching node of the power conversion stage. When configured as a synchronous buck, the voltage swing on SW normally traverses from slightly below ground to above V<sub>IN</sub>. Parasitic inductance in the high-side FET conduction path and the output capacitance (C<sub>oss</sub>) of the low side FET form a resonant circuit that can produce high frequency (> 100MHz) ringing on this node. The voltage peak of this ringing will exceed V<sub>IN</sub>. Care must be taken not to exceed the maximum voltage rating of this pin. The main areas available to impact this amplitude are: the driver voltage magnitude (V<sub>GG</sub>) and the parasitic source and return paths for the MOSFET (V<sub>IN</sub>, PGND). In some cases, a series resistor and capacitor snubber network connected from this pin to PGND can be helpful in damping the ringing and decreasing the peak amplitude. In general this should not be necessary due to the integrated nature of this part.

## BST

The BST pin provides the drive voltage for the high-side FET. A bootstrap capacitor is connected from this pin to the BST-SW node. Internally, a diode connects the BST pin to the V<sub>GG</sub> supply. In normal operation, when the high side FET is off and the low-side FET is on, the SW node is pulled to ground and, thus, holds one side of the bootstrap capacitor at ground potential. The other side of the bootstrap capacitor is clamped by the internal diode to V<sub>GG</sub>. The voltage across the bootstrap capacitor at this point is the magnitude of the gate drive voltage available to switch-on the high-side FET. The bootstrap capacitor should be a low ESR ceramic type, a minimum value of 0.22μF is recommended.

In order to ensure that the bootstrap capacitor has sufficient time to recharge, the steady-state duty cycle must not exceed what is shown in Figure 13. The curve in Figure 13 is for C<sub>BST</sub>= 0.22μF. Different values of C<sub>BST</sub> will have different DMAX limitations.

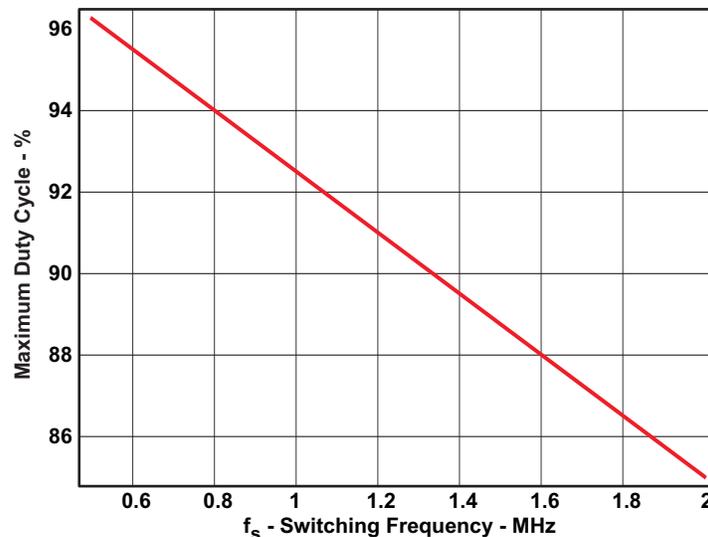


Figure 13.

## BST-SW

Electrically this node is the same as the SW pin. However, it is physically closer to the BST pin so as to minimize parasitic inductance effects of trace routing to the BST capacitor. Keeping the external traces short should minimize turn on and off times.

This pin is not sized for conducting inductor current and should not be tied to the SW pin. It is only for the BST pin capacitor connection.

## IMON

MOSFET current sense monitor output. This pin provides a current source output that is proportional to the current flowing in the power MOSFETs. The gain on this pin is equal to  $20\mu\text{A}/\text{A}$ . The  $I_{\text{MON}}$  pin should be connected to a resistor to GND to produce a voltage proportional to the power-stage load current. For example, a value of  $10\text{k}\Omega$  to ground produces a voltage of  $2.0\text{V}$  when the power stage current is  $10\text{A}$ . The accuracy of the reported current is a function of the peak to peak ripple current in the inductor ( $\Delta I$ ). The nominal behavior is described by Equation 1. The plot illustrates the possible variability in the sensed current as a function of load for a  $\Delta I=4\text{A}$ . If no PWM is detected for  $8\mu\text{s}$  IMON will report  $0\text{V}$ .

$$I_{\text{MON}}(I_{\text{OUT}}, \Delta I) = \begin{cases} 20 \frac{\mu\text{A}}{\text{A}} I_{\text{OUT}} & \text{If } I_{\text{OUT}} \geq \frac{\Delta I}{2} \\ 10 \frac{\mu\text{A}}{\text{A}} I_{\text{OUT}} + 5 \frac{\mu\text{A}}{\text{A}} \Delta I & \text{If } I_{\text{OUT}} < \frac{\Delta I}{2} \end{cases} \quad (1)$$

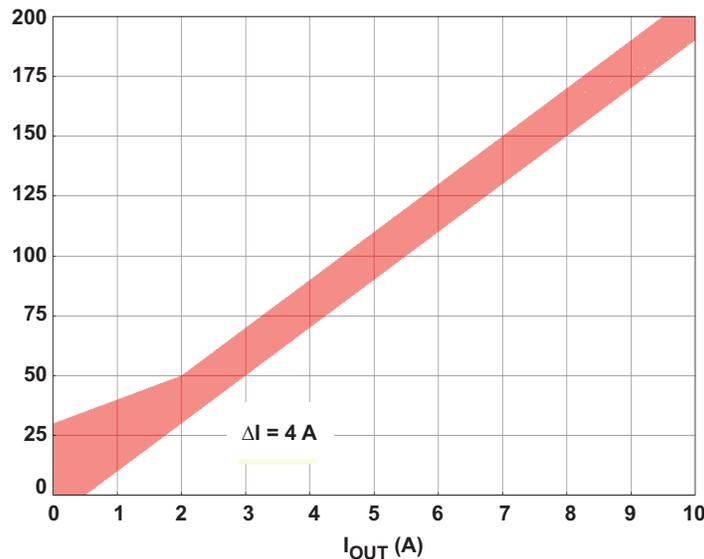


Figure 14. Sensed Current Variability

## TMON

The voltage on this pin is proportional to the die temperature with a gain of  $10\text{mV}/^\circ\text{C}$  and an offset voltage of  $0.47\text{V}$  at  $T_J = 0^\circ\text{C}$  (Equation 2):

$$T_{\text{MON}}(T_J) = 0.47\text{V} + \frac{10\text{mV}}{^\circ\text{C}}(T_J) \quad (2)$$

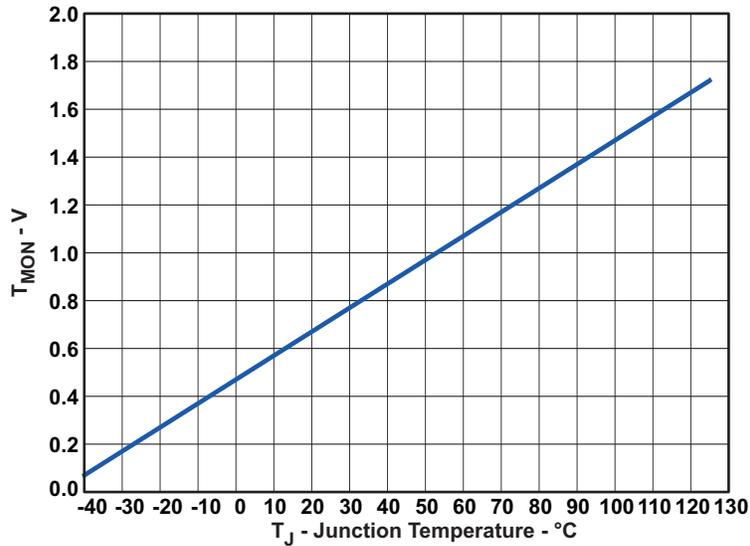


Figure 15. Typical Characteristics

If the junction temperature exceeds approximately 170°C, the device will enter thermal shutdown. This will assert the FLT pin, both MOSFETs will be turned off and the switch node will go high impedance. When the junction temperature cools by approximately 20°C, the device will exit thermal shutdown and resume switching as directed by the PWM and SRE pins. During a thermal shutdown event, the voltage on the Temp pin is driven to 3.3V.

**FLT**

This signal is a 3.3V digital output which is latched high when the current in the high-side FET exceeds the current limit trip point. When tripped, high-side FET drive pulses are truncated to limit output current. FLT is cleared on the falling edge of the first PWM pulse without a fault. Additionally, if the die temperature exceeds 170°C, the temperature sensor will initiate a thermal shutdown that halts output switching and sets the FLT flag. Normal operation resumes when the die temperature falls below the thermal hysteresis band. The FLT flag will clear after a PWM pulse occurs without a fault. Current limit is ignored during the high side blanking time. If an over current event occurs during the blanking time the part will not initiate current limit for ~50ns.

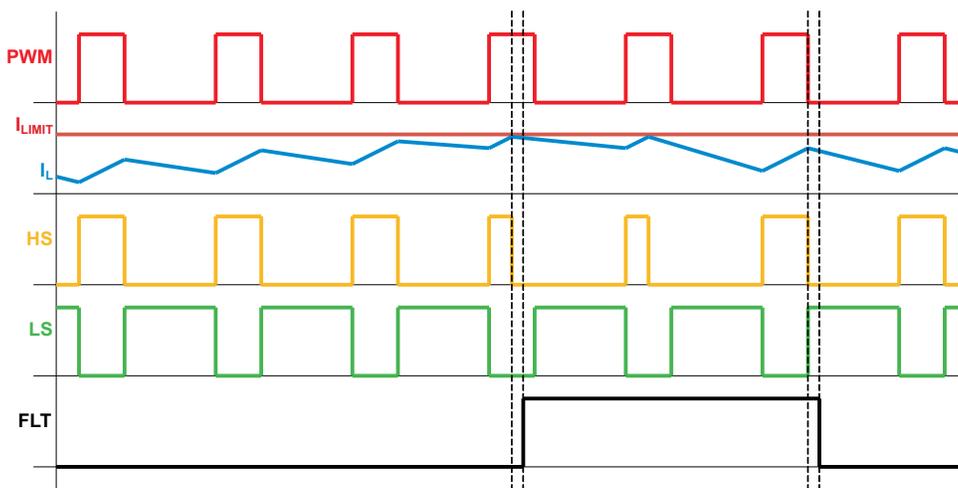


Figure 16. FLT Signal



## OPERATING FREQUENCY

Switching frequency is a key place to start the design of any DC/DC converter. This will set performance limits on things such as: maximum efficiency, minimum size, and achievable closed loop bandwidth. A higher switching frequency is, generally, going to yield a smaller design at the expense of a lower efficiency. The size benefit is principally a result of the smaller inductor and capacitor energy storage elements needed to maintain ripple and transient response requirements. The additional losses result from a variety of factors, however, one of the largest contributors is the loss incurred by switching the MOSFETs on and off. The integrated nature of the UCD7242 makes these losses drastically smaller and subsequently enables excellent efficiency from a few hundred kHz up to the low MHz. For a reasonable trade off of size versus efficiency, 750kHz is a good place to start.

### $V_{GG}$

If  $4.75V < V_{IN} \leq 6V$  a simple efficiency enhancement can be achieved by connecting  $V_{GG\_DIS}$  and  $V_{GG}$  directly to  $V_{IN}$ . This allows the solution to bypass the drop out voltage of the internal  $V_{GG}$  linear regulator, subsequently improving the enhancement of the MOSFETs. When doing this it is critical to make sure that  $V_{GG}$  never exceeds the absolute maximum rating of 7V.

## INDUCTOR SELECTION

There are three main considerations in the selection of an inductor once the switching frequency has been determined. Any real world design is an iterative trade off of each of these factors.

1. The electrical value which in turn is driven by:
  - (a) RMS current
  - (b) The maximum desired output ripple voltage
  - (c) The desired transient response of the converter
2. Losses
  - (a) Copper ( $P_{Cu}$ )
  - (b) Core ( $P_{fe}$ )
3. Saturation characteristics of the core

## INDUCTANCE VALUE

The principle equation used to determine the inductance is:

$$v_L(t) = L \frac{di_L(t)}{dt} \quad (3)$$

During the on time of the converter the inductance can be solved to be:

$$L = \frac{V_{IN} - V_{OUT}}{\Delta I} \frac{D}{f_s} \quad (4)$$

Where:

$V_{IN}$	Input Voltage
$V_{OUT}$	Output voltage
$f_s$	Switching frequency
D	Duty cycle ( $V_{OUT}/V_{IN}$ for a buck converter)
$\Delta I$	The target peak to peak inductor current.

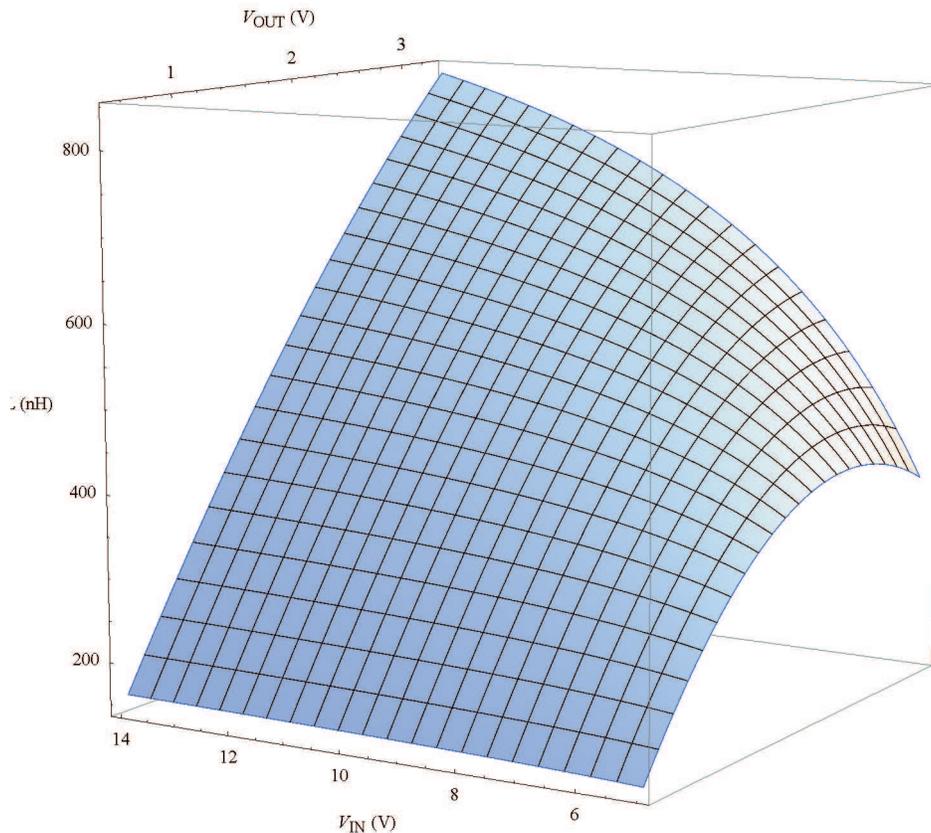
In general, it is desirable to make  $\Delta I$  large to improve transient response and small to reduce output ripple voltage and RMS current. A number of considerations go into this however,  $\Delta I = 0.4 I_{OUT}$  results in a small  $I_{LRMS}$  without an unnecessary penalty on transient response. It also creates a reasonable ripple current that most practical capacitor banks can handle. Here  $I_{OUT}$  is defined as the maximum expected steady state current.

Plugging these assumptions into the above inductance equation results in:

$$L = 5 \frac{V_{IN} - V_{OUT}}{2 \times I_{OUT}} \frac{D}{f_s} \quad (5)$$

For example, plotting this result as a function of  $V_{IN}$  and  $V_{OUT}$  results in:

$$I_{OUT} = 10.0A, f_s = 750.0kHz, N_{CRIT} = 5.00, \frac{\Delta I}{I_{OUT}} = 40.0\%, \Delta I = 4.0A$$



**Figure 17. Inductance vs.  $V_{IN}$  and  $V_{OUT}$**

In this graph  $I_{OUT}$  is 10A, the switching frequency is 750kHz and the inductor  $\Delta I$  is 4A. If the switching frequency is cut in half then the resulting inductance would be twice the value shown. Notice that the maximum inductance occurs at the maximum  $V_{IN}$  and  $V_{OUT}$  shown on the plot. In general, this inductance value should be used in order to keep the inductor ripple current from becoming too large over the range of supported  $V_{IN}$  and  $V_{OUT}$ .

## INDUCTOR LOSSES AND SATURATION

The current rating of an inductor is based on two things: the current necessary to raise the component temperature by 40°C and the current level necessary to reduce the inductance to 80% of its initial value (saturation current <sup>(1)</sup>). The current rating is the lower of these two numbers. Both of these factors are influenced by the choice of core material. Popular materials currently in use are: ferrite, powdered alloy and powdered iron.

Ferrite is regarded as the highest performance material and as such is the lowest loss and the highest cost. Solid ferrite all by itself will saturate with a relatively small amount of current. This can be addressed by inserting a gap into the core. This, in effect, makes the inductor behave in a linear manner over a wide DC current range. However, once the inductance begins to roll off, these gapped materials exhibit a “sharp” saturation characteristic. In other words, the inductance value reduces rapidly with increases in current above the saturation level. This small inductance that results, can produce dangerously high current levels.

(1) Although “saturation current” is standard terminology among many inductor vendors, technically saturation does not occur until the relative permeability of the core is reduced to approximately 1. This is a value much larger than what is typically seen on data sheets.

Powdered iron has the advantage of lower cost and a soft saturation characteristic; however, its losses can be very large as switching frequencies increase. This can make it undesirable for a UCD7242 based application where higher switching frequency may be desired. It's also worth noting that many powdered iron cores exhibit an aging characteristic where the core losses increase over time. This is a wear-out mechanism that needs to be considered when using these materials.

The powdered alloy cores bring the soft saturation characteristics of powdered iron with considerable improvements in loss without the wear-out mechanism observed in powdered iron. These benefits come at a cost premium.

In general the following relative figure of merits can be made:

	<b>Ferrite</b>	<b>Powdered Alloy</b>	<b>Powdered Iron</b>
Cost	High	Medium	Low
Loss	Low	Medium	High
Saturation	Rapid	Soft	Soft

When selecting an inductor with an appropriate core it's important to have in mind the following:

1.  $I_{LRMS}$ , maximum RMS current
2.  $\Delta I$ , maximum peak to peak current
3.  $I_{MAX}$ , maximum peak current

The RMS current can be determined by [Equation 6](#):

$$I_{LRMS} = \sqrt{I_{OUT}^2 + \frac{\Delta I^2}{12}} \quad (6)$$

When the 40% ripple constraint is used at maximum load current, this equation simplifies to:  $I_{LRMS} \approx I_{OUT}$ .

It is widely recognized that the Steinmetz equation ( $P_{fe}$ ) is a good representation of core losses for sinusoidal stimulation. It is important to recognize that this approximation applies to sinusoidal excitation only. This is a reasonable assumption when working with converters whose duty cycles are near 50%, however, when the duty cycle becomes narrow this estimate may no longer be valid and considerably more loss may result.

$$P_{fe} = k \times f^\alpha \times B_{AC}^\beta \quad (7)$$

The principle drivers in this equation are the material and its respective geometry ( $k$ ,  $\alpha$ ,  $\beta$ ), the peak AC flux density ( $B_{AC}$ ) and the excitation frequency ( $f$ ). The frequency is simply the switching frequency of the converter while the constant  $k$ , can be computed based on the effective core volume ( $V_e$ ) and a specific material constant ( $k_{fe}$ ).

$$k = k_{fe} \times V_e \quad (8)$$

The AC flux density ( $B_{AC}$ ) is related to the conventional inductance specifications by the following relationship:

$$B_{AC} = \frac{L}{A_e \times N} \frac{\Delta I}{2} \quad (9)$$

Where  $L$  is the inductance,  $A_e$ , is the effective cross sectional area that the flux takes through the core and  $N$  is the number of turns.

Some inductor manufactures use the inductor  $\Delta I$  as a figure of merit for this loss, since all of the other terms are a constant for a given component. They may provide a plot of core loss versus  $\Delta I$  for various frequencies where  $\Delta I$  can be calculated as:

$$\Delta I = \frac{V_{IN} - V_{OUT}}{L} \frac{D}{fs} \quad (10)$$

$I_{MAX}$  has a direct impact on the saturation level. A good rule of thumb is to add 15% of head room to the maximum steady state peak value to provide some room for transients.

$$I_{MAX} = 1.15 \times \left( I_{OUT} + \frac{\Delta I}{2} \right) \quad (11)$$

For example for a 10A design has the following:

$I_{OUT}$	10A
$I_{LRMS}$	10A
$\Delta I$	4A
$I_{MAX}$	13.8A

Armed with this data one can now approach the inductor data sheet to select a part with a “saturation” limit above 13.8A and current “heating” limit above 10A. Furthermore, total losses can be estimated based on the datasheet DCR value ( $I_{LRMS}^2 DCR$ ) and the core loss curves for a given frequency and  $\Delta I$ .

## INPUT CAPACITANCE

Due to the non-zero impedance of the power planes of the input voltage rail, it is necessary to add some local capacitance near the UCD7242 to ensure that the voltage at this node is quiet and stable. The primary things to consider are:

1. The radiated fields generated by the  $di/dt$  and  $dv/dt$  from this node
2. RMS currents capability needed in the capacitors
3. The AC voltage present and respective susceptibility of any device connected to this node

$$I_{CINRMS} = \sqrt{I_{OUT}^2 \times D \times (1 - D) + \frac{\Delta I^2}{12} \times D} \quad (12)$$

As a point of reference if  $\Delta I = 0.4 I_{OUT}$  this places the worst case  $I_{CINRMS}$  at approximately 5A. This corresponds to a duty cycle of approximately 50%. Other duty cycles can result in a significantly lower RMS current.

A good input capacitor would be a 22 $\mu$ F X5R ceramic capacitor. Equally important as selecting the proper capacitor is placing and routing that capacitor. It is crucial that the decoupling be placed as close as possible to both the power pin ( $V_{IN}$ ) and ground (PGND). It is important to recognize that each power stage should have its own local decoupling. One 22 $\mu$ F capacitor should be placed across each  $V_{IN}$  and PGND pair. The proximity of the capacitance to these pins will reduce the radiated fields mentioned above.

## OUTPUT CAPACITANCE

The goal of the output capacitor bank is to keep the output voltage within regulation limits during steady state and transient conditions.

The total AC RMS current flowing through the capacitor bank can be calculated as:

$$I_{COUTRMS} = \frac{\Delta I}{\sqrt{12}} \quad (13)$$

For a single type of output capacitor the output ripple voltage wave form can be approximated by the following equation:

$$V_{OUT}(t) = I_C(t) \times esr + \frac{1}{C} \int_0^t I_C(\tau) \times d\tau \quad (14)$$

Where:

$$I_C(t) = \begin{cases} \frac{\Delta I \times f_s}{D} \times t - \frac{\Delta I}{2} & t < \frac{D}{f_s} \\ \frac{\Delta I \times f_s}{1-D} \times \left( t - \frac{D}{f_s} \right) + \frac{\Delta I}{2} & \text{otherwise} \end{cases} \quad (15)$$

After substitution and simplification yields

$$V_{OUT}(t) = \begin{cases} esr \times \left( \frac{\Delta I \times f_s}{D} \times t - \frac{\Delta I}{2} \right) + \frac{1}{C} \times \left( \frac{t \times \Delta I \times (f_s \times t - D)}{2 \times D} - \frac{\Delta I \times (1 - 2 \times D)}{12 \times f_s} \right) & t < \frac{D}{f_s} \\ esr \times \left( \frac{\Delta I \times f_s}{1-D} \times \left( t - \frac{D}{f_s} \right) + \frac{\Delta I}{2} \right) + \frac{1}{C} \times \left( \frac{\Delta I \times (f_s \times t - 1) \times (D - f_s \times t)}{2 \times (1-D) \times f_s} - \frac{\Delta I \times (1 - 2 \times D)}{12 \times f_s} \right) & \text{otherwise} \end{cases} \quad (16)$$

The term in this equation multiplied by the esr gives the ripple voltage component due to esr and the term multiplied by  $1/C$  gives the ripple voltage component due to the change in charge on the capacitor plates. In the case where the esr component dominates the peak to peak output voltage can be approximated as:

$$V_{PPesr} \approx \Delta I \times esr \quad (17)$$

When the charge term dominates the peak to peak voltage ripple becomes:

$$V_{PPQ} \approx \frac{\Delta I}{8 \times C \times f_s} \quad (18)$$

It is tempting to simply add these two results together for the case where the voltage ripple is significantly influenced by both the capacitance and the esr. However, this will yield an overly pessimistic result, in that it does not account for the phase difference between these terms.

Using the ripple voltage equations and the RMS current equation should give a design that safely meets the steady state output requirements. However, additional capacitance is often needed to meet transient requirements and the specific local decoupling requirements of any IC that is being powered off of this voltage. This is not just a function of the capacitor bank but also the dynamics of the control loop. See the *UCD9240 Compensation Cookbook* for additional details.

## DECOUPLING

It is necessary that  $V_{GG}$  and BP3 have their own local capacitance as physically close as possible to these pins. The  $V_{GG}$  capacitor should be connected as close as possible to pin 5 and PGND with a  $4.7\mu F$  ceramic capacitor. The BP3 capacitor should be connected as close as possible to pin 22 and AGND with a  $1\mu F$  ceramic capacitor.

The UCD7242 also supports the ability to operate from input voltages down to 2.2V. In these cases an additional supply rail must be connected to  $V_{GG}$  and  $V_{GG\_DIS}$  must be shorted to  $V_{GG}$ . Potential external bias supply generators for low  $V_{IN}$  operation: *TPS63000*, *TPS61220*. The amount of current required for this supply is dependant on the  $V_{GG}$  voltage, the switching frequency and the number of active channels used in the UCD7242. When both sides are active, use [Figure 11:  \$V\_{GG}\$  Supply Current with 2 Rails Operating](#) for current draw estimates. If only one side is active, use [Figure 10:  \$V\_{GG}\$  Supply Current with 1 Rail Operating and 1 Rail Off](#).

## CURRENT SENSE

An appropriate resistor must be connected to the current sense output pins to convert the  $I_{MON}$  current to a voltage. In the case of the UCD9XXX digital controllers, these parts have a full scale current monitor range of 0V to 2V. It is desirable to maximize this range to make full use of the current monitoring resolution inside the controller. In order to ensure that current sensing will occur all the way to  $I_{MAX}=10A$  a 1.8V target is chosen. In this case a resistor  $9.09k\Omega$  would work.

$$R_{MON} = \frac{V_{MON}}{I_{MAX} \times 20 \frac{\mu A}{A}} \quad (19)$$

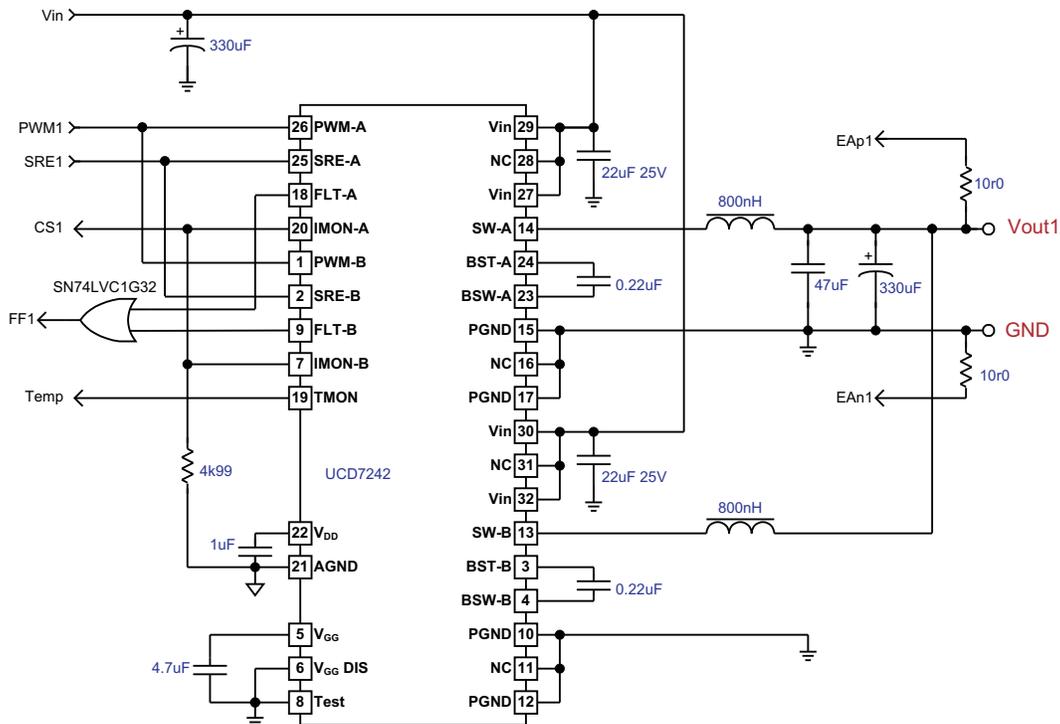
In some applications it may be necessary to filter the  $I_{MON}$  signal. The UCD7242  $I_{MON}$  pin is a current source output, so a capacitor to ground in parallel with the current-to-voltage conversion resistor is all that is required. As a rule of thumb, placing the corner frequency of the filter at 20% of the switching frequency should be sufficient.

For example, if the switching frequency is 500kHz or higher the ripple frequency will be easily rejected with a corner frequency of approximately 100kHz. With a 100kHz pole point, the filter time constant is  $1.6\mu s$ . A fast current transient should be detected within  $4.8\mu s$ .

$$C_{MON} = \frac{1}{2 \times \pi \times R_{MON} \times 20\% \times f_s} \quad (20)$$

## 20A Power Stage

It is possible to configure the UCD7242 to supply 20A by tying the outputs of two power stages together. When doing this it is required that the PWM pulse widths of the two PWM input signals be identical. The best way to do this is to drive PWM-A and PWM-B from the same signal. This ensures that balanced volt seconds will be applied to the external SW pins.



**Figure 18. 20A Design**

## Layout Recommendations

The primary thermal cooling path is from the  $V_{IN}$ , GND, and the SW “stripes” on the bottom of the package. Wide copper traces should connect to these nodes. 1-ounce copper should be the minimum thickness of the top layer; however, 2-ounce copper is better. Multiple thermal vias should be placed near the GND stripes that connect to a PCB ground plane. There is room to place multiple 10-mil (0.25mm) diameter vias next to the  $V_{IN}$  and GND stripes under the package.

For input bypassing, the 22 $\mu$ F input ceramic capacitors should be connected as close as possible to the  $V_{IN}$  and GND stripes. If possible, the input caps should be placed directly under the UCD7242 using multiple 10-mil vias to bring the  $V_{IN}$  and GND connections to the back side of the board. Minimizing trace inductance in the bypass path is extremely important to reduce the amplitude of ringing on the switching node.

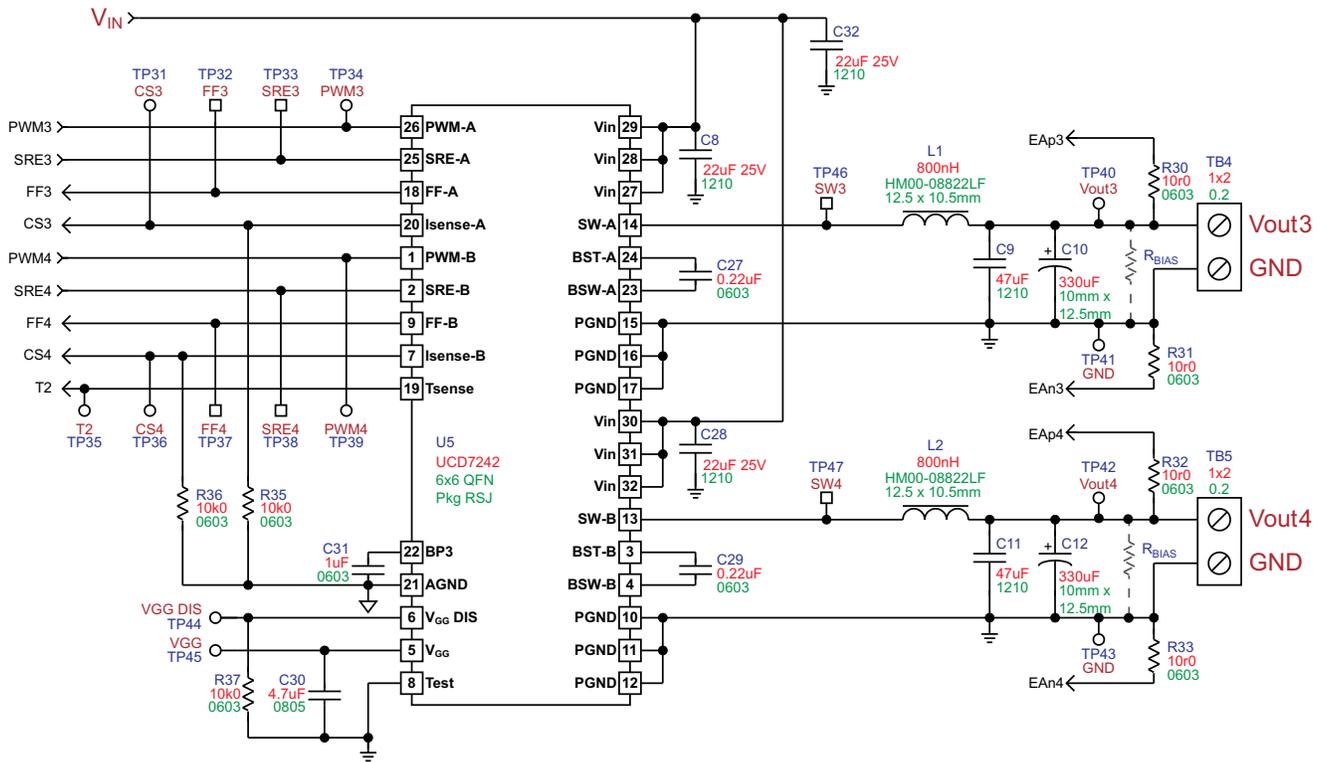


Figure 19. Schematic Fragment from 4-Output EVM

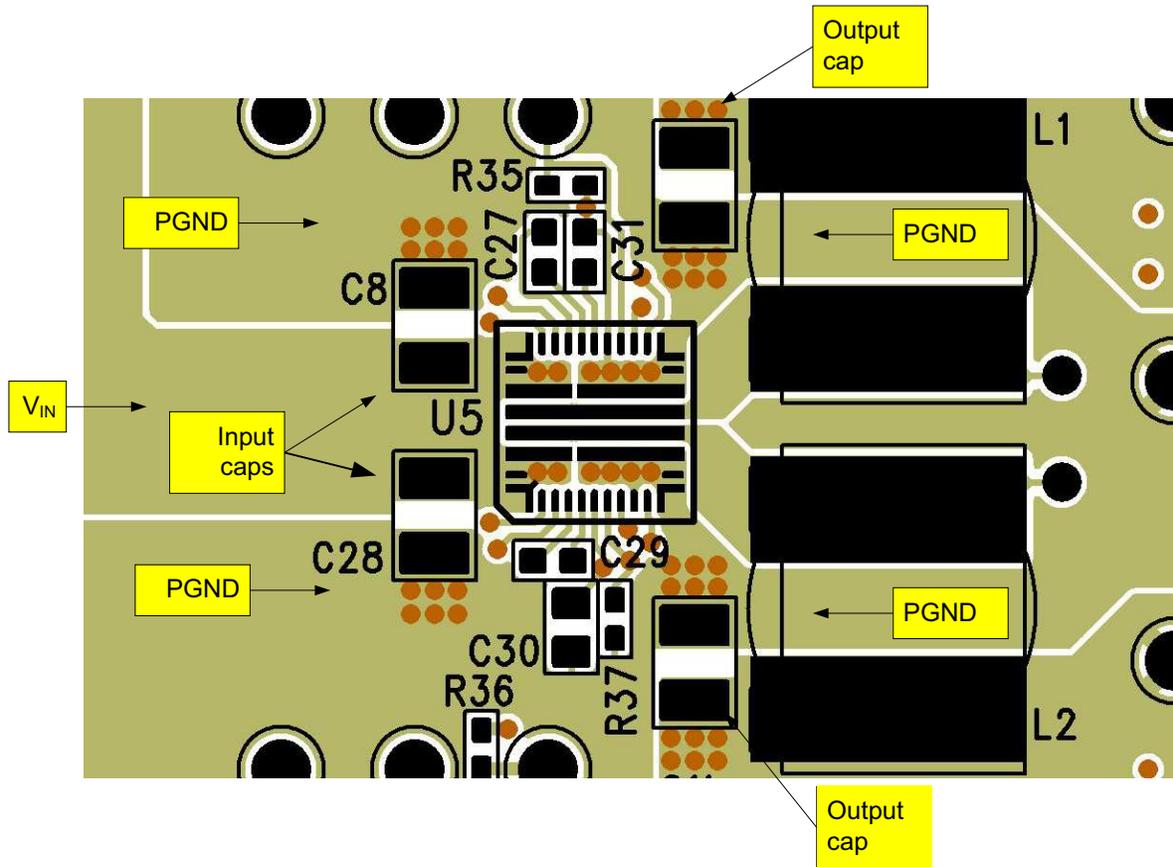
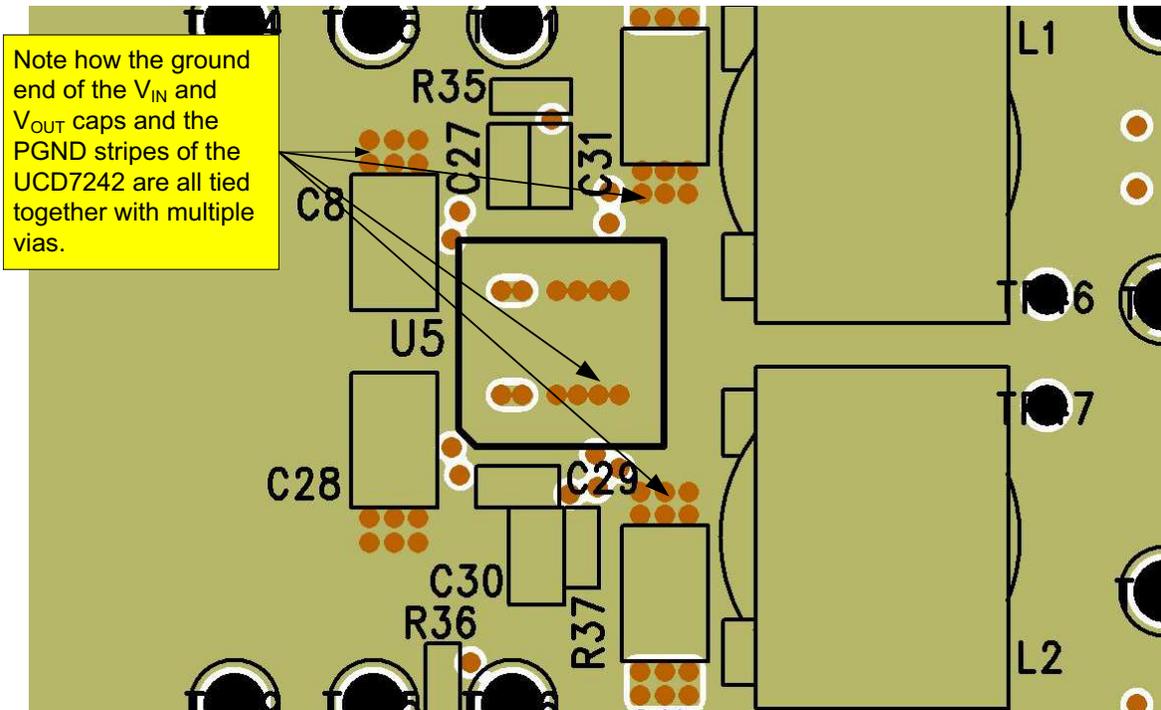


Figure 20. Top Layer



Note: This is the primary heat dispersal layer as well as the major return-current path.

Figure 21. Layer 2 - Power GND Plane

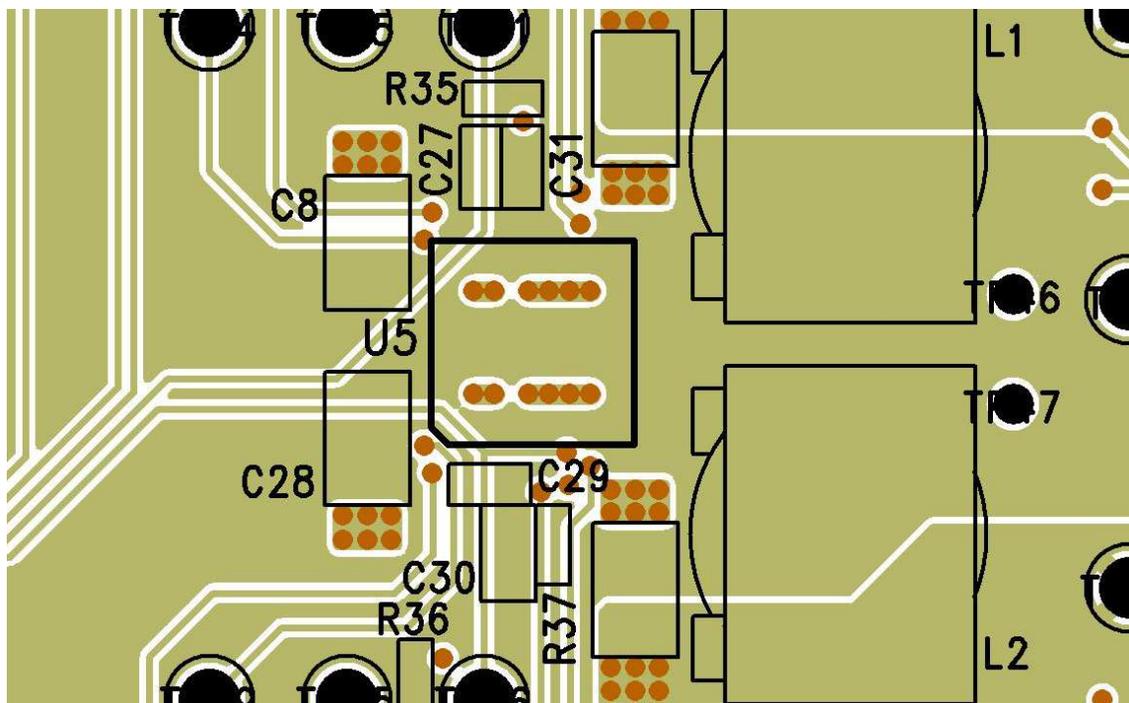


Figure 22. Layer 3

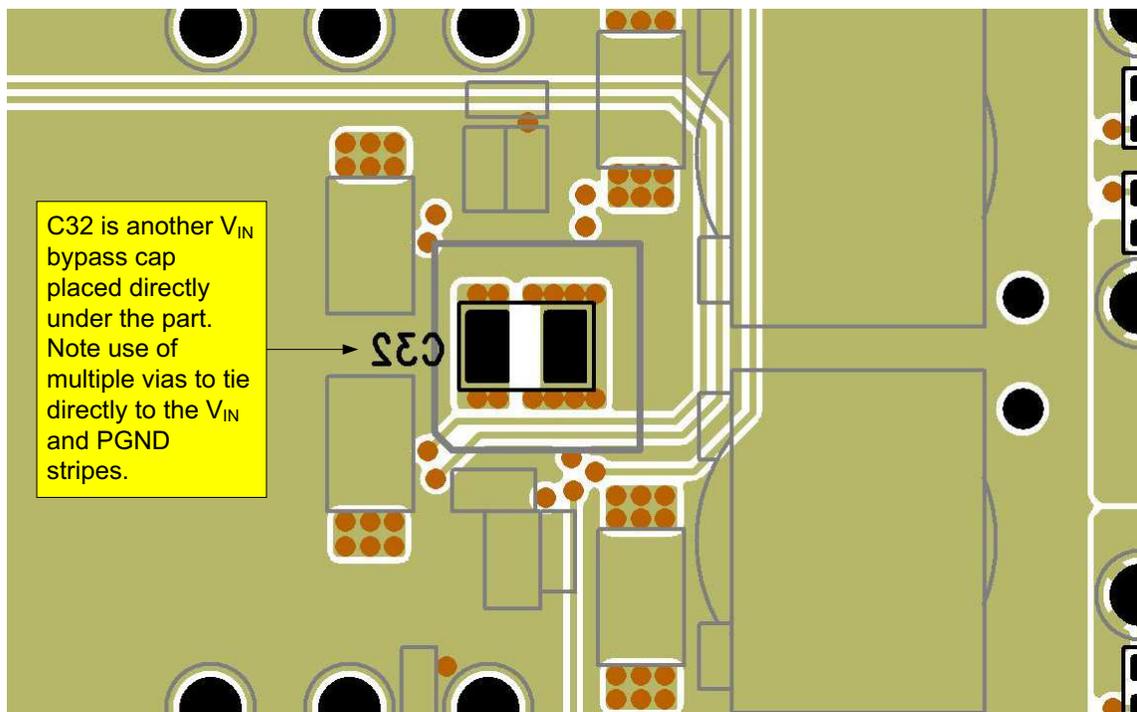


Figure 23. Bottom Layer (X-ray View)

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">UCD7242MRSJREP</a>	Active	Production	VQFN-HR (RSJ)   32	2500   LARGE T&R	ROHS Exempt	NIPDAU	Level-1-260C-UNLIM	-55 to 125	UCD7242 EP
<a href="#">V62/14601-01XE</a>	Active	Production	VQFN-HR (RSJ)   32	2500   LARGE T&R	ROHS Exempt	NIPDAU	Level-1-260C-UNLIM	-55 to 125	UCD7242 EP

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**OTHER QUALIFIED VERSIONS OF UCD7242-EP :**

- Catalog : [UCD7242](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCD7242MRSJREP	VQFN-HR	RSJ	32	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2

**TAPE AND REEL BOX DIMENSIONS**

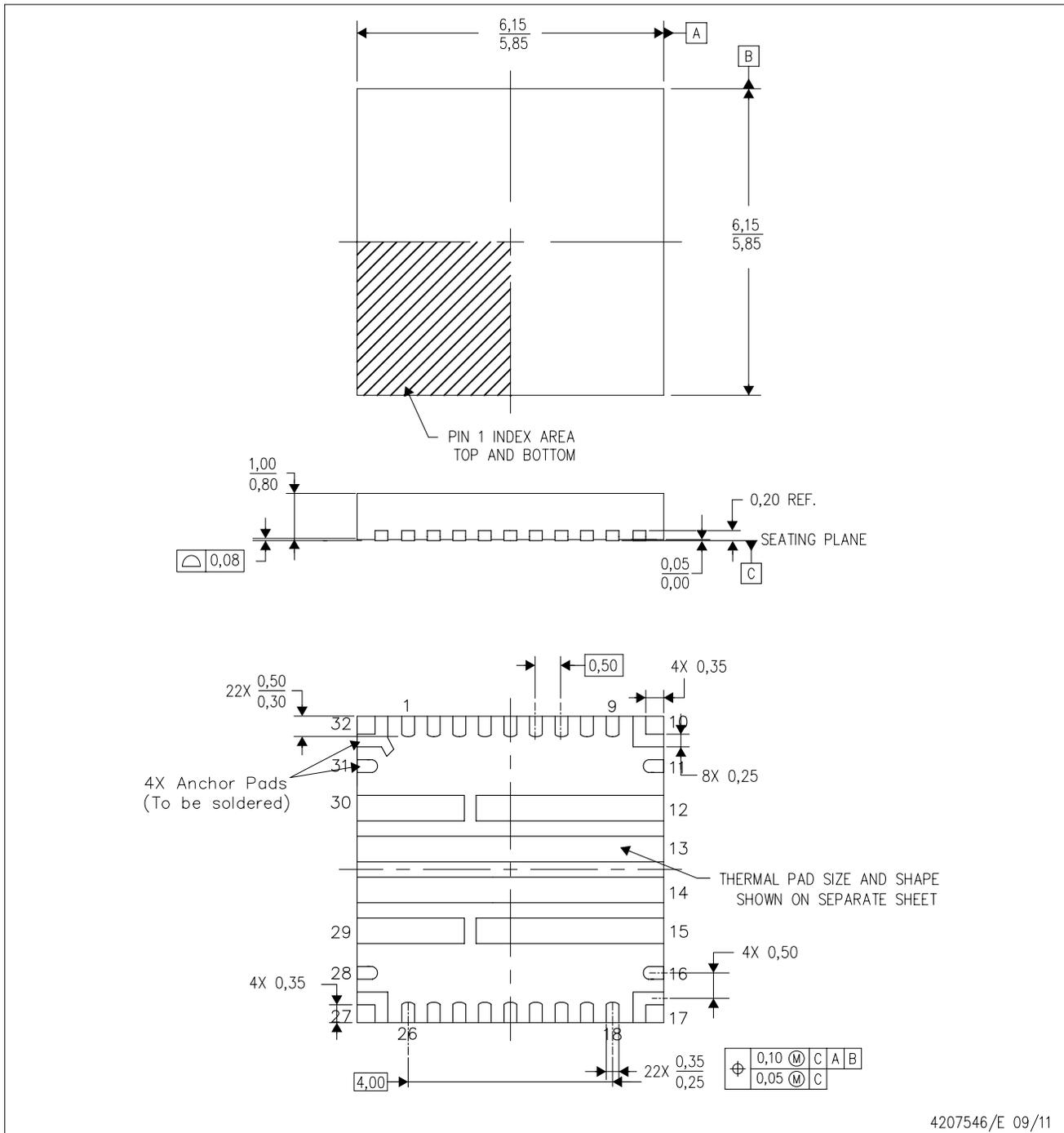

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCD7242MRSJREP	VQFN-HR	RSJ	32	2500	353.0	353.0	32.0

# MECHANICAL DATA

RSJ (S-PVQFN-N32)

PLASTIC QUAD FLATPACK NO-LEAD



4207546/E 09/11

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - Quad Flatpack, No-leads (QFN) package configuration.
  - The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

# THERMAL PAD MECHANICAL DATA

RSJ (S-PVQFN-N32)

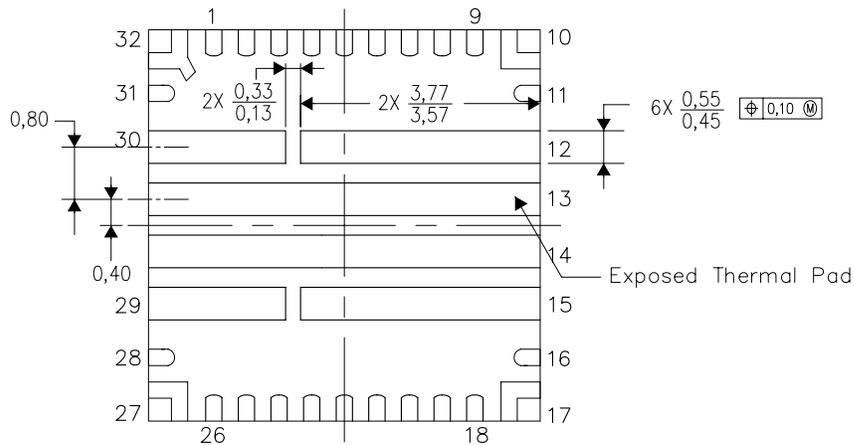
PLASTIC QUAD FLATPACK NO-LEAD

## THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

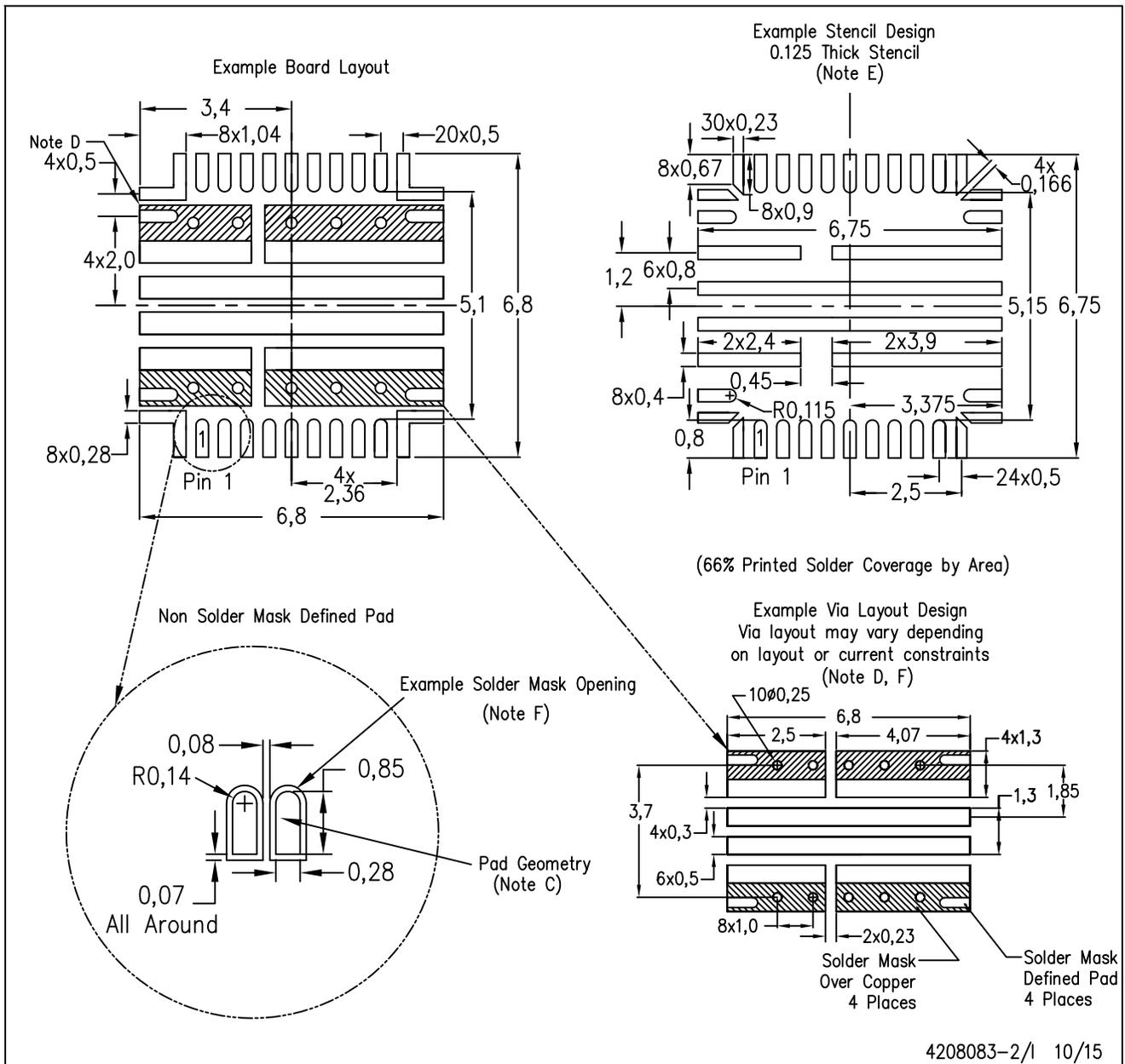
Exposed Thermal Pad Dimensions

4208082/F 09/11

NOTE: All linear dimensions are in millimeters

RSJ (S-PVQFN-N32)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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Last updated 10/2025