



## High-Current, Synchronous Buck Power Stage

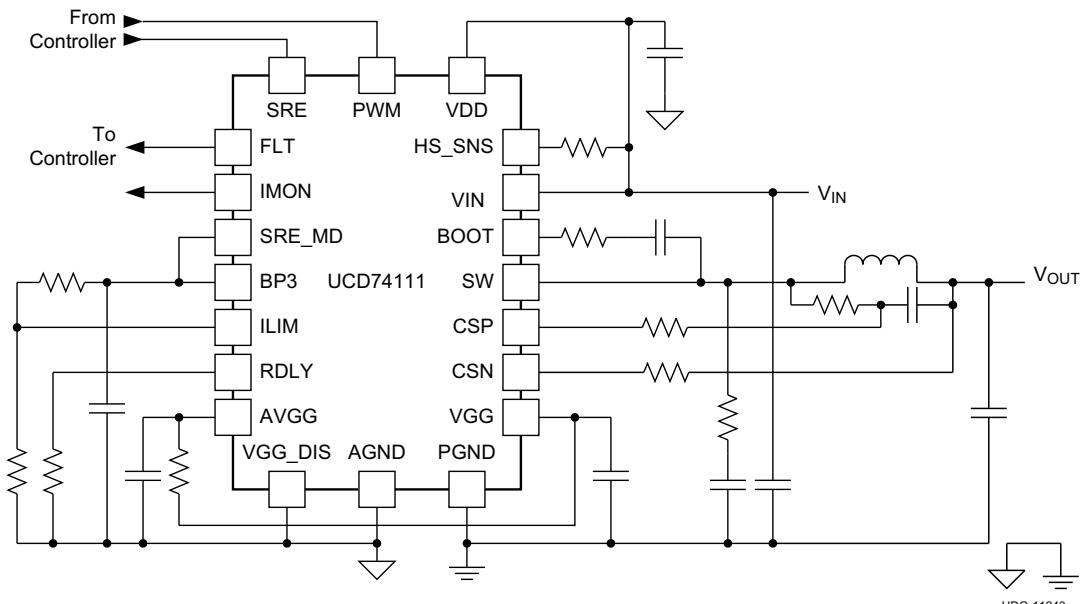
### FEATURES

- Integrates Synchronous Buck Driver and NexFET™ Power MOSFET Technology for High Power Density and High Efficiency
- 15-A Output Current Capability for DSP and ASIC
- 4.7-V to 14-V Input Voltage Range
- Operational Switching Frequency Up to 2 MHz
- Built-In High-Side Current Protection
- DCR Current Sensing for Overcurrent Protection and Output Current Monitoring
- Voltage Proportional to Load Current Monitor Output
- Tri-State PWM Input for Power Stage Shutdown
- UVLO Housekeeping Circuit
- Integrated Thermal Shutdown
- 40-Pin, 5 mm x 7 mm, PQFN PowerStack™ Package

### APPLICATIONS

- Digital or Analog POL Power Modules
- High Power Density DC-DC Converters for Telecom and Networking Applications

### APPLICATION DIAGRAM



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### ORDERING INFORMATION<sup>(1)</sup>

TEMPERATURE RANGE	PINS	PACKAGE	ORDERING NUMBER
–40°C to 125°C	40	RVF	UCD74111RVF

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at [www.ti.com](http://www.ti.com).

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		VALUE	UNIT
		MIN	MAX
Voltage range	VDD, VIN	–0.3	16
	SW DC	–1	16
	SW Pulse < 400 ns, E = 20 μJ	–2	20
	SW Pulse < 64 ns	–5	22
	SW Pulse < 40 ns	–7	25
	VGG, AVGG (Externally supplied)	–0.3	7
	BOOT DC	–0.3	23
	BOOT Pulse (SW at 20 V < 400 ns)	–0.3	27
	BOOT Pulse (SW at 22 V < 64 ns)	–0.3	29
	BOOT Pulse (SW at 25 V < 40 ns)	–0.3	32
	ILIM, VGG_DIS, IMON, FLT	–0.3	3.6
	CSP, CSN, RDLY, PWM, SRE, SRE_MD	–0.3	5.6
Temperature	HS_SNS	–0.3	16
	T <sub>J</sub>	–40	150
	T <sub>stg</sub>	–55	150

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those included under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods of time may affect device reliability.

## THERMAL INFORMATION

THERMAL METRIC <sup>(1)</sup>	UCD74111	UNITS
	PQFN (RVF) 40-PIN	
θ <sub>JA</sub> Junction-to-ambient thermal resistance	28.9	°C/W
θ <sub>JCTop</sub> Junction-to-case (top) thermal resistance	15.4	
Ψ <sub>JT</sub> Junction-to-top characterization parameter	0.2	
Ψ <sub>JB</sub> Junction-to-board characterization parameter	5.1	
θ <sub>JCbot</sub> Junction-to-case (bottom) thermal resistance	0.8	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](http://www.ti.com).

**RECOMMENDED OPERATING CONDITIONS**

		MIN	TYP	MAX	UNIT
VDD, VIN		4.7		14	V
VGG, AVGG	Externally supplied gate drive voltage	4.6		6.5	V
T <sub>J</sub>	Operating junction temperature	-40		125	°C

**ELECTROSTATIC DISCHARGE (ESD) PROTECTION**

		MIN	TYP	MAX	UNIT
Human body model (HBM)		1.5			kV
Charge device model (CDM)		500			V

## ELECTRICAL CHARACTERISTICS

$T_J = -40^\circ\text{C}$  to  $125^\circ\text{C}$ ,  $V_{\text{VDD}} = V_{\text{VIN}} = 12\text{ V}$ , all parameters at zero power dissipation (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>INPUT SUPPLY</b>					
$V_{\text{VIN}}$	Input supply voltage range		4.7	14	V
$V_{\text{VDD}}$					
$I_{\text{VDD}}$	Supply current	Not switching, PWM = LOW	8	10	mA
<b>GATE DRIVE UNDER-VOLTAGE LOCKOUT</b>					
$V_{\text{GG-ON}}$	UVLO on voltage		4.4	4.6	V
$V_{\text{GG-OFF}}$	UVLO off voltage		4.1	4.3	V
$V_{\text{GG-HYS}}$	UVLO hysteresis voltage		80		mV
<b>VGG SUPPLY GENERATOR</b>					
$V_{\text{GG}}$	Output voltage	$V_{\text{VIN}} = 12\text{ V}$ , $I_{\text{GG}} = 50\text{ mA}$	5.3	6.0	6.8
$V_{\text{DO}}$	Dropout voltage, $V_{\text{VDD}} - V_{\text{GG}}$	$V_{\text{VIN}} = 4.7\text{ V}$ , $I_{\text{GG}} = 50\text{ mA}$		350	mV
<b>BP3 REGULATOR</b>					
$V_{\text{BP3}}$	Output voltage	$V_{\text{VIN}} = 12\text{ V}$ , $I_{\text{BP3}} = 2\text{ mA}$	3.0	3.2	3.3
<b>DIGITAL INPUT SIGNALS (PWM, SRE)</b>					
$V_{\text{IH-PWM}}$	Positive-going input threshold voltage		1.8	2.1	V
$V_{\text{IL-PWM}}$	Negative-going input threshold voltage		0.8	0.9	V
PWM	Input voltage hysteresis, ( $V_{\text{IH}} - V_{\text{IL}}$ )		0.9		V
$V_{\text{IH-SRE}}$	Positive-going input threshold voltage		1.5	1.7	V
$V_{\text{IL-SRE}}$	Negative-going input threshold voltage		0.9	1.0	
SRE	Input voltage hysteresis, ( $V_{\text{IH}} - V_{\text{IL}}$ )		0.45		V
$I_{\text{PWM}}$	Input current	$V_{\text{PWM}} = 5\text{ V}$	140		$\mu\text{A}$
		$V_{\text{PWM}} = 3.3\text{ V}$	70		
		$V_{\text{PWM}} = 0\text{ V}$	-63		
$I_{\text{SRE}}$	Input current	$V_{\text{SRE}} = 5\text{ V}$	190		$\mu\text{A}$
		$V_{\text{SRE}} = 3.3\text{ V}$	12		
		$V_{\text{SRE}} = 0\text{ V}$	-330		
$t_{\text{HLD-R}}^{(1)}$	tri-state hold-off time	$V_{\text{PWM}}$ transition from 0 V to 1.65 V, time until low-side drive falls to 0 V	450	600	750
<b>OUTPUT CURRENT LIMIT (ILIM)</b>					
$R_{\text{ILIM-IN}}^{(1)}$	ILIM input impedance		250		$\text{k}\Omega$
$V_{\text{ILIM}}$	ILIM set point range		0.5	3	V
$V_{\text{FLT-HI}}$	FLT output high level	$I_{\text{LOAD}} = -2\text{ mA}$	2.7	3.3	V
$V_{\text{FLT-LO}}$	FLT output low level	$I_{\text{LOAD}} = 2\text{ mA}$		0.1	0.6
$t_{\text{FAULT-FLT}}^{(1)}$	Fault detection time. Delay until FLT asserted	$V_{\text{ILIM}} = 1.5\text{ V}$ , $(V_{\text{CSP}} - V_{\text{CSN}}) = 20\text{ mV}$ , $V_{\text{CSN}} = 1.8\text{ V}$		350	475
$t_{\text{DLY}}^{(1)}$	Propagation delay from PWM to reset FLT	PWM falling to FLT falling after a current limit event clears. PWM pulse width $\geq 100\text{ ns}$		85	200
<b>CURRENT SENSE BLANKING (RDLY, HS_SNS)</b>					
$I_{\text{RDLY}}$	RDLY source current	8.06 $\text{k}\Omega$ resistor from RDLY to AGND	90		$\mu\text{A}$
$R_{\text{RDLY}}^{(1)}$	RDLY resistance range		5.00	8.06	25.00
$t_{\text{BLANK}}$	HS_SNS blanking time	$R_{\text{RDLY}} = 8.06\text{k}\Omega$ . From SW rising to HS fault comparator enabled.	110	125	140
$I_{\text{OCH}}$	Overcurrent threshold for high-side FET	$T_J = 25^\circ\text{C}$ , $(V_{\text{BOOT}} - V_{\text{SW}}) = 5.5\text{V}$		30	A

(1) Ensured by design. Not production tested.

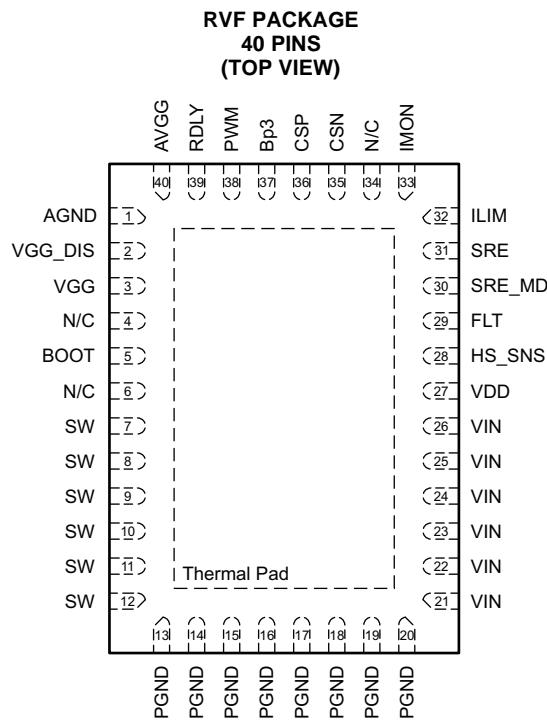
## ELECTRICAL CHARACTERISTICS (continued)

$T_J = -40^\circ\text{C}$  to  $125^\circ\text{C}$ ,  $V_{\text{VDD}} = V_{\text{VIN}} = 12\text{ V}$ , all parameters at zero power dissipation (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>CURRENT SENSE AMPLIFIER (IMON, CSP, CSN)</b>					
$V_{\text{IMON}}$	IMON voltage at no load	CSP = CSN = 1.8V	0.46	0.50	0.54
$R_{\text{CS-IN}}^{(2)}$	Input impedance	Differential, $(V_{\text{CSP}} - V_{\text{CSN}})$	100		$\text{k}\Omega$
$G_{\text{CS}}$	Closed loop DC gain	$(V_{\text{CSP}} - V_{\text{CSN}}) = 10\text{ mV}$ , $0.5\text{ V} \leq V_{\text{CSN}} \leq 3.3\text{ V}$	48	50.2	52.4
		Gain with 2.49 $\text{k}\Omega$ resistors in series with CSP, CSN	45.0	47.0	49.2
$V_{\text{CM}}^{(2)}$	Input common mode voltage range	$V_{\text{CM}}$ maximum limit is $(V_{\text{VGG}} - 1.2\text{ V})$	-0.3	5.3	V
$V_{\text{IMON(min)}}$	Minimum IMON voltage	$V_{\text{CSP}} = 1.2\text{ V}$ ; $V_{\text{CSN}} = 1.3\text{ V}$ , $I_{\text{IMON}} = -250\text{ }\mu\text{A}$	0.1	0.15	V
$V_{\text{IMON(max)}}$	Maximum IMON voltage	$V_{\text{CSP}} = 1.3\text{ V}$ ; $V_{\text{CSN}} = 1.2\text{ V}$ , $I_{\text{IMON}} = 500\text{ }\mu\text{A}$	3.0	3.2	3.3
SR <sup>(2)</sup>	Sampling rate		5		Msp
<b>OUTPUT STAGE</b>					
$R_{\text{HI}}$	High side device resistance	$T_J = 25^\circ\text{C}$ , $V_{\text{BOOT}} - V_{\text{SW}} = 5.5\text{ V}$	4.5	6.5	$\text{m}\Omega$
$R_{\text{LO}}$	Low side device resistance	$T_J = 25^\circ\text{C}$	1.9	2.7	
<b>BOOTSTRAP DIODE</b>					
$V_F$	Forward voltage	Forward bias current 20 mA	0.4		V
<b>THERMAL SHUTDOWN</b>					
$T_{\text{TSD-R}}^{(2)}$	Rising threshold		155	165	175
$T_{\text{TSD-F}}^{(2)}$	Falling threshold		135	145	155
$T_{\text{TSD-HYS}}^{(2)}$	Hysteresis		20		$^\circ\text{C}$

(2) Ensured by design. Not production tested.

## DEVICE INFORMATION



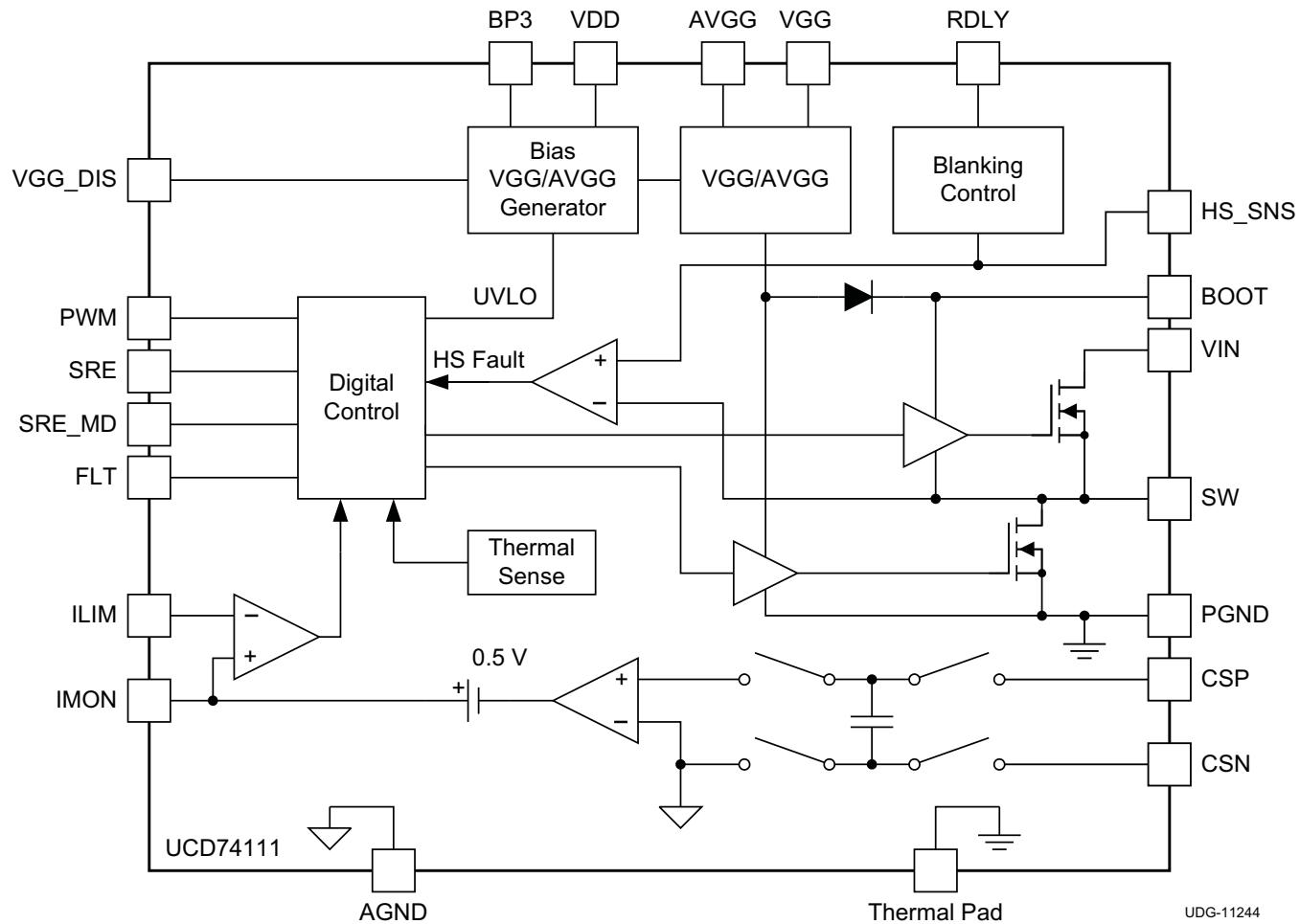
The thermal pad functions as an electrical ground connection.

## PIN FUNCTIONS

PIN		I/O	DESCRIPTION
NAME	NO.		
AGND	1		Analog ground return for all circuits except the low-side gate driver. The analog ground and power ground should be connected together at one point, near the AGND pin.
AVGG	40	I/O	Voltage supply to internal control circuitry. Connect a low ESR bypass ceramic capacitor of 100 nF or greater from this pin to AGND. Also a resistor of 1Ω to 2Ω must be connected between VGG and this pin.
BOOT	5	I/O	Floating bootstrap supply for high side driver. Connect the bootstrap capacitor between this pin and the SW node. The bootstrap capacitor provides the charge to turn on the high-side FET. A low ESR ceramic capacitor of 220 nF or greater from this pin to SW must be connected.
BP3	37	O	Output bypass for the internal 3.3V regulator. Connect a low ESR bypass ceramic capacitor of 1 μF or greater from this pin to AGND.
CSN	35	I	Inverting input of the output current sense amplifier and current limit comparator.
CSP	36	I	Non-inverting input of the output current sense amplifier and current limit comparator.
FLT	29	O	Fault Flag. The FLT signal is a 3.3V digital output which asserts high when an overcurrent, over-temperature, or UVLO fault is detected. After the device detects an overcurrent event, the flag resets to low on the falling edge of the next pulse, provided the overcurrent condition no longer exists during the on-time of the PWM signal. For UVLO and over-temperature faults, the flag is reset when the fault condition no longer exists.
HS_SNS	28	I	A 2-kΩ resistor must be connected from this pin directly to the drain of the high-side FET.
ILIM	32	I	Output current limit threshold set pin. The voltage on this pin sets the fault threshold voltage on the IMON pin. The nominal threshold voltage range is 0.5 V to 3.0 V. When $V_{IMON}$ exceeds $V_{ILIM}$ , the FLT pin is asserted and the high-side gate pulse truncates.
IMON	33	O	Current sense linear amplifier output. The output voltage level on this pin represents the average output current. $V(IMON) = 0.5 V + 50.2(V(CSP) - V(CSN))$ .
N/C	4		Not internally connected.
	6		
	34		

**PIN FUNCTIONS (continued)**

PIN		I/O	DESCRIPTION
NAME	NO.		
PGND	13		Power ground pins. These pins provide a return path for low-side FET and the low-side gate driver.
	14		
	15		
	16		
	17		
	18		
	19		
	20		
PWM	38	I	PWM input. This pin is a digital input that accepts 3.3 V or 5 V logic level signals. A Schmitt trigger input comparator desensitizes this pin from external noise. When SRE mode is high, this pin controls both gate drivers. When SRE mode is low, this pin only controls the high-side driver. This pin can detect when the input drive signal has switched to a high impedance (tri-state) mode. When the high impedance mode is detected, both the high-side gate and low-side gate signals are held low.
RDLY	39	I	Requires a resistor to AGND for setting the current sense blanking time for the high-side current sense comparator and output current limit circuitry.
SRE	31	I	Synchronous rectifier enable or low-side input. This pin is a digital input capable of accepting 3.3V or 5V logic level signals. A Schmitt trigger input comparator desensitizes this pin from external noise. When SRE mode is high, this signal, when low, disables the synchronous rectifier FET. The low-side gate signal is held off. When SRE mode is high, this signal, when high, allows the low-side gate signal to function according to the state of the PWM pin. When SRE mode is low, this pin is a direct input to the low-side gate driver.
SRE_MD	30	I	Synchronous rectifier enable mode select pin. When pulled high to BP3, the high-side and low-side gate drive timing is controlled by the PWM pin. Anti-cross-conduction logic prevents simultaneous application of high-side and low-side gate drive. When pulled low to AGND, independent operation of the high-side and low-side gate is selected. The high-side gate is directly controlled by the PWM signal. The low-side gate is directly controlled by the SRE signal. No anti-cross-conduction circuitry is active in this mode. This pin should not be left floating.
SW	7	I/O	Sense line for the adaptive anti-cross conduction circuitry. Serves as common connection for the flying high side FET driver.
	8		
	9		
	10		
	11		
	12		
VDD	27	I	Input voltage to internal driver circuitry and control circuitry. Connect a low ESR bypass ceramic capacitor of 100 nF or greater from this pin to AGND.
VGG	3	I/O	Gate drive voltage supply. When VGG_DIS is low, VGG is generated by an on-chip linear regulator. Nominal output voltage is 6.4 V. When VGG_DIS is high, an externally supplied gate voltage can be applied to this pin. Connect a 4.7 $\mu$ F low ESR ceramic capacitor from this pin to PGND.
VGG_DIS	2	I	VGG disable pin. When pulled high to BP3, the on-chip VGG linear regulator is disabled. When disabled, an externally supplied gate voltage must be connected to the VGG pin. Connect this pin to AGND to use the on-chip regulator.
VIN	21–26	I	Power input to the high-side FET.
Thermal Pad		Power Pad for better thermal performance. It is also connected to PGND internally.	

**BLOCK DIAGRAM**


## DETAILED DESCRIPTION

### Introduction

The UCD74111 is a power stage for synchronous buck converter with current measurement and fault detection capabilities making it an ideal partner for digital power controllers. This device incorporates two high-current gate drive stages, two high-performance NexFET power MOSFETs, and sophisticated current measurement circuitry that allows for the monitoring and reporting of output load current. Two separate fault detection blocks protect the power stage from excessive load current or short circuits. On-chip thermal shutdown protects the device in case of severe over-temperature conditions. The device detects faults immediately, truncates the power conversion cycle in progress, without controller intervention, and asserts a digital fault flag (FLT). An on-chip linear regulator supplies the gate drive voltage. If desired, this regulator can be disabled and an external gate drive voltage can be supplied. Mode selection pins allow the device to be used in synchronous mode or independent mode. In synchronous mode, the high-side and low-side gate timing is controlled by a single PWM input. Anti-cross-conduction dead-time intervals are applied automatically to the gate drives. The PWM and SRE pins directly controls the high-side and low-side gate drive signals. In independent mode, the automatic dead-time logic is disabled in this mode. When operating in synchronous mode, the use of the low-side FET can be disabled under the control of the SRE pin. This feature facilitates start-up into a pre-bias voltage and is also used in some applications to reduce power consumption at light loads.

### PWM Input (PWM)

The PWM input pin accepts the digital signal from the controller that represents the desired high-side FET on-time duration. This input accepts 3.3-V logic levels, but also tolerates 5-V input levels. The SRE mode pin sets the behavior of the PWM pin. When the SRE mode pin asserts high, the device goes into synchronous mode. In this mode, PWM input signal controls both the timing duration of the high-side gate drive and the low-side gate drive. When PWM is high, the high-side gate drive (HS Gate) is on and the low-side gate drive is off. When PWM is low, the high-side gate drive is off and the low-side gate drive is on. Automatic anti-cross-conduction logic monitors the gate to source voltage of the FETs to verify that the proper FET is turned OFF before the other FET is turned ON. When the SRE mode pin is asserted low, the device goes into independent mode. In this mode the PWM input controls the high-side gate drive only. When PWM is high, the high-side gate drive is on. While in independent mode, the SRE pin directly controls the low-side FET. Independent mode does not activate any anti-cross-conduction logic. The user must ensure that the PWM and SRE signals do not overlap.

The PWM input supports a tri-state detection feature. It detects when the PWM input signal has entered a tri-state mode. When the device detects a tri-state mode, both the high-side and low-side gate drive signals remain OFF. To support this mode, the PMW input pin has an internal pull-up resistor of approximately 50 k $\Omega$  connected to the 3.3 V input. It also has a 50 k $\Omega$  pull-down resistor to ground. During normal operation, the PWM input signal swings below 0.8 V and above 2.5 V. If the source driving the PWM pin enters a tri-state or high impedance state, the internal pull-up/pull-down resistors tends to pull the voltage on the PWM pin to 1.65 V. If the voltage on the PWM pin remains within the 0.8 V to 2.5 V tri-state detection range for longer than the tri-state detection hold-off time ( $t_{HLD\_R}$ ), then the device enters tri-state mode and turns both gate drives OFF. This behavior occurs regardless of the state of the SRE mode and SRE pins. When exiting tri-state mode, PWM should first be asserted low. This ensures that the bootstrap capacitor is recharged before attempting to turn on the high-side FET.

The logic threshold of this pin typically exhibits 900 mV of hysteresis to provide noise immunity and ensure glitch-free operation of the gate drivers.

## Synchronous Rectifier Enable Input (SRE)

The SRE (synchronous rectifier enable) pin is a digital input with an internal  $10\text{-k}\Omega$  pull-up resistor connected to the 3.3-V input. It is designed to accept 3.3-V logic levels, but is also tolerant of 5-V levels. The SRE mode pin sets the behavior of the SRE pin. When the SRE mode pin is asserted high, the device enters synchronous mode. In synchronous mode, the input, when asserted high, enables the operation of the low-side synchronous rectifier FET. The PWM input controls the state of the low-side gate drive signal. When SRE is asserted low while in synchronous mode, the low-side FET gate drive holds low, keeping the FET off. While remaining OFF, the low-side FET restricts the current flow to the intrinsic body diode. When the SRE mode pin is asserted low, the device enters independent mode. In independent mode, the state of the low-side gate drive signal follows the state of the SRE signal. It is completely independent of the state of the PWM signal. No anti-cross-conduction logic is active in independent mode. The user must ensure that the PWM and SRE signals do not overlap.

The logic threshold of this pin typically exhibits 450 mV of hysteresis to provide noise immunity and ensure glitch-free operation of the low-side gate driver.

### SRE Mode (SRE\_MD)

The SRE mode pin is a digital input that accept 3.3-V logic levels, and levels up to 5-V. The SRE pin sets the operational mode on the device. When asserted high, the device enters synchronous mode. In synchronous mode, the PWM input controls the behavior of both the high-side and low-side gate drive signals. When asserted low, this pin configures the device for independent mode. In independent mode the PWM pin controls the high-side FET and the SRE pin controls the low-side FET. The SRE mode pin should be s permanently tied high or low depending on the power architecture being implemented. It not intended to be switched dynamically while the device is in operation. This pin can be tied to the BP3 pin to always select synchronous mode.

## Input Voltage for Internal Circuits (VDD)

The VDD pin supplies power to the internal circuits of the device. An internal linear regulator that provides the  $V_{VGG}$  gate drive voltage conditions the input power. A second regulator that operates off of the  $V_{VGG}$  rail produces an internal 3.3-V supply that powers the internal analog and digital functional blocks. The BP3 pin provides access for a high frequency bypass capacitor on this internal rail. The VGG regulator produces a nominal output of 6.4 V. The undervoltage lockout (UVLO) circuitry monitors the output of the VGG regulator. The device does not attempt to produce gate drive pulses until the VGG voltage is above the UVLO threshold. This delay ensures that there is sufficient voltage available to drive the power FETs into saturation when switching activity begins.

## Voltage Supply for Gate Drive and Internal Control Circuitry (VGG and AVGG)

The VGG pin is the gate drive voltage for the high current gate drive stages. The AVGG pin is the voltage supply to internal control circuitry. The on-chip regulator can supply the voltage internally on the VGG pin, or the user can supply the voltage externally. When using the internal regulator, the VGG\_DIS pin should be tied low. When an external source of VGG is to be used, the VGG\_DIS pin must be tied high. Current is drawn from the VGG supply in fast, high-current pulses. Connect a  $4.7\text{-}\mu\text{F}$  ceramic capacitor between the VGG pin and PGND pin as close as possible to the package.

Connect a resistor with a value between  $1\ \Omega$  and  $2\ \Omega$  between the AVGG pin and the VGG pin. A low ESR bypass ceramic capacitor of 100 nF or greater needs to be connected from AVGG pin to AGND as well.

Whether the voltage is internally or externally supplied, UVLO circuitry monitors the voltage on the VGG pin. The voltage must be higher than the UVLO threshold before power conversion can occur. Note that the FLT pin is asserted high when  $V_{VGG}$  is below the UVLO threshold.

### VGG Disable (VGG\_DIS)

The VGG\_DIS pin, when asserted high, disables the on-chip VGG linear regulator. When tied low, the VGG linear regulator is derives the VGG supply from  $V_{IN}$ . Permanently tie the VGG\_DIS pin high or low depending on the power architecture being implemented. The VGG\_DIS pin should not be switched dynamically while the device is in operation.

## Switching Node (SW)

The SW pin connects to the switching node of the power conversion stage. It acts as the return path for the high-side gate driver. When configured as a synchronous buck stage, the voltage swing on SW normally traverses from below ground to well above  $V_{IN}$ . Parasitic inductance in the high-side FET and the output capacitance ( $C_{oss}$ ) of both power FETs form a resonant circuit that can produce high frequency ( $> 100$  MHz) ringing on this node. The voltage peak of this ringing, if not controlled, can be significantly higher than  $V_{IN}$ . Ensure that no peak ringing amplitude exceeds the absolute maximum rating limit for the pin.

In many cases, connecting a series resistor and capacitor snubber network connected from the switching node to PGND can dampen the ringing and decreasing the peak amplitude. Make allowances for snubber network components during the layout of the printed circuit board. If testing reveals that the ringing amplitude at the SW pin exceeds the limit, then populate the snubber components.

Placing a BOOT resistor with a value between  $5\ \Omega$  and  $10\ \Omega$  in series with the BOOT capacitor slows down the turn-on of the high-side FET and can help to reduce the peak ringing at the switching node as well.

## Bootstrap (BST)

The BST pin provides the drive voltage for the high-side FET. A bootstrap capacitor connects this pin to the SW node. Internally, a diode connects the BST pin to the VGG supply. In normal operation, when the high-side FET is off and the low-side FET is on, the SW node is pulled to ground and, thus, holds one side of the bootstrap capacitor at ground potential. The other side of the bootstrap capacitor is clamped by the internal diode to VGG. The voltage across the bootstrap capacitor at this point is the magnitude of the gate drive voltage available to switch-on the high-side FET. The bootstrap capacitor should be a low ESR ceramic type, with a recommended minimum value of  $0.22\ \mu F$ . The recommended minimum voltage rating is 16 V or higher.

## Current Sense (CSP, CSN)

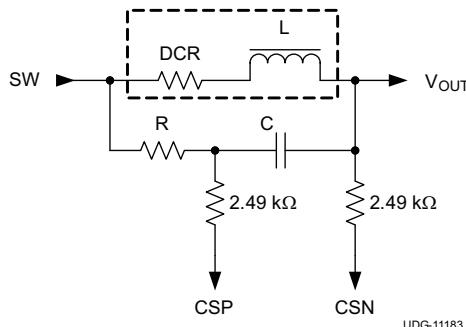
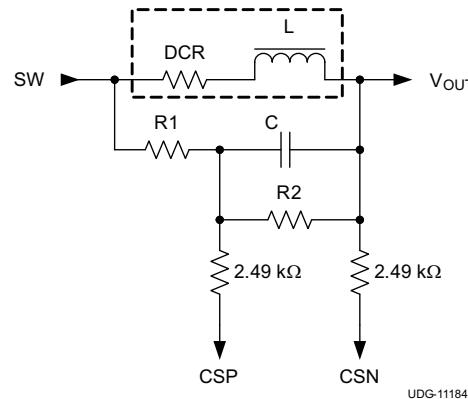
The CSP and CSN pins are the input to the differential current sense amplifier. The current sense positive (CSP) pin connects to the non-inverting input, the current sense negative (CSN) connects to the inverting input. This amplifier provides the means to monitor and measure the output current of the power stage. The circuitry can be used with a discrete, low value, series current sense resistor, or can make use of the popular inductor DCR sense method.

Figure 1 illustrates the DCR method of current sensing. A series resistor and capacitor network is added across the buck stage power inductor. When the value of  $L/DCR$  is equal to  $RC$ , then the voltage developed across the capacitor,  $C$ , is a replica of the voltage waveform the *ideal current* would induce in the dc resistance (DCR) of the inductor. This method does *not* detect changes in current due to changes in inductance value caused by saturation effects. The value used for  $C$  should be between  $0.1\ \mu F$  and  $2.2\ \mu F$ . This maintains a low impedance of the sense network, which reduces its susceptibility to noise pickup from the switching node. The trace lengths of the CSP and CSN signals should be kept short and parallel. To aid in rejection of high frequency common-mode noise, a series  $2.49\text{-}k\Omega$  resistor should be added to both the CSP and CSN signal paths, with the resistors being placed close to the pins at the package. This small amount of additional resistance slightly lowers the current sense gain.

Select power inductors with the lowest possible DCR in order to minimize losses. Typical DCR values range between  $0.5\ m\Omega$  and  $5\ m\Omega$ . With a load current of  $15\ A$ , the voltage presented across the CSP and CSN pins is between  $7.5\ mV$  and  $75\ mV$ . Note that this small differential signal is superimposed on a large common mode signal that is the dc output voltage. This makes the current sense signal challenging to process.

The UCD74111 uses switched capacitor technology to perform the differential to single-ended conversion of the sensed current signal. This technique offers excellent common mode rejection. The differential CSP-CSN signal is amplified by a factor of 47 and then a fixed  $500\text{-}mV$  pedestal voltage is added to the result. This signal is presented to the IMON pin.

When using inductors with DCR values of  $2.0\ m\Omega$  or higher, it may be necessary to attenuate the input signal to prevent saturation of the current sense amplifier. Add of resistor R2 as shown in Figure 2 to provide attenuation.


**Figure 1. DCR Current Sense**

**Figure 2. Attenuating the DCR Sense Signal**

The amount of attenuation is equal to  $R2/(R1 + R2)$ . The equivalent resistance value to use in the  $L/DCR = RC$  formula is the parallel combination of  $R1$  and  $R2$ . Thus, when using the circuit shown in [Figure 2](#),

$$\frac{L}{DCR} = \frac{C \times R1 \times R2}{(R1 + R2)} \quad (1)$$

### Current Monitor (IMON)

The IMON pin signal is a voltage proportional to the output current delivered by the power stage. [Figure 1](#) describes the voltage magnitude when using the circuit shown in [Figure 1](#).. [Equation 2](#) reflects the gain reduction caused by the series 2.49-kΩ resistors.

$$V(I_{OUT}) = 0.5 + 47 \times DCR \times I_{LOAD} \quad (2)$$

If the calculated value of  $V_{IMON}$  at maximum load exceeds 2.5 V, then the circuit of [Figure 2](#) should be used. When using the circuit shown in [Figure 2](#), the modified [Equation 3](#) describes the voltage on IMON.

$$V(I_{OUT}) = 0.5 + 47 \times DCR \times I_{LOAD} \times \left( \frac{R2}{R1 + R2} \right) \quad (3)$$

In either case, the output voltage is 500 mV at no load. Current that is sourced to the load causes the IMON voltage to rise above 500 mV. Current that is forced into the power stage (sinking current) is considered *negative* current and causes the IMON voltage to fall below 500 mV. The usable dynamic range of the IMON signal is approximately 100 mV to 3.1 V. Note that this signal swing could exceed not just the maximum range of an analog to digital converter (ADC) that may be used to read or monitor the IMON signal, but also the maximum programmable limit for the fault OC threshold. For example, the UCD92xx family of digital controllers has maximum limit of 2.5 V for the ADC converter and 2.0 V for the fault overcurrent threshold, even though the input pin can tolerate voltages up to 3.3 V.

The device internally feeds the IMON voltage ( $V_{IMON}$ ) to the non-inverting input of the output overcurrent fault comparator. Set the overcurrent threshold to approximately 150% of the rated power stage output current plus one half of the peak-to-peak inductor ripple current.. This setting requires that the IMON signal remain within its linear dynamic range at this threshold load current level. This requirement may force the use of the attenuation circuit of [Figure 2](#). Note that the IMON voltage (that goes to the output overcurrent fault comparator) is held during the blanking interval set by the resistor on the RDLY pin. This means that the IMON pin does not reflect output current changes during the blanking interval, and that a fault is not flagged until the blanking interval terminates.

### Current Limit (ILIM)

The ILIM pin feeds the inverting input of the output overcurrent fault comparator. The voltage applied to this pin sets the overcurrent fault threshold. When the voltage on the  $I_{MON}$  pin exceeds the voltage on this pin, a fault is flagged. The voltage on this pin can be set by a voltage divider, a DAC, or by a filtered PWM output. The usable voltage range of the ILIM pin is approximately 0.6V to 3.1V. This represents the linear range of the IMON signal for sourced output current. When using a voltage divider to set the threshold, a small (0.01μF) capacitor to BP3 can be added to improve noise immunity.

## Blanking Time (RDLY)

The RDLY pin sets the blanking time of the high-side fault detection comparator. A resistor to AGND sets the blanking time according to the following formula, where  $t_{BLANK}$  is in nanoseconds and RDLY is in k $\Omega$ . Do not use a value greater than 25 k $\Omega$  for the RDLY resistor.

$$R_{RDLY} = \frac{(t_{BLANK} - 54.4)}{8.76} \quad (4)$$

To calculate the nominal blanking time for a given value of resistance, use [Equation 5](#).

$$t_{BLANK} = 8.76 \times R_{RDLY} + 54.4 \quad (5)$$

The blanking interval begins on the rising edge of SW. During the blanking time the high-side fault comparator is held off. A high-side fault is flagged when the voltage drop across the high-side FET exceeds the threshold set by the HS\_SNS pin. Blanking is required because the high amplitude ringing that occurs on the rising edge of SW would otherwise cause false triggering of the fault comparator. The required amount of blanking time is a function of the high-side FET, the PCB layout, and whether or not a snubber network is being used. A value of 100 ns is a typical starting point. An  $R_{RDLY}$  of 8.06 k $\Omega$  provides 125 ns of blanking. Maintains a blanking interval as short as possible, consistent with reliable fault detection. The blanking interval sets the minimum duty cycle pulse width where high-side fault detection is possible. When the duty-cycle of the PWM pulses are narrower than the blanking time, the high-side fault detection comparator is held off for the entire on-time and is, therefore, blind to any high-side faults.

Internally, a 90- $\mu$ A current source supplies the RDLY. When using the default value of 8.06 k $\Omega$ , the voltage measured on the RDLY pin is approximately 725 mV.

## Fault Flag (FLT)

The fault flag (FLT) is a digital output pin that asserts when a significant fault is detected. It alerts the host controller to an event that has interrupted power conversion. The device holds the FLT pin low in normal operation.

When a fault is detected, the FLT pin asserts high (3.3 V). There are four events that can trigger the FLT signal:

- output overcurrent
- high-side overcurrent
- undervoltage lockout (UVLO)
- thermal shutdown

The [Fault Behavior](#) section describes operation of the device during fault conditions. When asserted in response to an overcurrent fault, the FLT signal is reset low upon the falling edge of a subsequent PWM pulse, provided no faults are detected during the on-time of the pulse. If the fault is still present, the flag remains asserted. When asserted in response to an UVLO or thermal shutdown event, the FLT pin automatically de-asserts itself when the UVLO or thermal event has passed. If the on-time of the PWM pulse is less than 100 ns, then more than one pulse may be required to reset the flag.

## 3.3-V BP Regulator (BP3)

The BP3 pin provides a connection point for a bypass capacitor that quiets the internal 3.3-V voltage rail. Connect a 1- $\mu$ F (or greater) ceramic capacitor from this pin to analog ground. Do not draw current from this pin. The BP3 pin is not intended to be a significant source of 3.3-V input voltage. However, the user can design an application that includes 3.3-V source for an ILIM voltage divider and a tie point for the SRE mode pin. Limit the current drawn 100  $\mu$ A or less.

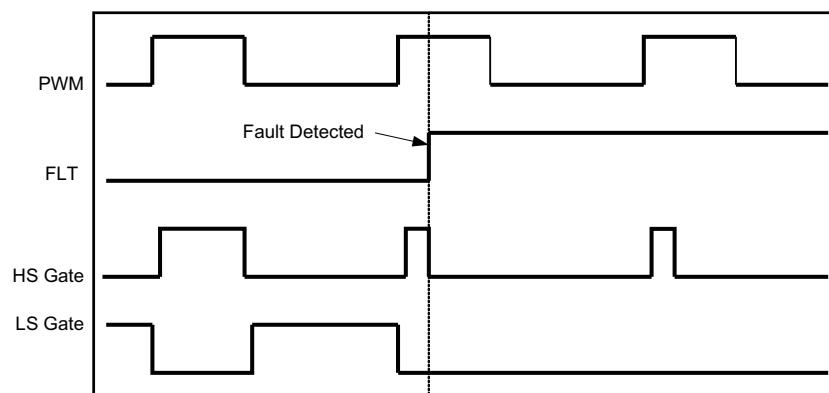
## Fault Behavior

When faults are detected, the device reacts immediately to minimize power dissipation in the FETs and protect the system. The type of fault influences the behavior of the gate drive signals.

Immediately after a thermal shutdown fault occurs, the device forces both high-side gate and low-side gate low. They remain low (regardless of the state of the PWM and the SRE pin) for the duration of the thermal shutdown.

A UVLO fault occurs when the voltage on the V<sub>GG</sub> pin is less than the UVLO threshold. During this time both the high-side gate and low-side gate are driven low, regardless of the state of PWM and SRE. The fault automatically clears when V<sub>GG</sub> rises above the UVLO threshold.

When the device detects either a high-side fault or an output overcurrent fault, the FLT pin asserts high, and the device immediately pulls both gate signals to low. During a high-side fault, the device issues a high-side gate pulse with each incoming PWM pulse. If the fault is still present, the high-side gate signal again truncates. This behavior repeats on a cycle-by-cycle basis until the fault clears or the PWM input remains low. [Figure 3](#) illustrates this behavior.

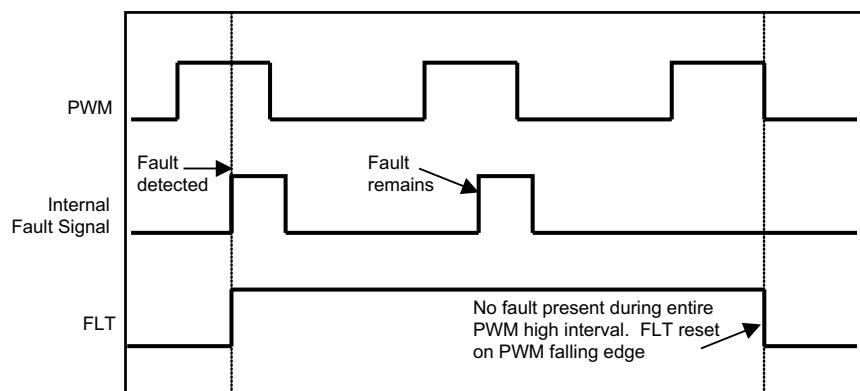


**Figure 3. High-side Overcurrent Fault Response**

When the device detects a high-side fault and output overcurrent fault concurrently, then it immediately turns OFF and holds OFF both FET drives. If the output overcurrent fault remains present at the next PWM rising edge, then the device issues no high-side gate pulse continue to be hold both gates OFF. Unlike the high-side fault detection circuitry, the output overcurrent fault circuitry does not reset on a cycle-by-cycle basis. The output current must fall below the overcurrent threshold before switching resumes.

### FLT Reset

With the exception of a UVLO fault or a thermal shutdown fault, subsequent PWM pulses clear the FLT flag, after it is asserted. The device clears the FLT flag at the falling edge of the next PWM pulse, provided a fault condition is not asserted during the entire on-time of the PWM pulse. If the device detects a fault during the on-time interval, the FLT pin remains asserted. [Figure 4](#) illustrates this behavior.



**Figure 4. FLT Reset Sequence**

Whenever the voltage on the VGG pin is below the UVLO falling threshold, as at the time of initial power-up, for example, the FLT pin asserts. When the voltage on the VGG pin rises above the UVLO rising threshold, the device clears the FLT automatically. This feature permits the FLT pin to be used as a *power not good* signal at initial power-up to signify that there is insufficient gate drive voltage available to permit proper power conversion. When FLT goes low, it is an indication of *gate drive power good* and power conversion can commence. After initial power-up, the assertion of the FLT flag should be interpreted that power conversion has stopped or has been limited by a fault condition.

### **Thermal Shutdown**

If the junction temperature exceeds approximately 165°C, the device enters thermal shutdown. This asserts the FLT pin and both gate drivers are turned OFF. When the junction temperature cools by approximately 20°C, the device exits thermal shutdown. The FLT flag resets upon exiting thermal shutdown.

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UCD74111RVFR	Active	Production	LQFN-CLIP (RVF)   40	3000   LARGE T&R	ROHS Exempt	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	UCD74111
UCD74111RVFT	Active	Production	LQFN-CLIP (RVF)   40	250   SMALL T&R	ROHS Exempt	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	UCD74111
UCD74111RVFTG4	Active	Production	LQFN-CLIP (RVF)   40	250   SMALL T&R	ROHS Exempt	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	UCD74111

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

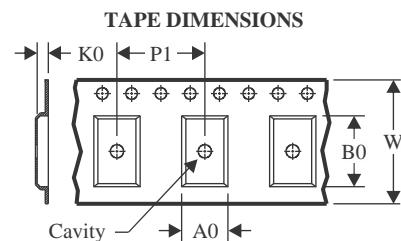
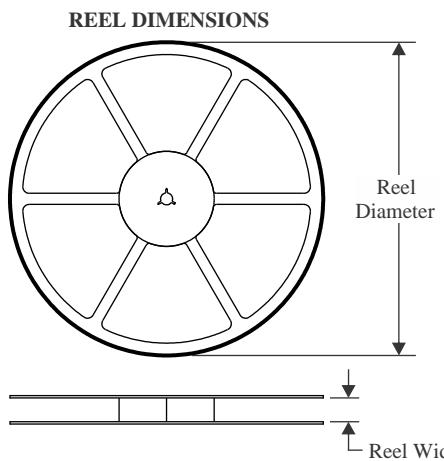
<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

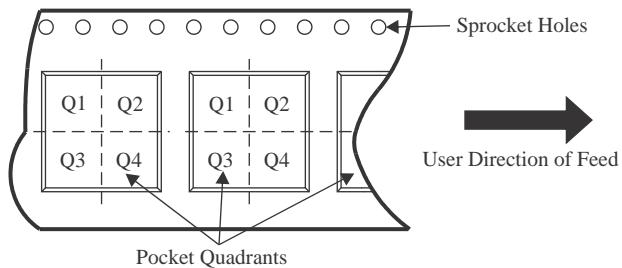
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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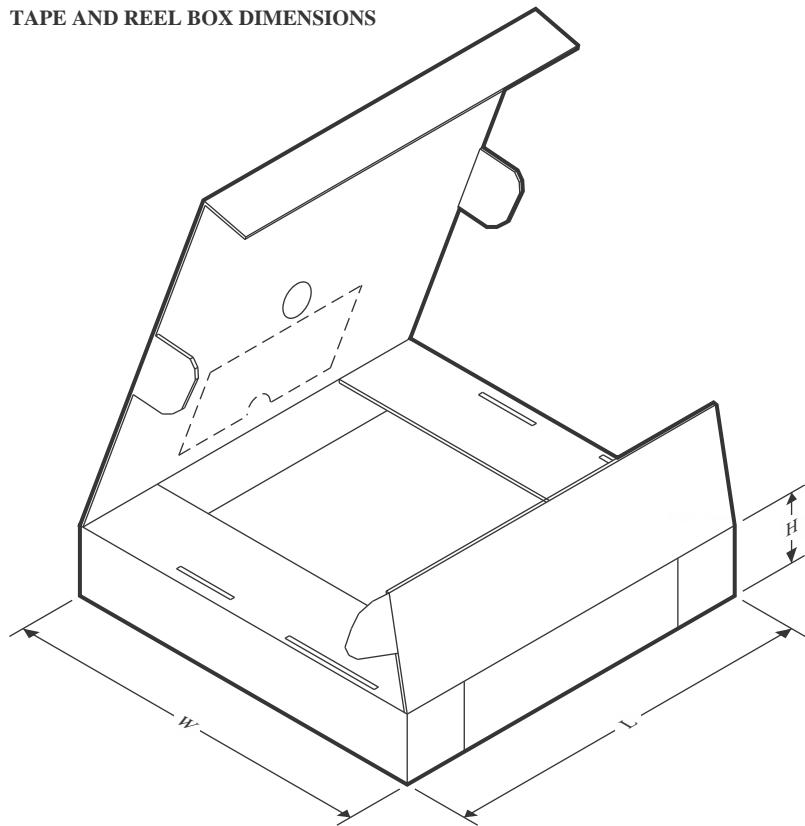
**TAPE AND REEL INFORMATION**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCD74111RVFR	LQFN-CLIP	RVF	40	3000	330.0	16.4	5.35	7.35	1.7	8.0	16.0	Q1
UCD74111RVFT	LQFN-CLIP	RVF	40	250	180.0	16.4	5.35	7.35	1.7	8.0	16.0	Q1
UCD74111RVFTG4	LQFN-CLIP	RVF	40	250	180.0	16.4	5.35	7.35	1.7	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

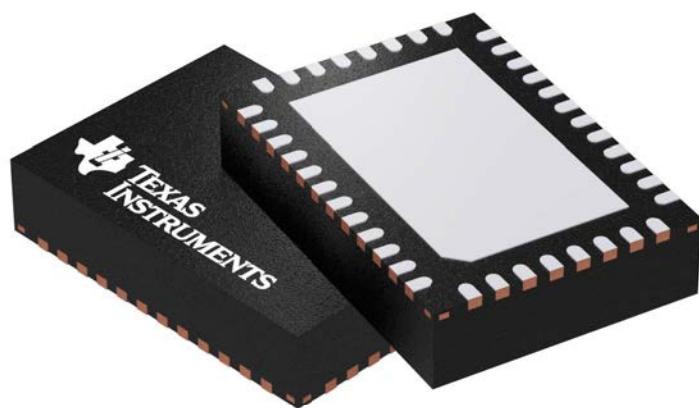
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCD74111RVFR	LQFN-CLIP	RVF	40	3000	367.0	367.0	38.0
UCD74111RVFT	LQFN-CLIP	RVF	40	250	210.0	185.0	35.0
UCD74111RVFTG4	LQFN-CLIP	RVF	40	250	210.0	185.0	35.0

## GENERIC PACKAGE VIEW

**RVF 40**

**LQFN-CLIP - 1.52 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4211383/D

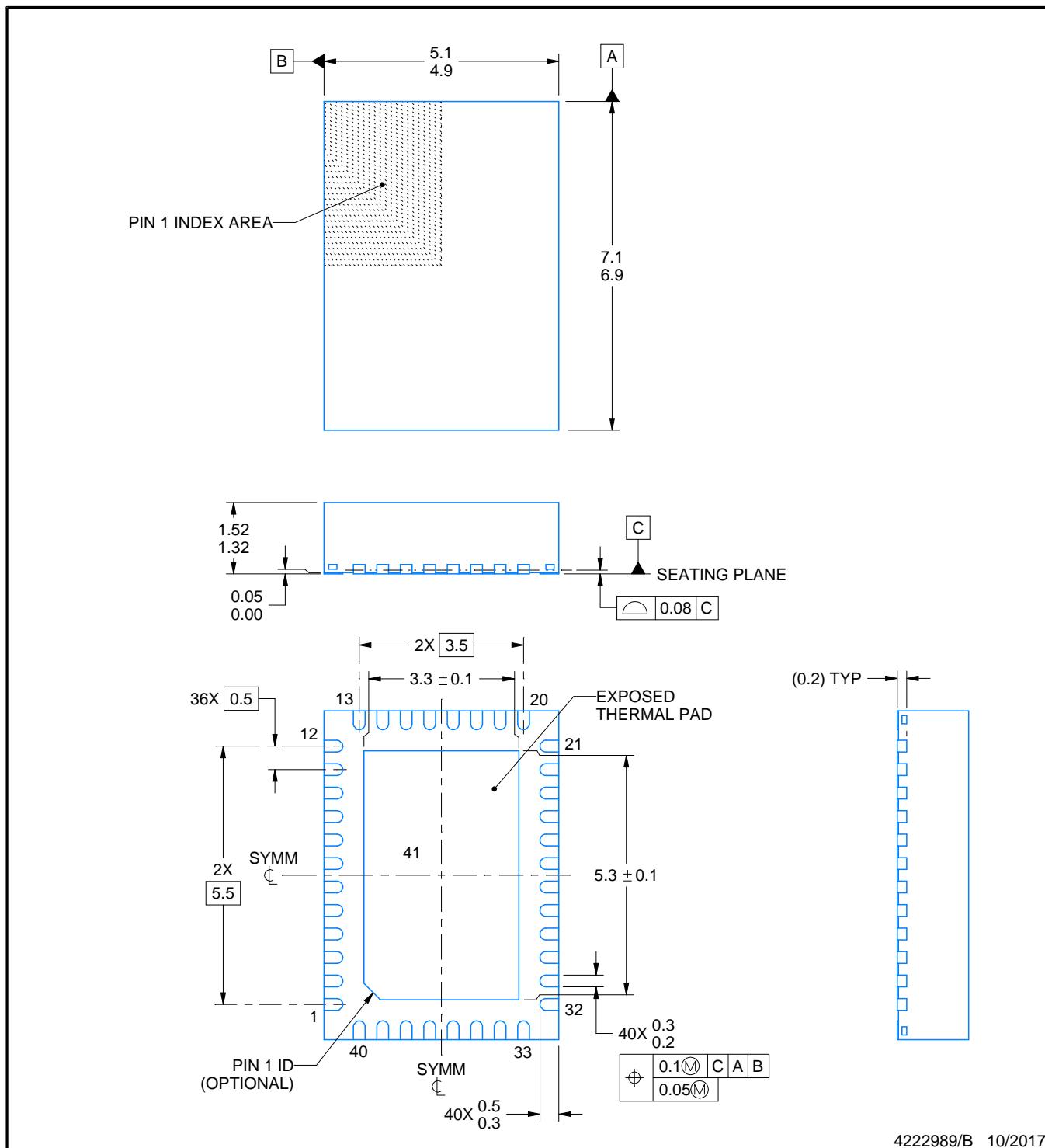
## PACKAGE OUTLINE

**RVF0040A**



## LQFN-CLIP - 1.52 mm max height

**PLASTIC QUAD FLATPACK - NO LEAD**



4222989/B 10/2017

## NOTES:

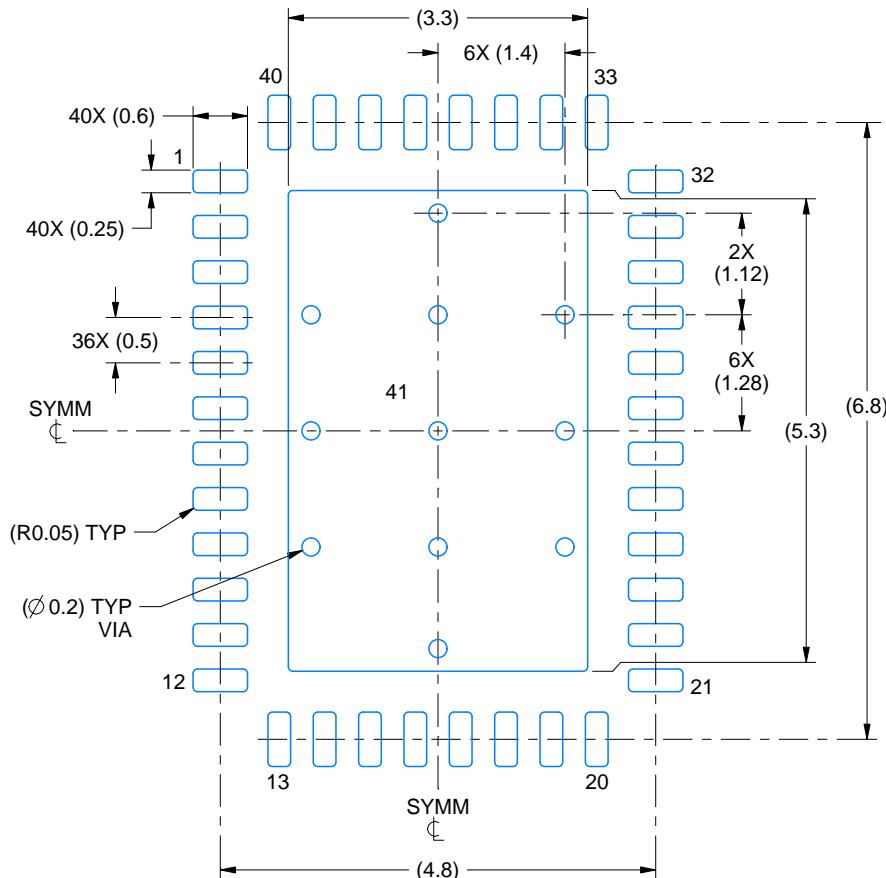
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Reference JEDEC registration MO-220.

## EXAMPLE BOARD LAYOUT

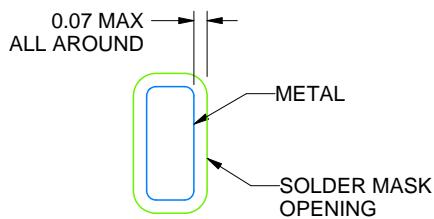
**RVF0040A**

## LQFN-CLIP - 1.52 mm max height

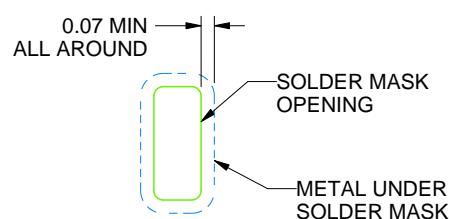
#### PLASTIC QUAD FLATPACK - NO LEAD



## LAND PATTERN EXAMPLE



NON SOLDER MASK  
DEFINED  
(PREFERRED)



## SOLDER MASK DEFINED

## SOLDER MASK DETAILS

4222989/B 10/2017

#### NOTES: (continued)

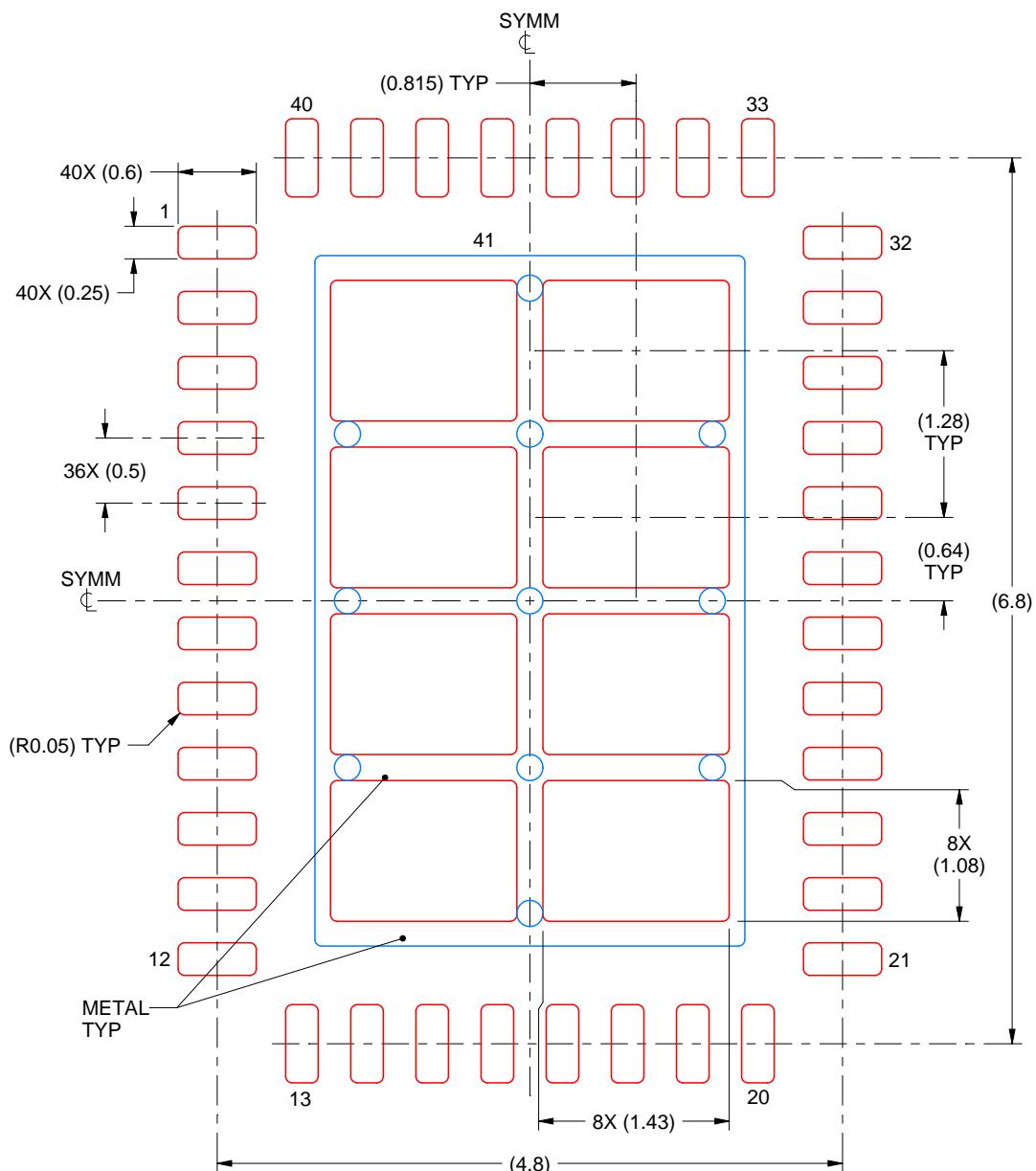
5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).

# EXAMPLE STENCIL DESIGN

RVF0040A

LQFN-CLIP - 1.52 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD  
71% PRINTED SOLDER COVERAGE BY AREA  
SCALE:18X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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