ULN2803C Darlington Transistor Array

1 Features

- 500mA-rated collector current (single output)
- High-voltage outputs: 50V
- Output clamp diodes
- Inputs compatible with various types of logic

2 Applications

- Factory automation and control
- Building automation
- Appliances
- IP network camera
- HVAC valve and actuator control
- Relay, solenoid, and lamp driving
- Stepper motor driving

3 Description

The ULN2803C device is a 50V, 500mA Darlington transistor array. The device consists of eight NPN Darlington pairs that feature high-voltage outputs with common-cathode clamp diodes for switching inductive loads. The collector-current rating of each Darlington pair is 500mA. The Darlington pairscan be connected in parallel for higher current capability.

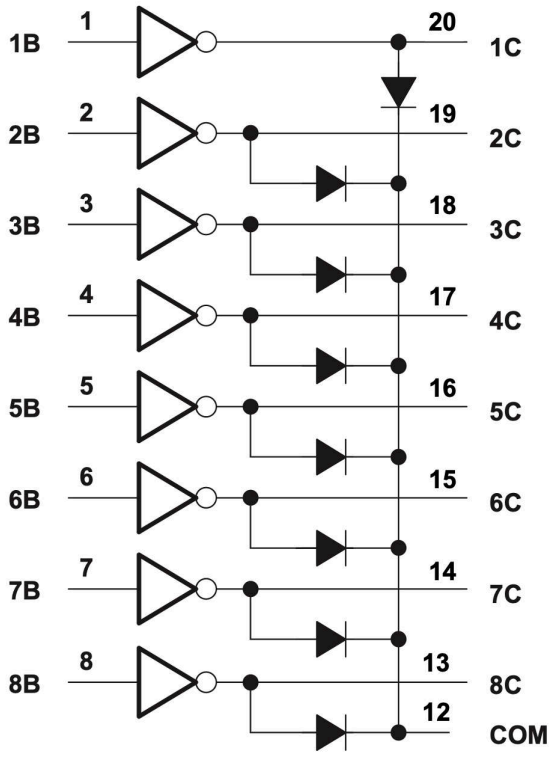
Applications include relay drivers, hammer drivers, lamp drivers, display drivers (LED and gas discharge), line drivers, and logic buffers. The ULN2803C device has a 2.7kΩ series base resistor for each Darlington pair for operation directly with TTL or 5V CMOS devices.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
ULN2803CDW	DW (SOIC, 20)	12.80mm × 10.3mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.

Logic Diagram



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4 Pin Configuration and Functions

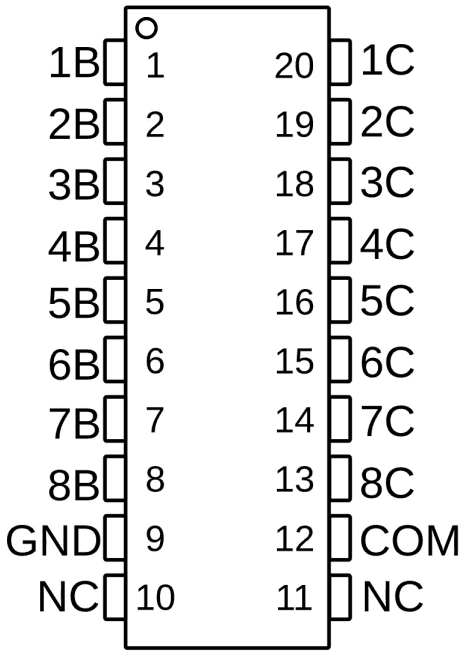


Figure 4-1. DW Package, 20-Pin SOIC (Top View)

Table 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
1B	1	I	Channel 1 through 8 Darlington base input.
2B	2		
3B	3		
4B	4		
5B	5		
6B	6		
7B	7		
8B	8		
1C	20	O	Channel 1 through 8 Darlington collector output.
2C	19		
3C	18		
4C	17		
5C	16		
6C	15		
7C	14		
8C	13		
GND	9	—	Common emitter shared by all channels (typically tied to ground).
COM	12	I/O	Common cathode node for flyback diodes (required for inductive loads).
NC	10, 11	—	No connect pin.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{CC}	Collector-emitter voltge		50	V
V_I	Input voltage		30	V
I_C	Peak collector current		500	mA
I_{OK}	Output clamp current		500	mA
I_{MAX}	Total substrate-terminal current		-2.5	A
T_J	Junction temperature	-65	150	°C
T_{STG}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/ JEDEC JS-001, allpins(1)	±2000	V
		Charged device model (CDM), per JEDEC specificationJESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less is possible with the necessary precautions. Pins listed may actually have higher performance.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
V_{CE}	Collector-emitter voltge	0		50	V
T_J	Junction temperature	–40		85	°C

5.4 Thermal Information

THERMAL METRIC(1)		ULN2803C DW (SOIC) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	75.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	43.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	48.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	16.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	47.5	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.5 Electrical Characteristics

Typical Values are at 25°C

PARAMETER	TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
Datasheet Specs						

5.5 Electrical Characteristics (continued)

Typical Values are at 25°C

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
$V_{I(ON)}$	ON-state input voltage	V_{CE} = 2V, I_C = 200mA	25°C			2.4	V
		V_{CE} = 2V, I_C = 250mA	25°C			2.7	V
		V_{CE} = 2V, I_C = 300mA	25°C			3	V
$V_{CE(SAT)}$	Colllector-emmiter saturation voltage	I_I = 250uA, I_C = 100mA	25°C		0.9	1.1	V
		I_I = 350uA, I_C = 200mA	25°C		1	1.3	V
		I_I = 500uA, I_C = 350mA	25°C		1.2	1.6	V
I_{CEX}	Collector cutoff current	V_{CE} = 50V, I_I = 0A	25°C			50	uA
V_F	Clamp forward voltage	I_F = 350mA	25°C		1.3	2	V
$I_{I(OFF)}$	OFF-state input current	V_{CE} = 50V, IC = 500uA	70°C	50	65		uA
I_I	Input current	V_I = 3.85V	25°C		0.93	1.35	mA
I_R	Clamp reverse current	V_R = 50V	25°C			50	uA
C_I	Input capacitance	V_I = 0V, f = 1MHz	25°C		15	25	pF

5.6 Switching Characteristics

Unless otherwise noted, the typical characteristics in the following table applies at 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	V_S = 50 V, C_L = 15 pF, R_L = 163 Ω		130		ns
t_{PLH}	Propagation delay time, low- to high-level output	V_S = 50 V, C_L = 15 pF, R_L = 163 Ω		20		ns
V_{OH}	High-level output voltage after switching	V_S = 50 V, I_O = 300 mA	V_S - 20			mV

5.7 Typical Characteristics

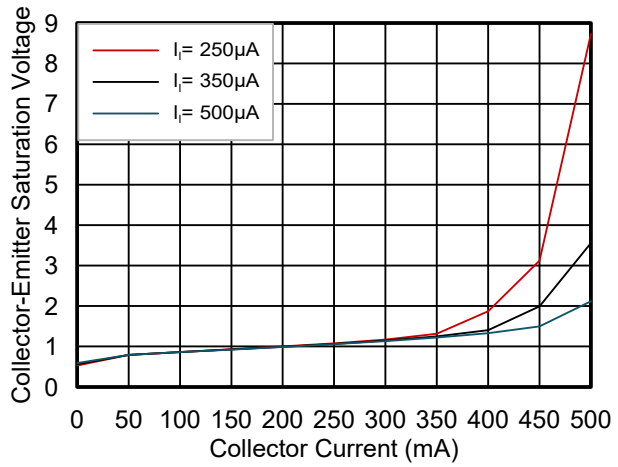


Figure 5-1. Collector-Emitter Saturation Voltage vs Collector Current (One Darlington)

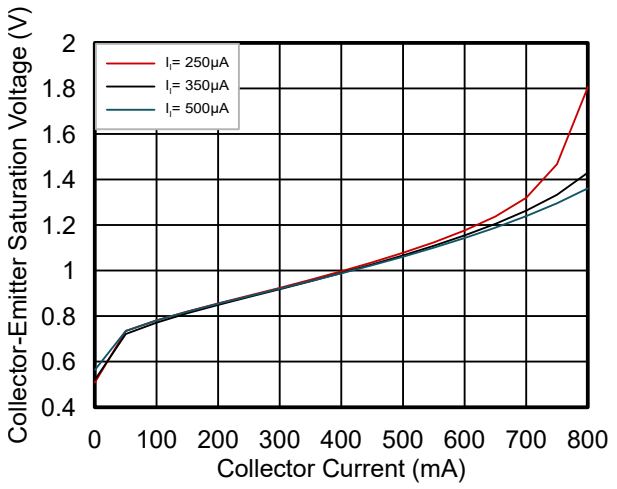


Figure 5-2. Collector-Emitter Saturation Voltage vs Total Collector Current (Two Darlingtons in Parallel)

6 Parameter Measurement Information

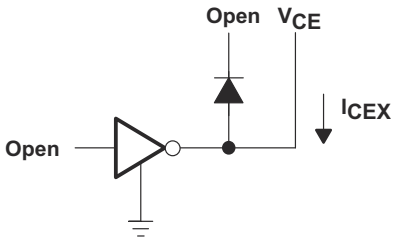


Figure 6-1. I_{CEX} Test Circuit

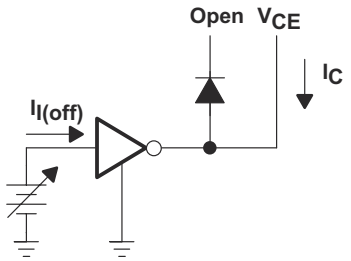


Figure 6-2. $I_{I(off)}$ Test Circuit

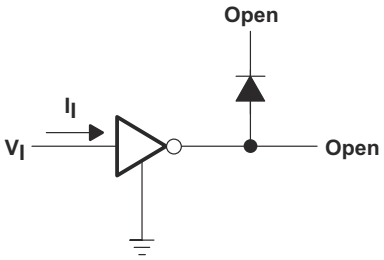


Figure 6-3. $I_{I(on)}$ Test Circuit

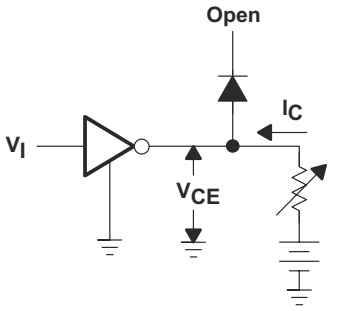


Figure 6-4. $V_{I(on)}$ Test Circuit

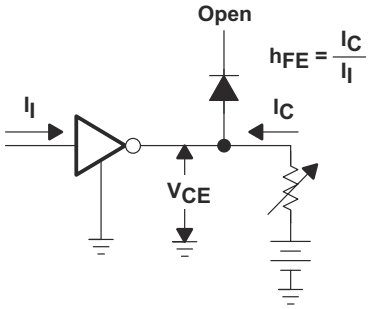


Figure 6-5. h_{FE}, $V_{CE(sat)}$ Test Circuit

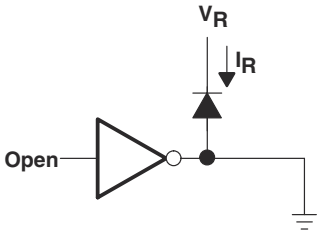


Figure 6-6. I_R Test Circuit

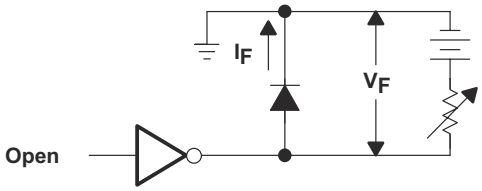
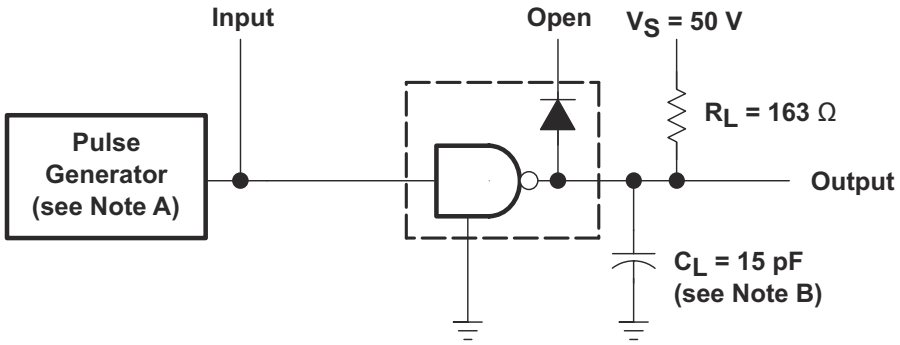
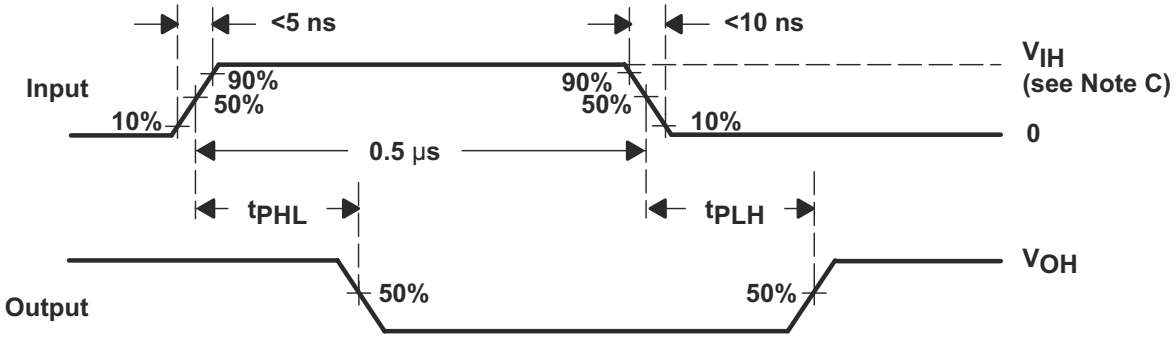


Figure 6-7. V_F Test Circuit



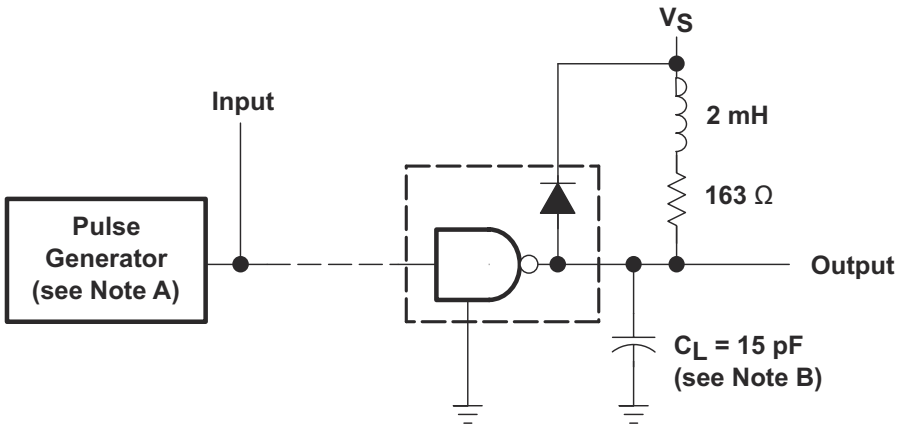
Test Circuit



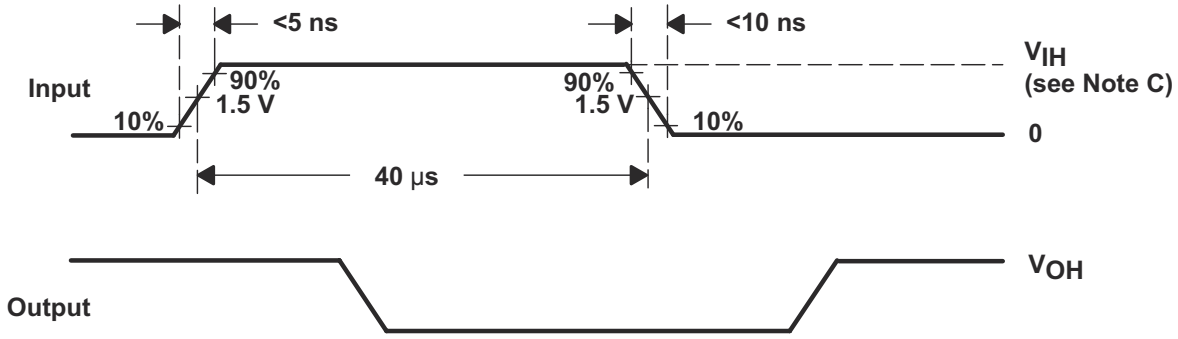
Voltage Waveforms

A. The pulse generator has the following characteristics: PRR = 12.5 kHz, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.
C. V_{IH} = 3 V.

Figure 6-8. Propagation Delay Times



Test Circuit



Voltage Waveforms

A. The pulse generator has the following characteristics: PRR = 12.5 kHz, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.
C. V_{IH} = 3 V.

Figure 6-9. Latch-Up Test

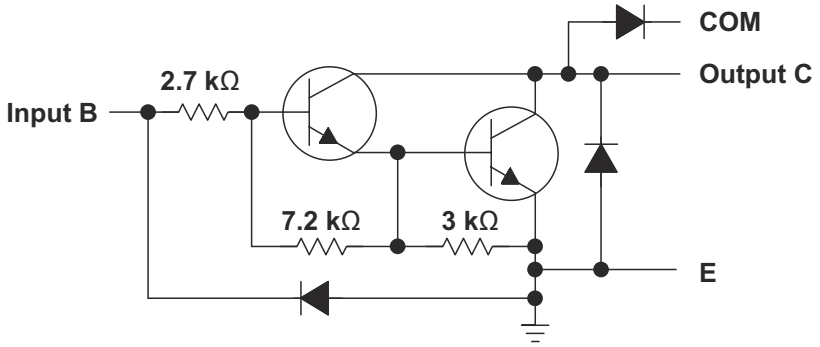
7 Detailed Description

7.1 Overview

This standard device has proven ubiquity and versatility across a wide range of applications. This feature is due to its integration of eight Darlington transistors that are capable of sinking up to 500 mA and wide GPIO range capability.

The ULN2803C is comprised of eight high voltage, high current NPN Darlington transistor pairs. All units feature a common emitter and open collector outputs. To maximize their effectiveness, these units contain suppression diodes for inductive loads. The ULN2803C has a series base resistor to each Darlington pair, thus allowing operation directly with TTL or CMOS operating at supply voltages of 5 V or 3.3 V. The ULN2803C offers solutions to a great many interface needs, including solenoids, relays, lamps, small motors, and LEDs. Applications requiring sink currents beyond the capability of a single output can be accommodated by paralleling the outputs.

7.2 Functional Block Diagram



7.3 Feature Description

Each channel of ULN2803C consists of Darlington connected NPN transistors. This connection creates the effect of a single transistor with a very-high current gain. The very high β allows for high output current drive with a very-low input current, essentially equating to operation with low GPIO voltages.

The GPIO voltage is converted to base current through the 2.7-kΩ resistor connected between the input and base of the predriver Darlington NPN.

The diodes connected between the output and COM pin are used to suppress the kickback voltage from an inductive load that is excited when the NPN drivers are turned off (stop sinking) and the stored energy in the coils causes a reverse current to flow into the coil supply through the kickback diode.

In normal operation, the diodes on base and collector pins to emitter are reverse biased. If these diodes are forward biased, internal parasitic NPN transistors draw (a nearly equal) current from other (nearby) device pins.

7.4 Device Functional Modes

7.4.1 Inductive Load Drive

When the COM pin is tied to the coil supply voltage, ULN2803C can drive inductive loads and suppress the kickback voltage through the internal free wheeling diodes.

7.4.2 Resistive Load Drive

When driving resistive loads, COM can be left unconnected or connected to the load voltage supply. If multiple supplies are used, connect to the highest voltage supply.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

ULN2803C is typically used to drive a high-voltage or current peripherals from an MCU or logic device that cannot tolerate these conditions. The following design is a common application of ULN2803C, driving inductive loads. This includes motors, solenoids, and relays. Each load type can be modeled by what is seen in Figure 8-1.

8.2 Typical Application

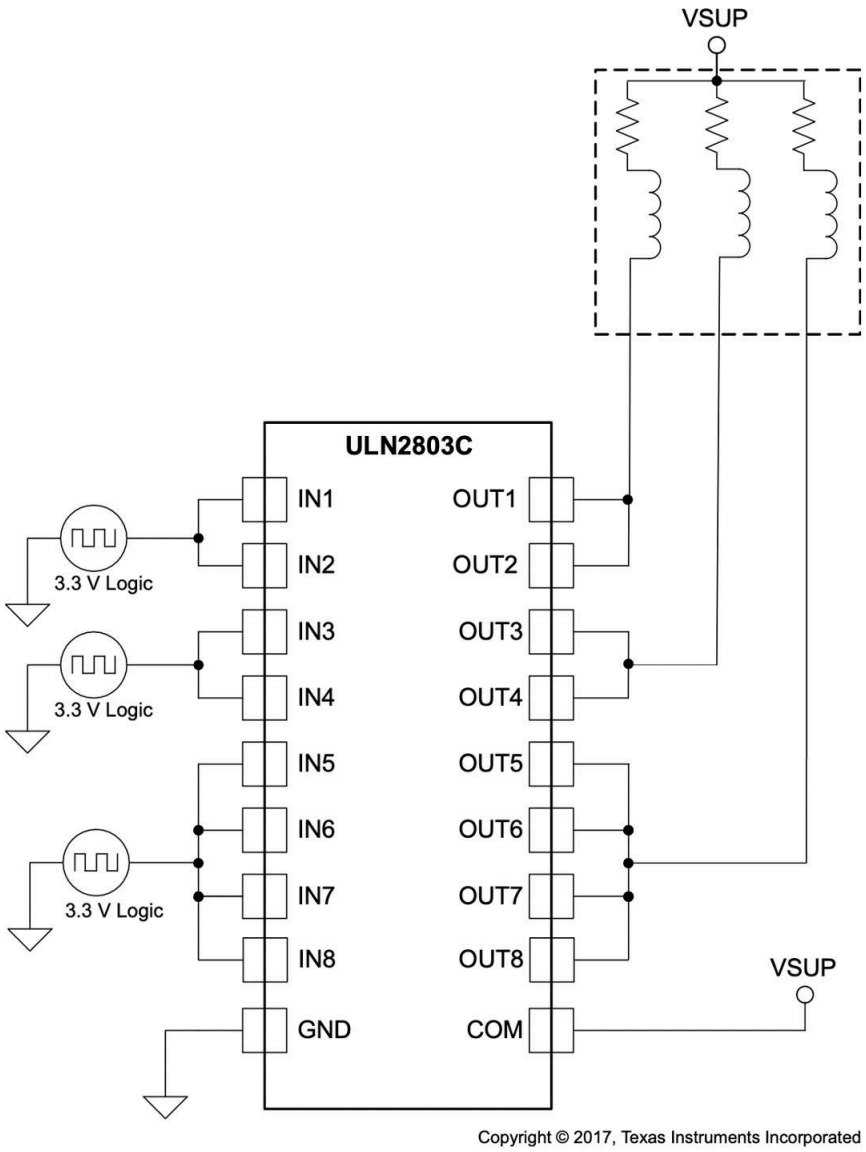


Figure 8-1. ULN2803C as Inductive Load Driver

8.2.1 Design Requirements

For this design example, use the parameters listed in Table 8-1 as the input parameters.

Table 8-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
GPIO voltage	3.3 or 5 V
Coil supply voltage	12 to 50 V
Number of channels	8
Output current (R_{COIL})	20 to 300 mA per channel
Duty cycle	100%

8.2.2 Detailed Design Procedure

When using ULN2803C in a coil driving application, determine the following:

- Input voltage range
- Temperature range
- Output and drive current
- Power dissipation

8.2.2.1 Drive Current

The coil current is determined by the coil voltage (VSUP), coil resistance, and output low voltage (V_{OL} or $V_{CE(SAT)}$).

$$I_{COIL} = (V_{SUP} - V_{CE(SAT)}) / R_{COIL} \quad (1)$$

8.2.2.2 Output Low Voltage

The output low voltage (V_{OL}) is equivalent to $V_{CE(SAT)}$ and can be determined by Figure 5-1, Figure 5-2, or using Section 5.5.

8.2.2.3 Power Dissipation and Temperature

The number of coils driven is dependent on the coil current and on-chip power dissipation. To determine the number of coils possible, use Equation 2 to calculate ULN2803C on-chip power dissipation P_D.

$$P_D = \sum_{i=1}^{N} V_{OLi} \times I_{Li} \quad (2)$$

where

- N is the number of channels active together.
- V_{OLi} is the OUT_i pin voltage for the load current I_{Li}. This is the same as $V_{CE(SAT)}$.

To ensure the reliability of ULN2803C and the system, the on-chip power dissipation must be lower that or equal to the maximum allowable power dissipation (P_D) dictated by Equation 3.

$$PD_{(MAX)} = \frac{\left(T_{J(MAX)} - T_A\right)}{\theta_{JA}} \quad (3)$$

where

- $T_{J(MAX)}$ is the target maximum junction temperature.
- T_A is the operating ambient temperature.
- θ_{JA} is the package junction to ambient thermal resistance.

TI recommends to limit the ULN2803C IC die junction temperature to < 125°C. The IC junction temperature is directly proportional to the on-chip power dissipation.

8.2.3 Application Curves

The following curves are generated with ULN2803C driving an OMRON G5NB relay – V_{in} = 5.0 V; V_{sup}= 12 V and R_{COIL}= 2.8 kΩ.

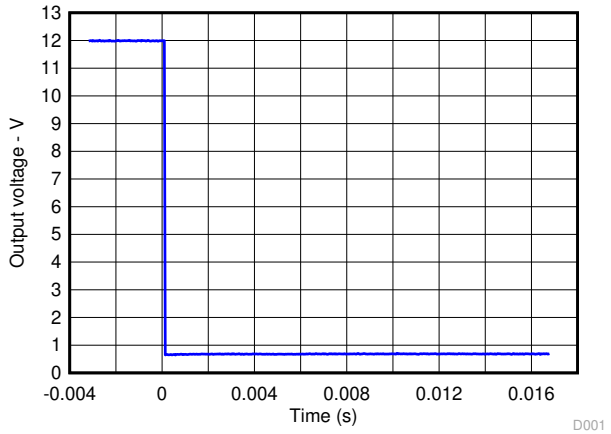


Figure 8-2. Output Response with Activation of Coil (Turn-On)

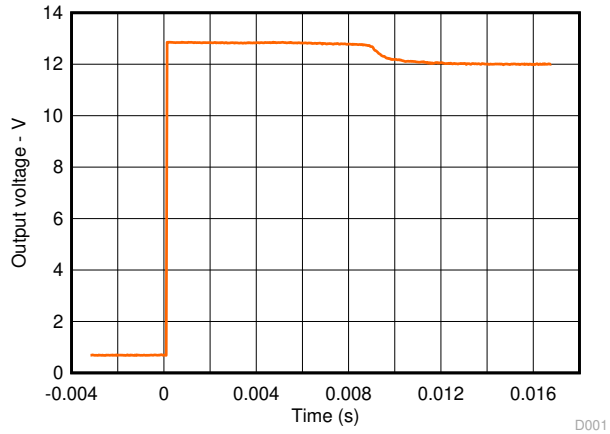


Figure 8-3. Output Response with De-activation of Coil (Turn Off)

8.3 Power Supply Recommendations

This devicedoes not need a power supply; however, the COM pin is typically tied to the system power supply. With this case, make sure that the output voltage does not heavily exceed the COM pin voltage. This action can heavily forward bias the flyback diodes and cause a large current to flow into COM, potentially damaging the on-chip metal or overheating the part.

8.4 Layout

8.4.1 Layout Guidelines

Thin traces can be used on the input due to the low current logic that is typically used to drive ULN2803C. Take care to separate the input channels as much as possible, as to eliminate crosstalk. TI recommends thick traces for the output to drive high currents as desired. Wire thickness can be determined by the trace material current density and desired drive current.

Because all of the channels currents return to a common emitter, size that trace width to be very wide. Some applications require up to 2.5 A.

8.4.2 Layout Example

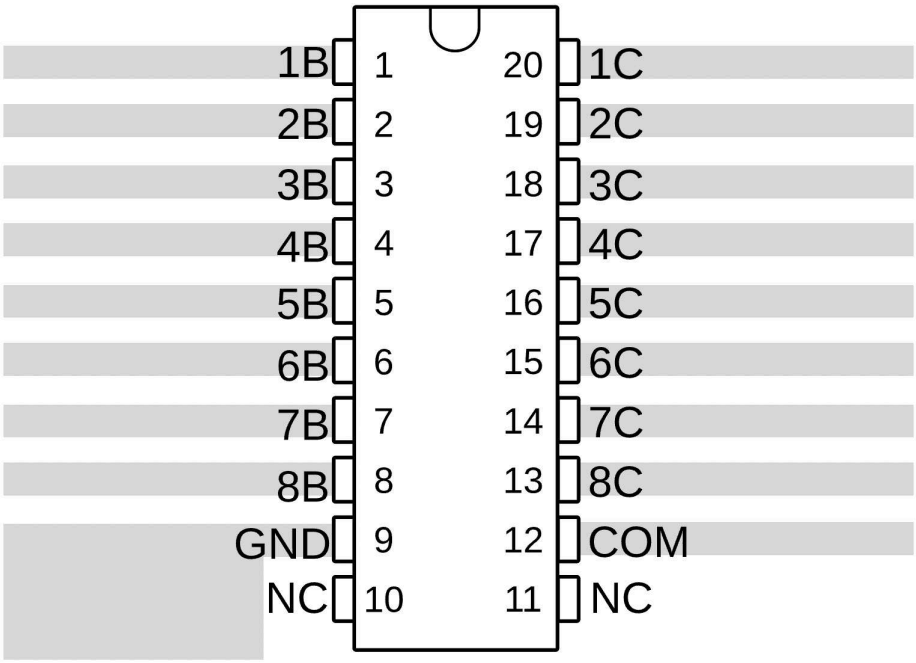


Figure 8-4. ULN2803C Layout Example

9 Device and Documentation Support

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (March 2024) to Revision B (September 2024)	Page
• Changed part number from ULN2803A to ULN2803C in the *Thermal Information* section	4

Changes from Revision * (August 2022) to Revision A (March 2024)	Page
• Updated thermal parameters in the *Thermal Information* section	4
• Changed typical specification for V_F, Clamp forward voltage from 1.7V : to 1.3V in the *Electrical Characteristics* section	4
• Updated graphs in the *Typical Characteristics* section	4

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ULN2803CDWR	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ULN2803C
ULN2803CDWR.A	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ULN2803C

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

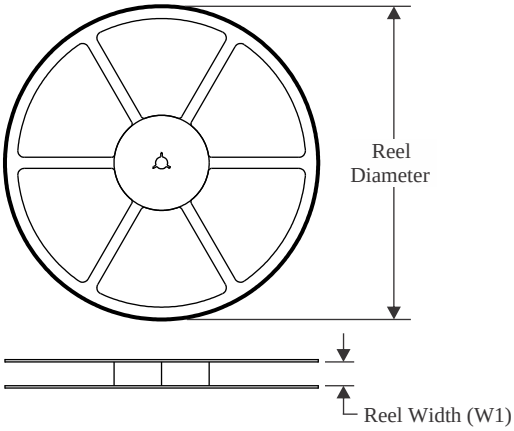
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

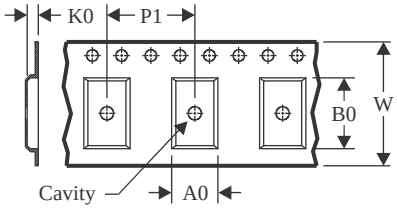
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

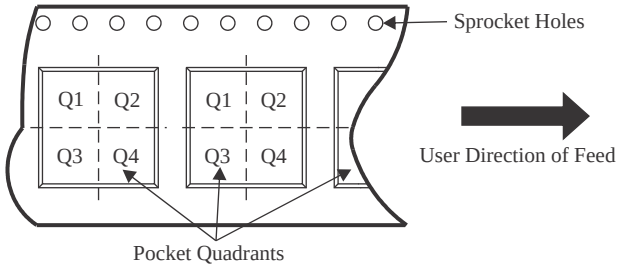


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

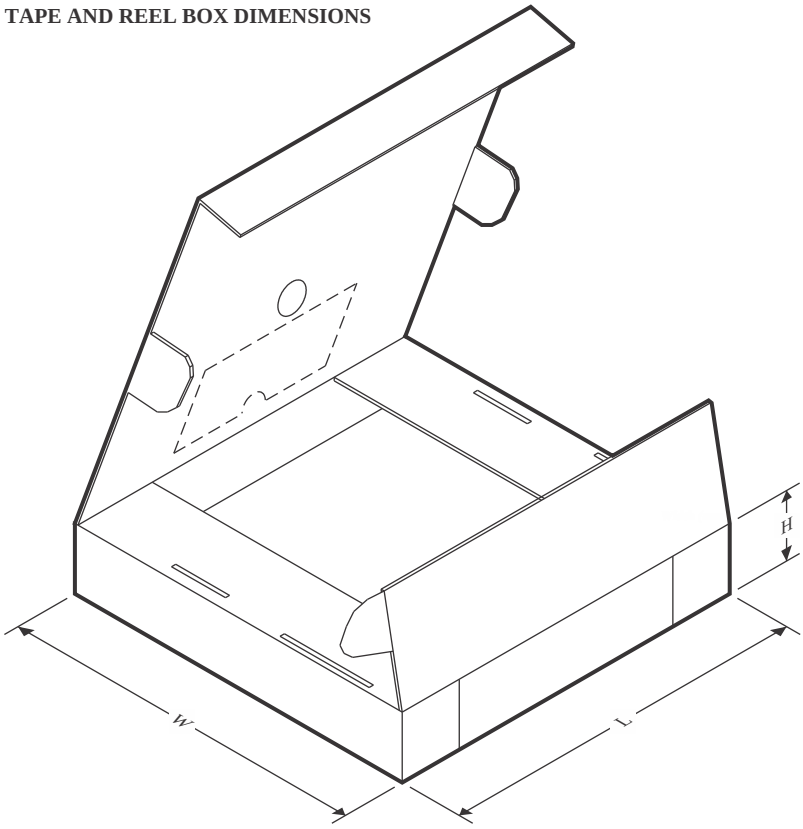
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

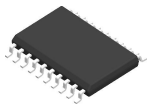
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ULN2803CDWR	SOIC	DW	20	2000	330.0	24.4	10.9	13.3	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ULN2803CDWR	SOIC	DW	20	2000	356.0	356.0	45.0

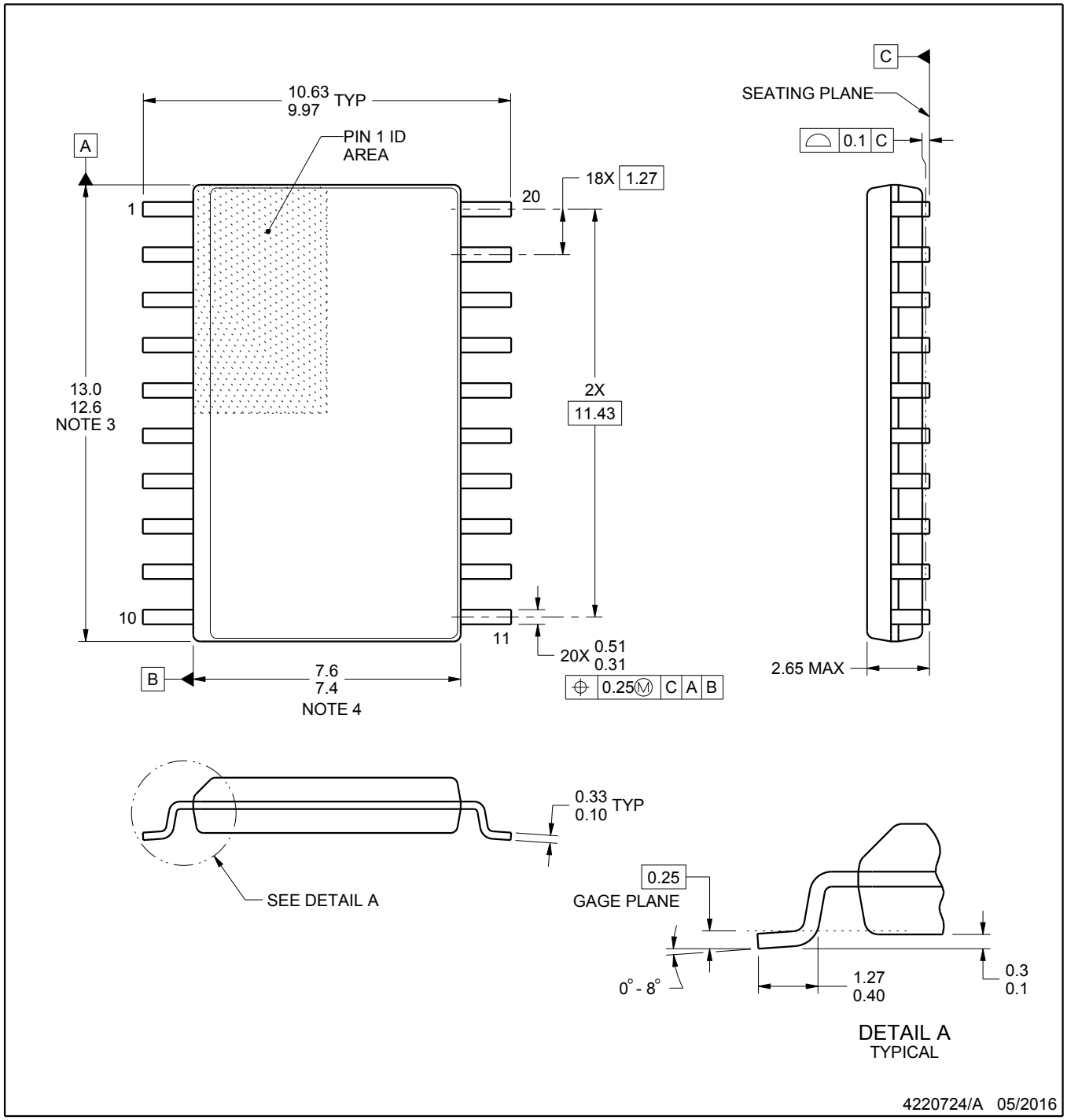


PACKAGE OUTLINE

DW0020A

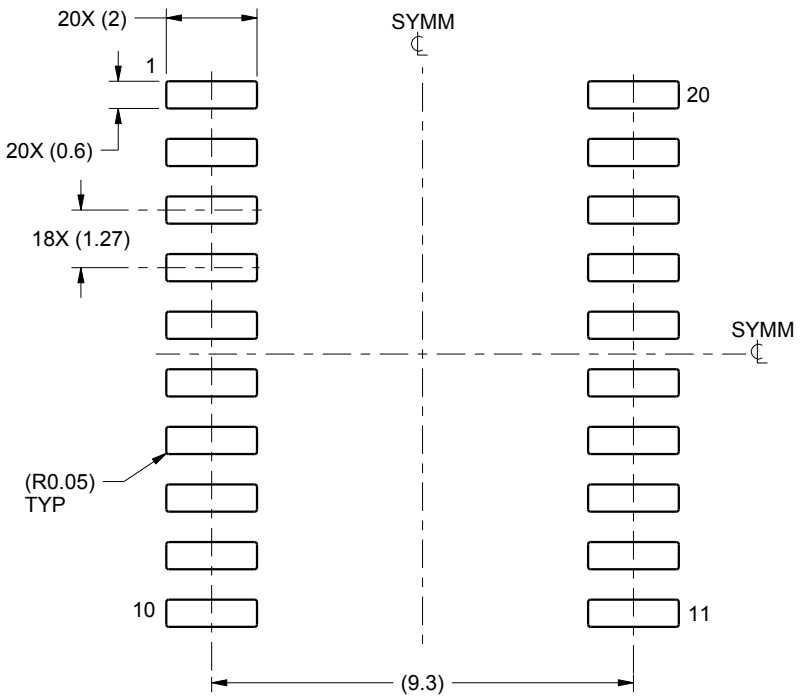
SOIC - 2.65 mm max height

SOIC

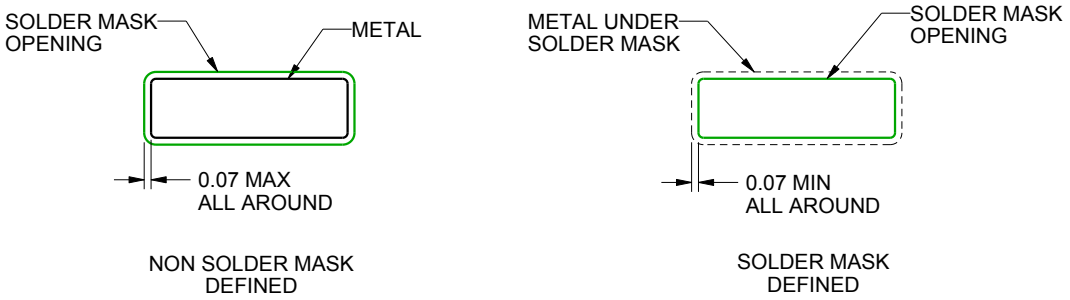


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X

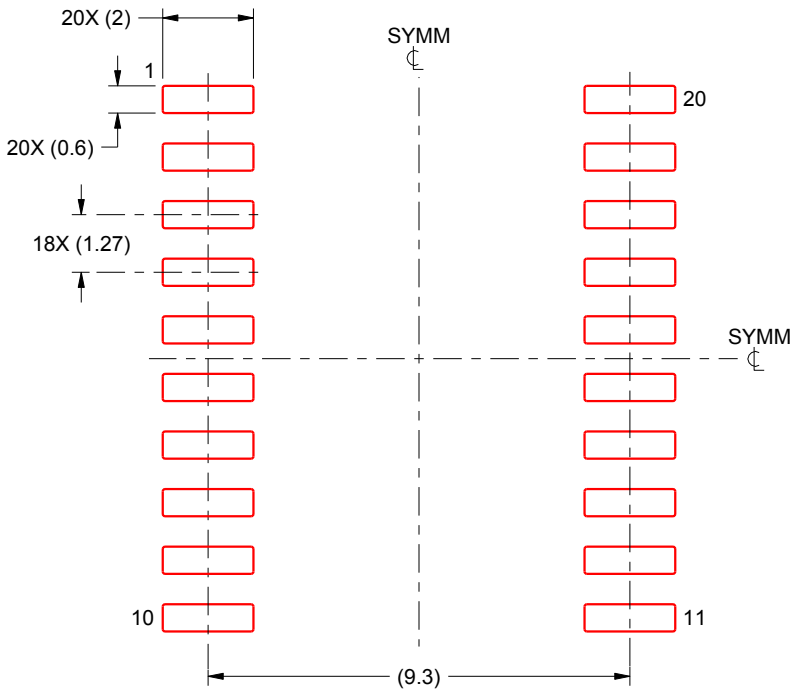


SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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