

Application Report

TPS745-Q1 Functional Safety FIT Rate, FMD and Pin FMEA



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1 Overview

This document contains information for TPS745-Q1 (DRV and DRB package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the Adjustable Version With Open-Drain Power-Good functional block diagram for reference.

Figure 1-2 shows the Adjustable Version With Push-Pull Power-Good functional block diagram for reference.

Figure 1-3 shows the Fixed Voltage Version With Open-Drain Power-Good functional block diagram for reference.

Figure 1-4 shows the Fixed Voltage Version With Push-Pull Power-Good functional block diagram for reference.

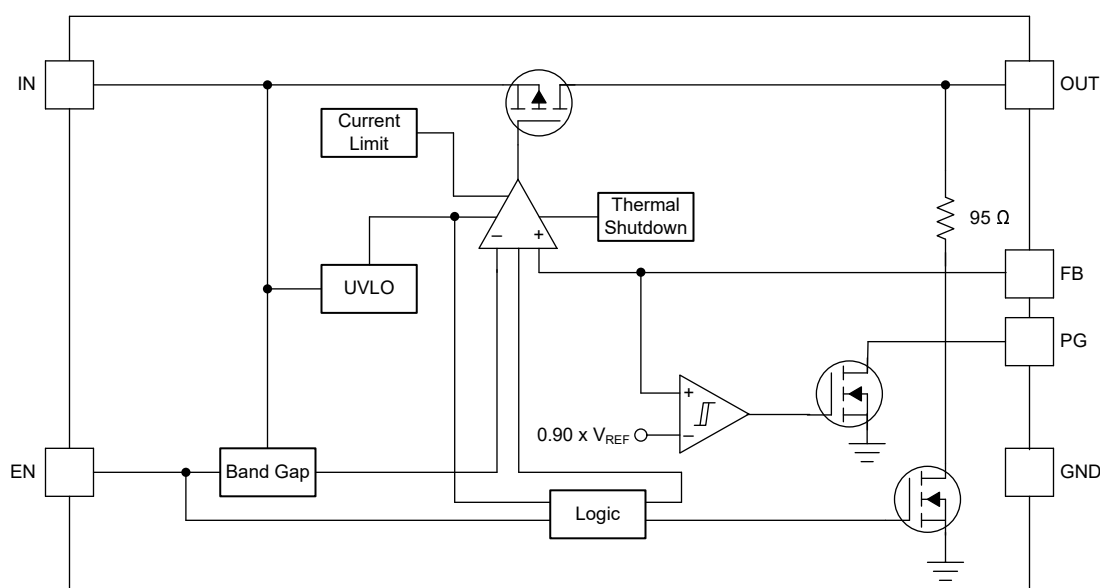


Figure 1-1. Adjustable Version With Open-Drain Power-Good

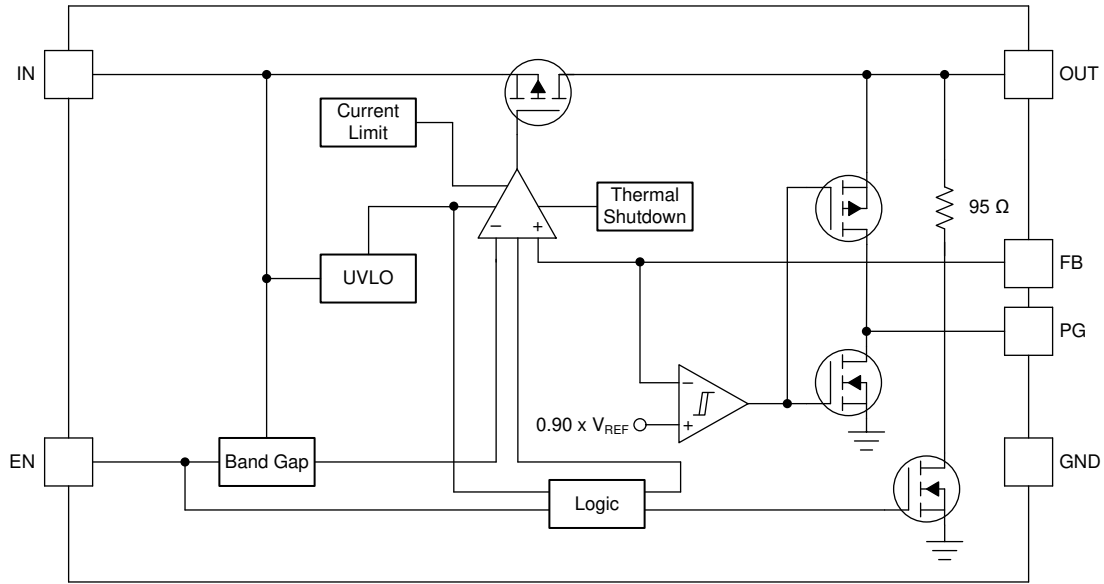


Figure 1-2. Adjustable Version With Push-Pull Power-Good

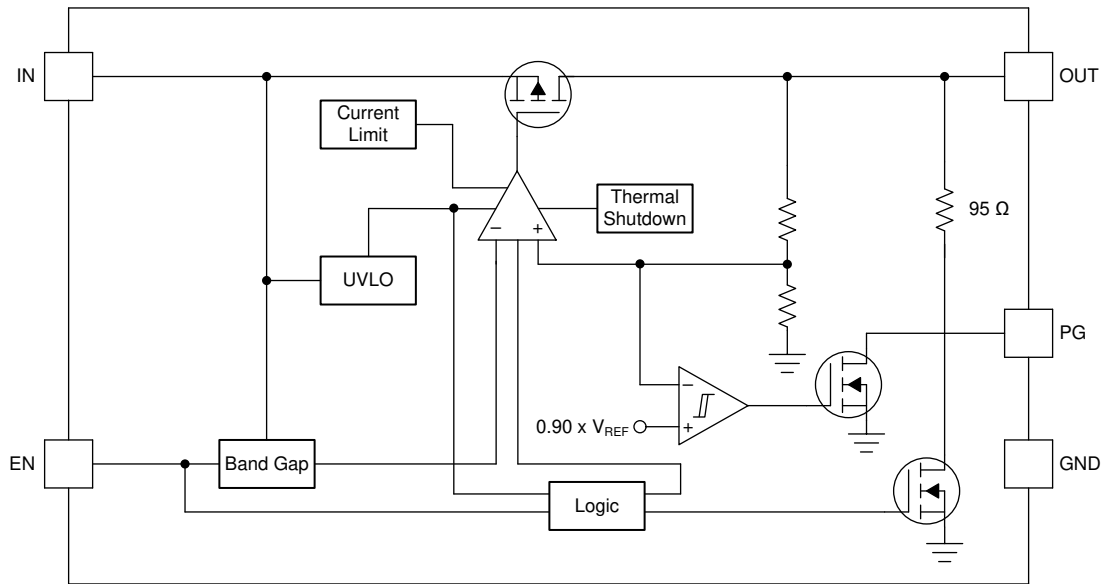


Figure 1-3. Fixed Voltage Version With Open-Drain Power-Good

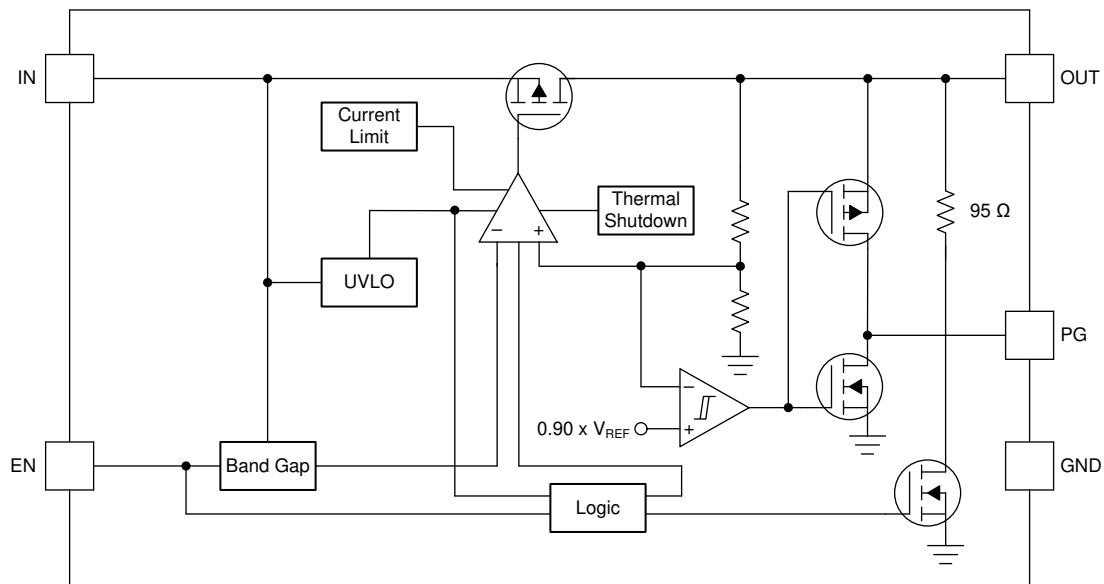


Figure 1-4. Fixed Voltage Version With Push-Pull Power-Good

TPS745-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for TPS745-Q1 based on two different industry-wide used reliability standards:

- [Table 2-1](#) provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- [Table 2-2](#) provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10 ⁹ Hours)	
	WSON-6	WSON-8
Package		
Total Component FIT Rate	7	9
Die FIT Rate	5	5
Package FIT Rate	2	4

The failure rate and mission profile information in [Table 2-1](#) comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 350 mW
- Climate type: World-wide Table 8
- Package factor (λ_3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T _J
5	CMOS, BICMOS Digital, analog / mixed	25 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in [Table 2-2](#) come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for TPS745-Q1 in [Table 3-1](#) comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
VOUT High (Following VIN)	15%
VOUT Not in Specification - Voltage or Timing	60%
VOUT Low (No Output)	15%
PG False Trigger, Fails to Trigger	5%
Short Circuit Any Two Pins	5%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the TPS745-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see [Table 4-3](#))
- Pin open-circuited (see [Table 4-4](#))
- Pin short-circuited to an adjacent pin (see [Table 4-5](#))
- Pin short-circuited to supply (see [Table 4-6](#))

[Table 4-3](#) through [Table 4-6](#) also indicate how these pin conditions can affect the device as per the failure effects classification in [Table 4-1](#).

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

[Figure 4-1](#) shows the TPS745-Q1 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the TPS745-Q1 data sheet.

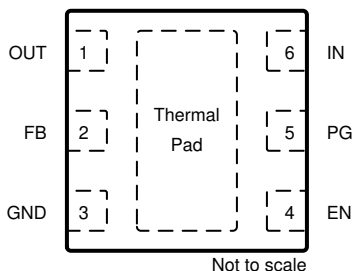


Figure 4-1. Pin Diagram Adjustable TPS745-Q1 DRV Package

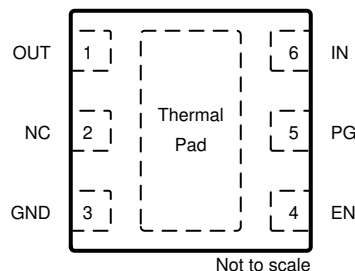


Figure 4-2. Pin Diagram Fixed TPS745-Q1 DRV Package

Table 4-2. Pin Functions

PIN		I/O	Description
Name	No.		
OUT	1	Output	Regulated Output
FB/NC	2	-	[Adjustable Output] Input to the Control Loop Error Amplifier [Fixed Output] No Internal Connection [Fixed Output] No Internal Connection
GND	3	-	Ground
EN	4	Input	Drive Greater Than $V_{EN(HIGH)}$ to Turn On the Regulator. Drive Less Than $V_{EN(LOW)}$ to Put Regulator in Shutdown Mode
PG	5	Output	Power-Good Output
IN	6	Input	Input Supply
Thermal Pad		-	Connect Thermal Pad to Ground for Improved Thermal Performance

Table 4-3. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
OUT	1	Output voltage will be near/at ground - Device will enter current limit. It may cycle in and out of thermal shutdown depending on power dissipation	B
FB/NC	2	[Adjustable Output] Device will stop regulating. V_{OUT} becomes equal to V_{IN} minus dropout because the pass fet is driven on as hard as possible [Fixed Output] No effect	B/D
GND	3	-	D
EN	4	Device will turn off	B
PG	5	PG function will not work	D
IN	6	No output voltage. Input supply can be 0V	B

Table 4-4. Pin FMA for Device Pins Open-Circuited

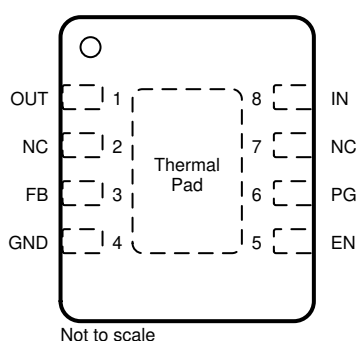
Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
OUT	1	Output voltage is disconnected from load	B
FB/NC	2	[Adjustable Output] Error amplifier input is left floating, output voltage will not equal to set voltage [Fixed Output] No effect	B/D
GND	3	Device may disable	B
EN	4	Device may disable	B
PG	5	PG function does not work	D
IN	6	No output voltage	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Short with	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
OUT	1	FB/NC	2	[Adjustable Output] V_{OUT} will be set to $V_{FB} = 0.55V$ [Fixed Output] No effect	B/D
FB/NC	2	GND	3	[Adjustable Output] Device will stop regulating. V_{out} becomes equal to V_{IN} minus dropout because the pass fet is driven on as hard as possible [Fixed Output] No effect	B/D
GND	3	EN	4	Output is forced OFF, V_{OUT} is 0.0V	B
EN	4	PG	5	The device will stay OFF	B
PG	5	IN	6	PG Function does not work	D

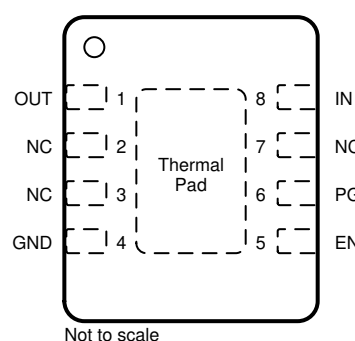
Table 4-6. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
OUT	1	Output is not Regulated. $V_{OUT} = V_{IN}$	B
FB/NC	2	[Adjustable Output] FB pin will be damaged if V_{in} is higher than 2V [Fixed Output] No effect	A/D
GND	3	No Output Voltage. Either input supply is at 0.0V, or input fuse is blown	B
EN	4	Output is forced ON regardless of enable signal	B
PG	5	PG function does not work	D
IN	6	No Effect	D



Not to scale

Figure 4-3. Pin Diagram Adjustable TPS745-Q1 DRB Package



Not to scale

Figure 4-4. Pin Diagram Fixed TPS745-Q1 DRB Package

Table 4-7. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
OUT	1	Output voltage will be near/at ground - Device will enter current limit. It may cycle in and out of thermal shutdown depending on power dissipation	B
NC	2	Improved Thermal Performance	D
FB/NC	3	[Adjustable Output] Device will stop regulating. V_{OUT} becomes equal to V_{IN} minus dropout because the pass fet is driven on as hard as possible [Fixed Output] No effect	B/D
GND	4	-	D
EN	5	Device will turn off	B
PG	6	PG function will not work	D
NC	7	Improved Thermal Performance	D
IN	8	No output voltage.	B

Table 4-8. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
OUT	1	Output voltage is disconnected from load	B
NC	2	No Effect	D
FB/NC	3	[Adjustable Output] Error amplifier input is left floating, output voltage will not equal to set voltage [Fixed Output] No effect	B/D
GND	4	Device may disable	B
EN	5	Device may disable	B
PG	6	PG function does not work	D
NC	2	No Effect	D
IN	8	No output voltage	B

Table 4-9. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Short with	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
OUT	1	NC	2	Reduced thermal performance	D
NC	2	FB/NC	3	No Effect	D
FB/NC	3	GND	4	[Adjustable Output] Device will stop regulating. V _{out} becomes equal to V _{IN} minus dropout because the pass fet is always on [Fixed Output] No effect	B/D
GND	4	EN	5	Output is forced OFF, V _{OUT} is 0.0V	B
EN	5	PG	6	The device will stay OFF	B
PG	6	NC	7	No Effect	D
NC	7	IN	8	Reduced thermal performance	D

Table 4-10. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
OUT	1	Output is not Regulated. V _{OUT} = V _{IN}	B
NC	2	No Effect	D
FB/NC	3	[Adjustable Output] FB pin will be damaged if V _{in} is higher than 2V [Fixed Output] No effect	A/D
GND	4	No Output Voltage. Either input supply is at 0.0V, or input fuse is blown	B
EN	5	Output is forced ON regardless of enable signal	B
PG	6	PG function does not work	D
NC	7	No Effect	D
IN	8	No Effect	D

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