Design Summary for 56GQL (48- and 56-pin functions) MicroStar Junior™ BGA

**PCB Design Guidelines**

**Package Via to Board Land Area Configuration**

- **Near-Sn/Pb eutectic solder** with liquidus temperature of 178°C to 210°C
- Package ball via
  - A = Via diameter on package = 0.33 mm (for 0.65-mm pitch)
  - B = Land diameter on PCB
- Ratio A/B should equal 1.0 for optimum reliability

**Solder Ball Collapse**

- Overall Height < 1.0 mm
- 0.2 mm typical

**VFBGA Recommended Land Pad Design**

- **Solder Mask Defined Pad**
  - A = 0.43 mm
  - B = 0.33 mm
- **Non Solder Mask Defined Pad**
  - A = 0.30 mm
  - B = 0.45 mm

**Trace Width/Spacing Dimensions (mm [in.])**

- **Non-Solder Mask Defined Pad**
  - 0.117 [.0046] min. space
  - 0.65 [.0256] Trace
  - 0.117 [.0046] Solder Pad
  - 0.65 [.0256]

- **Recommended Board Routing**

  **Recommended Routing for VFBGA-48**
  - GND
  - V_CC

  **Recommended Routing for VFBGA-56**
  - GND
  - V_CC

  Note: Typical for most devices. Refer to data sheet for specific applications.
**Geometric Dimensional Tolerances**

**Coplanarity**

This geometric dimensioning and tolerancing (GD & T) term \( 0.08 \text{ mm} \) means that this package meets a coplanarity of 0.08 mm as shown below. Coplanarity is defined as a unilateral tolerance zone measured upward from the seating plane. (Reference ASME Y14.5-1994).

**Position Tolerance**

This GD & T term \( \square \odot 0.05 \) is described below:

- \( \odot \) This is the symbol for true position.
  - True position is defined as the theoretically exact centerline location of the solder ball(s).

- \( \square \) 0.05 This symbol/number represents how much the centerline of the solder ball(s) is allowed to vary from it’s true position.
  - This symbol/letter is defined as the maximum material condition of the solder ball(s) which is 0.45 mm DIA.

The graphic representation is shown below for the top, left solder ball of this package.

![Graphic representation of coplanarity and position tolerance](image)

- \( \odot \) Pattern locating boundary for the centerline of the solder ball. (0.05 mm DIA)
- \( \square \) Pattern locating boundary containing the collective dimensions of the maximum size of the solder ball (0.45 mm) and the maximum variance of the centerline of the solder ball (0.05 mm) for a total boundary of 0.50 mm DIA.
  - I.E., the solder ball, regardless of size, must fall within this boundary. (Defined as "virtual condition" per ASME standard Y14.5 - 1994).
  - Please note that a smaller diameter solder ball will have more tolerance in this boundary than the maximum diameter solder ball.

- \( \square \) *These two dimensions are calculated based on a package with nominal body width and length dimensions.*

**IR Reflow Profile**

**Ideal (1st and 2nd) Reflow Profile**

<table>
<thead>
<tr>
<th>Temperature Range</th>
<th>Time Duration</th>
</tr>
</thead>
<tbody>
<tr>
<td>Room Temp to 140 C</td>
<td>60 - 90 sec.</td>
</tr>
<tr>
<td>140 C to 160 C</td>
<td>90 - 120 sec.</td>
</tr>
<tr>
<td>Time above 200 C</td>
<td>30 - 60 sec.</td>
</tr>
<tr>
<td>Peak Temp:</td>
<td>235 C ±5 C</td>
</tr>
<tr>
<td>Time within 5 C Peak Temp</td>
<td>10-20 sec.</td>
</tr>
<tr>
<td>Ramp down rate:</td>
<td>1 - 3 C/sec. max.</td>
</tr>
</tbody>
</table>

Note:
- This is an ideal profile, and actual conditions obtained in any specific reflow oven will vary. This profile is based on convection or RF plus forced convection heating.
Tape and Reel Packing

- Desiccant
- Humidity Indicator
- Reeled Units
- Aluminum Bag
- Pizza Box
- Bar Code
- ESD Label

Note: for air module packing, pizza box are placed directly.
48/56GQL (4.5 x 7.0 mm, 0.65 mm pitch)

**Package Outline**

- Electrical Characteristics
  - R(ohms) L(nH) C(pF)
    - Min. 0.048 1.470 0.182
    - Mean 0.066 2.257 0.264
    - Max. 0.116 3.965 0.430

**Thermal Characteristics**

- Eight Thermal Vias, High K

**Daisy Chain Net List**

**Pinout**

- Pinout for 48-pin functions
  - Min. 0.048 1.470 0.182
  - Mean 0.066 2.257 0.264
  - Max. 0.116 3.965 0.430

**Package Reliability Data**

- Required Sample Size / #Fails
- ALVCH16501GQL Actual Sample Size / # Fails

- Simultaneous Switching Life Test (SSLT), 150 C, 300 Hours 39 / 0 39 / 0
- Highly Accelerated Life Test (HAST), 130 C, 85% RH, 100 Hours 39 / 0 39 / 0
- Temperature Cycle Test, -65 C to 150 C, 1000 Hours 77 / 0 77 / 0
- Autoclave, 121 C, 96 Hours 77 / 0 77 / 0
- Solderability, 8 Hours 8 / 0 8 / 0
- Flammability (UL) 5 / 0 5 / 0
- Flammability (IEC) 5 / 0 5 / 0
- Thermal Shock 26 / 0 26 / 0
- X-Ray, Top View Only 5 / 0 5 / 0
- Physical Dimensions 15 / 0 15 / 0
- Manufacturability pass pass

**Board Level Reliability Data**

- 56 GQL Package
- Sample Size = 32
- Temp Cycle Range -40 C to 125 C
- No Underfill

- Board Thickness (mm) 1.6 0.8 0.8, no Au
- 0 cycle 0 0 0
- 250 cycle 0 0 0
- 500 cycle 0 0 0
- 750 cycle 0 0 0
- 1000 cycle 2* 0 0
- 1250 cycle 15 1 0
- 1500 cycle 19 8 0
- 1750 cycle N/A 20 1
- 2000 cycle N/A N/A 0

* First failure at 951 cycles

**Note:** This is a topside view
Questions and Answers

Board Design/Electrical Issues

Q. Where can the decoupling capacitors go for the VFBGA package?
A. The recommended capacitance value and number of capacitors for decoupling is a 0.1 nF capacitor for each VCC on the VFBGA package. The decoupling capacitors should be connected as close as possible to the GROUND and VCC planes.

Q. Any EMI concerns for traces under the package and how can customers design their board to minimize EMI?
A. EMI can be controlled by minimizing any complex current loops on the PCB trace. Some helpful hints include:
   - Solid ground and power planes be used in the design. Partitioned ground and power planes must be avoided. These ground and power partitions may create complex current loops increasing radiation.
   - Avoid right angles or "T" crosses on the trace. Right angles can cause impedance mismatch and increase trace capacitance causing signal degradation.
   - Minimize power supply loops by keeping power and ground traces parallel and adjacent to each other. Significant package EMI can be reduced by using this method.
   - Use decoupling capacitors as described in the previous question.

Lead-Free

Q. Is TI developing a lead-free version of MicroStar Junior BGAs?
A. Yes, Texas Instruments is working toward eliminating lead in the solder balls to comply with lead-free environmental policies. The lead-free solder is in final sample availability.

Assembly Process/Yield Considerations

Q. What size land diameter for these packages should I design on my board?
A. Land size is the key to board-level reliability, and Texas Instruments strongly recommends following the design rules included in this bulletin.

Q. Can customers mount MicroStar Junior BGA packages on the bottom side of the PCB board?
A. Yes, they can and the ideal 2nd reflow profile is the same as the 1st (IR profile is recommended in the bulletin). The root causes for solder ball off are:
   - Excess amount of solder paste during customers board assembly. TI recommends minimizing the amount of solder paste on the bottom side by using a stencil thickness of 0.15 mm with 0.33-mm aperture opening.
   - Moisture absorption also affects the ball off issue. The package was qualified at Moisture Level 2, and has been released at Moisture Level 2A. The first and second reflow must be completed within 4 weeks.

Q. Should I use underfill?
A. No, the package qualification results show that this is not necessary and is only an added process expense.

Q. Can the boards be repaired?
A. Yes, there are rework and repair tools and profiles available (see references 4 and 7). We strongly recommend that removed packages be discarded.

Q. How do the board assembly yields of MicroStar Junior BGAs compare to TSSOPs?
A. Many customers are initially concerned about assembly yields. However, once they had MicroStar Junior BGAs in production, most of them report improved process yields compared to TSSOPs. This is due to the elimination of bent and misoriented leads, the wider terminal pitch than with 0.5-mm pitch TSSOPs, and the ability of these packages to self align during reflow. The collapsing solder balls also mean that the coplanarity is improved over leaded components.

Q. What alignment accuracy is possible?
A. Alignment accuracy for the 0.85-mm pitch package is dependent upon board level pad tolerance, placement accuracy, and solder ball position tolerance. Nominal ball position tolerances are specified at ±50 microns. These packages are self-aligning during solder reflow, so final alignment accuracy may be better than placement accuracy.

Q. Are there specific recommendations for SMT processing?
A. Texas Instruments recommends alignment with the solder balls for the CSP package, although it is possible to use the package outline for alignment. Most customers have found they do not need to change their reflow profile.

Q. Can the solder joints be inspected after reflow?
A. Process yields of 5-ppm rejects are typically seen, so no final inline inspection is required. Some customers are achieving satisfactory results during process setup with lamographic X-ray techniques.

References

Recommended References:
1. MicroStar BGA Packaging Reference Guide - SSYZ015
2. 96 and 114 ball LFBGA Application Note - IDT, Philips Semiconductor and Texas Instruments
3. Board Level Reliability Evaluations of 40 and 32 Ball Pitch Ball Grid Array Packages Over -40 to 125 C - Puligandla Viswanadham, Steve Dunford and Ted Carper, Circuit Card Assemblies Center of Excellence Raytheon Systems Co.
TI Worldwide Technical Support

Internet
TI Semiconductor Home Page
www.ti.com/sc

MicroStar Junior BGA Home Page
www.ti.com/sc/msjunior

TI Distributors
www.ti.com/sc/docs/general/distrib.htm

Logic Overview Page
www.ti.com/sc/logic

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