TI-RSLK MAX

Texas Instruments Robotics System Learning Kit

Texas Instruments

Module 18

Lecture: Serial Communication - UART

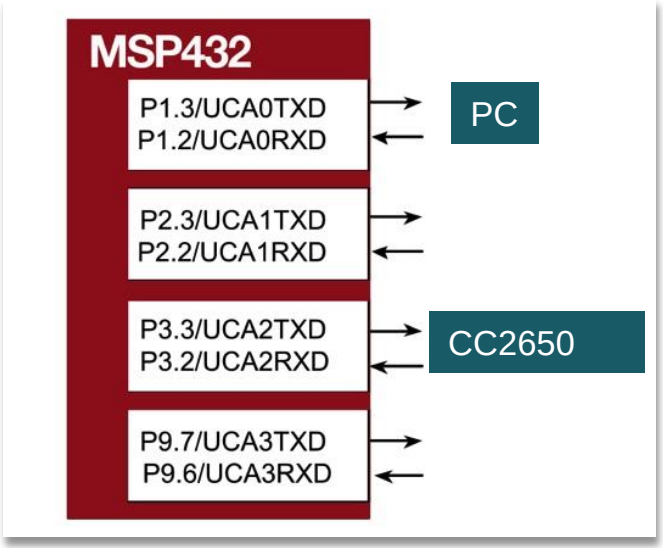
Serial Communication

You will learn in this module

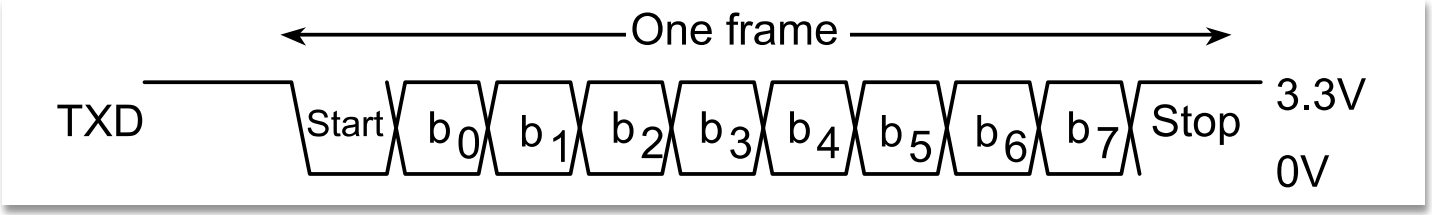
- Communication
  - Encode
  - Transmit
  - Decode

- Serial: Universal Asynchronous Receiver Transmitter
  - Interrupts
  - Baud rate

- Performance measures
  - Bandwidth
  - Response time



Universal Asynchronous Receiver/Transmitter (UART)

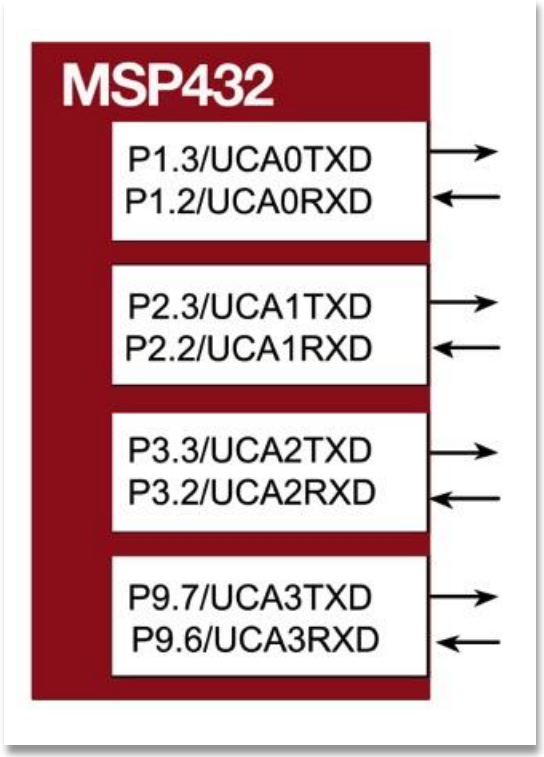


- Send/receive a **frame**
  - 1 start (low), 5-8 data bits , 1 stop (high)
  - Serial fashion, one bit every **bit-time**
  - No clock is sent, asynchronous, timing derived from data

- **Baud rate** is total number of bits per unit time
  - Baud rate = 1 / bit-time
  - Both transmitter and receiver agree and know the baud rate

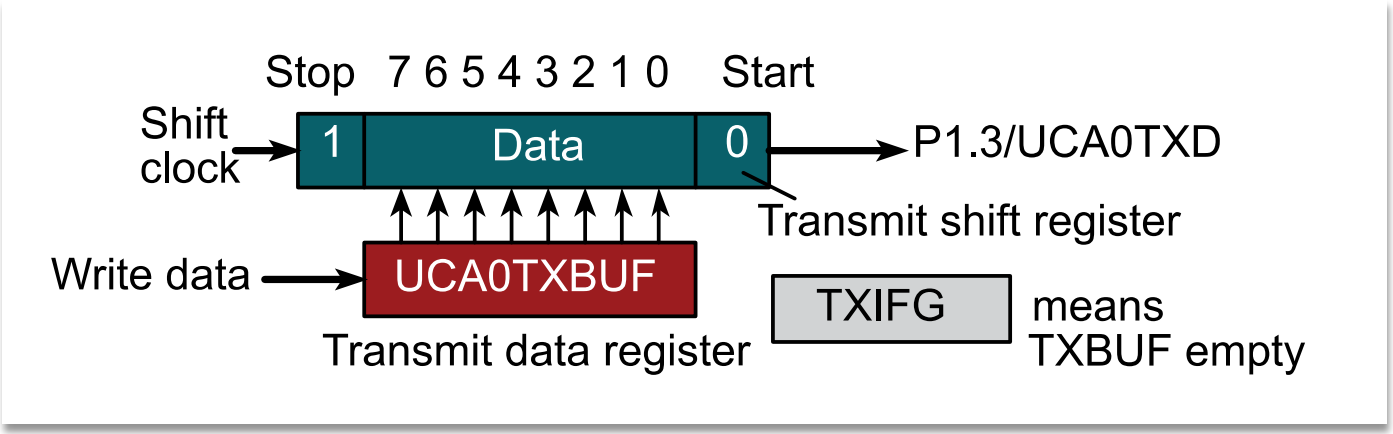
- **Bandwidth** is data or information per unit time
  - Bandwidth = (data-bits / frame-bits) * baud rate

UART Port Selection



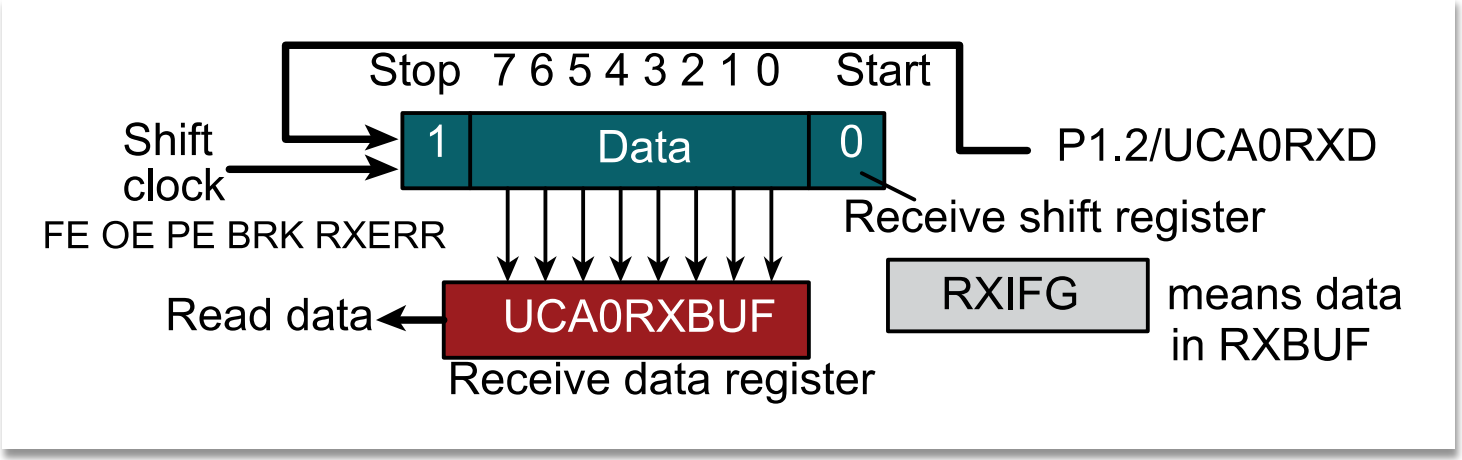
Pin	PxSEL1=0, PxSEL0=1
P1.2	UCA0RXD
P1.3	UCA0TXD
P2.2	UCA1RXD
P2.3	UCA1TXD
P3.2	UCA2RXD
P3.3	UCA2TXD
P9.6	UCA3RXD
P9.7	UCA3TXD

UART - Transmitter



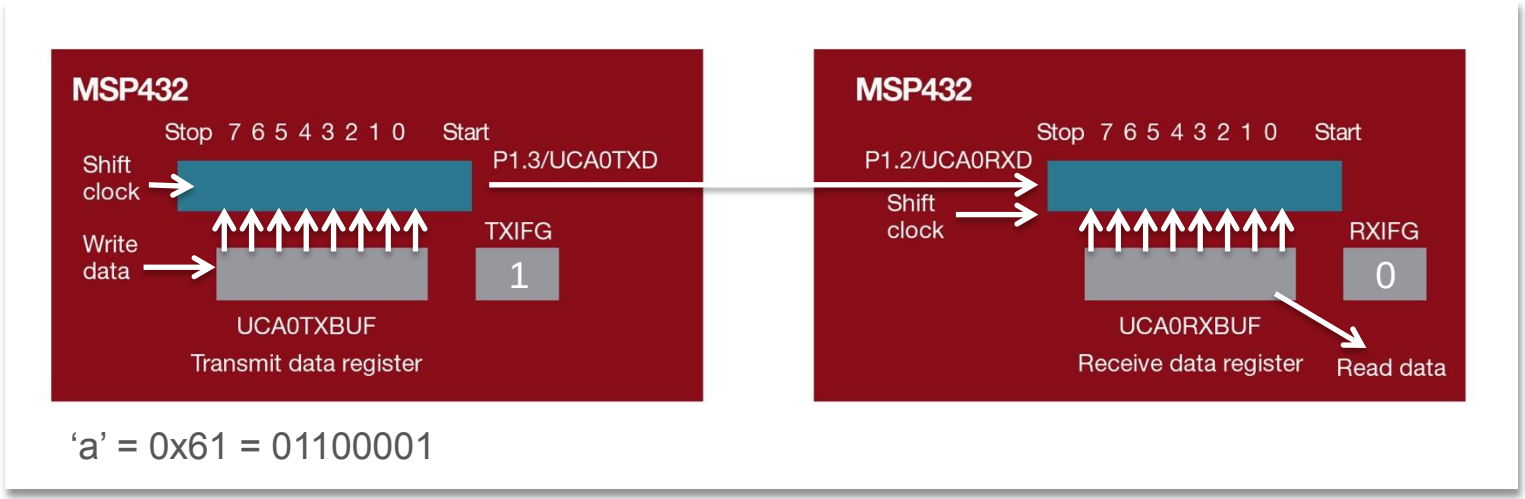
- Interrupt on TXIFG
- Data written to UCA0TXBUF
- Add start, stop bits
- Shift out at Baud Rate clock

UART - Receiver



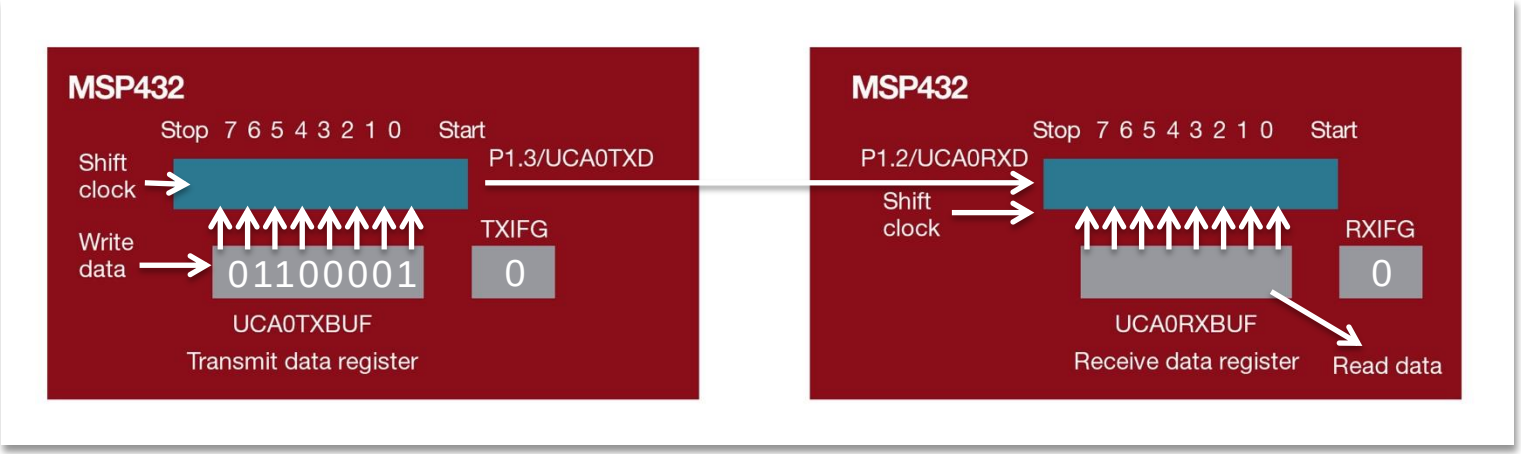
- Start bit synchronization, shift in at baud rate
- Interrupt on RXIFG
- Read data from UCA0RXBUF

UART - Communication



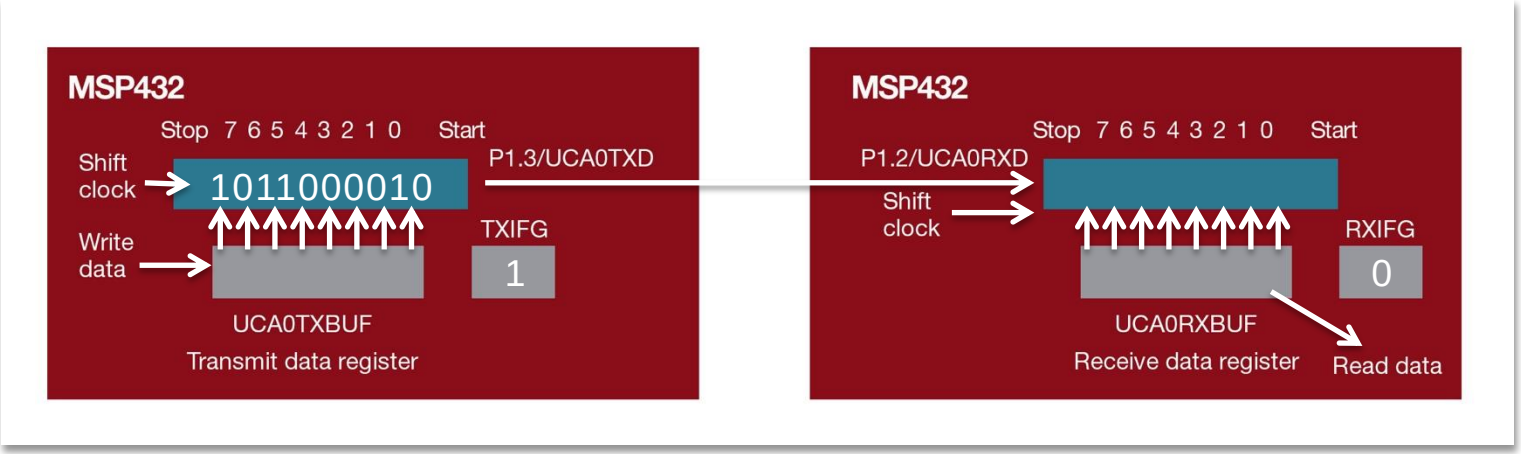
- TXIFG in transmitter is 1

UART - Communication



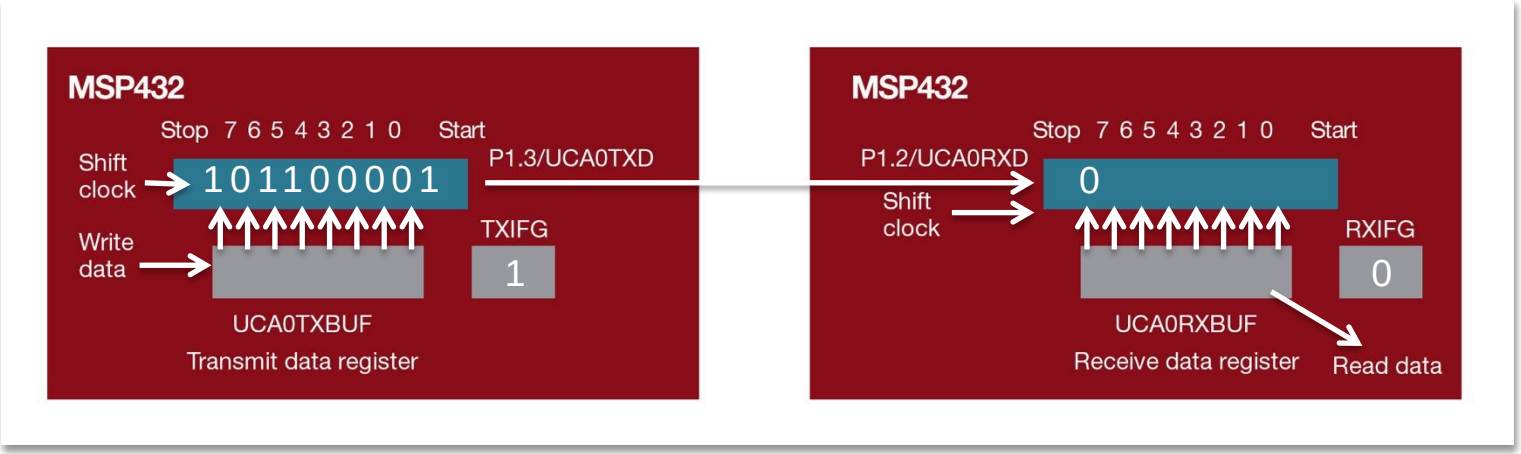
- Transmitter writes to UCA0TXBUF (‘a’ = 0x61 = 01100001)
- TXIFG in transmitter becomes 0

UART - Communication



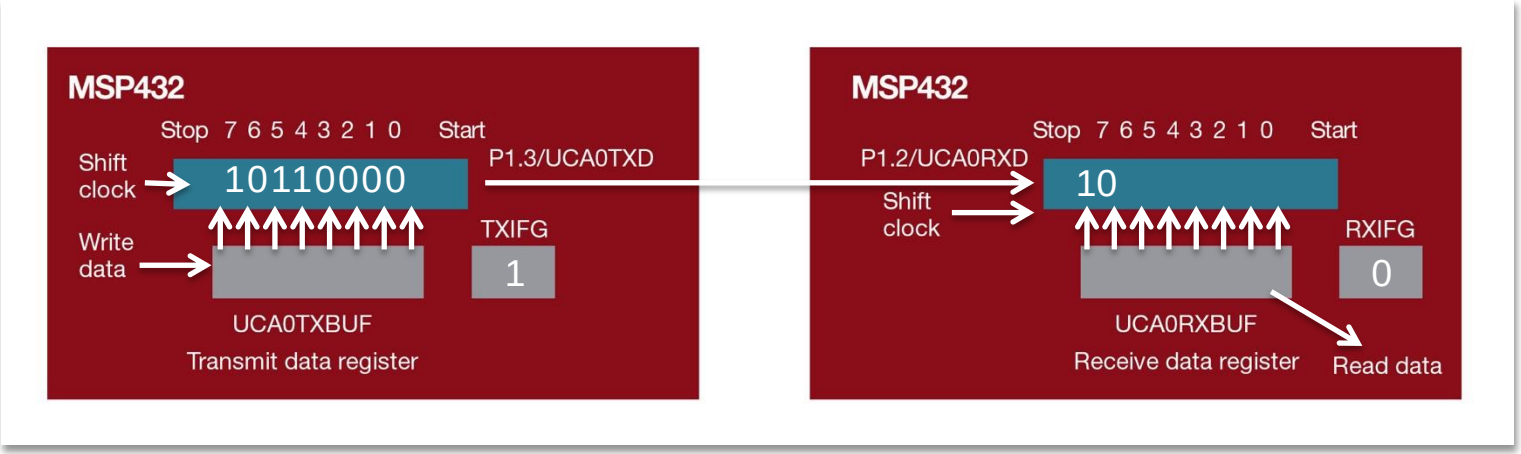
- Data is moved from TXBUF to shift register
- Start bit and stop bit added
- TXIFG in transmitter becomes 1

UART - Communication



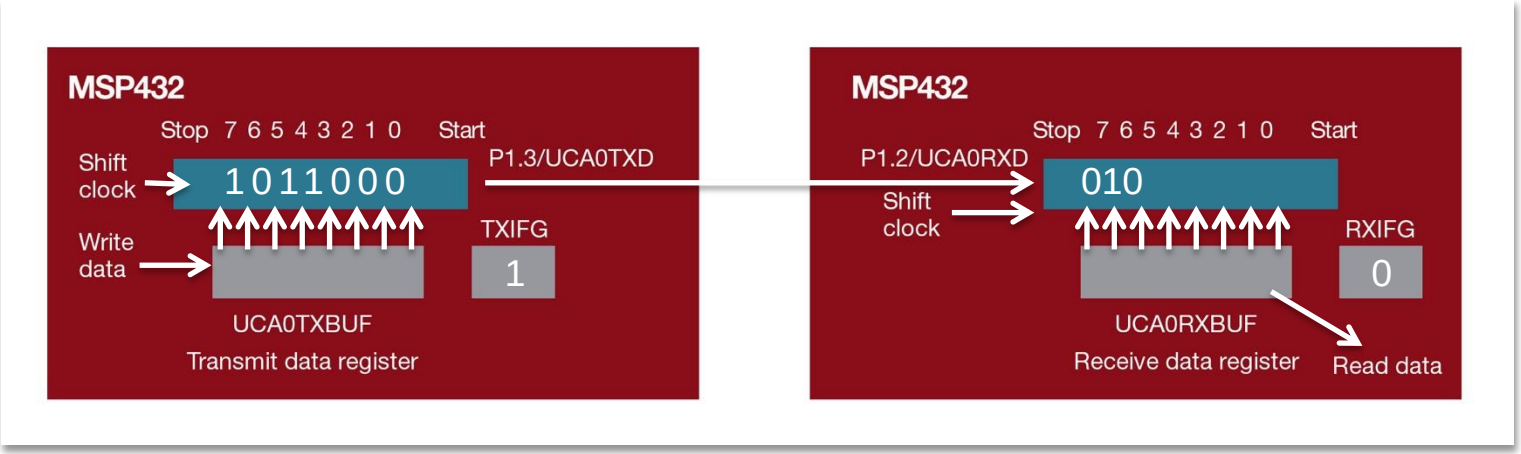
- Start bit shifted

UART - Communication



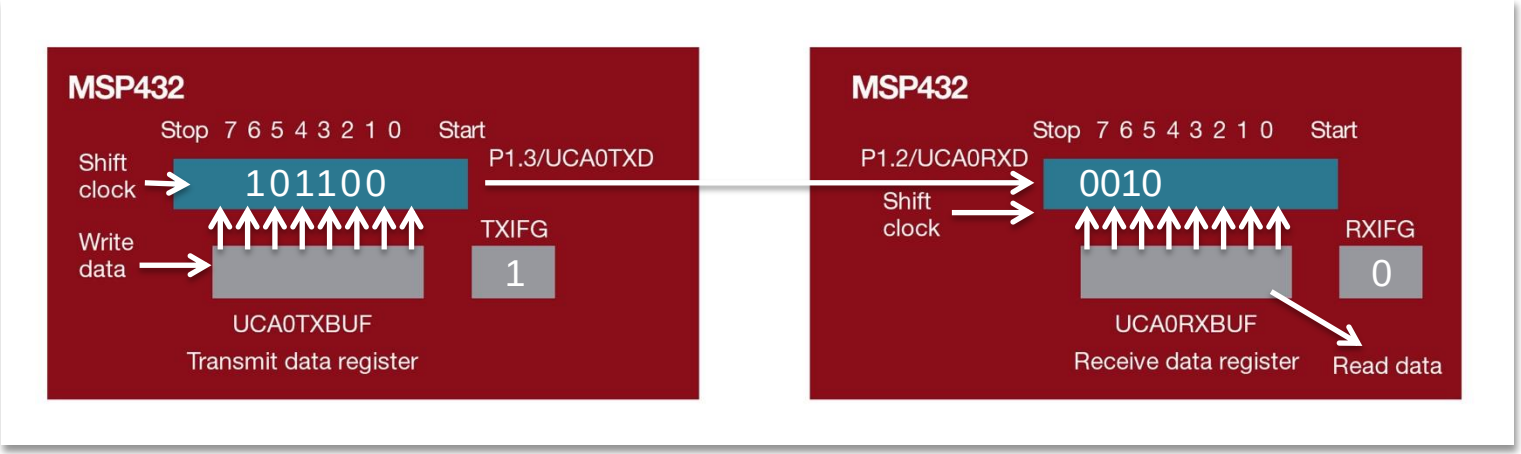
- Data bit 0 shifted

UART - Communication



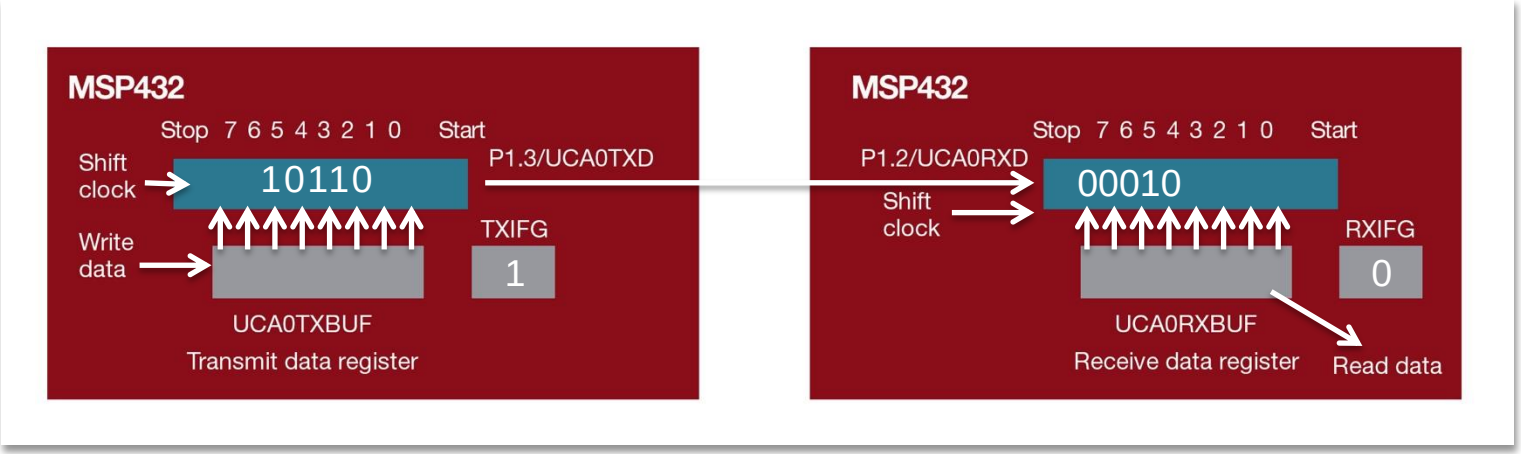
- Data bit 1 shifted

UART - Communication



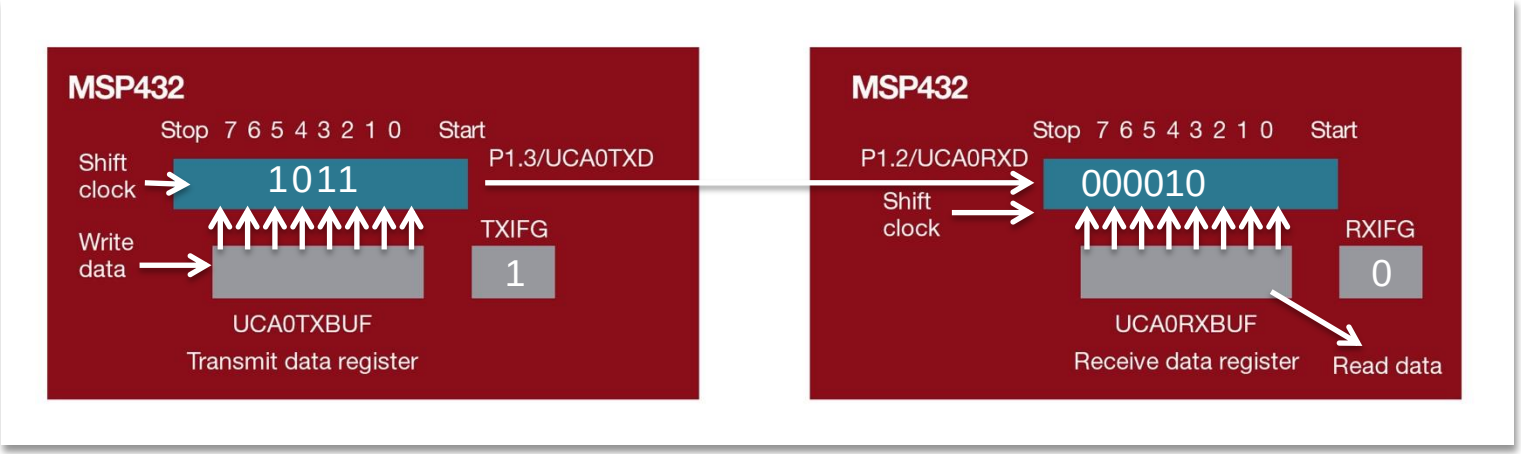
- Data bit 2 shifted

UART - Communication



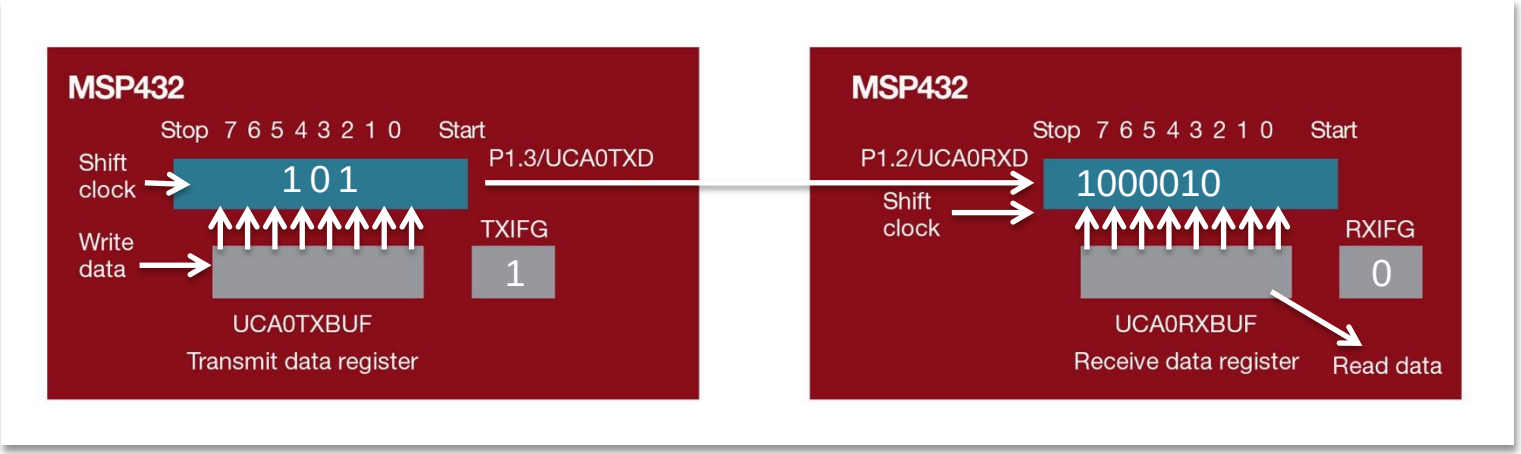
- Data bit 3 shifted

UART - Communication



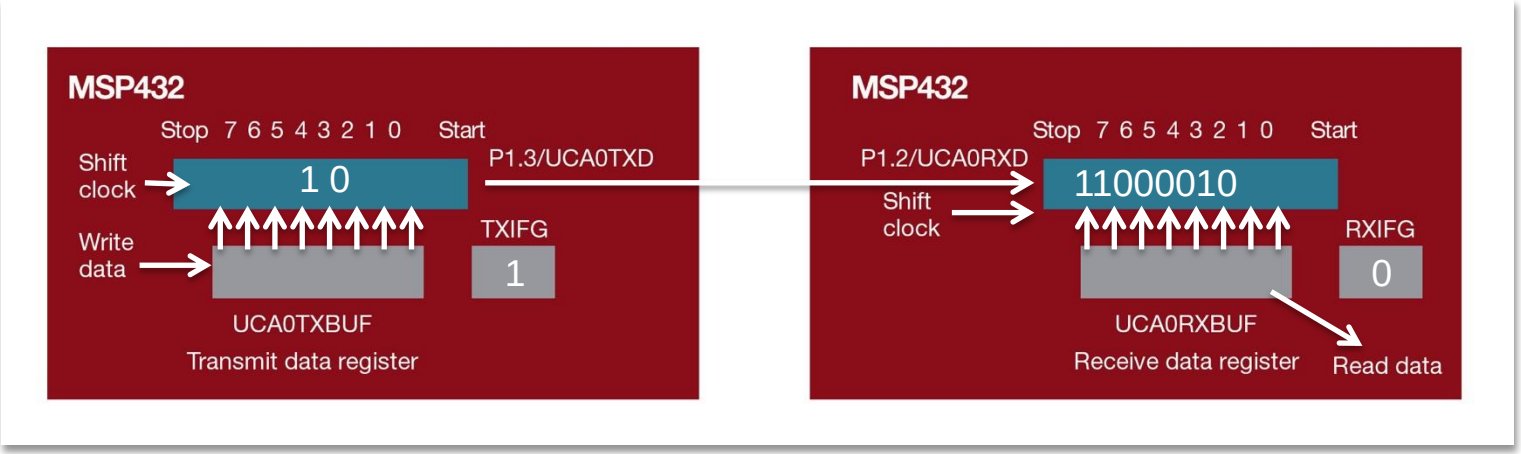
- Data bit 4 shifted

UART - Communication



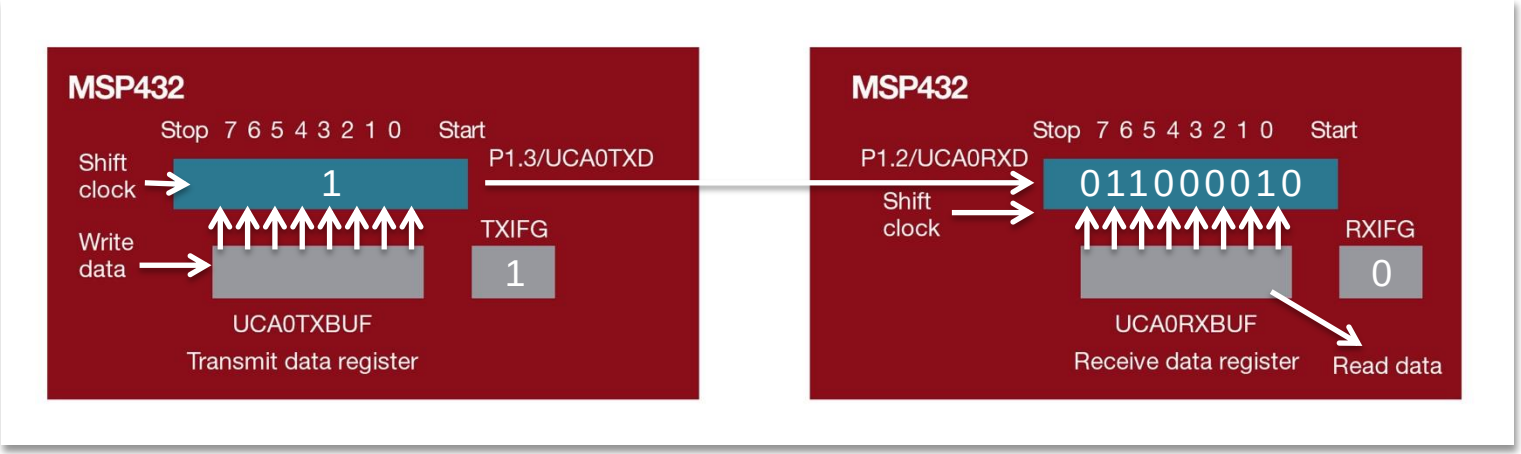
- Data bit 5 shifted

UART - Communication



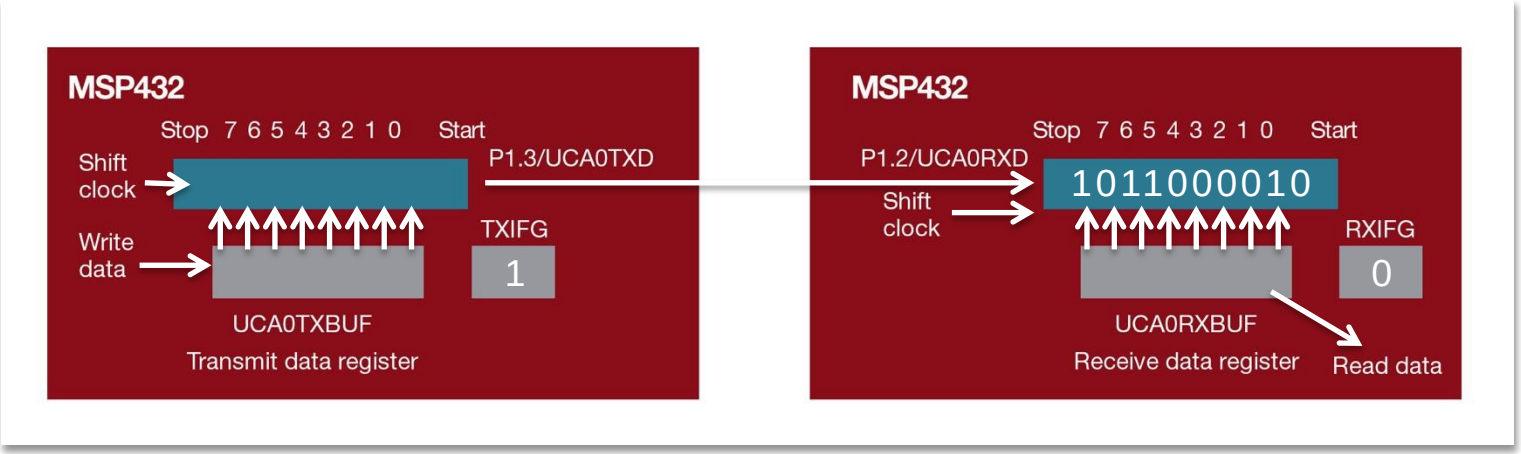
- Data bit 6 shifted

UART - Communication



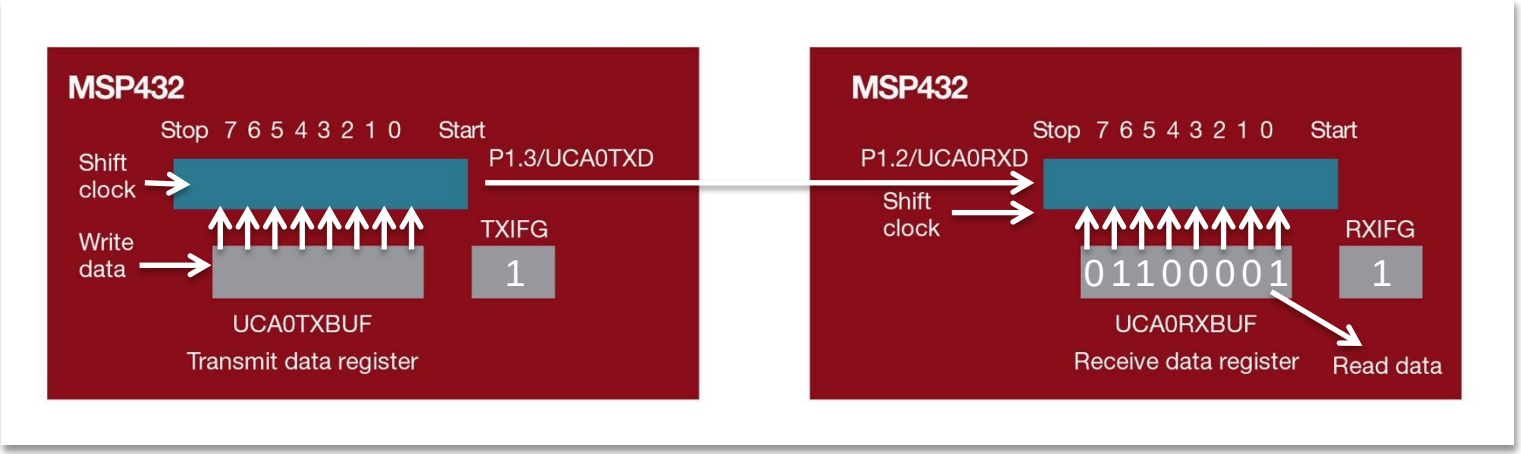
- Data bit 7 shifted

UART - Communication



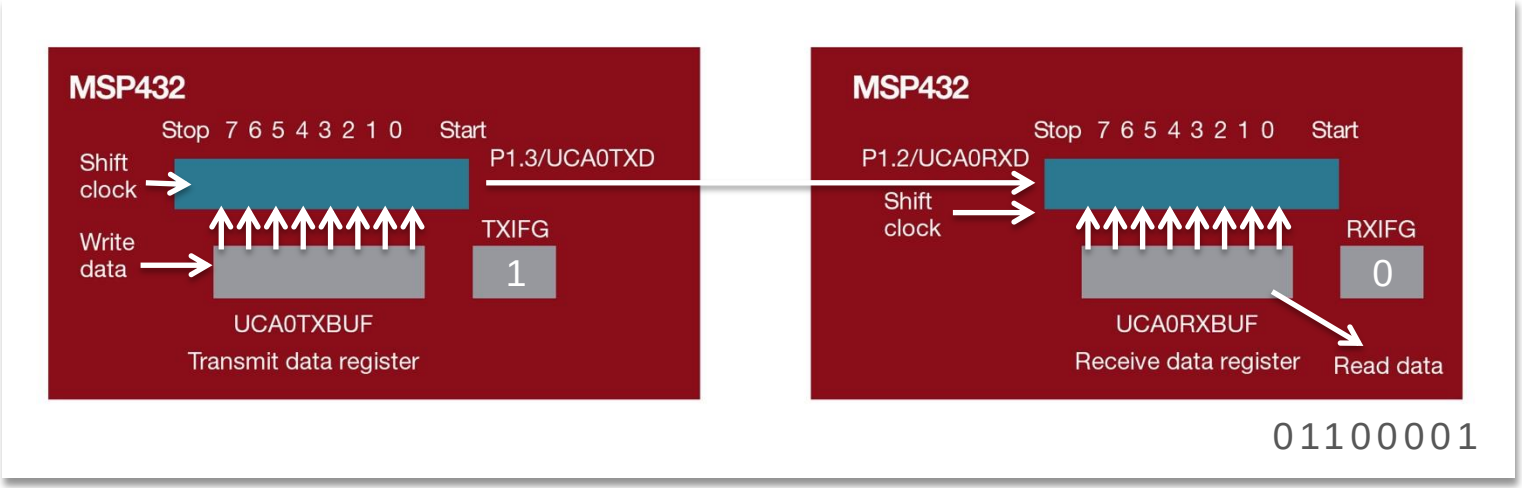
- Stop bit shifted

UART - Communication



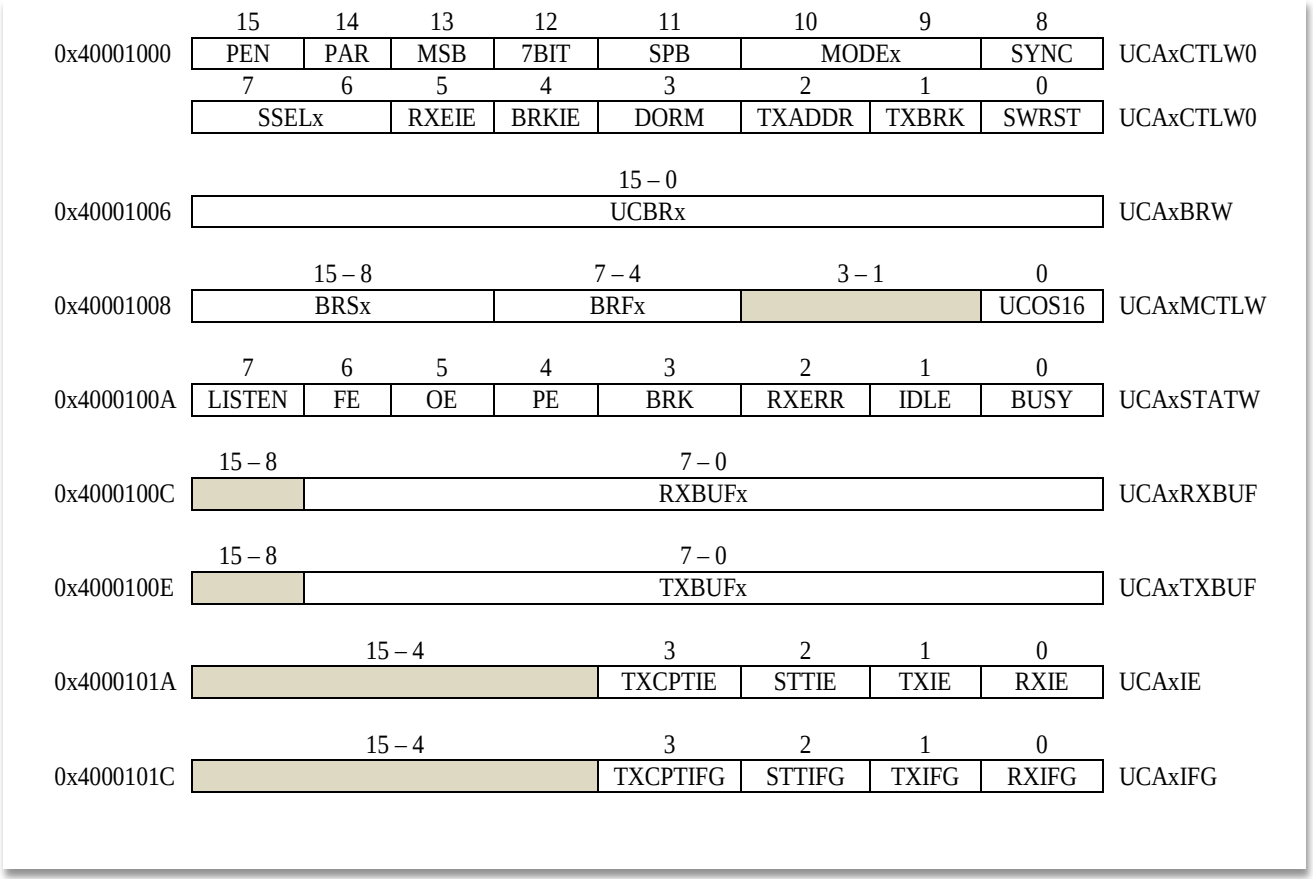
- Start bit and stop bit checked
- Data is moved from shift register to RXBUF
- RXIFG in receiver becomes 1

UART - Communication

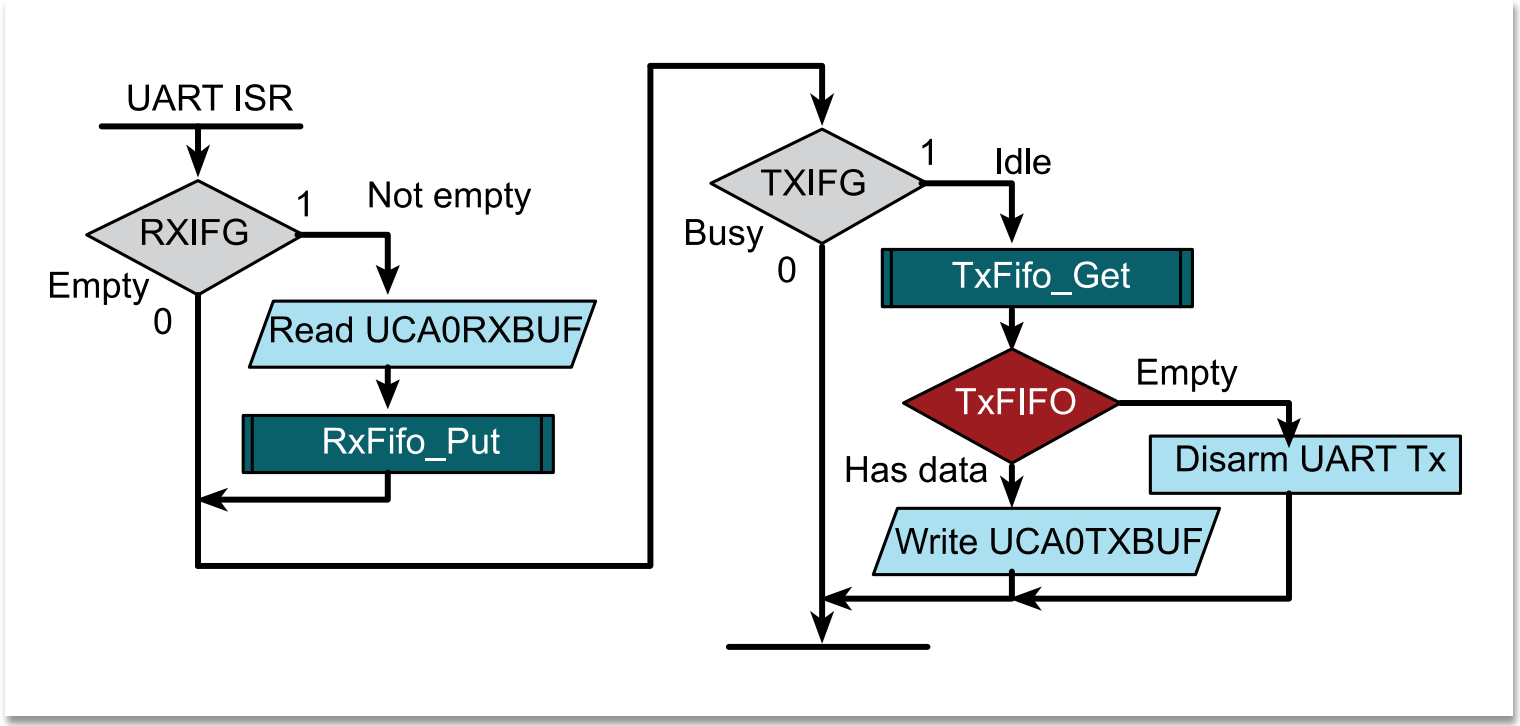


- Receiver reads from UCA0RXBUF (‘a’ = 0x61 = 01100001)
- RXIFG in transmitter becomes 0

UART Registers



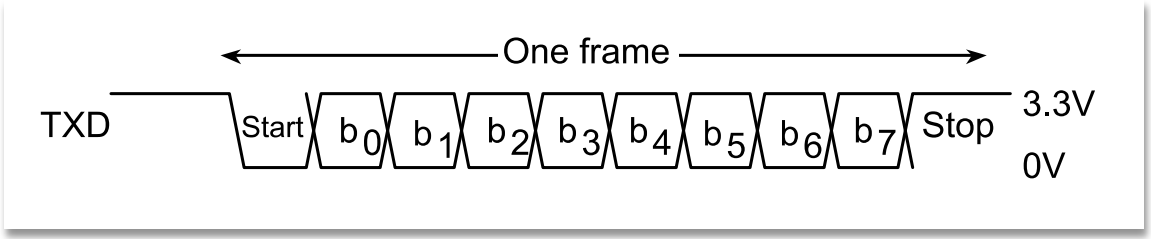
FIFO Usage


UART ISR
RXIFG
1
Not empty
Empty
0
Read UCA0RXBUF
RxFifo_Put
TXIFG
1
Idle
Busy
0
TxFifo_Get
TxFIFO
Empty
Disarm UART Tx
Has data
Write UCA0TXBUF

Summary

Serial Communication

- One bit at a time
- Asynchronous
- Interrupt-driven
- Baud rate
- Bandwidth



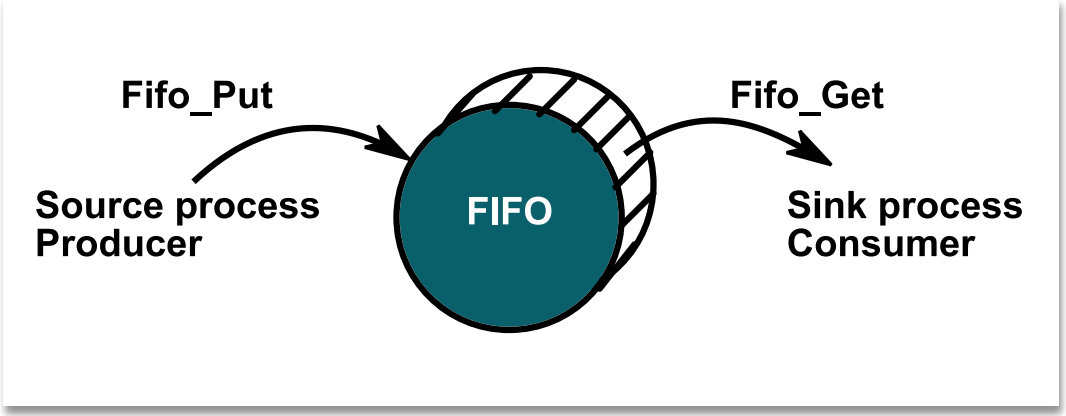
Module 18

Lecture: Serial Communication - FIFO

Serial Communication

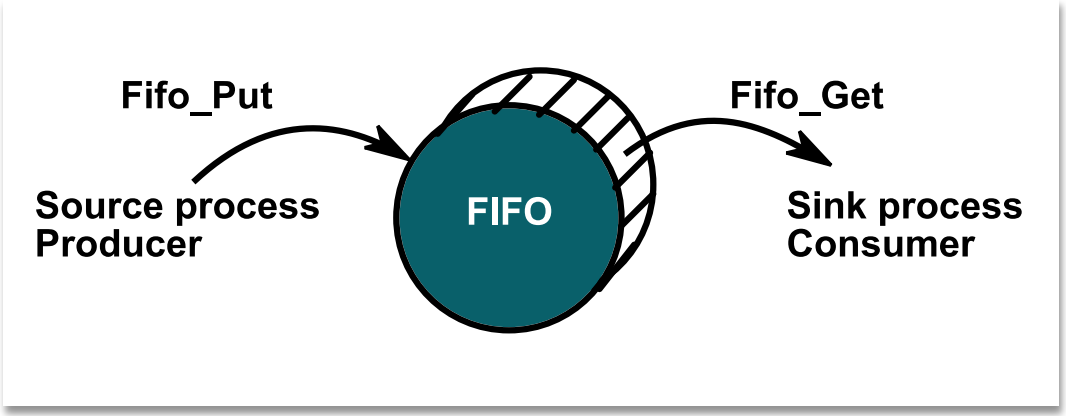
You will learn in this module

- FIFO Queues
  - Buffered I/O
  - Little's Theorem
- Performance measures
  - Bandwidth
  - Response time



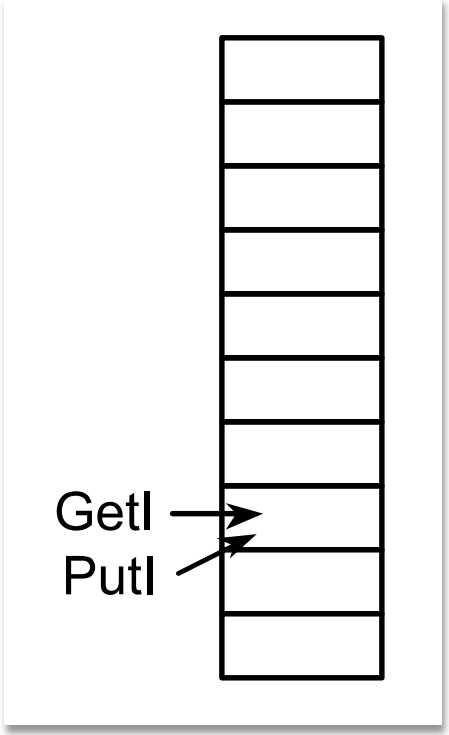
First In First Out (FIFO) Queue

- Order preserving
- Producer puts on tail end
- Consumer gets from head end
- Buffer decouples producer & consumer
  - Even out temporary mismatch in rates



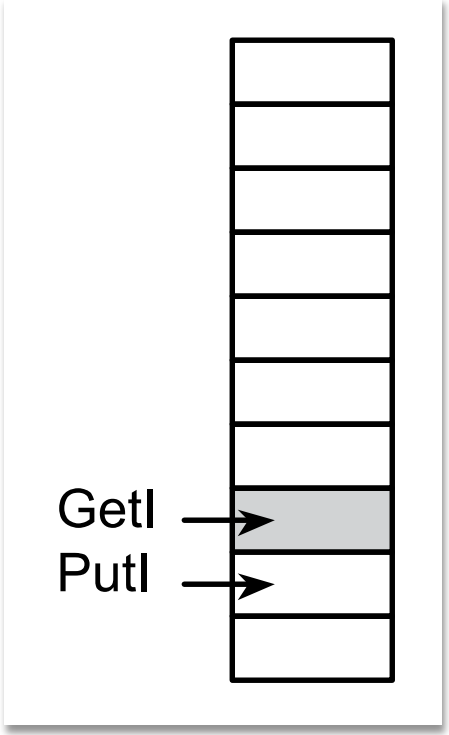
Empty FIFO

- GetI points to oldest
- PutI points to empty place
- This FIFO has 10 spaces
- It can hold up to 9 data



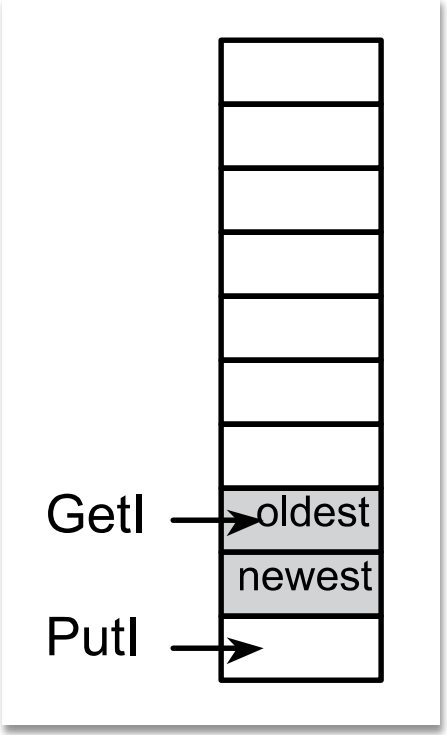
First Put

- Store at PutI
- Increment PutI



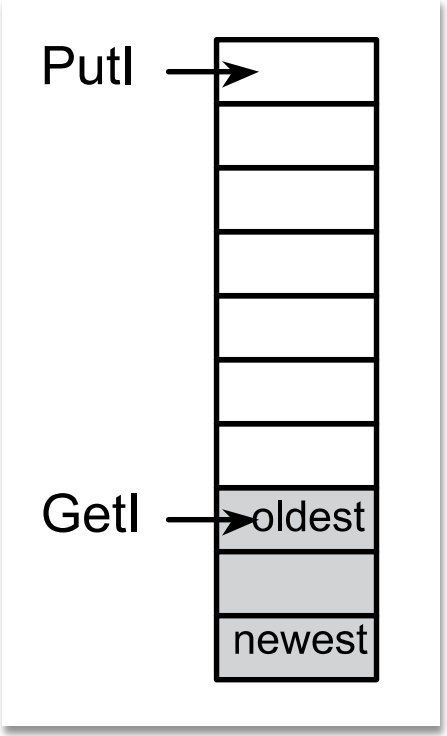
Second Put

- Store at PutI
- Increment PutI



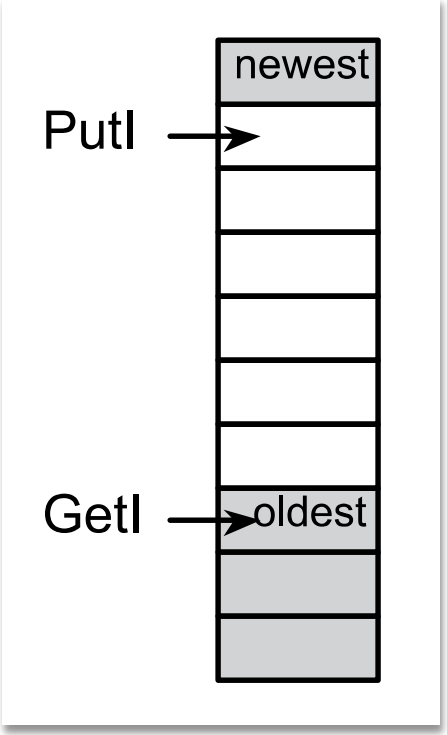
Third Put

- Store at PutI
- Increment PutI (wrap)



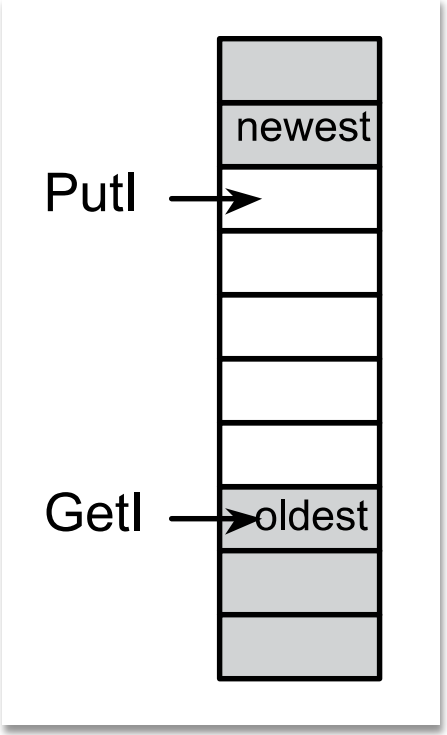
Fourth Put

- Store at PutI
- Increment PutI



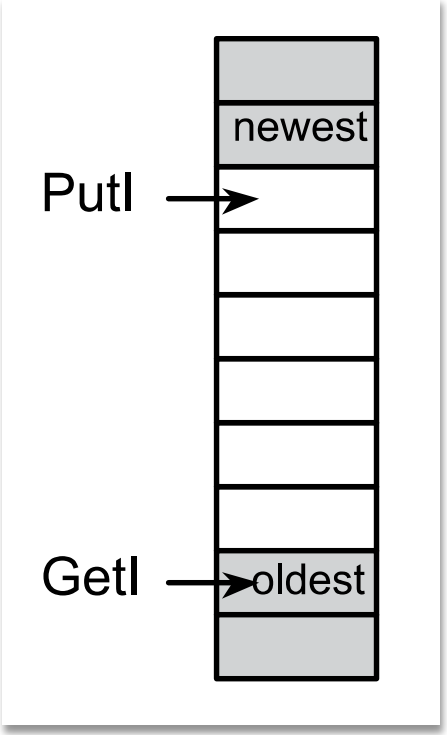
Fifth Put

- Store at PutI
- Increment PutI



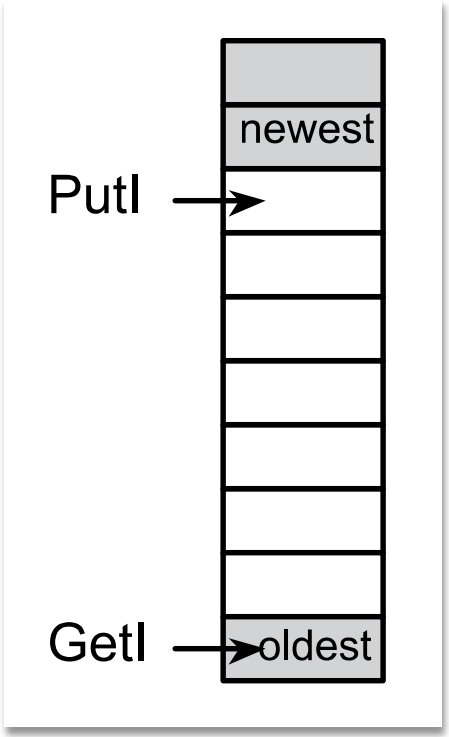
First Get

- Read from GetI
- Increment GetI



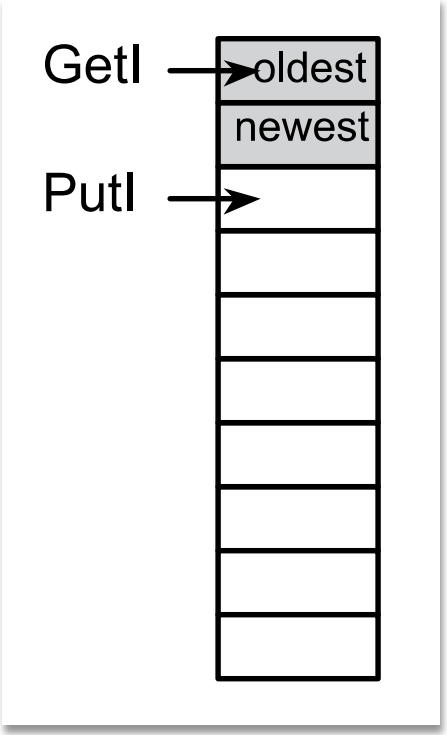
Second Get

- Read from GetI
- Increment GetI



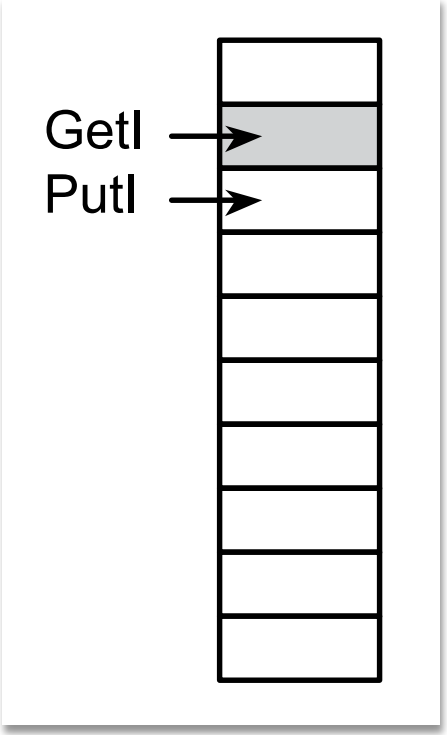
Third Get

- Read from GetI
- Increment GetI (wrap)



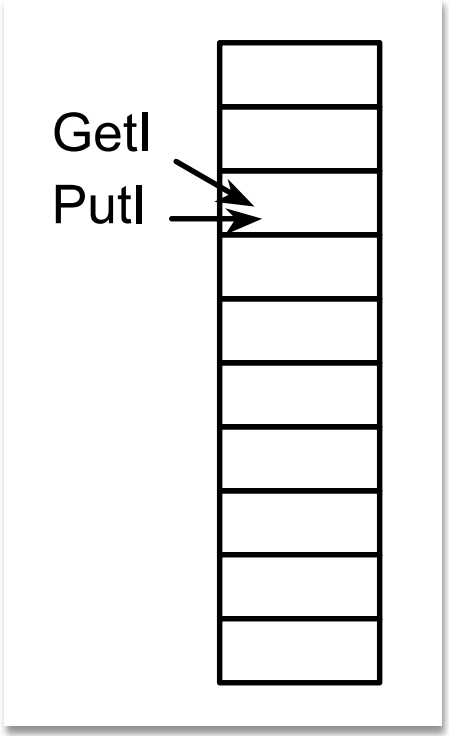
Fourth Get

- Read from GetI
- Increment GetI



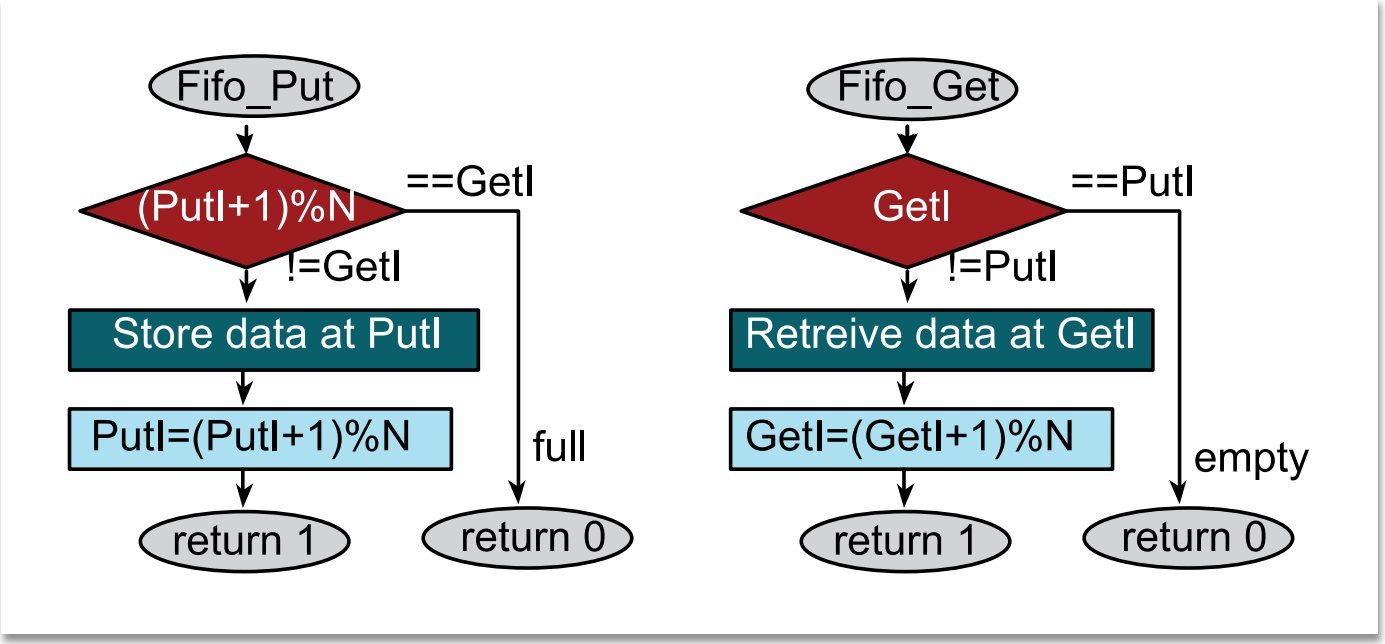
Fifth Get

- GetI points to data to get
- PutI points to place to put

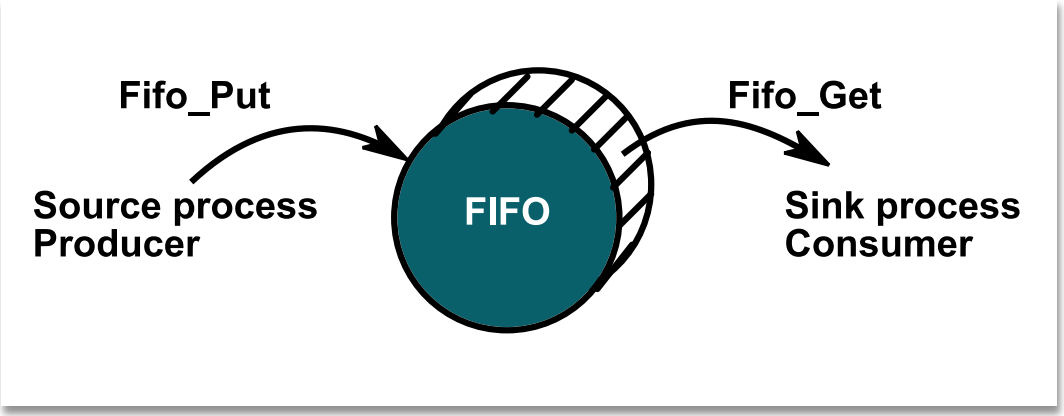


FIFO Implementation

- GetI points to data to get
- PutI points to place to put



Little's Theorem

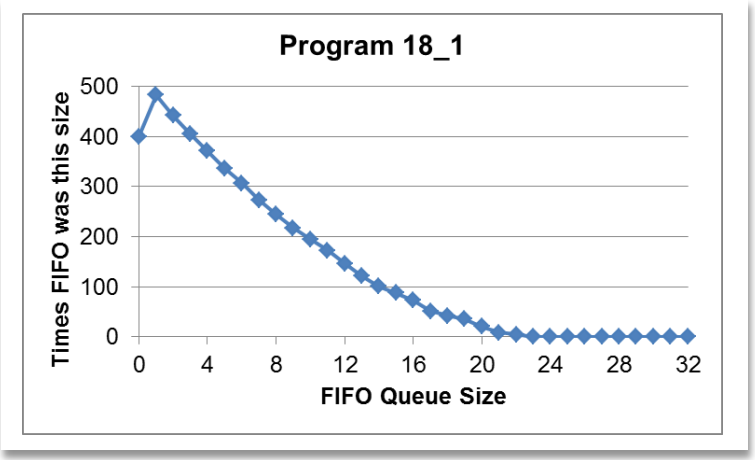


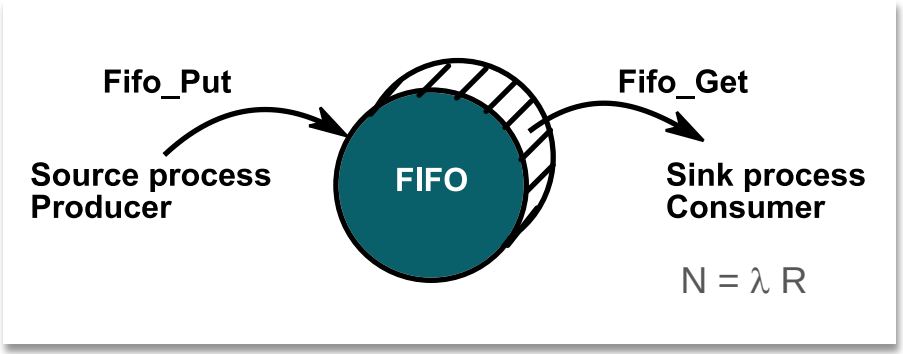
- N be the average number of data packets in the queue (plus 1)
- Let λ be the average arrival rate in packets per second (pps)
- Let R be the average response time of a packet
  - time waiting in the queue plus the
  - time for the consumer to process the packet
- Little's Theorem $N = \lambda R$

Summary

FIFO queue

- Data flow
- Order preserving
- Full error on put
- Empty error on get
- Little's Theorem





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