Fact Sheet

Military Semiconductor Products

SMJ320C3x SGYV004G December 2002

SMJ320C30 / 320C31 / 320LC31 / 320C32

HIGHLIGHTS

The SMJ320C30, C31, LC31, and C32 can perform parallel multiply and ALU operations on integer or floatingpoint data in a single cycle. Each processor also possesses a general-purpose register file, a program cache, dedicated auxiliary register arithmetic units (ARAU), internal dual-access memories, one DMA channel supporting concurrent I/O, and a short machine-cycle time. High performance and ease of use are results of these features.

An enhanced plastic processing option is available which provides the benefit of an enhanced qualification pedigree. For more information, go to http://www.ti.com/sc/ep

PERFORMANCE

- C31 40MHz, 40 MFLOPS, (GFA-141, HFG-132 packages, and KGD)
- LC31 40MHz, 40 MFLOPS, (PQ-132 plastic package, and KGD)

Minimum Clock Frequency is 1.65 MHz (606 ns)

PACKAGING

applicati GB (C30) — 181-pin (R _{0JA} = 2 GFA (C31) — 141-pin (Good Die is fully tested at temperature and speed, and specifically suited for MCM ons. KGD has the same reliability level as a tested and burned-in packaged part. Ceramic Pin Grid Array (cavity up). Weight: 17.97 grams. $6.6^{\circ}C/W$, $R_{\theta JC} = 1.1^{\circ}C/W$ Ceramic staggered Pin Grid Array (cavity up). Weight: 8.82 grams.
R _{θJA} = 3	9.0°C/W, $R_{\theta JC} = 4.3$ °C/W
, ,	Ceramic Quad Flat Pack, 25 mil lead spacing, cavity up, with a ceramic NCTB. 16.0 grams. $R_{\theta JA} = 28.9^{\circ}C/W, R_{\theta JC} = 1.3^{\circ}C/W$
, ,	Ceramic Quad Flat Pack, 25 mil lead spacing, cavity up, with a ceramic NCTB. 3.57 grams. $R_{\theta JA} = 44.3^{\circ}C/W, R_{\theta JC} = 2.1^{\circ}C/W$
PCM (C32) — 144-lead	plastic quad flat pack with 25-mil spacing.
•	5.63 grams. $R_{\theta JA} = 39^{\circ}C/W$, $R_{\theta JC} = 10.0^{\circ}C/W$ plastic quad flat pack with 25-mil spacing.
R _{0JA} Thermal linear fee	4.27 grams. $R_{\theta JA} = 49^{\circ}C/W$, $R_{\theta JC} = 11.0^{\circ}C/W$ resistance of a package without a path for heat dissipation. This is specified at a zero it per minute air flow. resistance of a package assuming an infinite path for heat dissipation.



DIE SIZE (Approximate)

' x 270 mils, die rev. 8.0, 0.65 micron †
x 270 mils, die rev. 8.0, 0.65 micron †
x 275 mils, die rev. 7.2, 0.65 micron †
x 275 mils, die rev. 7.2, 0.65 micron †
x 275 mils, die rev. 7.2, 0.72 micron ††
x 243 mils, die rev. 3.1, 0.65 micron †

TECHNOLOGY

† = 0.65 micron triple level metal EPIC GIZSSSE CMOS

tt = 0.7 micron triple level metal EPIC G1ZSE CMOS

PRODUCT RELEASES MATRIX

Device Name	Package	Speed	Voltage	DSCC SMD
SMJ320C30GBM40	181-pin CPGA	40 MHz	5 V	5962-9052604MXA
SMJ320C30GBM50	181-pin CPGA	50 MHz	5 V	5962-9052605MXA
SMJ320C30HFGM40	196-lead CQFP (NCTB)	40 MHz	5 V	5962-9052604MUA
SMJ320C30HFGM50	196-lead CQFP (NCTB)	50 MHz	5 V	5962-9052605MUA
SMJ320C31GFAM40	141-pin staggered CPGA	40 MHz	5 V	5962-9205803MXA
SMJ320C31GFAM50	141-pin staggered CPGA	50 MHz	5 V	5962-9205804MXA
SMJ320C31GFAS60	141-pin staggered CPGA	60 MHz	5 V	5962-9205805QXA
SMJ320C31HFGM40	132-lead CQFP (NCTB)	40 MHz	5 V	5962-9205803MYA
SMJ320C31HFGM50	132-lead CQFP (NCTB)	50 MHz	5 V	5962-9205804MYA
SMJ320C31HFGS60	132-lead CQFP (NCTB)	60 MHz	5 V	5962-9205805QYA
SM320LC31PQM40EP	132-lead PQFP	40 MHz	3.3 V	N/A
SMQ320LC31PQM40	QM40 132-lead plastic QFP		3.3 V	Order as 5962-9760601NXB
SMQ320C32PCMM50	144-lead plastic QFP	50 MHz	5 V	Order as 5962-9679001NXB
SMQ320C32PCMM60	SMQ320C32PCMM60 144-lead plastic QFP		5 V	Order as 5962-9679002NXB
SM320C32PCMM50EP	320C32PCMM50EP 144-pin PQFP		5 V	N/A
SM320C32PCMM60EP	144-pin PQFP	60 MHz	5 V	N/A

ROM CODE

The 320C30 on-chip ROM is mask programmable. The user's code must be inserted into the wafer fabrication process. There is a minimum order and NRE requirement. The following flow outlines the required steps:

1. Customer submits code via a new code release form.

- 2. TI loads into system, inserts testability code.
- 3. Customer verifies translation in writing.
- 4. TI creates mask.
- 5. Wafer lot is processed using mask.
- 6. TI builds prototypes.
- 7. Customer verifies prototypes in writing.
- 8. Production lot is started.



POWER DISSIPATION

	<u>C30-40</u>	<u>C30-50</u>	<u>C31-40</u>	<u>C31-50</u>	<u>C31-60</u>	LC31-40	<u>C32-50</u>	<u>C32-60</u>
Typical ICC:	175 mA	200 mA	160 mA	200 mA	225 mA	150 mA	200 mA	225 mA
Maximum ICC	: 600 mA	600 mA	400 mA	425 mA	675 mA	300 mA	425 mA	475 mA
Typical Pwr	1.0 W	1.1 W	0.8 W	1.0 W	1.0 W	0.5 W	1.0 W	1.0 W

All measurements at 25°C

Reference: "Calculation of TMS320C30 Power Dissipation Application Report"- Literature No. SPRA020

Explanation of Typical vs. Peak power :

For average power and thermal management considerations, the typical value should be used. The peak power of the 'C30 is highly dependent on the instructions executing. The worst case pattern set occurs when checkerboard patterns are being loaded out both ports from both RAM blocks. The next highest pattern sets show 340mA, 275, 240, ...

TEST VECTORS

The SMJ320C3X has >500,000 test vectors. The actual test vectors are TI proprietary information.

TOOLS SUPPORT

Part Number	Description
TMDS3240130PC	Code Composer is the DSP industry's first fully integrated development environment (IDE) with DSP-specific functionality. With its familiar MS-Visual C++ like environment, Code Composer lets you edit, build, debug, profile and manage projects from a single unified environment. Other unique features include graphical signal analysis, injection/extraction of data signals via file I/O, multi-processor debugging, automated testing and customization via a C- interpretive scripting language and much more. OS requirements = Windows / PC.
C3X-ADA-XX	Translates Ada source code into 320C3X assembly source code. OS requirements = UNIX & VMS Call (800) 477-8924, Ext. 5801
TDMS3243850-02	C3X/C4X PC Assembler/Linker—The assembler.converts assembly language to machine language. The linker combines object modules into a single executable object file, performs relocation and resolves external references. OS = Windows
TMDS3243855-02	C Compiler/Assembler/Linker—Translates C source code into 320C3X assembly source code and performs assembler/linker functions. OS = MS-DOS
TMDS324355508	C3X/4X UNIX C Compiler/Assembler/Linker. OS = UNIX
TMDS324063	UNIX OS Software debugger tool that simulates the operation of the 320C3 X. Note: For Windows- based systems, the debugger function is provided in the Code Composer IDE.
TMDS3243551-09	SunOS/OpenWin C3X UNIX Simulator. Note: For Windows-based systems, the simulator function is provided in the Code Composer IDE.
TMDS00510M	XDS5103X PC—The TMS320 Extended Development Systems (XDSs) are powerful, full-speed emulators used for system-level integration and debug. TI provides the world's first in-system scan- based emulators. OS = Windows
TMDS0051WSM	XDS5103X WS—The TMS320 Extended Development Systems (XDSs) are powerful, full-speed emulators used for system-level integration and debug. TI provides the world's first in-system scan- based emulators. OS = UNIX
TMDS3260030	Evaluation Module—This package includes the TMS320C3X assembler/linker and the C source debugger. A TMS320C30 PC halfcard is also included in this low-cost, rich development environment. OS = Windows
TMS3200031	DSP Starter Kit (DSK). The C3X DSK is a low-cost, simple, high-performance standalone application development board that lets you experiment with and use TMS320C3X DSPs for real-time signal processing. OS = Windows



KGD

Known Good Die (KGD) products are offered for use in Multichip Modules and Chip on Board (COB) applications. The current technology employed for KGD assurance is Hot Chuck Probe (HCP). This is an at-temperature and at-speed electrical test probe that will fulfill all testing requirements needed to assure the same quality and reliability as a packaged part.

- Offered for both the commercial or military temperature range.
- Very Dense form factor available.

ARCHITECTURE

The SMJ320C3X uses a highly parallel, pipelined architecture. This is Von Neumann externally (simplifying the programmer's task) but Harvard internally (faster execution). These features are transparent to the user.

INTERNAL MEMORY	Two blocks of 1Kx32 dual access RAM. Each block can provide two accesses to the CPU or the DMA every cycle. A reserved block of dual access ROM (4Kx32). This is mask programmable. See ROM code guidelines.
CACHE	Two segments of 32 words each. Operates on the standard least-recently-used algorithm using a serial load.
DMA	On-chip concurrent direct memory access controller. Cycle steals from the CPU to off load I/O tasks from the CPU.

DESIGN-IN SUPPORT <u>TI has the most extensive DSP application support</u>

Product Information Center:	(972) 644-5580 (For general information, availability, etc.)
DSP Developer's Village:	http://dspvillage.ti.com/docs/dspvillagehome.jhtml
DSP Knowledgebase:	http://www.ti.com/sc/docs/dsps/hotline/support.htm
Third Parties URL:	http://www.ti.com/sc/docs/general/dsp/third/index.htm
Military C3x DSP Info:	http://www.ti.com/sc/docs/products/military/processr/320c3x.htm

Product Information Center

North America

Telephone # - 972-644-5580 (English) Fax # - 972-480-7800 PIC – <u>http://www.ti.com/sc/docs/pic/home.htm</u> PIC E-mail - sc-infomaster@ti.com Military Products – <u>http://www.ti.com/sc/military</u>

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