Fact Sheet

Military Semiconductor Products

SMJ320C6201B / 5962-9857801QXA

SGYV045O April 2002

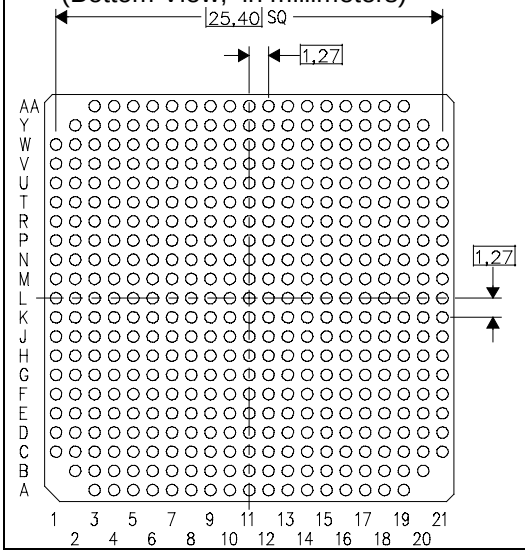
1200 - 1600 MIPS Fixed-Point DSP (Digital Signal Processor)

HIGHLIGHTS

- The SMJ320C6201B is the highest performance military programmable DSP; achieving 1200 MIPS (Million Fixed-Point Instructions Per Second) at 150 MHz operation over the extended temperature range of -55°C to +115°C. TI released the SM320C6201B achieving 1600 MIPS at 200 MHz over the extended temperature range of -40°C to +90°C. Both devices are offered in a 27 x 27 mm Ceramic Dimpled Ball Grid Array.

- 1.8-V Advanced VLIW CPU Core:
  - ⇒ 8 Highly Independent Functional Units:
    6 ALUs (32- / 40-bit); 2 16-bit Multipliers (32-bit Result)
  - ⇒ Load-Store Architecture:
    There are 32 32-bit General Purpose Registers.
  - ⇒ All Instructions can be conditional.

- 3.3-V Peripherals on the chip:
  - ⇒ 1 M-bit SRAM On Chip (½ M Dual Access Data RAM, ½ M Internal Program RAM/Cache)
  - ⇒ 32-bit External Memory Interface (EMIF), glueless to SDRAM, SBSRAM, SRAM, EPROM
  - ⇒ 4 Channel DMA, Bootloading Direct Memory Access Controller with an Auxiliary Channel
  - ⇒ 2 Multi-Channel Buffered Serial Ports (McBSPs)
  - ⇒ 2 32-bit General Purpose Timers
  - ⇒ 16-bit Flexible Host Port Interface (HPI)
  - ⇒ IEEE-1149.1 (JTAG) Boundary Scan Compatible

Package:	Details:
429-Ceramic Ball Grid Array (BGA) package (Bottom View, in millimeters) 	27 x 27 mm package outline This package requires less board area (a 40% area savings over a plastic 35 x 35 mm package). Ultra thin package (130 mils, 3.3 mm) supports military trend for higher integration and minimizing board space. 1.27 mm pitch on 46% Sn, 46% Pb, 8% Bi Solderballs Many peripheral solderballs will be no-connects and redundant V_{DD} and GNDs. These extra solder balls add additional package-to-board reliability. Better thermal characteristics than most of the packages available on the market. Lower package cost passed on to customer.

TEXAS INSTRUMENTS

KEY FEATURES/BENEFITS

Key features:	Benefits:
Advanced VLIW CPU with eight functional units including two multipliers and six arithmetic units	Up to 10 times the performance of typical DSPs. Allows designers to develop highly effective RISC-like code for fast development time.
Instruction packing (Write your code in a single thread, the compiler can turn it into parallel code.)	Code size equivalence for eight instructions executed serially or in parallel. Reduces code size, program fetches and power consumption.
100 percent conditional instructions	Reduces costly branching. Increases parallelism for higher sustained performance.
Code executes as programmed on highly independent functional units	Benchmark suite and DSP industry's first assembly optimizer for fast development time.
8/16/32-bit data support	Efficient memory support for a variety of applications.
40-bit arithmetic options	Extra precision for vocoders and other computationally intensive applications.
Saturation and normalization	Supports key arithmetic operations.
Bit-field manipulation and instruction: extract, set, clear, bit counting	Supports common operations found in control and data manipulation applications.
1 M-bit on-chip memory (512K bits program, 512K bits data)	Fast algorithm execution with fewer components per system.
32-bit glueless external memory interface supports SDRAM, SBSRAM and SRAM	High speed connections to external memory for maximum sustained performance.
Two Multi-channel Buffered Serial Ports (McBSPs)	Glueless interface to high bandwidth telecommunications trunks. Provides high speed interprocessor communication.
16-bit host access port	Host processor access to all memory (internal data memory, internal program memory, external memory).
Four data memory access (DMA) channels with bootloading capability	Efficient access to external memory/peripherals while minimizing CPU interrupts.
Flexible Phase-Locked-Loop (PLL) clock generator	Multiplies external clock rate by one or four for maximum CPU performance.

DESIGN-IN SUPPORT

TI has the most extensive DSP application support

Product Information Center:	(972) 644-5580 (For general information, availability, etc.)
DSP Developer's Village	http://dspvillage.ti.com/docs/dspvillagehome.jhtml
DSP Hotline (Technical questions)	http://www.ti.com/sc/docs/dsps/hotline/support.htm
Third Parties URL	http://www.ti.com/sc/docs/general/dsp/third/index.htm
Military C6x DSP Info	http://www.ti.com/sc/docs/products/military/processr/320c6201.htm
Ada Compiler	http://www.irvine.com

TECHNOLOGY

5-level metal CMOS Process; ESD level = Category III (> 4,000 V to 3,999 V)
0.18-µ silicon, 150/200 MHz Operation, 1.8-V CPU Core Voltage
3.3-V Peripherals, All I/Os, memory I/F, etc.

TEXAS INSTRUMENTS

DIE SIZE

386 x 386 mils for 0.18-µm PG3.x silicon.

PACKAGING

GLP 429 Ball C-DBGA (Ceramic - Dimple Ball Grid Array). A cavity up C-DBGA weighs 6.3 g.

The following table and notes define the typical thermal characteristics for the ceramic GLP package. This data is useful for preliminary engineering evaluations.

PARAMETER	TYP	UNIT
$R_{\theta JA}$	14.47	°C/W
$R_{\theta JMA}$ (airflow@150 fpm)	11.79	°C/W
$R_{\theta JMA}$ (airflow@250 fpm)	11.09	°C/W
$R_{\theta JMA}$ (airflow@500 fpm)	10.21	°C/W
$R_{\theta JC}$ /1	7.34	°C/W
$R_{\theta JC}$ /2	3.00	°C/W
$R_{\theta JB}$	6.20	°C/W

Typical GLP Package Thermal Characteristics

Notes:

$R_{\theta JA}$	Junction-to-ambient air thermal resistance: measured in a one cubic foot, still air enclosure.
$R_{\theta JMA}$	Junction-to-moving air thermal resistance: measured in a wind tunnel.
$R_{\theta JC}$ /1	Junction-to-case thermal resistance: measured to the top of the package lid.
$R_{\theta JC}$ /2	Junction-to-case thermal resistance: measured to the bottom of solder ball.
$R_{\theta JB}$	Junction-to-board thermal resistance: measured by soldering a thermocouple to one of the middle traces on the board at the edge of the package.

The above values were obtained by mounting the 429-GLP on a FR-4 board and testing per JESD-51-7, High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages. The board design connected all the GND balls directly to a GND plane, V_{DD} balls to a V_{DD} plane, and all the signals were routed on the top layer.

Key features of the thermal test board design are:

- Board material: FR-4
- Board design: 2S2P (double layer, double buried power plane)
- Board thickness: 0.062 +/- 0.006 inches
- Board dimensions: 4.0 x 4.5 inches
- Trace thickness: 0.0028 inches
- Traces: 2 oz +/- 20% copper for signals and 1 oz +/- 10% copper for V_{DD} and GND planes

POWER DISSIPATION

Typical:	~1.3 W	0.18-µm silicon @ 150 MHz (Available Now)
Maximum:	~1.9 W	0.18-µm silicon @ 200 MHz estimated (Available Now)

PROCESS/PERFORMANCE OPTIONS

Device	Package	Speed	DSCC SMD	Processing
SN00372GLG Available Now	372-ball C-BGA	n/a	n/a	CBGA Daisy-Chain Package Prototype
SM320C6201BGLPW15 Available Now	429-ball C-BGA	150 MHz	n/a	-55°C to +115°C
SMJ320C6201BGLPW15 Available Now	429-ball C-BGA	150 MHz	5962-9857801QXA	-55°C to +115°C Full Military, QML Processing
SM320C6201BGLPS20 Available Now	429-ball C-BGA	200 MHz	n/a	-40°C to +90°C

TEST VECTORS

The SM320C6201B's ~2,000,000 test vectors are TI proprietary information.

NOMENCLATURE

SMJ **320** **C6201B** **GLP** **W** **15**

SMJ = QML Process
SM = Commercial Process

DSP Family

Device

Package: GLP = Ceramic Ball Grid Array

W = Extended (-55°C -115°C)
S = Special, Per Datasheet

Speed: 15 = 150 MHz
20 = 200 MHz

TOOLS SUPPORT

A complete suite of C62x™ / C67x™ tools--just what programmers want!

Available Today:

- **C Compiler / Assembler / World's First Assembly Optimizer / and Linker:**
  -- TMDS3246855-07 for PC Win'95 and Win/NT
  -- TMDS3246555-07 for SPARC SunOS, Solaris
- **Software Simulator with Software Debugger:**
  -- TMDX3246851-07 for PC Win'95 and Win/NT
  -- TMDX3246551-07 for SPARC SunOS, Solaris & HP-UX
- **C Source Debugger with Emulation S/W for Hardware Debug/Emulation:**
  -- TMDX3240160-07 for PC Win'95 and Win/NT
  -- TMDX324066X-07 for SPARC SPARC-SunOS
- **IDE,** fully **Integrated Development Environment** from GO-DSP: **Available Today**
  Code Composer Studio™ is the DSP industry's first fully integrated development environment (IDE) with DSP-functionality. With its familiar MS-Visual C++ like environment, Code Composer lets you edit, build, debug, profile and manage projects from a single unified environment. Other unique features include graphical signal analysis, injection/extraction of data signals via file I/O, multi-processor debugging, automated testing and customization via a C-interpretive scripting language and much more. See http://dspvillage.ti.com/
- **Hardware Emulator Controller Kit:**
  -- TMDS00510 Emulator controller kit for PC
  -- TMDS00510WS Emulator controller kit for SPARC workstation
  The TMS320 family XDS-510 emulator is a user-friendly, PC-based development system which has all features necessary to perform full-speed, in circuit emulation with the TMS320C6000™.
- **Evaluation Module (EVM) Board:** A low-cost PCI interfaced PC board which includes a C6201B, SBSRAM, SDRAM, etc. It is well-suited for software algorithm development.

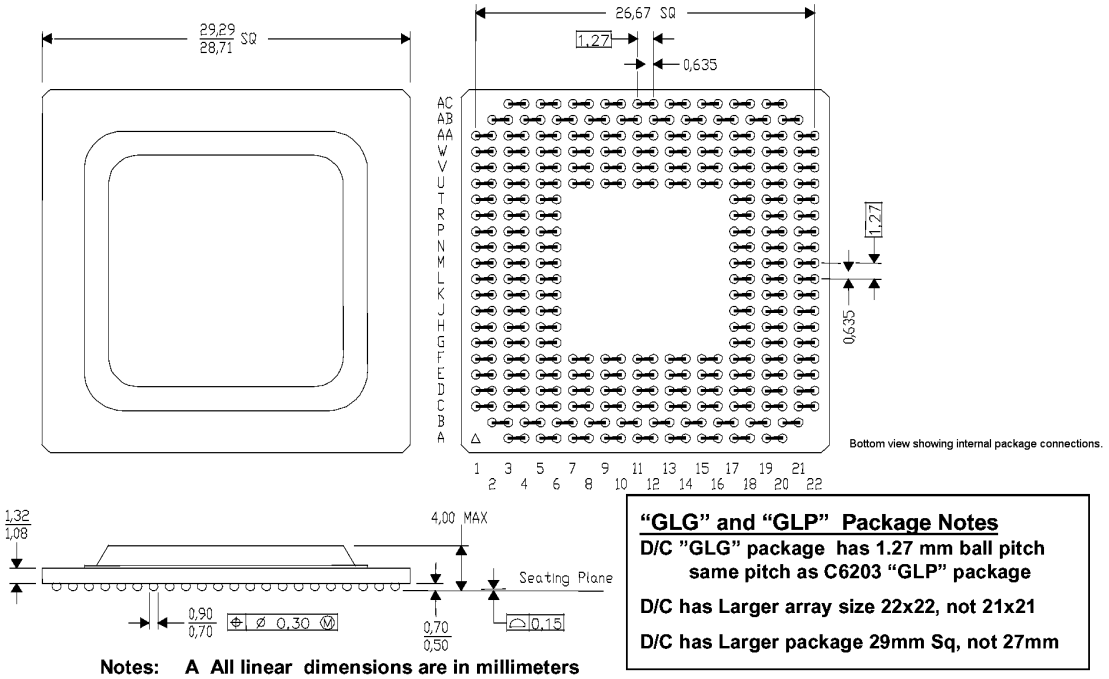
Literature Information		**Size:**	**Literature #**
Datasheet: http://www-s.ti.com/sc/psheets/sgus028a/sgus028a.pdf		(1093 KBytes)	SGUS028
User Guides / User Manuals:			
TMS320C6000	SOFTWARE TOOLS GETTING STARTED GUIDE	(364 KBytes)	SPRU185
TMS320C6000	ASSEMBLY LANGUAGE TOOLS USER'S GUIDE	(1929 KBytes)	SPRU186
TMS320C6000	OPTIMIZING C COMPILER USER'S GUIDE	(1042 KBytes)	SPRU187
TMS320C6000	C SOURCE DEBUGGER	(1322 KBytes)	SPRU188
TMS320C62X/67X	CPU AND INSTRUCTION SET REFERENCE GUIDE	(1034 KBytes)	SPRU189
TMS320C62X	PERIPHERALS REFERENCE GUIDE	(816 KBytes)	SPRU190
TMS320C62X	TECHNICAL BRIEF	(252 KBytes)	SPRU197
TMS320C62X/67X	PROGRAMMER'S GUIDE	(1157 KBytes)	SPRU198
TMS320C6000	ADDENDUM TO TMS320 DSP DEV. SPT. REF. GUIDE	(129 Kbytes)	SPRU226

TEXAS INSTRUMENTS

Daisy Chain packages are used to evaluate/measure the package to board assembly process. They allow designers to verify the reliability of the package-to-board interface over temp cycles, shocks, aging, etc.

Daisy Chain CBGA (p/n=SN00372GLG)

for Ceramic-BGA to board Evaluation only



"GLG" and "GLP" Package Notes

D/C "GLG" package has 1.27 mm ball pitch same pitch as C6203 "GLP" package

D/C has Larger array size 22x22, not 21x21

D/C has Larger package 29mm Sq, not 27mm

Notes: A All linear dimensions are in millimeters
B. This drawing is subject to change without notice

Use of Daisy Chain

- **Internal to the D/C package, each Solderball is connected to one adjacent**
  Pattern: o-o o-o o-o o-o o-o o-o

- **The balls are linked to each other by a similar pattern on the D/C PCB evaluation board, thus forming one long chain connecting every solderball on the package. (PCB can also connect D/C package chain to another pkg.)**

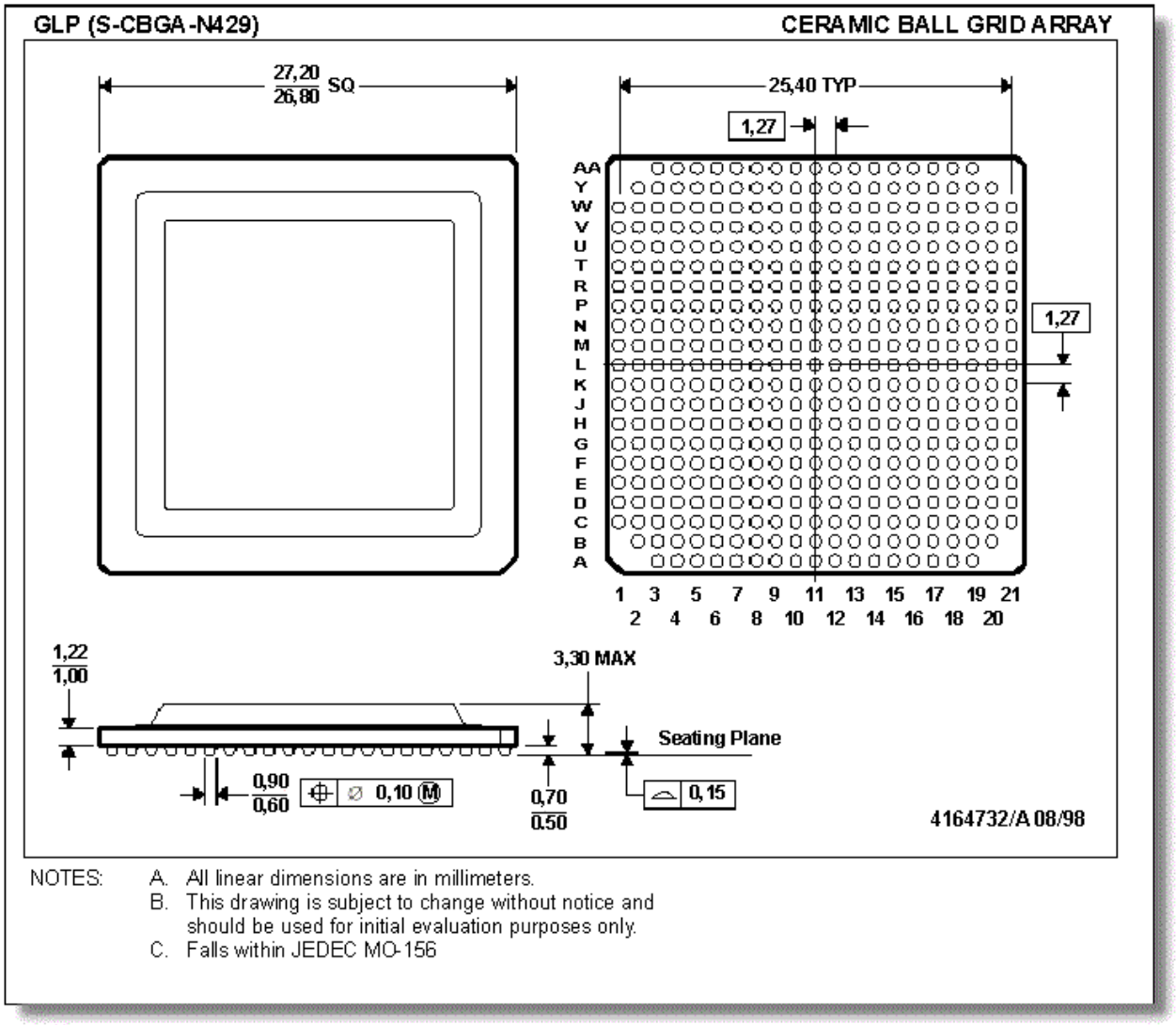
```
D/C Package Pattern:   o-o o-o o-o o-o o-o o-o
PCB Board Pattern:     o o=o o=o o=o o=o o=o o

Resulting Pattern:     o-o=o-o=o-o=o-o=o-o=o-o=o-o
                         (One long Chain)
```

- **Now, we can measure or monitor the <u>continuity</u> and <u>resistance</u> of all the D/C packages on an entire PCB (Every solderball of every package) by only two terminals.**

TEXAS INSTRUMENTS

The GLP package is used for the production versions of the ceramic C6X devices: 320C6201B and 320C6701. The C6201BGLP and C6701GLP have identical pinouts and identical footprints.



Test Socket Information

Q: Where can I find sockets for the ceramic versions of the C6201B and C6701?

A:
Test Sockets for 27 x 27 mm 1.27 mm pitch Ceramic Dimpled Ball Grid Array
High frequency test socket which we use on our test boards:
Tecknit p/n 33-40028 we use on test boards tele: 908-272-5500
Description: "21 x 21 x 429 LGA test socket" ~$4K per socket.

Burn-In sockets: we are evaluating for use at 10 MHz or less:
1. Tactic Electronics Inc., Distributor Dallas,TX 800-955-4707
Tactic p/n: 2441-8684-63-1902
http://www.tacticelectronics.com

2. Plastronics (Irvin TX) 972-258-1906
p/n: 441BG12A127-D

The C6201BGLP and C6701GLP have identical pinouts and identical footprints.

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