Section 4

Applying Undersampling Converters

High-Speed ADC Systems

ADCs for Undersampling Applications

- Undersampling
- Undersampling vs. Oversampling
- Sampling Theory (short version!)
- Undersampling Application
- Fundamental Blocks of an Undersampled System
- Signal Conditioning (A/D driver)
- Single-ended vs. Differential
- Circuit Examples
- Clock Jitter, etc.
- Summary

Using high-speed A/D converters to digitize input frequencies above the converter's baseband region (dc to fs/2) is gaining a lot of popularity in communications related applications. In these applications the intermediate frequency (IF) can be as high as 250 MHz, and that frequency is usually too high to be digitized in an oversampling process.

Direct-IF down-conversion, or *undersampling*, as it is often called, results in reduced component count because a complete analog down-conversion stage is eliminated.

Synonyms for “Undersampling”

Undersampling

- IF Downsampling
- IF Downconversion
- Sub-sampling
- Direct IF-to-Digital Conversion
- Harmonic Sampling
- Bandpass Sampling
- Super Nyquist

Comparison

Oversampling	Undersampling
◆ $F_{IN} \leq fs/2$	◆ $F_{IN} > fs/2$
◆ $BW_{IN} \leq fs/2$	◆ $BW_{IN} \leq fs/2$
◆ Requires anti-alias input filtering	◆ Requires anti-alias input filtering
◆ 'Process Gain' can be realized	◆ 'Process Gain' can be realized

$$Process Gain, PG = 10 \log\left[\frac{fs/2}{BW}\right]$$

Undersampling = Sampling at a rate below the Nyquist frequency, which implies a loss of information, unless the *Input Bandwidth* is restricted to less than fs/2. The alias products are used to translate the input signal (IF) down to baseband for further processing (e.g. demodulation, channel selection). The A/D converter must have sufficient 'Analog Input Bandwidth' for undersampling applications .

IF = Intermediate Frequency. The resulting output of modulated signal of higher frequency (RF) after a down conversion which contains the encoded baseband information.

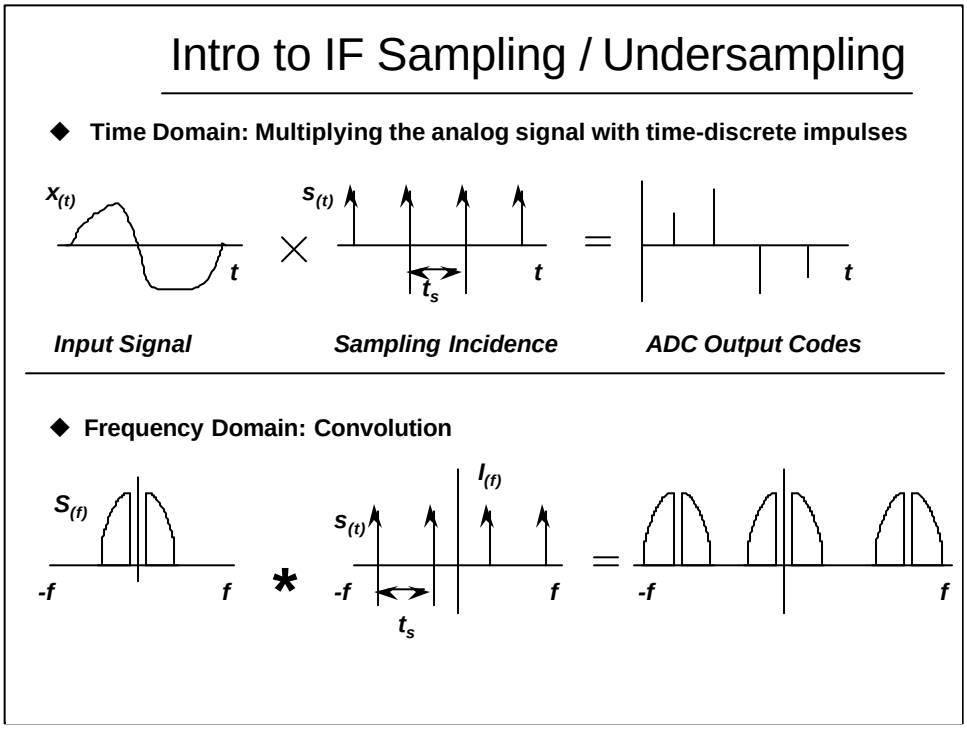
F_{IN} = Input Signal Frequency

BW = Input Signal Bandwidth

fs = Sampling or Clock Frequency

Process Gain:

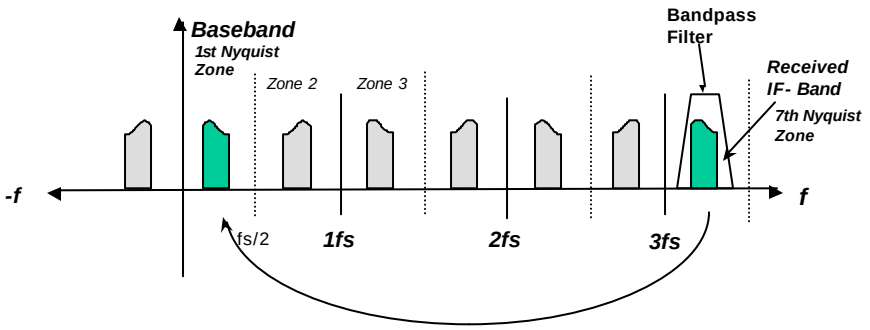
In a sampling system, the quantization noise of the A/D converter is evenly distributed over the entire Nyquist bandwidth of 0 Hz to fs/2 Hz. If the signal bandwidth (BW) is less than this fs/2, digital filtering can be employed to remove the noise components outside of this signal bandwidth, and effectively increasing the SNR. For example, if the bandwidth is limited to fs/4, the additional increase in SNR due to process gain is 3 dB.



In the time domain, sampling can be viewed as multiplication of a time-continuous analog signal x(t) by an impulse train that has sampling incidence with a defined time spacing (ts). The impulse train often represents the sampling points of an A/D converter.

The equivalent process in the frequency domain is convolution of the analog signal spectrum s(f) with the impulse train spectrum I(f). The result of convolution is a set of similar images of the original spectrum at integer multiples of the sampling incidence.

Undersampling Theory— Example



Requirement: IF-BW £ fs/2

Undersampling will produce an alias spectrum in the 1st Nyquist Zone (Baseband).

Nyquist Zones are defined as intervals of fs/2, with the first Zone spanning the 0 to fs/2 baseband.

This example shows an IF-band being received in the 7th Nyquist zone. It is sufficiently band-limited by a bandpass filter to allow for complete recovery of the information.

Again, by convolution the IF-band appears in each zone. While the higher images are of no interest, the one falling into the 1st zone, baseband will be used for further processing.

Depending on the location of the input IF band, it may be necessary to 'mirror' the band that falls into the 1st Zone. This can be facilitated by the digital receiver that follows the A/D converter.

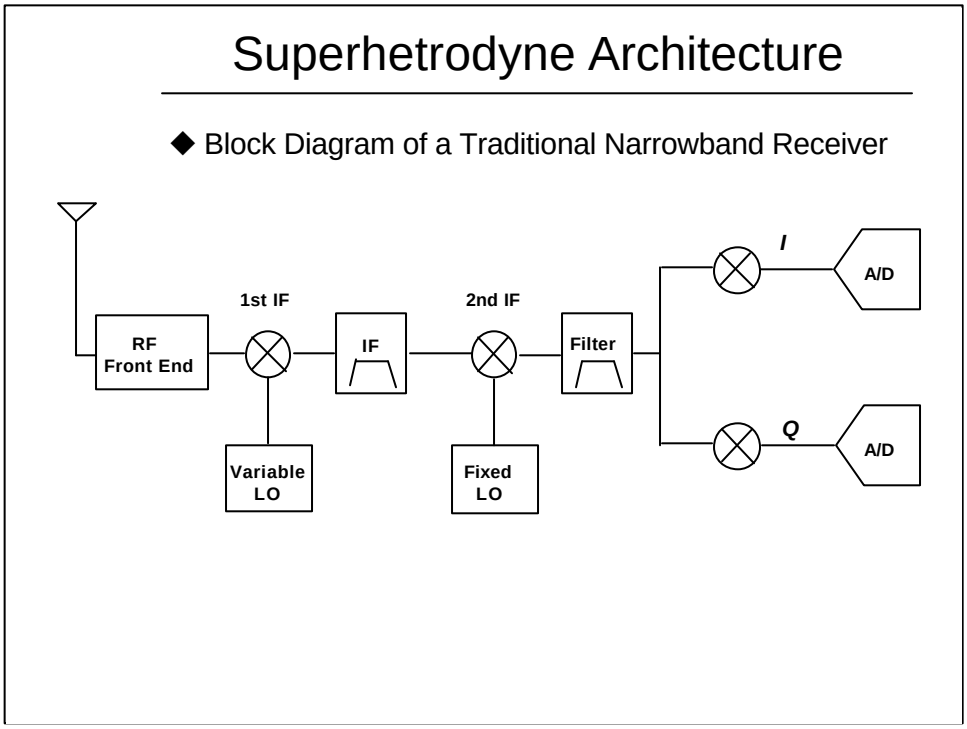
A 'Nyquist Zone' is defined as intervals of fs/2 in the frequency domain of the sampled signal.

Consequently, the 1st Nyquist Zone spans from 0 Hz to fs/2 Hz

As a result of the sampling process each input frequency is repeated at every fs/2, according to:

$$fin' = |fin - M \times fs| \;;$$

where fin' is the alias of the input frequency fin, fs<fs/2, and M is an integer.

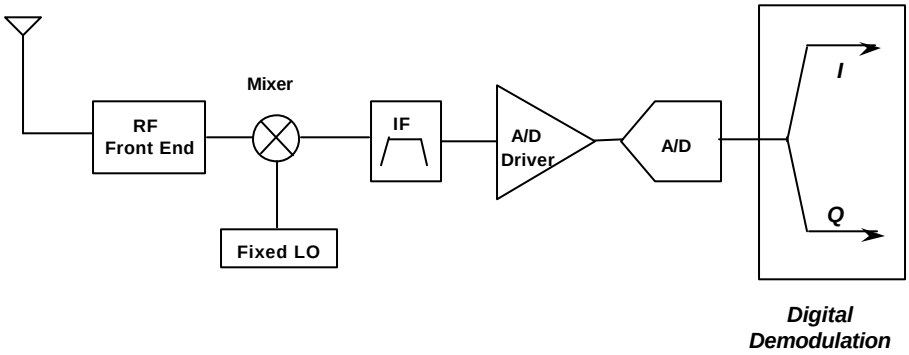


This is the block diagram of a traditional 'Superhet' receiver. The received RF is down-converted to the 1st IF frequency with a variable local oscillator and a bandpass filter provides selectivity. Next, the signal is down-converted to lower IF with a second LO and mixer. Since the resulting frequency is still an 'intermediate' frequency, a third conversion is required. This is done with an I/Q demodulator (assuming the original signal was previously modulated in a quadrature format). After this down-conversion and demodulation, the signals are now split into two components, the 'in-phase' and the 'quatrature –phase' baseband information. Therefore, the digitization requires two A/D converters.

This topology is well established and understood, but the number of analog down-conversion stages required increases cost.

Wideband Undersampling Digital Receiver

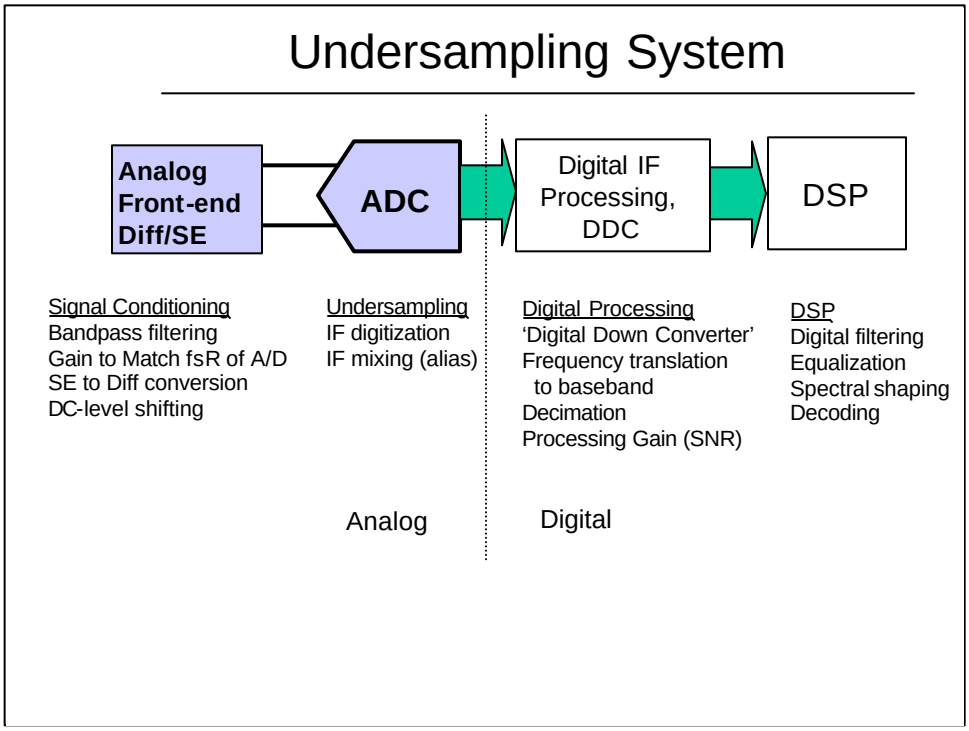
◆ **Block Diagram of a 'New' Receiver Architecture using IF Sampling**



This is a 'Direct-IF' receiver, or digital receiver. Basically, this architecture moves the A/D converter closer to the antenna. As a result, only one down-conversion to an IF stage is required and one complete analog mixer stage is eliminated. All further frequency down-conversion and demodulation is handled in the digital domain. Reduced analog complexity is gained, but the performance requirements for the A/D converter are much more demanding for "Undersampling" architectures.

Undersampling Application

IF Sampling System



This slide outlines the essential blocks of an "undersampling" system. This seminar focuses on the analog components like the front-end and the A/D converter.

The analog front-end block encompasses the signal conditioning necessary to interface with the A/D converter. For example, filtering, gain, single-ended to differential signal conversion etc. may be performed in this system block.

The name A/D converter symbolizes the mixed-signal nature of this part. The A/D converter should be treated as an analog component to obtain its best performance. It is especially important that the analog specifications of A/D converters used for undersampling be adequate to support the design. This is because the A/D converter performs the equivalent function of an analog mixer as well as the digitization of the analog input (high frequency, IF).

The clock circuitry is a critical part of the 'ADC', and it requires as much care and attention as the analog circuitry does.

The two blocks on the digital side complete an undersampling system. Depending on the nature of the input signal, several digital signal processing steps are performed.

Selecting A/D Topology

ADC Topology	***F conversion***	***Resolution***	***Comments***
SAR	< 2Msps	Up to 18-Bit	Too slow
Delta-Sigma	< 20Msps	Up to 24-Bit	Not enough input bandwidth; Resolution not needed
Flash	< 500Msps	Up to 10-Bit	Speed not really needed; SNR may not be sufficient
Pipeline	< 200Msps	Up to 16-Bit	Offers excellent dynamic specs; Most suitable

The table separates the ADCs into four groups by the ADC architecture. Each architecture has distinct characteristics that must be understood to match the proper ADC with an application.

Typically, only the Flash- and Pipeline converters are used for high-speed applications because of their high conversion rate. Pipeline converters are readily available, and offer the dynamic performance specifications required to support undersampling applications.

Critical System Criteria

Selection Criteria:

- What is the input frequency and bandwidth?
- What is the resolution required (ENOB)?
- What is the required Dynamic Range (SFDR,SNR)?
  - SFDR over bandwidth of interest?
- Clock frequency?
  - Fixed, or can it be chosen for alias ‘positioning’?

Operating the ADC in an undersampling application requires knowledge of the converter’s dynamic performance at frequencies above fs/2 (Nyquist). Often, manufacturers provide relevant specifications like ‘Analog Input Bandwidth’ and typical performance curves in their datasheets.

This slide lists a selection of primary considerations that will help define the system and component requirements.

In addition, secondary aspects such as power supplies, external references or data interface may need to be considered.

A/D Specifications Review

- Important Specs
  - Analog input bandwidth
  - Resolution
  - ENOB, Effective Number of Bits
  - SFDR, Spurious-Free Dynamic Range
  - SNR (total), SINAD
    - Jitter (SNR)
- Consider:
  - T&H of ADC replaces an analog mixer
  - Performance requirements of a wideband mixer now placed on the ADC

In general, as the input signal frequency to the converter increases, SFDR, SNR, and ENOB performance degrades. How rapidly the degradation proceeds depends on the each converter.

Analog Input Bandwidth

- Large Signal vs. Small Signal
- Input T&H of ADC determines the input bandwidth
- Full-power bandwidth is directly related to the full-scale input range of the ADC
- FPBW is a theoretical number

Analog Input Bandwidth

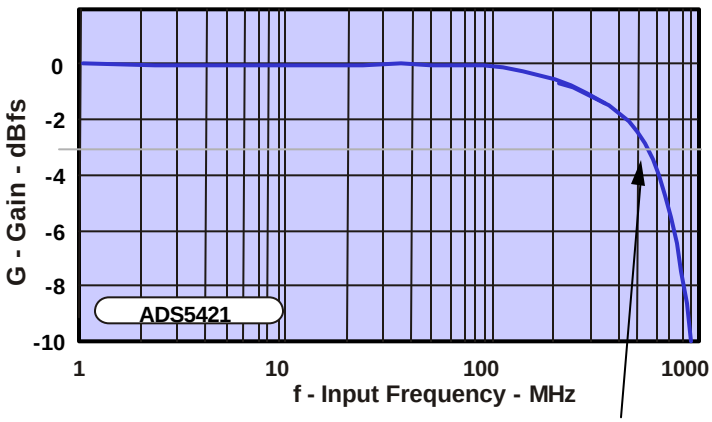
The T&H performance of an ADC is the most significant function that determines the input bandwidth:

> The slew rate capability of the T&H determines the 'Full-power Bandwidth' (FPBW) for large signals.
>
> The frequency response of the T&H determines the small signal bandwidth (typically signifies the -3dBfs point) for small signals.

Full-Power bandwidth is directly related to the full-scale input range of the ADC and therefore can be used as an initial selection criteria when comparing converter for their undersampling capabilities.

FPBW is a quasi theoretical number, because it does not relate to ac-performance levels of the ADC. SFDR, SNR, THD and ENOB performance curves must be analyzed to determine ac performance.

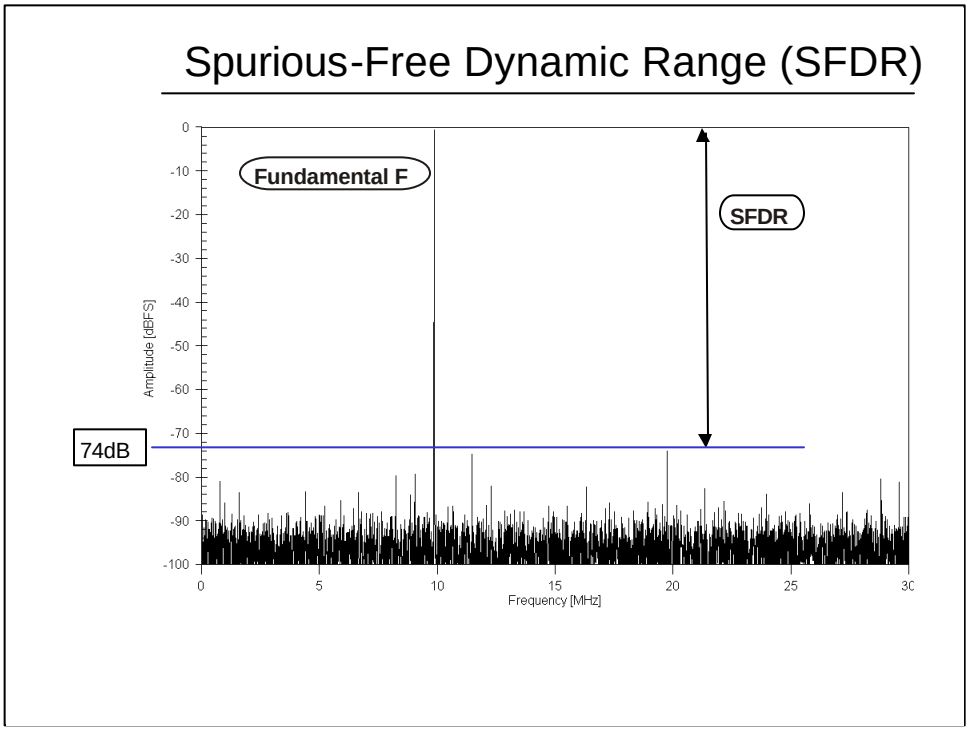
Analog Input Bandwidth of a Pipeline ADC



ADS5421
14-bit , 40-MSPS Pipeline ADC

FPBW approx. 550 MHz

Example of the ‘Analog Input Bandwidth’ of the ADS5421, a 14-bit, 40-Msps pipeline A/D converter. This CMOS converter uses a differential track-and-hold circuit. The switched capacitor architecture allows for a very wide analog input bandwidth.



Typically, a Fast Fourier Transformation, FFT, is employed to evaluate the dynamic performance of an A/D converter. This is a FFT plot of a 10-bit, 60-MHz converter. The fundamental, or input signal, is a 9.9-MHz single tone at full-scale amplitude. The spurious-free dynamic range can easily be calculated by analyzing the plot. The 2nd harmonic at about 19.8 MHz is the highest spur, thus it defines the SFDR. The second highest spur, located close to the fundamental, does not seem to be a harmonic product.

In addition to the SFDR number, FFT calculations typically provide results for SNR, SINAD and THD.

Undersampling and Input Filter

- Substitutes analog mixer, filter, etc. with digital components (ADC, DDC, DSP)
- Smaller and better analog filter available for higher input frequencies
- IF-sampling
  - 'Positioning' of sampling frequency and IF can help moving dominant harmonics out of the bandwidth of interest
  - 'Dominant Harmonics' are typically 2nd HD and 3rd HD
  - Achievable in-band SFDR often defined by 'Worst Other Spur'

Benefits of undersampling/IF-sampling:

Substitutes analog mixer, filter, etc. with digital components (ADC, DDC, DSP)

Avoids high tolerances of analog components

Digital allows for near ideal accuracy

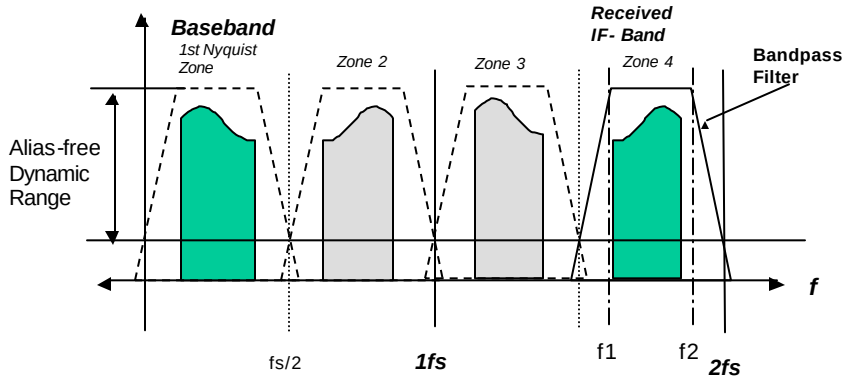
Programmable digital filters allow for flexibility

Smaller and better analog filter available for higher input frequencies

Baseband processing often requires higher order low-pass filter for alias filtering

IF-sampling allows usage of inexpensive, high-Q SAW filter for bandpass filtering

Input Filter Defines Dynamic Range



Example: BP Filter slopes: f2 to 2fs – f2
f1 to fs – f1

Similar for Nyquist sampling applications, the filter characteristics defines the achievable dynamic range. Depending on the stopband attenuation, a certain amount of out-of band noise and signal will alias into the passband.

ADC Interface Solutions

Once the A/D converter is identified the question becomes:

"How do I interface my incoming IF signal to the converter to get the best possible performance results?"

ADC Interface Solutions for Undersampling

Identify an appropriate interface configuration!

Simple Selection Matrix:

	Single-Ended Input	Differential Input
AC-coupled	**High Amplitude Signal Required**	**More Complex Circuit**
DC-coupled	Limited Use for This Application	Limited Use for This Application

Note: 'SE' or 'Diff' refers to the immediate A/D input configuration

AC-Coupled

Single-Ended Input

Bandlimited IF does not contain a dc-component so it is ac-coupled.

Single-ended input requires twice the signal amplitude out of the driver to match ADC full-scale.

ac-coupling eliminates common-mode voltage (Vcm) between the driver op amp and the A/D.

Differential Input

More complex driver circuit than single-ended.

Reduced signal amplitude leads to improved distortion due to increased headroom for the driver amps.

Offers common-mode noise and even-order harmonic rejection

DC-Coupled

Single-Ended Input

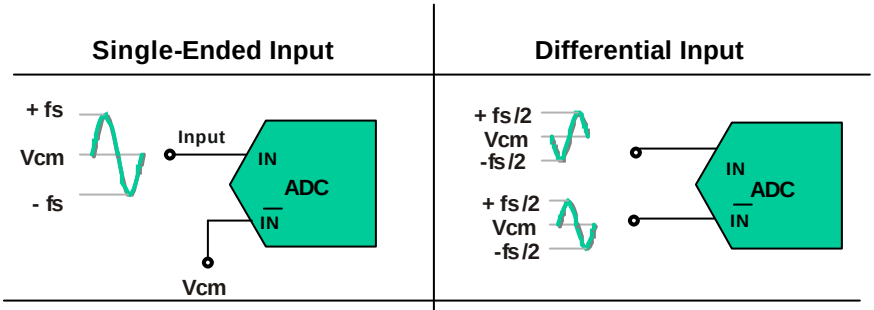
Limited use because input bandwidth does not include LF or DC.

Differential Input

Differential I/O amps may be used depending on input frequency range.

ADC Interface Solutions

Principle Configuration Choices

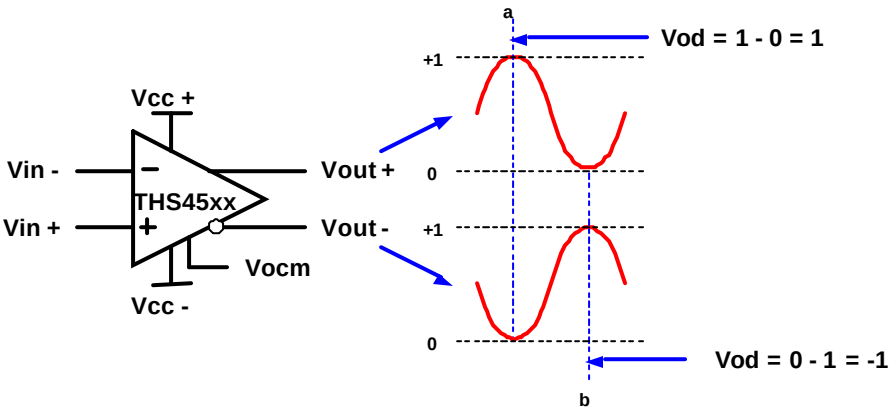


Requires full input swing from +fs to –fs
2x the swing compared to differential
Input signal at IN typically requires a common-mode voltage for bias
Input IN\ also requires a Vcm for correct dc-bias

Combined Differential inputs result in full-scale input of +fs to –fs
Each input only requires 0.5x the swing compared to single-ended
Both inputs require a Vcm for correct dc-bias

Most CMOS pipeline ADCs are operated on a single-supply. This typically requires the inputs to be biased to a common-mode voltage, Vcm, which is typically set to mid-supply (+Vs/2). The converter inputs are often provided in differential form, but can be driven from the source in two ways: either single-ended or differential. Both configurations have their advantages and disadvantages.

Increased Dynamic Range

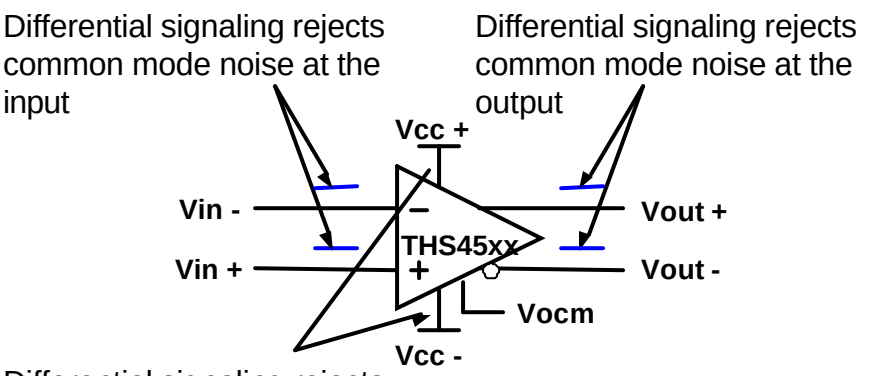


Differential output results in $V_{od\ p\text{-}p}$ = 1 - (-1) = 2X SE output

Lower power supply requirements

Due to the change in phase between the differential outputs, the dynamic range increases by 2X over a single-ended output with the same voltage swing. This lowers the power supply requirements for a given output voltage swing.

Common Mode Noise Rejection



Invariably when signals are routed from one place to another, noise is coupled into the wiring. In a differential system, keeping the transport wires as close as possible to one another makes the noise coupled into the conductors appear as a common-mode voltage. Noise that is common to the power supplies will also appear as a common-mode voltage. Since the differential amplifier rejects common-mode voltages, the system is more immune to external noise. The figure shows the common-mode noise immunity of a fully differential amplifier pictorially.

ADC Interface Solutions

Single-ended vs. Differential

Conclusion:

"In Undersampling applications, using the Differential Input Configuration along with ac-coupling results in the best obtainable ADC performance."

Differential Interface

- Theoretically, differential signaling results in cancellation of even-order harmonics.

  This would be ideal since 2nd HD is usually dominant.

- In reality, complete suppression is not achievable. However, design optimization includes best possible matching of:
  - Components (consider parasitics)
  - Layout; i.e. symmetry between signal paths

Reduced even order harmonics

Use power series expansion:

Non-inverted output:

$$Vout + = k_1(Vin) + k_2(Vin)^2 + k_3(Vin)^3 + ...$$

Inverted output:

$$Vout - = k_1(-Vin) + k_2(-Vin)^2 + k_3(-Vin)^3 + ...$$

Differential output:

$$Vod = (Vout +) - (Vout -) = 2k_1Vin + 2k_3Vin^3 + ...$$

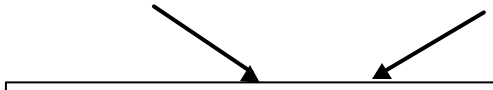
Differential signal contains no even order terms

Expanding the transfer functions of circuits into a power series is a typical way to quantify the distortion products. In general $Vout = k_1Vin + k_2Vin^2 + k_3Vin^3 + \ldots$, where k_1, k_2, k_3, etc. are some constants. If the input to this circuit is a sinusoid: , trigonometric identities show the quadratic, cubic and higher order terms give rise to 2nd, 3rd and higher order harmonic distortion. In similar manner, if the input is comprised of two sinusoidal tones, trigonometric identities show the quadratic and cubic terms give rise to 2nd, 3rd and higher order intermodulation distortion.

In a fully differential amplifier, the odd order terms retain their polarity, but the even order terms are always positive. When the differential is taken the even order terms cancel.

Implementation of Differential Circuits

- Active = Op Amps
  - VFA, CFA
  - Good for providing gain
  - I/O impedance isolation
  - Op Amps have 'SE' I/O
  - Can add noise and distortion
  - Supply sets headroom and common-mode limit
  - DC- and AC-coupling
- Passive = Transformer
  - Simple SE to Diff conversion
  - Step-up types for 'noiseless' gain
  - Common-mode voltage can easily be added to center-tap
  - Need impedance matching
  - Bandpass response
  - AC-coupling only



Actual circuit implementations may use a combination of both!

Driver Op Amp Selection

Observation:

Performance levels of high-speed A/Ds are high and finding suitable driver op amps with sufficiently low distortion is difficult!

Current-Feedback (CFA) vs. Voltage-Feedback Amplifier (VFA):

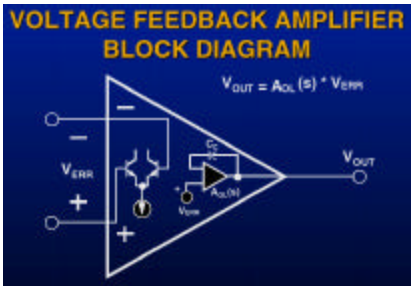
- CFAs maintain good distortion up to very high frequencies
- CFAs typically have good IP3 performance due to high slew rate
  - Good 'prerequisites' for IF-applications/Undersampling
- VFAs typically have superior distortion performance at baseband frequencies

The op amp used to drive the ADC should have better distortion and noise performance than the A/D converter to preserve the ADC performance. When differential inputs require two op amps, a dual op amp may offer better matching (over temperature) than two singles. Additionally, the output voltage swing of the op amps should accommodate the full-scale input range of the A/D converter to achieve full dynamic range performance. Most high-speed A/D converters use a single supply, but dual supplies are often required to power input drive op amps.

The transient response of the driver circuitry can have a significant affect on the performance of high-speed converters, so the drive circuitry must insure that transient currents and voltages at the output of the amplifiers are sufficiently settled before the A/D converter acquires the input signal sample. The bandwidth should be adequate to prevent attenuation of higher frequencies.

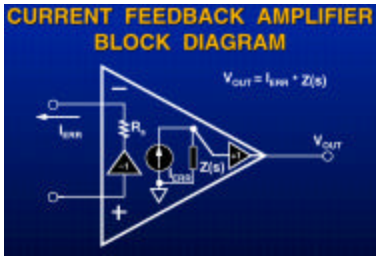
Voltage Feedback Op-Amps

- Advantages
- “Error” signal is a voltage
- Input stage is matched or symmetric
- High levels of DC accuracy
- OPA277
- Disadvantages
- Bandwidth is dependent on closed loop gain
- Some are not stable in unity gain (OPA37)



Current Feedback Op-Amps

- Advantages
- "Error" signal is a current
- Bandwidth is independent of closed loop gain
- Higher speed
- Always unity gain stable
- OPA642
- Disadvantages
- Input stage is not symmetric
- Not as accurate
- Higher bias current
- More current noise



Driver Op Amp Selection

- Important Considerations
- Review Performance Curves:
  - Distortion vs. Frequency and,
  - Distortion vs. Amplitude and Load
    - Op amp specs typically refer to a 100-Ω load, while the input impedance of an A/D converter is in the range of 500 Ω+
    - This will improve the distortion
- Output impedance vs. frequency
- High slew rate, fast settling
- Stability with capacitive load
- Output voltage swing must match A/D fs-input
- Single- or dual-supply system?

Several factors have to be considered when selecting the driver op amp. Most data sheets provide specifications and/or typical performance curves for distortion (THD) over a range of frequencies. Almost all high-speed op amps are specified in a 50-Ω environment, thus the standard load condition for the typical performance curves is double-terminated 50-Ω or 100-Ω total load.

The input impedance of a pipeline A/D converter is much higher than 100 Ω, typically, several hundred Ohms, and this higher load condition usually leads to improved distortion performance of the driver amplifier.

The implication is that the pipeline A/D converter has a switched capacitor T&H in its input. This means two things: first, the op amp has to drive a capacitive load; and second, the input impedance of the converter is dynamic.

Z_{IN} is a function of sampling rate, and Z_{IN} declines with an increase in fs.

Ultra-Wideband, Current Feedback Amplifier

OPA685

Features

- Gain = +2, Bandwidth (900 MHz)
- Gain = +8, Bandwidth (420 MHz)
- Wide Output Voltage Swing: ±3.6 V
- 90-mA drive capability enables it to drive 2 mixers
- Low Power: 129 mW (±5 V)
- Low Disabled Power: 3 mW

Applications

- Wideband ADC Driver
- Cost Effective IF Amplifier
- LO Buffer

Device	V_S (V)	BW_{-3dB} (MHZ)	SR (V/ms)	THD_{1MHz} (dB)	IP3 (dBm)	$V_{n\ 10MHz}$ (nV/√Hz)	$T_{s(0.1\%)}$ (ns)
OPA685	5-12	1200	4200	80	40	1.7	3

Mini Data Sheet at ±5V, 25°C, typ, I_Q per channel

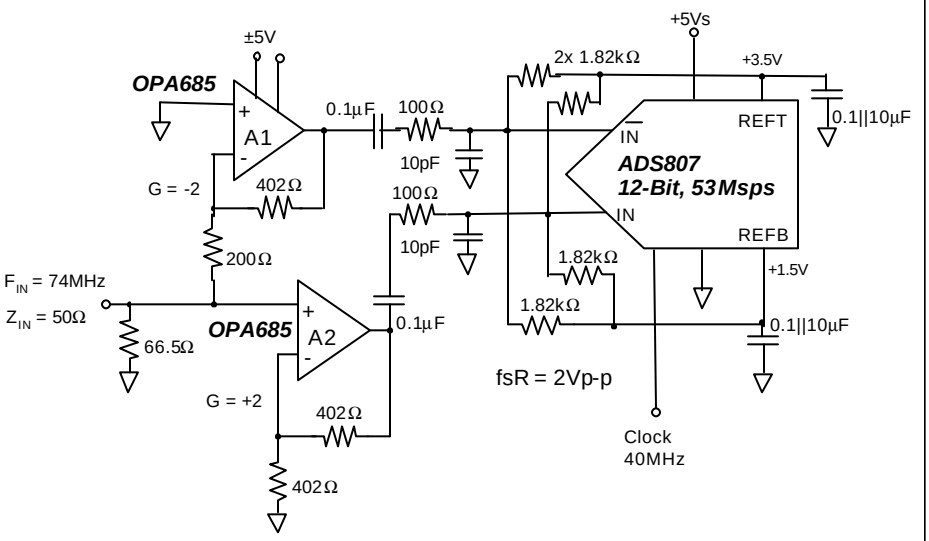
High-Speed A/D Converter Products

Model	Bits	Speed (Msps)	A-BW (MHz)	SFDR@ 10MHz	SNR @10MHz	Jitter (rms)
ADS826	10	60	300	73dB	58dB	1.2ps
ADS828	10	75	300	68dB	57dB	1.2ps
ADS805	12	20	270	74dB	68dB	2ps
ADS807	12	53	270	82dB	68dB	1.2ps
ADS809	12	80	500	68dB	65dB	0.25ps
ADS5421	14	40	500	83dB	75dB	0.25ps
ADS5422	14	60	500	82dB	74dB	0.25ps

A selection of high-speed pipeline A/D converters suitable for use in undersampling applications.

Complete information can be found on TI's web site: www.ti.com

Example—Op Amp Driver Circuit



This undersampling configuration digitizes a 74-MHz input signal with a 40-MHz sampling rate. The input signal is converted down to a 6-MHz fundamental.

For this circuit example, the OPA685 was chosen to drive the inputs of the ADS807, a 12-bit, 53-Msps pipeline converter.

The OPA685's outputs are ac-coupled to the converter. This allows the input signal amplitude to be centered around 0 V, or mid-supply, in order to maintain a symmetric headroom and consequently minimize the distortion.

For the A/D converter inputs, the necessary common-mode voltage is derived from the internal references. The mid-points of the two-resistor strings (2x1.82k) produce a +2.5-V common-mode voltage.

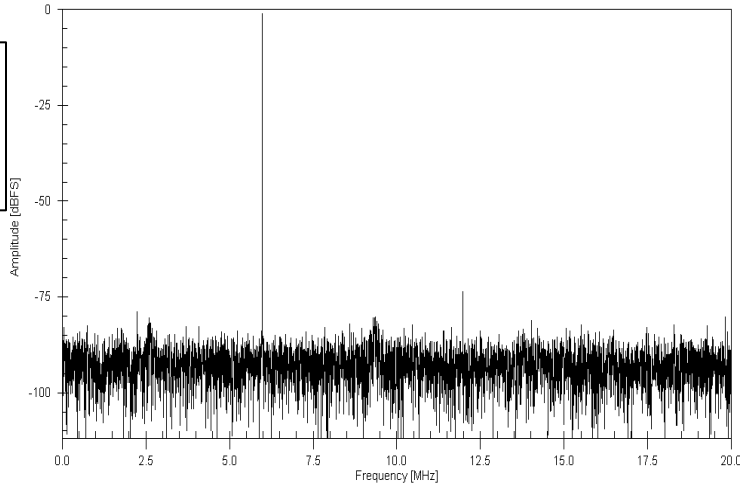
The amplifiers are set for a signal gain of 2. However, due to their different configuration, their noise gains are not matched which could potentially degrade the performance.

The simple RC filter (100 Ω, 10 pF) provides some attenuation of the high-frequency noise.

Op Amp Driver Circuit - FFT

F_{IN} = 74 MHz
fs = 40 Msps
A_{IN} = -1 dBfs

SFDR = 73.5 dB
SNR = 53.7 dBc
SINAD = 53.6 dBc



This is an FFT of the previous driver circuit, in which the OPA685 is used to drive the ADS807. Even though attention was paid to the symmetry of the differential signal path, the second harmonic continues to be the dominant spur.

Test Results

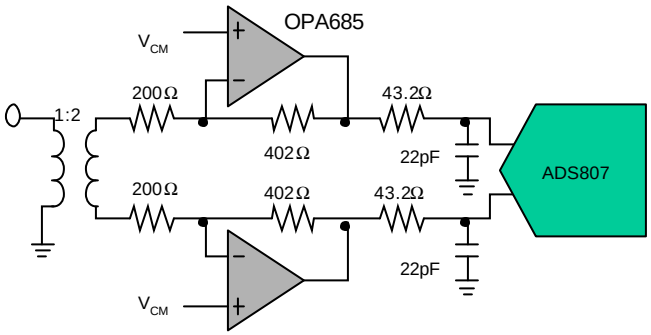
A_{IN} (dBfs)	SNR (dBc)	SINAD (dBc)	SFDR (dB)
-1	53.7	53.6	73.5
-3	53.6	53.5	77.7
-6	53.3	53.1	78.6
-12	51.8	51.7	86.1
-20	47.2	47.0	85.2

Conditions:
Fin = 74 MHz, Fin' = 6 MHz, fsR = 2 Vp-p
Input signal filtered with a 80 MHz, 9th order passive BP (TTE)
Clock = 40 MHz,
Vs = +5 V, VDRV = +3 V
Driver amp: OPA685, Gain 2

Listed here in tabular form are more test results from the OPA685 driver circuit. Note that the SNR and SINAD are relative to the fundamental
(in dBc) and remain fairly constant. It also shows that an improvement in the dynamic range (SFDR) can be realized by reducing the amplitude of the input signal.

Differential ADC Driver Solutions

Two High-Speed Amplifiers



- Noise Gain Matched
- Parts Are Symmetrical
- Excellent Distortion Performance

Compared to the previously shown circuit, this example improves upon the matching of the differential signal. A transformer provides SE-to-Diff conversion and it is combined with the OPA685 current-feedback amplifier. This allows for both amplifiers to operate in the same inverting configuration resulting in improved noise gain (bandwidth) matching.

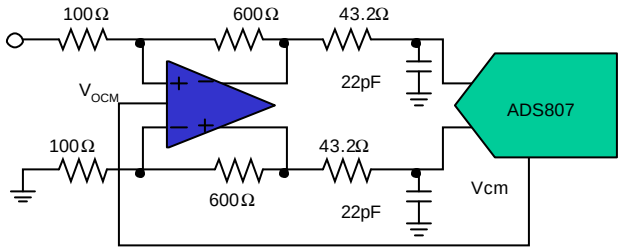
The op amps are dc-coupled to the ADS807. The required common-mode voltage (Vcm) is applied to the non-inverting inputs of the OPA685s to correctly bias the ADC inputs.

Using a step-up transformer in the input helps reduce the gain requirements for the driver op amps.

This circuit can achieve excellent distortion performance up to very high frequencies (IF).

Differential ADC Driver Solutions

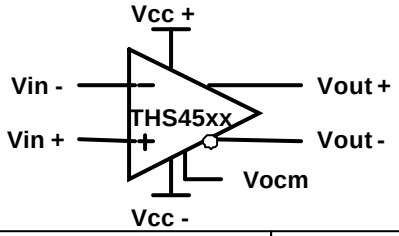
Fully Differential I/O Amplifier



- Ideal Baseband Driver Solution:
  - No transformer
  - VCM matched to ADC
  - Good even-order harmonic rejection
  - Easily configured for gain and low-pass filter

Fully differential input/output amplifiers have recently become available. These new high-speed devices are particularly suited for driving differential A/D converters. Their features enable a very effective applications solution were dc-coupling is required.

Voltage Definitions



	Differential	Common Mode
Input voltage definition	Vid = (Vin+) - (Vin-)	$Vic = \frac{(Vin+) + (Vin-)}{2}$
Output voltage definition	Vod = (Vout+) - (Vout-)	$Voc = \frac{(Vout+) + (Vout-)}{2}$
Transfer function	Vod = a(f) x Vid	Voc = Vocm

To understand how a fully differential amplifier behaves, it is important to understand the voltage definitions that are used to describe the amplifier. The diagram shows a fully differential amplifier and its input and output voltage definitions.

Input Voltages

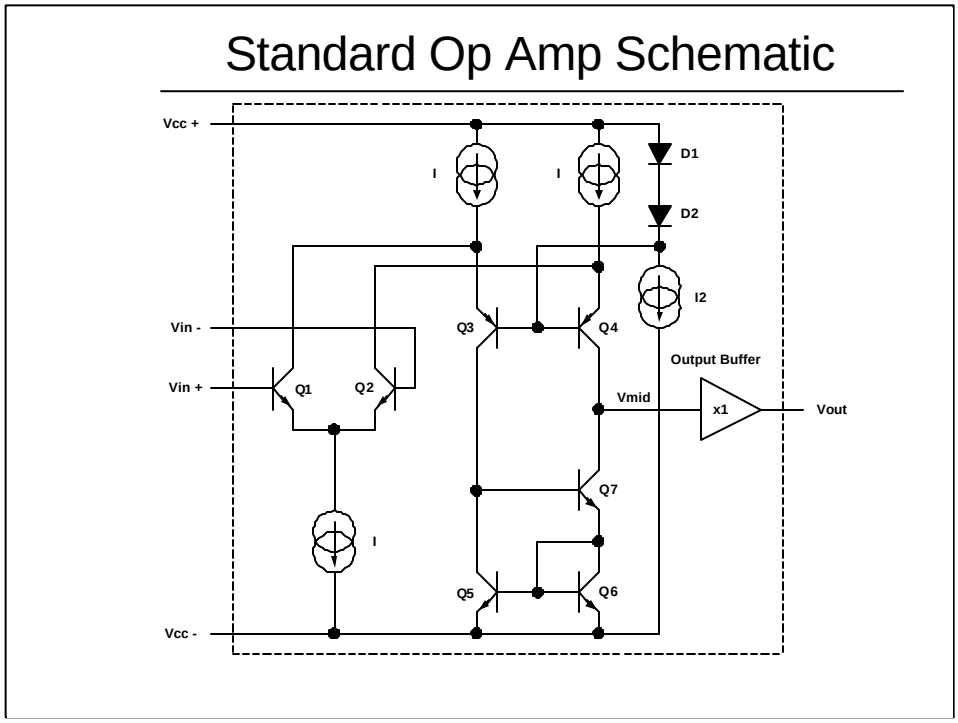
The voltage difference between the plus and minus inputs is the input differential voltage, Vid. The average of the two input voltages is the input common-mode voltage, Vic.

Output Voltages

The difference between the voltages at the plus and minus outputs is the output differential voltage, Vod. The output common-mode voltage, Voc, is the average of the two output voltages.

Transfer Fuctions

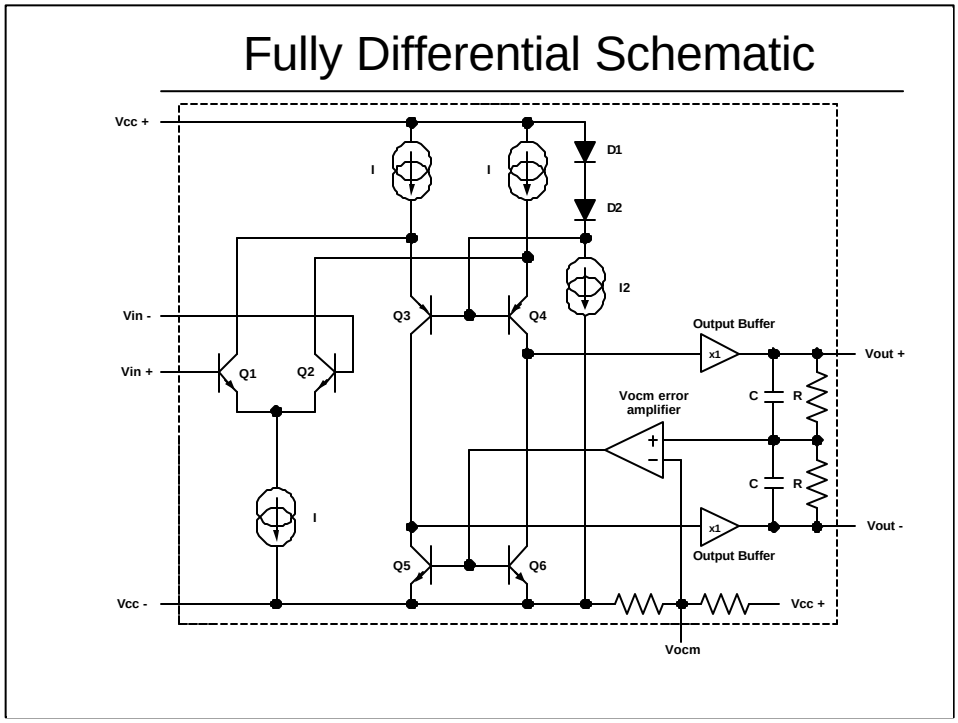
a(f) is the frequency dependent open loop gain of the main differential amplifier so that Vod = a(f) x Vid. Voc is controlled by the voltage at Vocm.



A simplified schematic of a high-speed op amp is shown. Vcc+ is the positive power supply input, and Vcc - is the negative power supply input. Vin+ and Vin- are the signal input pins, and Vout is the signal output. The op amp amplifies the differential voltage across its input pins to generate the output. By convention, the input voltage is the difference voltage, Vid = (Vin+) – (Vin-). It is amplified by the open loop gain of the amplifier to produce the output voltage, Vout = a(f)Vid, where a(f) is the frequency dependent open loop gain of the amplifier.

The input pair is balanced so the collector currents are equal when the input differential voltage is zero, Ic1 = Ic2. Applying a voltage across the input pins causes Ic1 ≠ Ic2.

Q3 and Q4 folds the difference current, Ic1 - Ic2, from the input stage into the Wilson current mirror formed by Q5, Q6, and Q7. The mirror presents high impedance to the difference current and generates the voltage at Vmid, which is then buffered to the output.

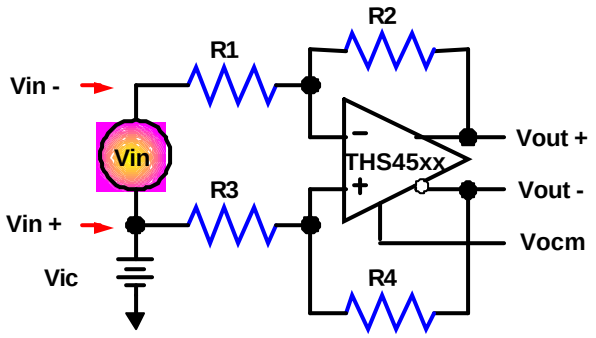


A simplified version of an integrated fully differential amplifier is shown . Q1 and Q2 are the input differential pair. In a standard op amp, the difference current from the input differential pair is used to develop a single-ended output voltage. In a fully differential amplifier, the difference current is used to develop differential voltages at the high impedance nodes at the collectors of Q3/Q5 and Q4/Q6. These voltages are then buffered to the differential outputs Vout + and Vout -.

To first order approximation, voltage common to Vin+ and Vin- does not produce a change in the current flow through Q1 or Q2 and thus produces no output voltage – it is rejected. The output common-mode voltage is not controlled by the input. The Vocm error amplifier maintains the output common-mode voltage at the same voltage applied to the Vocm pin, by sampling the output common-mode voltage, comparing it to the voltage at Vocm, and adjusting the internal feedback. If not connected, Vocm is biased to the midpoint between Vcc + and Vcc - by an internal voltage divider.

Note: there are two feedback paths around the main differential amplifier, and there is also the Vocm error amplifier.

Differential to Differential



$$\beta_1 = \frac{R3}{R3 + R4}$$

$$\beta_2 = \frac{R1}{R1 + R2}$$

$$Vin = (Vin+) - (Vin-)$$

$$Vout = (Vout+) - (Vout-)$$

Generalized Gain Formula

$$Vout = \frac{2[(Vin+)(1-\beta_1) - (Vin-)(1-\beta_2) + (Vocm)(\beta_1 - \beta_2)]}{(\beta_1 + \beta_2)}$$

Symmetrical Case $\beta_1 = \beta_2$

$R1 = R3 = R_G$ & $R2 = R4 = R_F$ ⇒ $\frac{Vout}{Vin} = \frac{1-\beta}{\beta} = \frac{R_F}{R_G}$

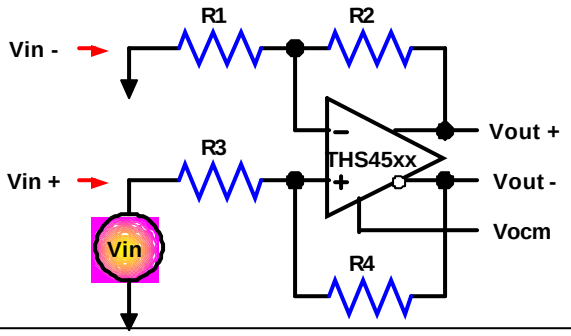
In a fully differential amplifier, there are two feedback paths possible in the main differential amplifier, one for each side. This naturally forms two inverting amplifiers, and inverting topologies are easily adapted to fully differential amplifiers. The figure shows a fully differential amplifier with negative feedback around both sides.

Symmetry in the two feedback paths is important to have good CMRR performance. CMRR is directly proportional to the resistor matching error – 0.1% error results in 60dB of CMRR.

Signals at Vin appear as differential inputs to the amplifier, and are amplified to the output. Common mode inputs like Vic are rejected by the amplifier.

The Vocm error amplifier is independent of the main differential amplifier. The action of the Vocm error amplifier is to maintain the output common-mode voltage at the same level as the voltage input to the Vocm pin. With symmetrical feedback, output balance is maintained, and Vout + and Vout - swing symmetrically plus and minus from the voltage at the Vocm input.

Single Ended to Differential



$$\beta_1 = \frac{R3}{R3 + R4}$$

$$\beta_2 = \frac{R1}{R1 + R2}$$

$$(Vin+) = Vin, \quad (Vin-) = 0$$

$$Vout = (Vout+) - (Vout-)$$

Generalized Gain Formula

$$Vout = \frac{2[(Vin)(1-\beta_1) + (Vocm)(\beta_1 - \beta_2)]}{(\beta_1 + \beta_2)}$$

Symmetrical Case $\beta_1 = \beta_2$

$R1 = R3 = R_G$ & $R2 = R4 = R_F$ ⇒ $\frac{Vout}{Vin} = \frac{1-\beta}{\beta} = \frac{R_F}{R_G}$

In the past, generation of differential signals has been cumbersome. Different means have been used, requiring multiple amplifiers, transformers and dc blocking capacitors. The integrated fully differential amplifier provides a more elegant solution. The figure shows an example of converting single ended signals to differential signals.

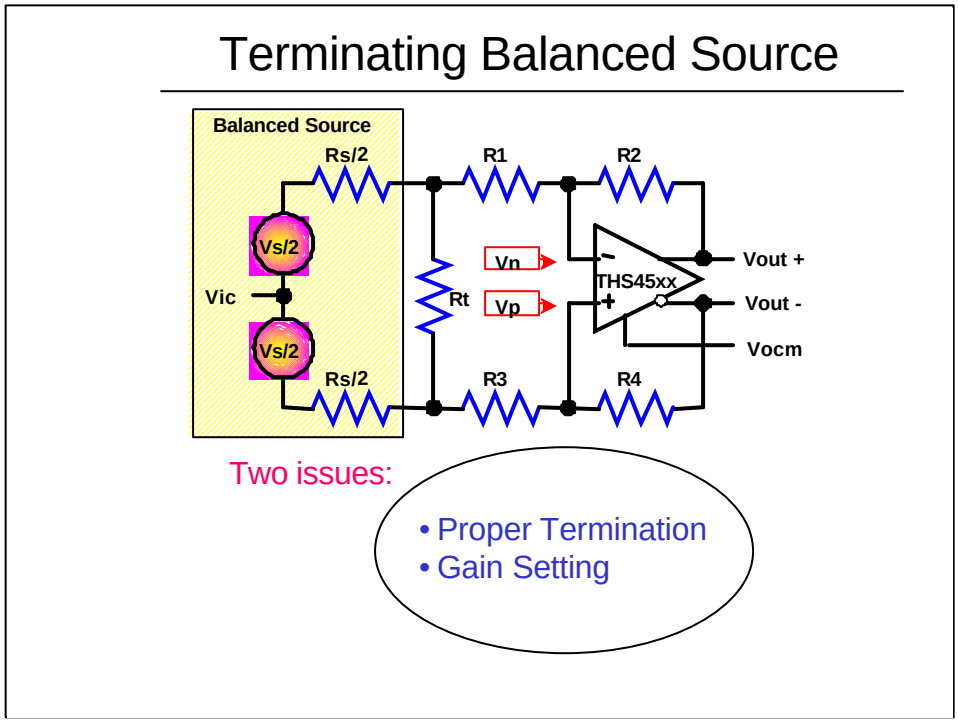
Signals at Vin appear as differential inputs to the amplifier. This may include unwanted dc offsets.

Input Termination

As RAP might say:

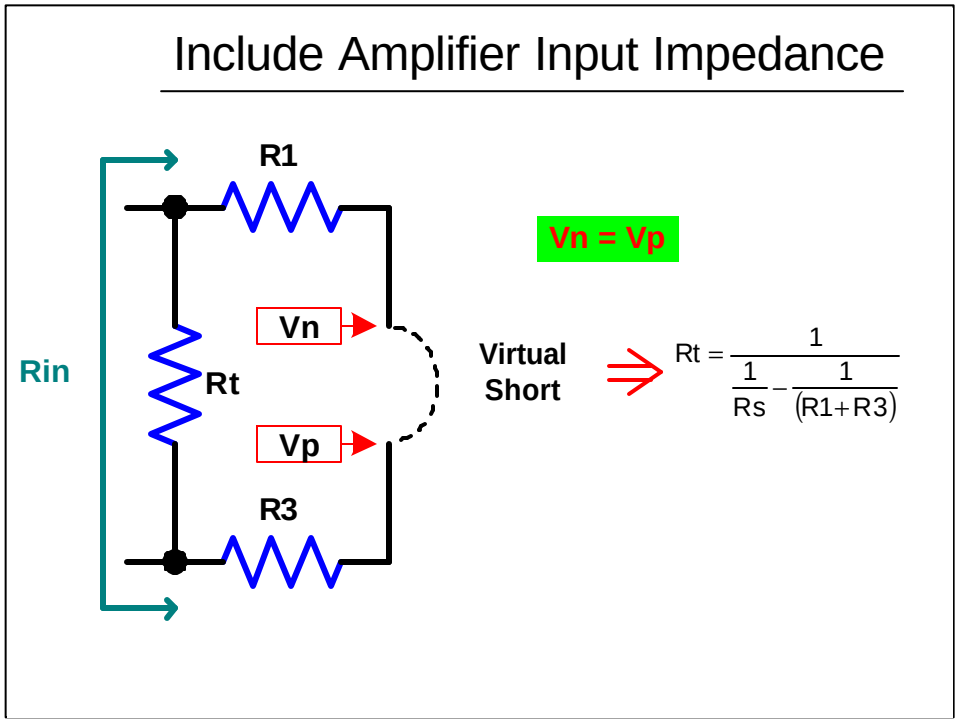
"What's all this input termination stuff anyway?"

- Double termination is commonly used in high-speed systems to insure signal integrity
- It may appear simple, but attention to detail is required to get it right
- Two cases:
  - Single ended
  - Differential

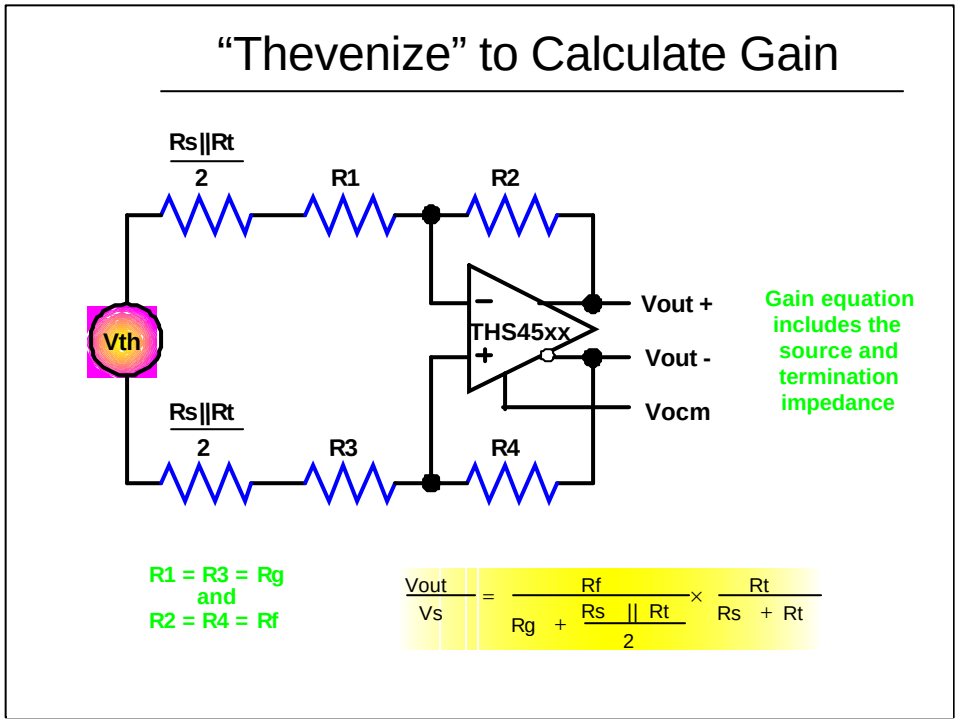


Double termination is typically used in high-speed systems to reduce transmission line reflections. With double termination, the transmission line is terminated with the same impedance as the source. Common values are 50O, 75O, 100O, and 600O. When the source is differential, the termination is placed across the line. When the source is single-ended, the termination is placed from the line to ground. The idea of terminating the input may seem trivial, but a bit of work is required to get it right.

The figure above shows an example of terminating a differential signal source. The situation depicted is balanced so that ½ Vs and ½ Rs is attributed to each input, with Vic being the center point. Rs is the source impedance and Rt is the termination resistor. The circuit is balanced, but there are still two issues to resolve: 1) proper termination, and 2) gain setting.



As long as a(f) >> 1 and the amplifier is in linear operation, the action of the amplifier keeps $Vn \approx Vp$. Thus, to first order approximation, a virtual short is seen between the two nodes as shown in . The termination impedance is the parallel combination: Rt || (R1+R3). The value of Rt for proper termination is calculated as shown.



Once Rt is found, the required gain is found by "Thevenizing" the circuit. The circuit is broken between Rt and the amplifier input resistors R1 and R3. Vic does not concern us at this point, so we will leave it out, and combine the ½ Vs's.

$$Vth = Vs \times \frac{Rt}{Rt + Rs}$$

Rth = Rs || Rt (½ is attributed to each side). The Thevenin equivalent is shown. The proper gain is calculated by:

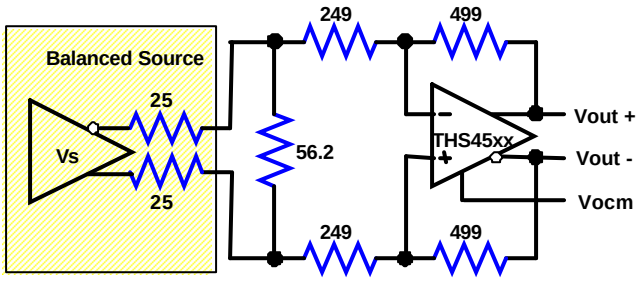
$$\frac{Vout}{Vth} = \frac{Rf}{Rg + \frac{Rs \parallel Rt}{2}}$$

where Vout = (Vout+) – (Vout-). Substituting for Vth, this becomes:

$$\frac{Vout}{Vs} = \frac{Rf}{Rg + \frac{Rs \parallel Rt}{2}} \times \frac{Rt}{Rs + Rt}$$

where Rf is the feedback resistor (R2 or R4), and Rg is the input resistor (R1 or R3). Remember: for symmetry keep the gain equal on the two sides with R2 = R4 and R1 = R3.

Terminating 50Ω Source, Gain = 1



Example: terminating a balanced 50 ohm source
with overall gain = 1

As an example, suppose you are terminating a 50O differential source that is balanced, and want an overall gain of one from the source to the differential output of the amplifier. Start the design by first choosing the values for R1 and R3, then calculate Rt and the feedback resistors.

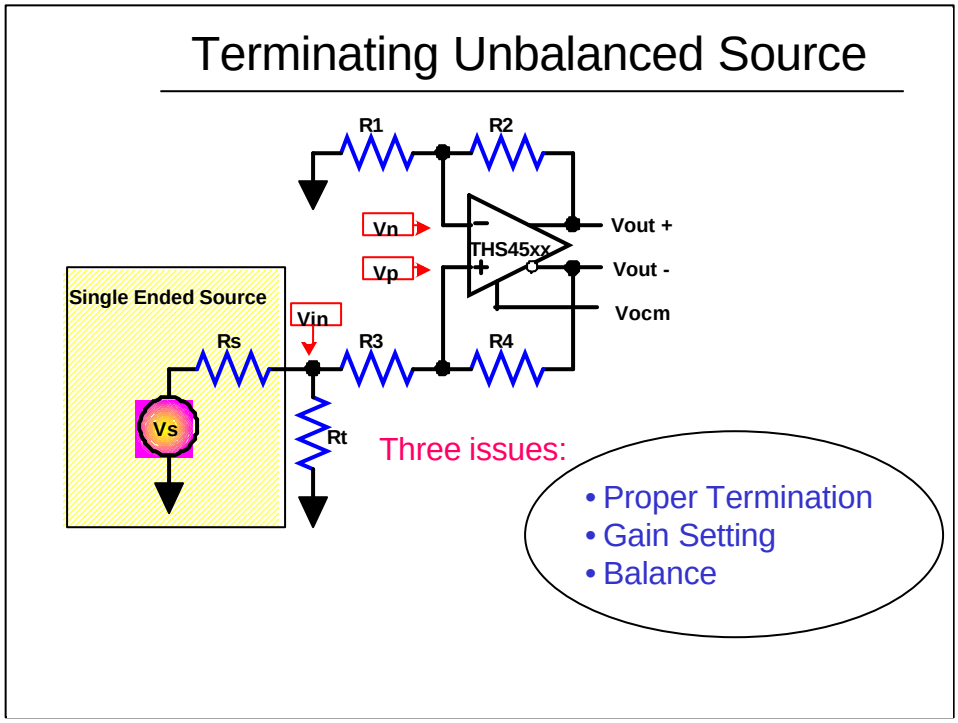
With the voltage divider formed by the termination, it is reasonable to assume that a gain of about two will be required in the amplifier. Also, feedback resistor values of approximately 500O are reasonable for a high-speed amplifier. Using these starting assumptions, choose R1 and R3 equal to 249O. Next calculate Rt from the formula:

$$Rt = \frac{1}{\frac{1}{Rs} - \frac{1}{(R1+R3)}} = \frac{1}{\frac{1}{50} - \frac{1}{(249+249)}} = 55.6\Omega$$

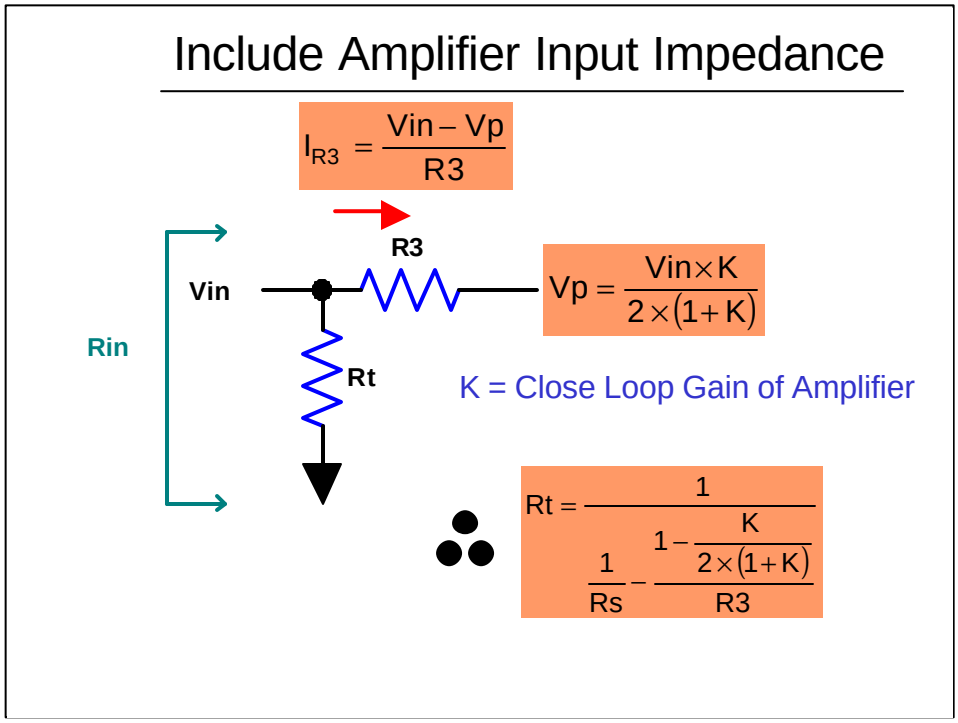
(the closest standard 1% value is 56.2O). The gain is now set by calculating the value of the feedback resistors:

$$Rf = \left(\frac{Vout}{Vs}\right)\left(Rg + \frac{Rs \,||\, Rt}{2}\right)\left(\frac{Rs+Rt}{Rt}\right) = (1)\left(249 + \frac{50 \,||\, 56.2}{2}\right)\left(\frac{50+56.2}{56.2}\right) = 495.5\Omega$$

(the closest standard 1% value is 499O). The solution is shown with standard 1% resistor values.



The figure shows an example of terminating a single-ended signal source. Rs is the source impedance and Rt is the termination resistor. The circuit is not balanced, so there are three issues to resolve: 1) proper termination, 2) gain setting, and 3) balance.



To determine the termination impedance seen from the line looking into the amplifier's input at Vin, remove Vs and Rs and short all other sources. As long as a(f) >> 1 and the amplifier is in linear operation, the action of the amplifier keeps $Vn \approx Vp$. Vn will see the voltage at Vout+ multiplied by the resistor ratio:

$$\frac{R1}{R1+R2}$$

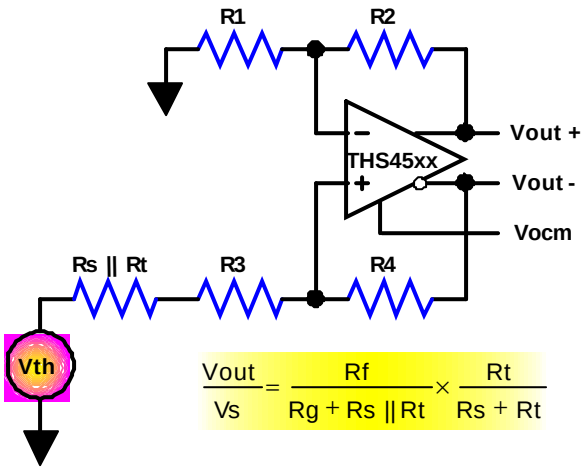
Assuming the amplifier is balanced: $Vout+ = K \times \frac{Vin}{2}$

where K is the closed loop gain of the amplifier (Vocm = 0). The termination impedance is the parallel combination: Rt in parallel with

$$Rt \parallel \frac{Vin}{I_{R3}} = Rt \parallel \left(\frac{R3}{1 - \frac{K}{2 \times (1+K)}} \right)$$

The analysis is shown pictorially along with how to calculate the value of Rt for proper termination.

"Thevenize" to Calculate Gain



$$\frac{Vout}{Vs} = \frac{Rf}{Rg + Rs \,||\, Rt} \times \frac{Rt}{Rs + Rt}$$

Gain equation includes the source and termination impedance

R1 = R3 + Rs || Rt = Rg
and
R2 = R4 = Rf

Once Rt is found, the required gain is found by Thevenizing the circuit. The circuit is broken between Rt and the amplifier's input resistor R3.

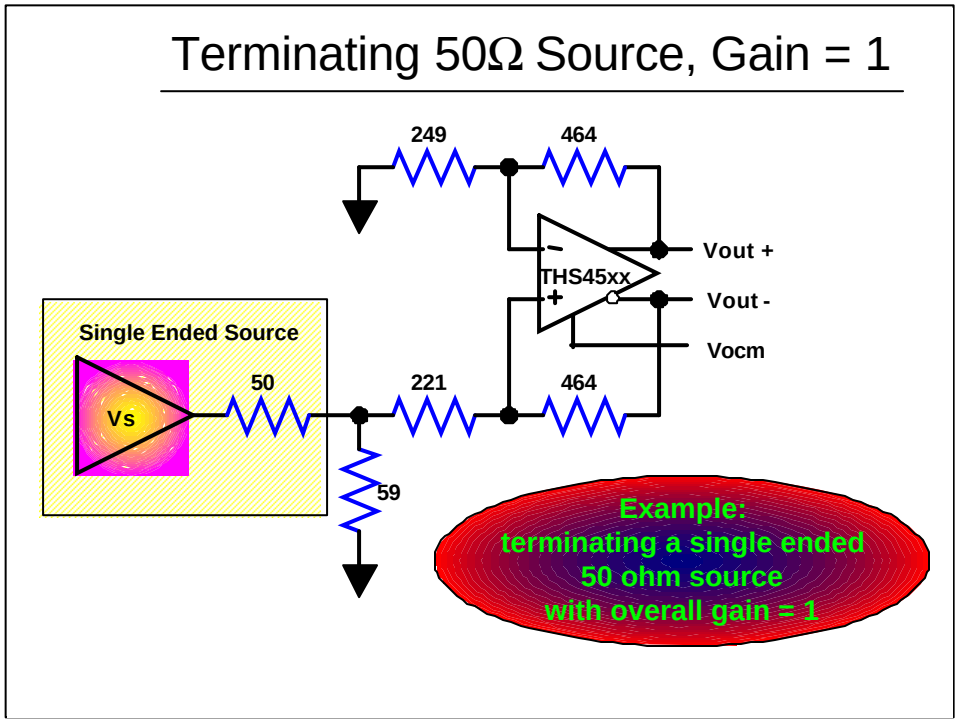
$Vth = Vs \times \frac{Rt}{Rt + Rs}$, and Rth = Rs || Rt.

The resulting Thevenin equivalent is shown. The gain is set on the upper side by: $\frac{Vout}{Vth} = \frac{R2}{R1}$, and on the lower side by: $\frac{Vout}{Vth} = \frac{R4}{R3 + (Rs \,||\, Rt)}$

where Vout = (Vout+) – (Vout-). Substituting for Vth, this becomes:

$$\frac{Vout}{Vs} = \frac{R2}{R1} \times \frac{Rt}{Rs + Rt} \quad \text{and} \quad \frac{Vout}{Vs} = \frac{R4}{R3 + (Rs \,||\, Rt)} \times \frac{Rt}{Rs + Rt}$$

For symmetry keep the gain equal on the two sides with R2 = R4 and R1 = R3 + (Rs || Rt).



As an example, suppose you are terminating a 50O single-ended source, and want an overall gain of one from the source to the differential output of the amplifier. Start the design by first choosing the value for R3, then calculate Rt and the feedback resistors. This will be seen to be an iterative process starting with some initial assumptions and then refined.

Start with the assumption that Rt = 50O and a gain of two will be required in the amplifier. Also, feedback resistor values of approximately 500O are reasonable for a high-speed amplifier. Using these starting assumptions, choose R1 = 249O and R3 = R1 – Rs || Rt = 249O – 25O = 224O . Next calculate Rt from the formula:

$$Rt = \frac{1 - \frac{K}{2(1+K)}}{\frac{1}{Rs} - \frac{1}{R3}} = \frac{1 - \frac{2}{2(1+2)}}{\frac{1}{50} - \frac{1}{224}} = 58.7\Omega$$

Now calculate the value of the feedback resistors:

$$R2 = \left(\frac{Vout}{Vs}\right)(R1)\left(\frac{Rs+Rt}{Rt}\right) = (1)\times(249)\times\left(\frac{50+58.7}{58.7}\right) = 460.9\Omega$$

$$R4 = \left(\frac{Vout}{Vs}\right)(R3 + Rs \parallel Rt)\left(\frac{Rs+Rt}{Rt}\right) = (1)\times(224 + 50 \parallel 58.7)\times\left(\frac{50+58.7}{58.7}\right) = 464.7\Omega$$

It can be seen that the process is iterative because the gain is not 2 as originally assumed, but rather 460.9 / 249 = 1.85, and Rt calculated to be 58.7O not 50O. Iterating through the calculations two more time results in: R3 = 221.9O (the closest standard 1% value is 221O), Rt = 59.0 (which is a standard 1% value), and R2 = R4 = 460.9 (the closest standard 1% value is 464O). Standard 1% resistor values are used in the solution shown.

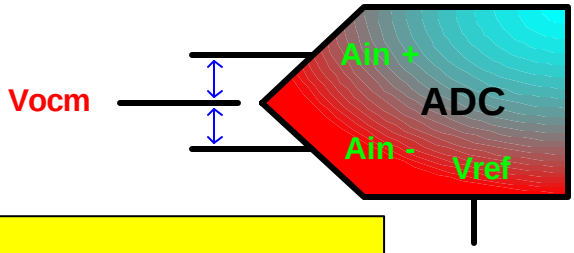
Using a spread sheet makes the iterative process described above a very simple matter. Also, component values can be easily adjusted to find a better fit to the standard available values.

Interfacing to ADCs

- Design issues:
  - Maximizing the ADC's dynamic range
  - Driving the Vocm pin
  - Not violating Vicr (SS issue)
  - Anti-alias filtering

Output Common Mode Voltage

To maximize dynamic range, Vocm must be set to the mid point between Vref + and Vref - of the ADC



$$\text{i.e. Vocm} = \frac{(\text{Vref}+) + (\text{Vref}-)}{2}$$

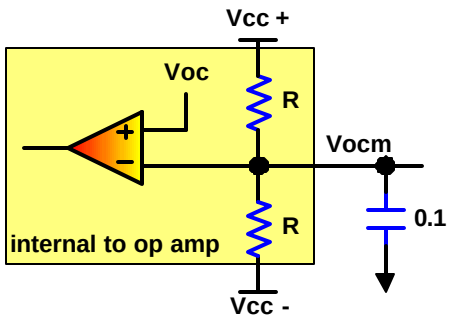
High-speed ADC inputs need symmetrical differential input signals to take advantage of the full dynamic range.

Typically the point of symmetry is half way between the voltage references, Vref + and Vref-. Driving the Vocm pin with this voltage insures the amplifier's output is centered on this same point.

Vref + defines the maximum input voltage on Ain + or Ain - for linear operation, and Vref - defines the minimum.

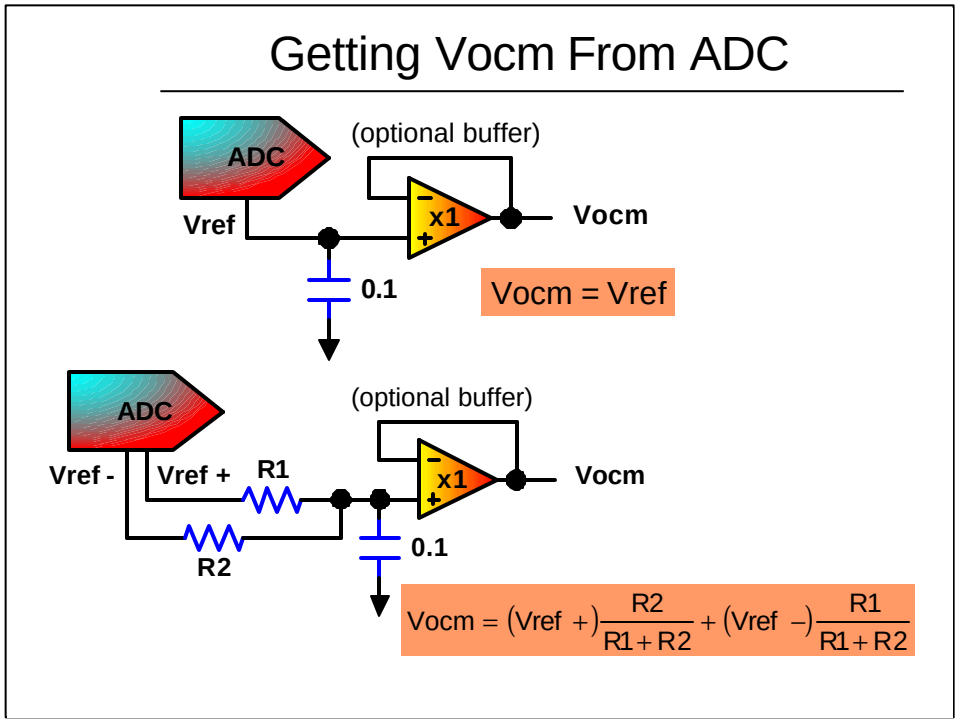
There are various methods for doing this.

Vocm Input

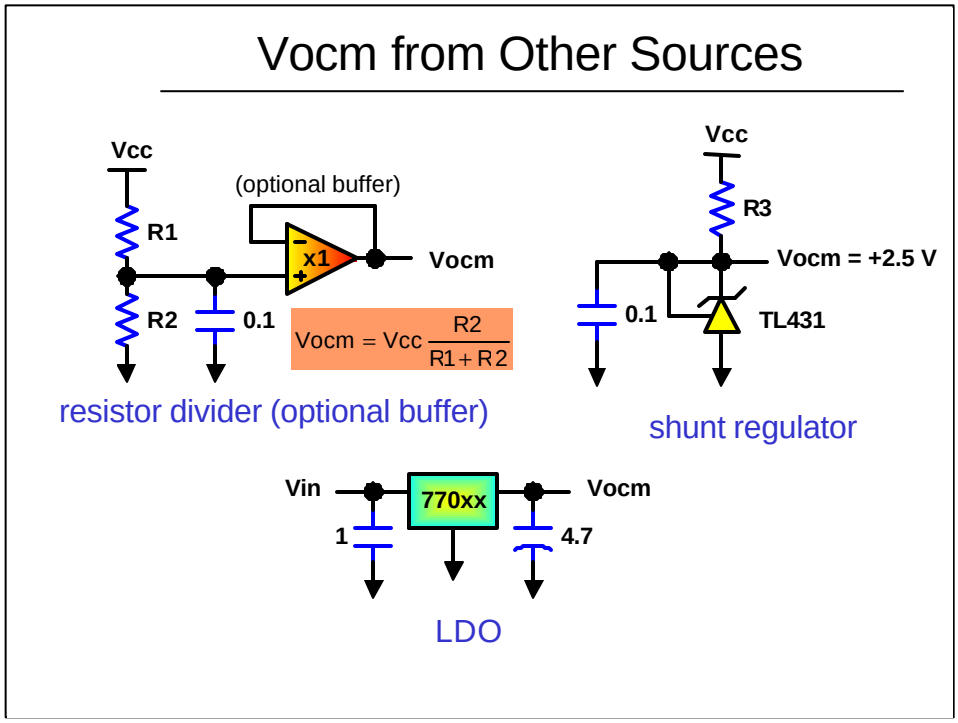


- With no input, Vocm is pulled to half way between power supply rails. Remember bypass capacitor.
- But what if this is not the right voltage?

An internal resistor divider between Vcc + and Vcc - sets Vocm half way between the power supply rails. If this is not the proper voltage, it can be over driven by an external source.



If the ADC has a voltage reference output, it can be used to drive the amplifier's Vocm pin. If not, the proper voltage can be derived from Vref + and Vref -. Buffering may be required, depending on the drive capability of the ADC.

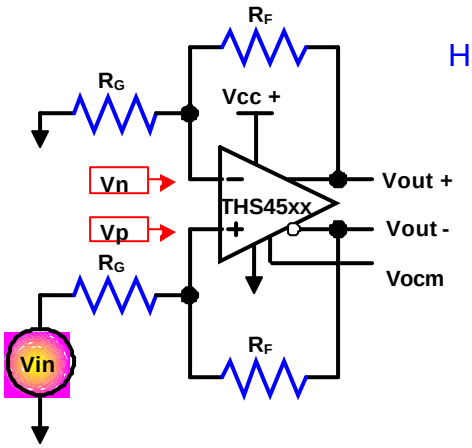


A resistor divider can be used to generate Vocm. The disadvantage to this solution is no power supply rejection. A buffer can be added as required.

Other alternatives are shunt regulators, small LDOs, or other voltage references. They provide both improved transient response and the ability to reject power supply variations.

Input Common Mode Voltage

Problem: single supply operation,
and gets worse at higher gains



Have to look at Vout + = Ain +
at maximum and minimum

$$Vn = (Vout+)\frac{R_F}{R_G + R_F}$$

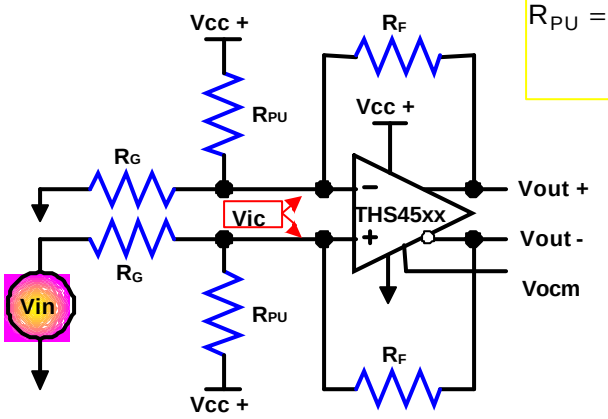
Vn = Vp = Vic

Nothing should be overlooked. It is obvious that the amplifier's output voltages must include the input voltage range of the ADC, but be certain to check for input voltage violations. A simple calculation of Vn with
Vout + set to its extreme values, Vref + and Vref -, will suffice.

Adjust Vic Using Pull-Up Resistors

Solution: use pull-up resistors

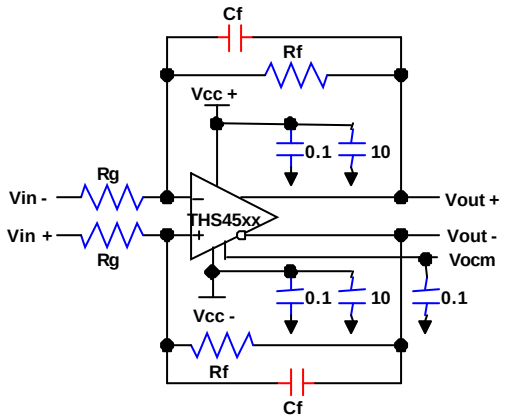
$$R_{PU} = \frac{Vic - (Vcc+)}{\frac{(Ain+_{(min)}) - Vic}{R_F} - \frac{Vic}{R_G}}$$



Products optimized for single supply operation such as THS4500/01 and THS4504/05

A problem with violating Vic can arise when operating from single supply and driving an ADC with high dynamic range. For example: driving the THS1206 with 4Vp-p input range. In this situation, pull-up resistors are the simplest method of adjusting Vic to be within specification.

1st Order Low-Pass Filter



$$\frac{Vout}{Vin} = \frac{Rf}{Rg} \times \frac{1}{1 + j2\pi f(RfCf)}$$

Vin = (Vin+) - (Vin-)
Vout = (Vout +) - (Vout -)

A major application for fully differential amplifiers is low-pass anti-alias filters for ADCs with differential inputs.

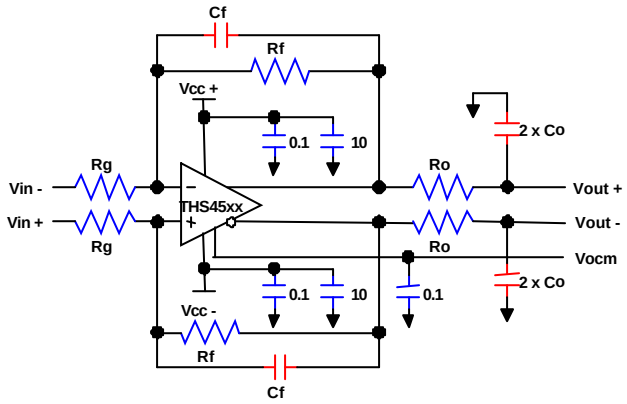
Creating an active 1st order low-pass filter is easily accomplished by adding capacitors in the feedback as shown. With balanced feedback, the transfer function is:

$$\frac{Vout}{Vin} = \frac{Rf}{Rg} \times \frac{1}{1 + j2\pi f(RfCf)}$$

where Vout = (Vout+) – (Vout-) and Vin = (Vin+) – (Vin-).

The pole created is a real pole on the negative real axis in the s-plane.

2nd Order LP Filter - Real Poles



$$\frac{Vout}{Vin} = \frac{Rf}{Rg} \times \frac{1}{1 + j2\pi f(RfCf)} \times \frac{1}{1 + j2\pi f \times 2 \times RoCo}$$

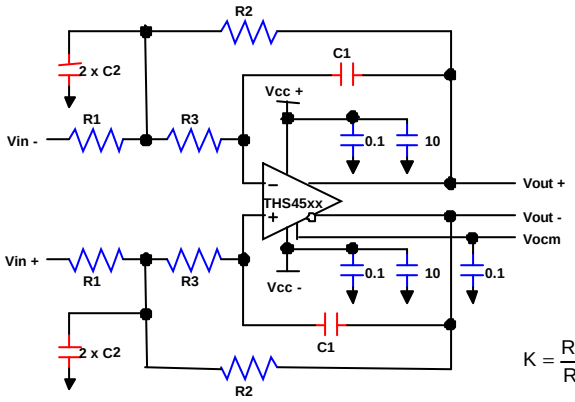
To create a two-pole low-pass filter, another passive real pole can be created by placing Ro and Co in the output as shown. With balanced feedback, the transfer function is:

$$\frac{Vout}{Vin} = \frac{Rf}{Rg} \times \frac{1}{1 + j2\pi f(RfCf)} \times \frac{1}{1 + j2\pi f \times 2 \times RoCo}$$

where Vout = (Vout+) – (Vout-) and Vin = (Vin+) – (Vin-).

The second pole created in the transfer function is also a real pole on the negative real axis in the s-plane. The capacitor, Co, can be placed differentially across the outputs as shown in solid lines, or two capacitors (of twice the value) can be place between each output and ground as shown in dashed lines. Typically, Ro will be a low value, and at frequencies above the pole frequency, the series combination with Co will load the amplifier. The extra loading will cause extra distortion in the amplifier's output. To avoid this, you might stagger the poles so that the RoCo pole is placed at a higher frequency than the RfCf pole. Then the amplifier's response is already rolling-off and the loading effect will not be as severe.

2nd Order LP Filter - Complex Poles



$$\frac{Vout}{Vin} = \left(\frac{K}{-\left(\frac{f}{FSF \times fc}\right)^2 + \frac{1}{Q}\frac{jf}{FSF \times fc} + 1} \right)$$

$$K = \frac{R2}{R1}$$

$$FSF \times fc = \frac{1}{2\pi\sqrt{2 \times R2R3C1C2}}$$

$$Q = \frac{\sqrt{2 \times R2R3C1C2}}{R3C1 + R2C1 + KR3C1}$$

The classic filter types like Butterworth, Bessel, Chebyshev, etc, (2nd order and greater) cannot be realized by real poles – they require complex poles. The multiple feedback (MFB) topology is used to create a complex pole pair, and is easily adapted to fully differential amplifiers as shown here.

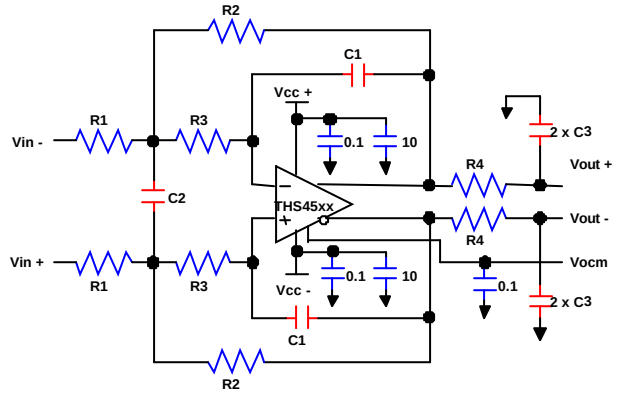
Capacitor C2 can be placed differentially across the inputs as shown in solid lines. Alternatively, for better common mode noise rejection, two capacitors of twice the value can be placed between each input and ground as shown in dashed lines.

In the transfer function shown, K sets the pass band gain, fc is the cut-off frequency of the filter, FSF is a frequency scaling factor, and Q is the quality factor.

$$FSF = \sqrt{Re^2 + |Im|^2} \quad \text{and} \quad Q = \frac{\sqrt{Re^2 + |Im|^2}}{2Re}$$

where Re is the real part, and Im is the imaginary part of the complex pole pair.

3rd Order Low-Pass Filter



$$K = \frac{R2}{R1}$$

$$\frac{Vout}{Vin} = \left(\frac{K}{-\left(\frac{f}{FSF \times fc}\right)^2 + \frac{1}{Q}\frac{jf}{FSF \times fc} + 1} \right) \times \left(\frac{1}{1 + j2\pi f \times 2 \times R4C3} \right)$$

$$FSF \times fc = \frac{1}{2\pi\sqrt{2 \times R2R3C1C2}}$$

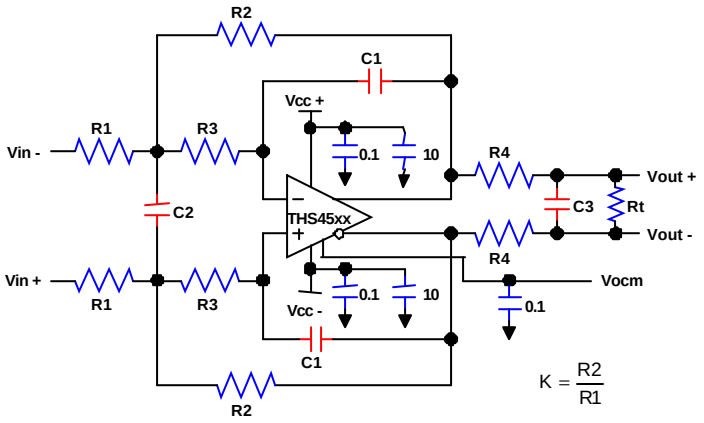
$$Q = \frac{\sqrt{2 \times R2R3C1C2}}{R3C1 + R2C1 + KR3C1}$$

A 3rd order filter is formed by adding R4(s) and C3 to the previous circuit. R4 and C3 are chosen to set the real pole in a 3rd order filter.

Capacitor C3 can be placed differentially across the outputs as shown in solid lines. Alternatively, for better common mode noise rejection, two capacitors of twice the value can be placed between each output and ground as shown in dashed lines.

Care should be exercised with setting this pole. Typically, R4 will be a low value, and at frequencies above the pole frequency, the series combination with C3 will load the amplifier. The extra loading will cause extra distortion in the amplifier's output. To avoid this, place the real pole at a higher frequency than the cut-off frequency of the complex pole pair.

3rd Order Filter with Termination



$$K = \frac{R2}{R1}$$

$$\frac{Vout}{Vin} = \left(\frac{K}{-\left(\frac{f}{FSF \times fc}\right)^2 + \frac{1}{Q}\frac{jf}{FSF \times fc} + 1} \right) \times \left(\frac{\frac{Rt}{2R4 + Rt}}{1 + j2\pi f \times C3 \times (2R4 \,||\, Rt)} \right)$$

$$FSF \times fc = \frac{1}{2\pi\sqrt{2 \times R2R3C1C2}}$$

$$Q = \frac{\sqrt{2 \times R2R3C1C2}}{R3C1 + R2C1 + KR3C1}$$

Taking into the effects of termination resistance adds a slight twist to the previous equations.

Example: 1MHz Butterworth

Set R2=R, R3=mR, C1=C, and C2=2n x C

$$FSF \times fc = \frac{1}{2\pi RC\sqrt{2n \times m}} \qquad Q = \frac{\sqrt{2n \times m}}{1 + m(1 - K)}$$

Fully Differential MFB, 2nd order low pass Butterworth, R2=R, R3=mR, C1=C, C2=nC and K= 1									
Set up			Calculate Component Values					Back Calculate	
Fc	Q	C1	C2	R1 & R2	stnd value	R3	stnd value	Fc	Q
1.00E+06	0.707	1.00E-10	2.20E-10	7.868E+02	787	7.319E+02	732	999,657	0.707
m and n calculations									
	Course				Fine				
m	2n	Q		m	2n	Q			
0.5	4.4	0.74162		0.9	4.4	0.7107053			
0.6	4.4	0.738549		0.91	4.4	0.7095744			
0.7	4.4	0.731247		0.92	4.4	0.7084381			
0.8	4.4	0.721602		0.93	4.4	0.7072969			
0.9	4.4	0.710705		0.94	4.4	0.7061513			
1	4.4	0.699206		0.95	4.4	0.7050017			
1.1	4.4	0.6875		0.96	4.4	0.7038484			

$FSF \times fc = \frac{1}{2\pi RC\sqrt{2n \times m}}$

$Q = \frac{\sqrt{2n \times m}}{1 + m(1 - K)}$

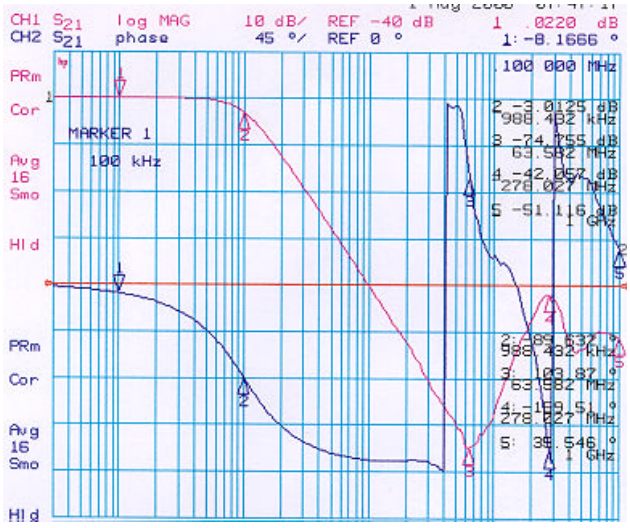
Setting the filter components as ratios where R2=R, R3=mR, C1=C, and C2=nC, results in:

$$FSF \times fc = \frac{1}{2\pi RC\sqrt{2n \times m}} \quad \text{and} \quad Q = \frac{\sqrt{2n \times m}}{1 + m(1 - K)}$$

Start the design by determining the ratios, m and n, required for the gain and Q of the filter type being designed, then select C, and calculate R for the desired fc.

Using a spread sheet eases the computational tasks, and reduces errors.

1Mhz Butterworth - THS4141



R1 = 787 Ω

R2 = 787 Ω

R3 = 732 Ω

R4 = 50 Ω

C1 = 100 pF

C2 = 220 pF

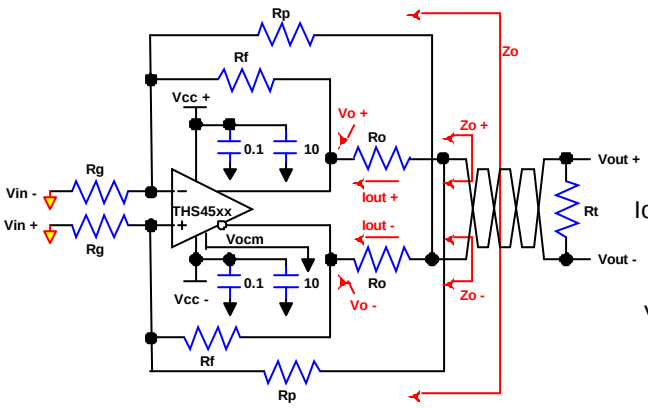
C3 = 100 pF

The gain and phase response of a 2nd order Butterworth low-pass filter with corner frequency set at 1MHz, and the real pole set by R4 and C3 at 15.9MHz. The components used are: R1 = 787O, R2 = 787O, R3 = 732O, R4 = 50O, C1 = 100pF, C2 = 220pF, C3 = 100pF, and the THS4141 fully differential amplifier. At higher frequencies, parasitic elements allow the signal to feed-through.

Line Driving

- Double termination is commonly used in high-speed systems to increase signal integrity
- Synthesized output impedance reduces power supply requirements
- How does synthesized output impedance work?

Synthesized Output Impedance



$$Zo+ = \frac{Vout+}{Iout+} \parallel Rp$$

$$Iout+ = \frac{(Vout+) - (Vo+)}{Ro}$$

$$Vo+ = (Vout-) \times \left(\frac{-Rf}{Rp}\right)$$

$$Zo\pm = \frac{Ro}{1 - \frac{Rf}{Rp}} \parallel Rp$$

$$A = \frac{Vout}{Vin} = \frac{Rf}{Rg} \times \frac{1}{\frac{2Ro + Rt \parallel 2Rp}{Rt \parallel 2Rp} - \frac{Rf}{Rp}}$$

Driving transmission lines differentially is a typical use for fully differential amplifiers. By using positive feedback, the amplifiers can be used to provide active termination as shown. The positive feedback makes the output resistor appear to be a value larger than what it actually is when viewed from the line. The voltage dropped across the resistor depends on its actual value. The result is increased efficiency, and reduced power supply requirements.

With double termination, the output impedance of the amplifier, Zo, will equal the characteristic impedance of the transmission line, and the far end of the line will be terminated with the same value resistor i.e. Rt = Zo. For proper balance, ½Zo is placed in each half of the differential output, so that Zo = 2 x Zo±.

To calculate the output impedance ground the inputs, insert either a voltage or current source between Vout+ and Vout-, and calculate the impedance from the circuit's response.

Due to symmetry, Zo+ = Zo-, Vout+ = -(Vout-), and Vo+ = -(Vo-). Calculating the impedance of one side provides the solution.

Example: Synthesized Impedance

- Given:
  - Gain of 1
  - Zo = 100Ω
- Choose:
  - Rf = 1kΩ
  - Ro = 10Ω

$$Rp = \frac{Rf - Ro}{1 - \frac{Ro}{Zo\pm}} = \frac{990\Omega}{1 - \frac{10\Omega}{50\Omega}} = 1237.5\Omega \Rightarrow 1.24k\Omega$$

$$Rg = \frac{Rf}{A} \times \frac{1}{\frac{2Ro + Rt \,||\, 2Rp}{Rt \,||\, 2Rp} - \frac{Rf}{Rp}} = \frac{1k\Omega}{\frac{20\Omega + 100\Omega \,||\, 2.48K}{100\Omega \,||\, 2.48K} - \frac{1k\Omega}{1.24k\Omega}} = 2490\Omega \Rightarrow 2.49k\Omega$$

$$Zo+ = \frac{Vout+}{Iout+} \qquad Iout+ = \frac{(Vout+) - (Vo+)}{Ro} \qquad Vo+ = (Vout-) \times \left(\frac{-Rf}{Rp}\right)$$

Looking back into the amplifier's outputs, the impedance seen by each side of the line will be the value of Ro divided by 1 minus the gain from the other side of the line:

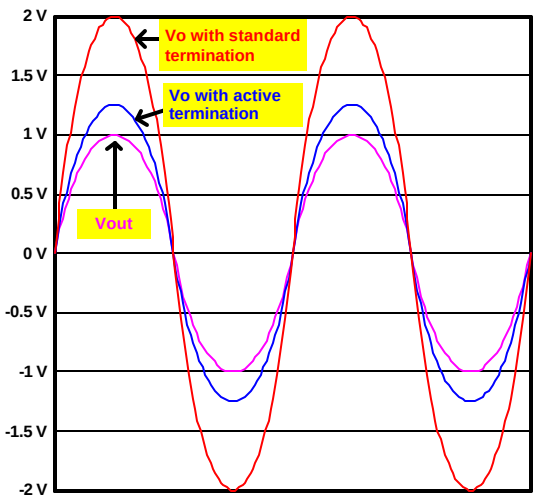
$$Zo\pm = \frac{Ro}{1 - \frac{Rf}{Rp}}$$

The positive feedback also affects the forward gain. Accounting for this affect and the voltage divider between Ro and Rt||2Rp, the gain from Vin = (Vin+) – (Vin-) to Vout = (Vout+) – (Vout-) is:

$$A = \frac{Vout}{Vin} = \frac{Rf}{Rg} \times \frac{1}{\frac{2Ro + Rt \,||\, 2Rp}{Rt \,||\, 2Rp} - \frac{Rf}{Rp}}$$

Design is easily accomplished by first choosing the value of Rf and Ro. Then calculate the required value of Rp to give the desired Zo. Then calculate Rg for the required gain.

Example: Synthesized Impedance



Termination	Power
Standard	20.00mW
Active	6.25mW

69% less power wasted

Lower power supply requirements

For example: Given you want a gain of 1, and to properly terminate a 100O line with Rf = 1kO and Ro = 10O. The proper value for Zo and Rt is 100O (Zo± = 50O). Rearranging the equations gives:

$$Rp = \frac{Rf}{1 - \frac{Ro}{Zo\pm}} = \frac{1k\Omega}{1 - \frac{10\Omega}{50\Omega}} = 1.25k\Omega$$

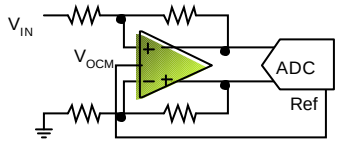
$$Rg = \frac{Rf}{A} \times \frac{1}{\frac{2Ro + Rt \,||\, 2Rp}{Rt \,||\, 2Rp} - \frac{Rf}{Rp}} = \frac{1k\Omega}{\frac{20\Omega + 100\Omega \,||\, 2.5K}{100\Omega \,||\, 2.5K} - \frac{1k\Omega}{1.25k\Omega}} = 2.45k\Omega$$

The circuit is built and tested with the nearest standard values to those computed above: Rf = 1KO, Rp = 1.24kO, Rg = 2.43kO, Rt = 100O, and Ro = 10O. Compare the output voltage waveforms (Vout = 2Vp-p) with active termination and standard termination shown (Vo = (Vo+) – (Vo-) and Vout = (Vout+) – (Vout-)). For standard termination, Rf = 1KO, Rp = open, Rg = 499O, Rt = 100O, and Ro = 50O.

20mW of power is dissipated in the output resistors with standard termination, as opposed to 6.25mW with active termination - 69% less.

Another feature about active termination that is very attractive in low-voltage applications is the effective increase in output voltage swing for a given supply voltage.

TI's Fully Differential Amplifiers

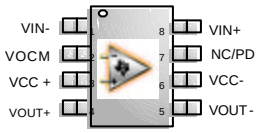


- Key Benefits
  - **Simplifies Single-Ended to Differential Conversion**
  - **Can be DC Coupled**
  - **Vocm pin sets output Common-mode**
  - **Powerdown feature on all devices**
    - **THS41x0**
  - **THS412x in CMOS process**
    - **Low Power applications, 3V only**
    - **Rail-to-rail output**
  - **THS413x for low noise applications**

Part	$BW_{(-3dB)}$ (MHz)	SR (V/µs)	$t_{S\ (0.1\%)}$ (ns)	$THD_{(1MHz)}$ (dBc)	V_n (nV/√Hz)	I_O (mA)	V_{IO} (mV)	I_S (mA)	V_S (V)	Package
THS4120 / 4121	100	43	82	-71	3.7	100	8	5.6	**3.0 - 3.6**	D, DGN
THS4130 / 4131	150	51	78	-80	**1.3**	85	2	14	+5 - ±15	D, DGN
THS4140 / 4141	160	450	96	-79	6.5	85	7	15	+5 - ±15	D, DGN
THS4150 / 4151	150	**650**	53	-84	7.6	85	7	17.5	+5 - ±15	D, DGN

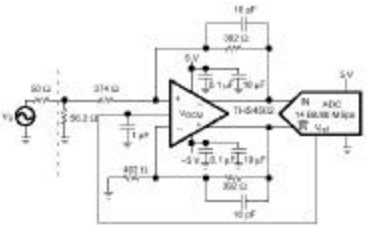
THS4500/01, THS4502/03

Fully Differential Amplifiers



Features

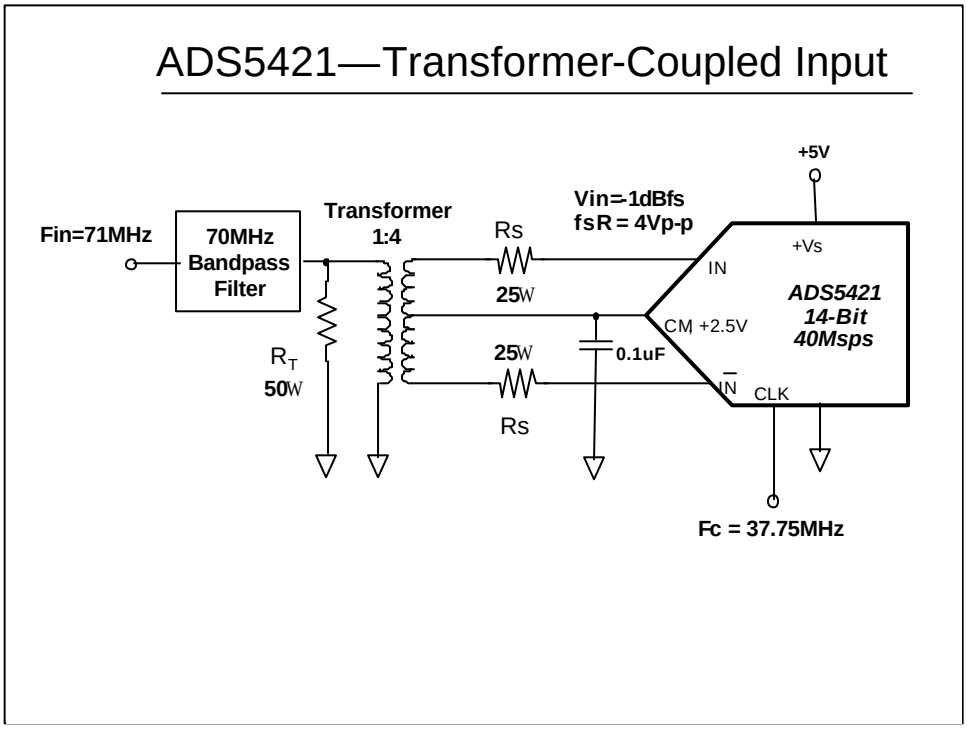
- **Differential Input / Differential Output**
- **Differential Reduced Second Harmonic Distortion**
- **THS4500/02/04 has Powerdown mode**
- **8-pin SOIC, MSOP available now**
  - **Leadless MSOP soon to come**
- **THS4500/01/04/05 with Common-mode range to negative rail for single-supply applications**
- **THS4504/05 is sampling now, release in August**



Competition:

- **AD8138, AD8132, AD8131(G=2)**

Part	$BW_{(-3dB)}$ (MHz)	SR (V/µs)	$V_{ICR(+/-5V)}$ (V)	$THD_{(30MHz)}$ (dBc)	$IMD3_{(50MHz)}$ (dBc)	V_n (nV/√Hz)	I_b (mA)	V_D (mV)	I_S (mA)	V_S (V)
THS4500 / 4501	370	2800	-5.5 - +2.5	-70	-84	7	120	4	23	+5 - ±5
THS4502 / 4503	370	2800	-3.7 - +3.7	-74	-84	6.8	120	1	23	+5 - ±5
THS4504 / 4505	260	1800	-5.7 - +2.6	-65	-78 (@20)	8	120	4	18	+5 - ±5



This slide shows a simple configuration employing a transformer to convert the single-ended input signal into a differential signal suitable to drive the A/D converter. The transformer also allows the common-mode voltage to be directly applied to the center tap of the secondary side.

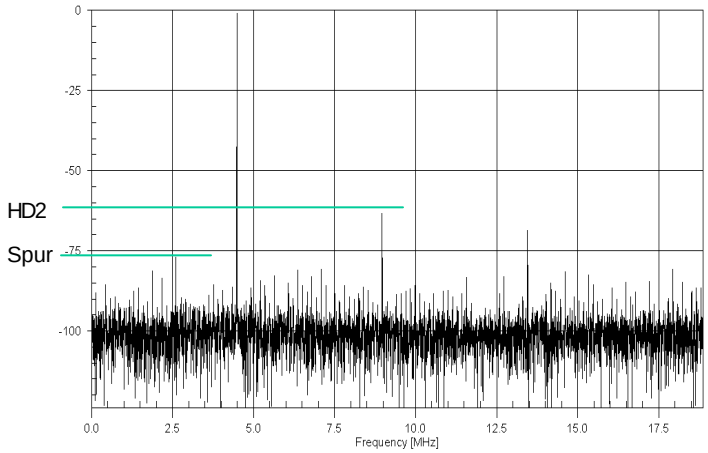
The 71-MHz input signal, in this case coming from a signal generator, was filtered using a 70-MHz bandpass filter.

The signal was undersampled with the ADS5421, a 14-bit pipeline converter clocked at 37.75 MHz.

Note:Value of input series resistors, Rs, are not important for impedance matching (50 Ω). Value depends on the converter model and input frequency.

Choosing a step-up transformer, this 1:4 model offers a voltage gain of 1:2, V_{IN}:V_{OUT}.

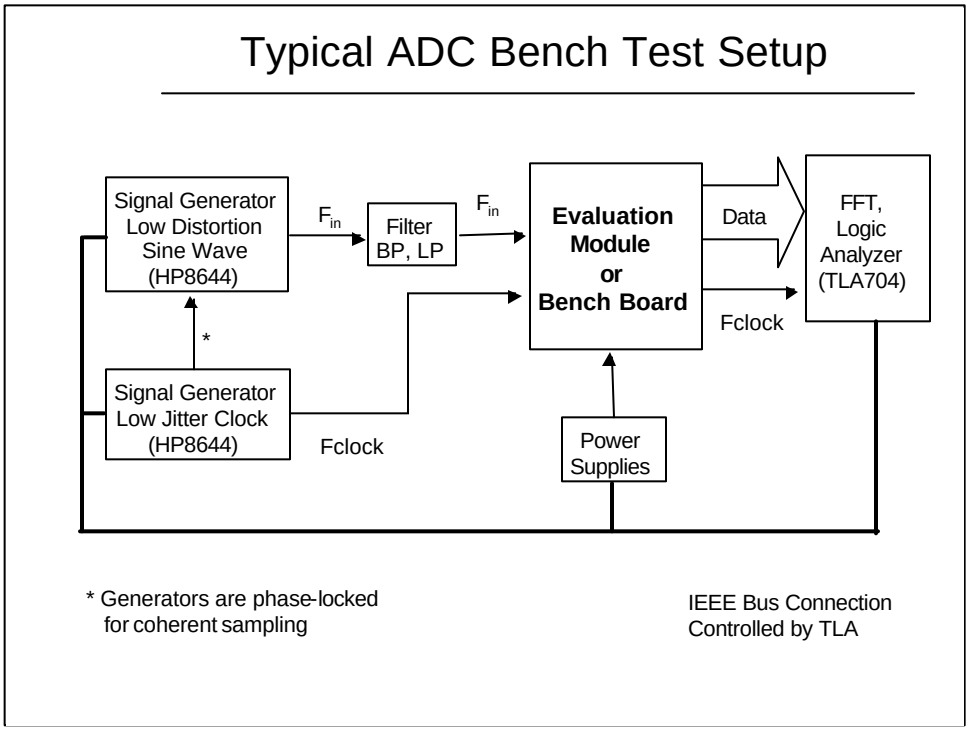
ADS5421 at F_{IN} = 71 MHz, FFT Result



- Fc = 37.75 MHz
- F = 4.483 MHz at -1 dBfs
- SNR = 61.9 dBc
- HD2=63.3 dB at 8.966 MHz
- Worst Other Spur = -77 dB

This is the FFT of the previous circuit example. The dynamic range over the full Nyquist range (0 to 19 MHz) is dominated by the second harmonic, which is located at approx. 8.9 MHz. During subsequent digital processing, this known harmonic may be filtered out. Then, the remaining highest spurs, sometimes referred to as 'Worst other spur' can be used to define the dynamic range. In this case, the resulting dynamic range will be 77 dB.

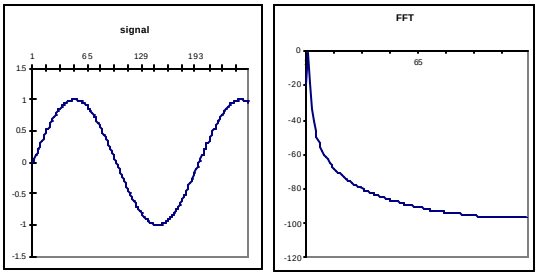
The signal-to-noise ratio, SNR, is close to a 12-bit effective resolution. Note that this is also calculated based on the noise power of the full Nyquist bandwidth.



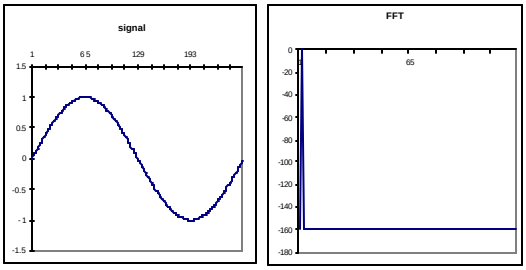
Equipment and configuration of a typical bench test set-up for high-speed A/D converter testing. One critical element is a very low jitter signal generator for the clock. The generator should also have a very high frequency resolution to perform coherent sampling and avoid windowing on the FFTs.

Coherent Sampling

Non-Coherent Sampling



Coherent Sampling



Coherent sampling simply means making sure that an integer number of cycles of the input signal are captured in the input data buffer. Since the FFT assumes that the signal in its input buffer is a continuous signal, if the endpoints of the waveform don't line up, the energy in the signal is spread over many frequency bins, giving the impression that the input signal has considerable harmonic distortion.

In the first graph above, a non-integer number of cycles of the waveform is captured in the data set. The resulting FFT appears to have energy in many frequency bins. In order to "fix" this dataset, a "window" would have to be applied to the data – this mathematical function would force the endpoints to line up and help prevent this spreading. But windowing introduces errors of its own.

So the preferred method is to have a signal generator that we can phase-lock to the sample frequency so that we can cause the dataset to contain only an integer number of cycles of the input signal – preferably a prime number of cycles – and the resulting FFT, as shown in the second graph, clearly shows the energy in the signal where it actually is. No windowing is required with coherent sampling.

Time Domain Effects of Sampling Clock

- Jitter is the time domain representation of clock noise
- Aperture Jitter = The rms variation in the aperture delay due to random noise effects
- Aperture Jitter influences achievable SNR:

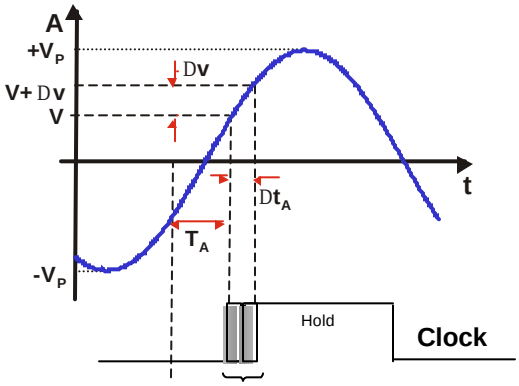
$$SNRj = 20\log 1 / (2\pi \times F_{IN} \times taj) \; ; \quad taj = \text{rms aperture jitter}$$

- Aperture Delay = usually a constant

The higher the input frequency, $f_{in,}$ the higher the jitter contribution to the SNR.

Aperture Delay = The time delay between the external sample command (typically the 50% point of the rising clock edge) and the time at which the signal is actually captured. Clock path propagation delays contribute (inside the IC) to aperture delay.

Aperture-Jitter (Sampling Uncertainty)



The Aperture Error is less than 1 LSB, if:

$$\Delta t_A < \frac{1}{2^n \times p \times f_{max}}$$

$\Delta ta_{p\text{-}p}$ = Aperture Jitter

Error due to Aperture-Jitter is directly proportional to dv/dt of input signal

$\Delta v = dv/dt \times \Delta t_A$

Aperture Jitter (Sampling Uncertainty)

A parameter which may decrease the SNR of the system is caused by the sampling uncertainty, or the Aperture-Jitter. If the aperture time varies by the time Δt_A, an error is caused which is equal to the change Δv in the voltage. This results into a degradation of the SNR of an ADC. To calculate the maximum time Δt_A which results into an error less than 1 LSB, a sine wave with the maximum frequency f_{max} as an input signal is considered. This can be expressed as:

$$v(t) = V_P \times \sin \omega t$$

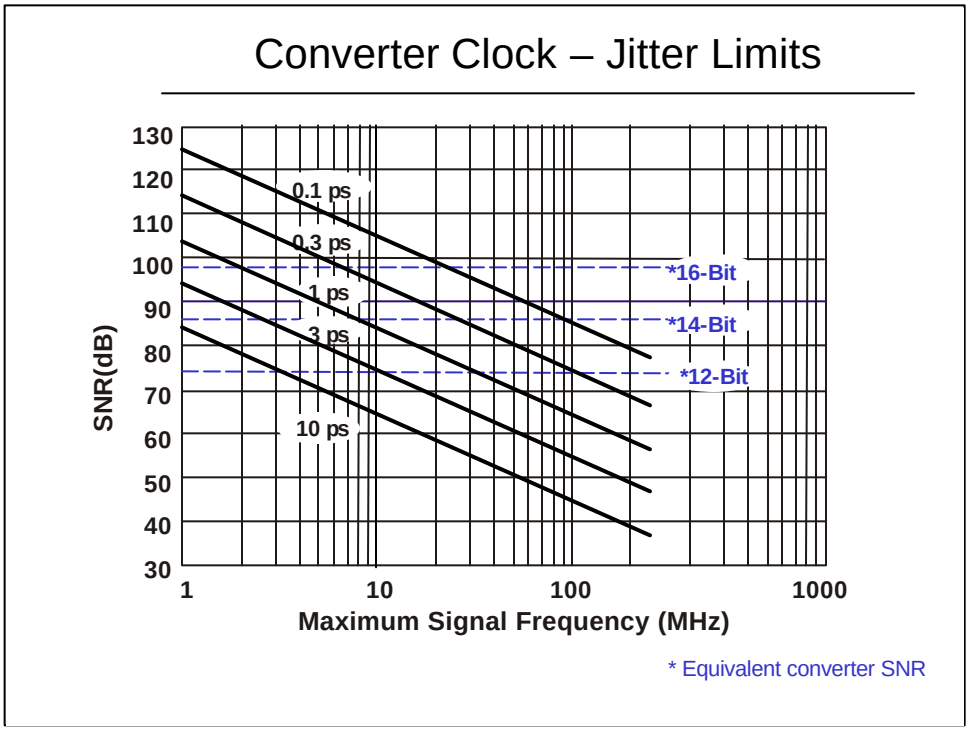
The slope of the sine signal is: $\frac{dv}{dt} = V_P \times \varpi \times \cos \varpi t$

The maximum slope occurs when $\cos \varpi t = 1$ or at the zero-crossing point. This results in:

$$\Delta t_A < \frac{1}{(2^n) \times \pi \times f_{max}}$$

In order to limit the error in the change of the voltage to less than 1 LSB (1 LSB can be expressed as $\frac{2V_P}{2^n}$), Δt_A results in:

$$\Delta t_A = \frac{\Delta v}{V_P \times \varpi}$$



A chart like this can be used to estimate the achievable SNR as a function of the clock jitter and over a range of signal frequency.

Clock Considerations for Undersampling

- Clock quality becomes major factor for Undersampling
  - Very low jitter required to maintain good SNR
    - Independent jitter sources sum by Root-Sum Square
      tajtot = $\sqrt{\text{(taj-ADC 2 + taj-Ext 2)}}$, in psrms
  - Fast rise/fall times
  - Duty cycle (50%) less important, if A/D operated below max. sampling speed
  - Use proper termination techniques to avoid reflection

The slew rate (dv/dt) of undersampled input signals are very high. Consequently, the effect of clock jitter is pronounced and therefore requires special consideration.

Dividing a higher frequency clock can be beneficial; however, each additional logic gate, etc. can potentially add to the total jitter. Since jitter is a random occurrence and sources are typically not correlated, they add by calculating the square-root of the sum of the squares.

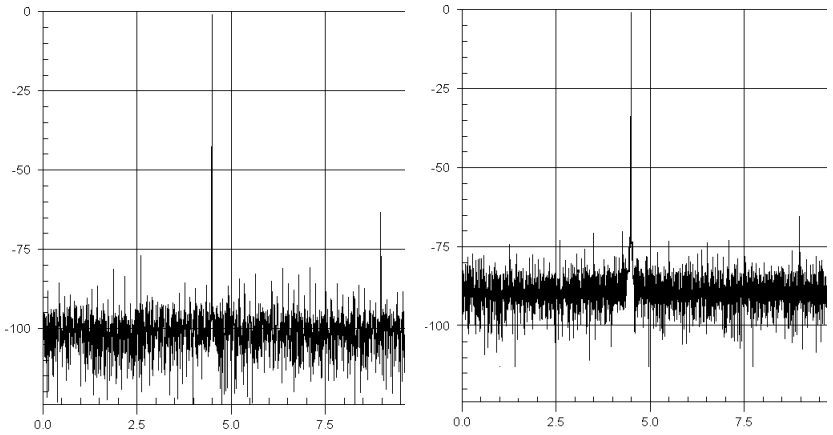
Consider using logic circuits that have sufficiently fast rise and fall times (1 ns) so they do not contribute to the jitter error.

The duty cycle requirement for the A/D converter clock may be relaxed, meaning it can vary from the ideal 50% point, if the converter is operated below its maximum sampling rate.

Clock Jitter Effects

Comparison of different clock sources

For Undersampling, the converter clock is as critical as the LO for an analog mixer



Good clock source

Not so good clock source

For this rather crude comparison the setup of the ADS5421 was used. The converter is digitizing at 37.75 Msps with an input frequency of approximately 71 MHz (-1dBfs). Both FFTs with 8k points.

In this undersampling situation it becomes critical to understand the impact of the clock source's jitter performance.

Since the jitter of the clock essentially translates into the achievable SNR, a side-by-side comparison of the FFT plots makes it relatively simple to make a quantitative assessment by comparing the noise floor. As can be seen in this example, a good clock source, like the HP8644, results in a lower noise floor than a not so good clock source (HP3325).

Also, the skirt on the fundamental exhibits a somewhat wider spread, indicating a reduced frequency resolution. The system uses coherent sampling and the clocks of the generators are phase locked together.

Notes on Jitter and Clock 1

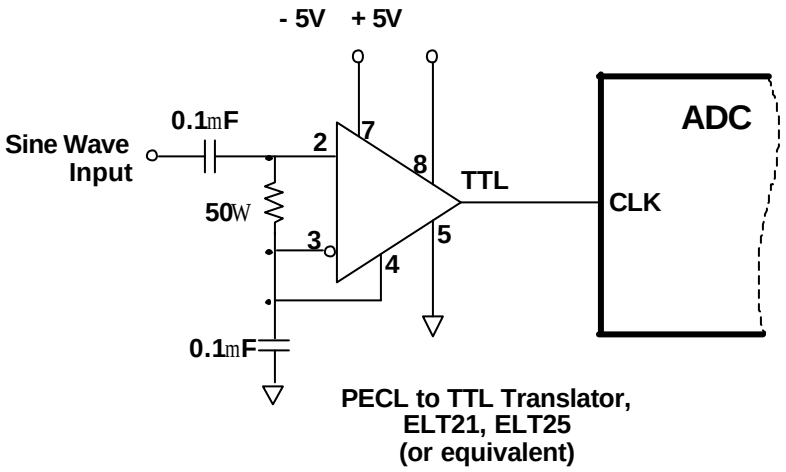
- If the noise floor (SNR) appears to be higher than expected when evaluating a high-speed converter (FFT plot), check the jitter contribution of the clock source
- Typically, higher frequency crystal clocks (fc >10 MHz) have low jitter of below 10 ps rms
- Lower frequency clocks usually have higher jitter
- Therefore, consider a higher Fc and divide down

Notes on Jitter and Clock 2

- Clocks from microcontrollers, DSPs etc., are usually not suitable for high-speed converters, especially not for undersampling applications
- Noise on the ADC power supply directly affects the internal clock circuitry and may lead to increased jitter
- Noise and spurs on the clock will be ‘mixed’ during sampling and lead to a decrease in dynamic range
- Many A/D converters now feature differential clock input designed for sine and square wave inputs

Clock Input #1

Sine Wave-to-TTL Conversion, Single-ended

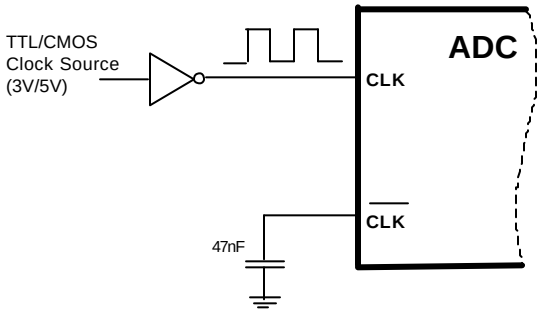


A standard application problem for basically all high-speed A/D converters is that they are sensitive to the clock quality. Clock jitter can easily become the main error source in a system and manifests itself in poor signal-to-noise readings. If your system exhibits SNR below expectations, the clock jitter should be investigated.

Low jitter crystal-controlled oscillators usually make very good clock sources, but they only come in discrete frequency ranges. If a flexible clock source is required, usually during evaluation of the converter, the circuit shown here can be employed. This circuit uses a PECL-to-TTL translator to convert from a sine wave source to a low-jitter TTL clock signal. The given circuit works consistently with low-level inputs (0 dBm), but is somewhat sensitive to jitter from the source itself. Increasing the level will help minimize this effect. If available, sine wave generators like the HP8644 or the Fluke 6080A, are good choices.

Clock Input #2

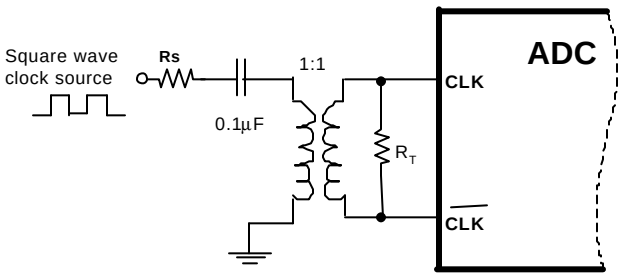
TTL/CMOS clock, Single-ended



In the event the A/D converter has a differential clock interface it is usually still possible to run the converter directly from a single-ended clock source. The other unused clock pin typically requires ac-grounding. However, it is necessary to read the specific application recommendation from the manufacturer.

Clock Input #3

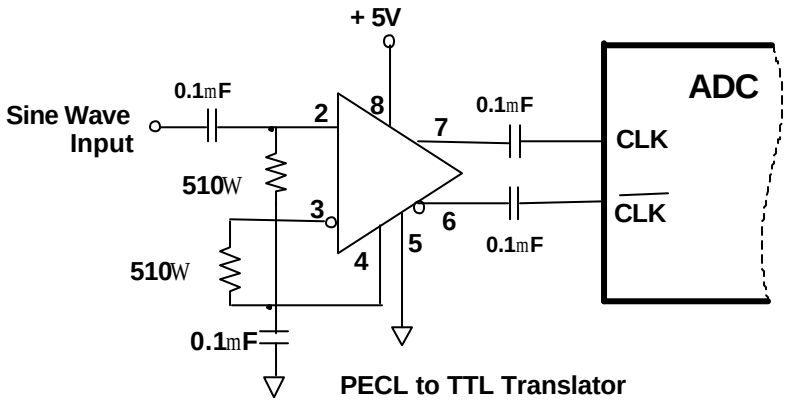
SE to Differential using Transformer



High-speed A/D converters that feature a differential clock input require a differential clock to achieve maximum performance. An RF transformer can be used here to convert a single-ended source into a differential source.

Clock Input #4

Sine Wave-to-TTL Conversion, Differential



This circuit is similar to the one shown as example #1, but uses a different type of PECL translator IC to produce a differential clock signal. This can then be ac-coupled directly to the A/D converter.

Undersampling—Summary

- A/D converter available to be used for Undersampling
- Converter specifications need to be examined and understood
- Focus on the analog front-end/driver circuit
- Front-end configuration largely depends on the individual application and system requirements
- Clock becomes one of the most critical issues
- Others are: proper high-speed pcb layout along with grounding and bypassing

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third–party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265