JESD204B Deterministic Latency

Texas Instruments High Speed Data Converter Training

Overview

- Latency in a JESD204B Link
- Deterministic Latency (DL) Definition
- Guaranteeing DL
- Designing for DL
- Verifying DL

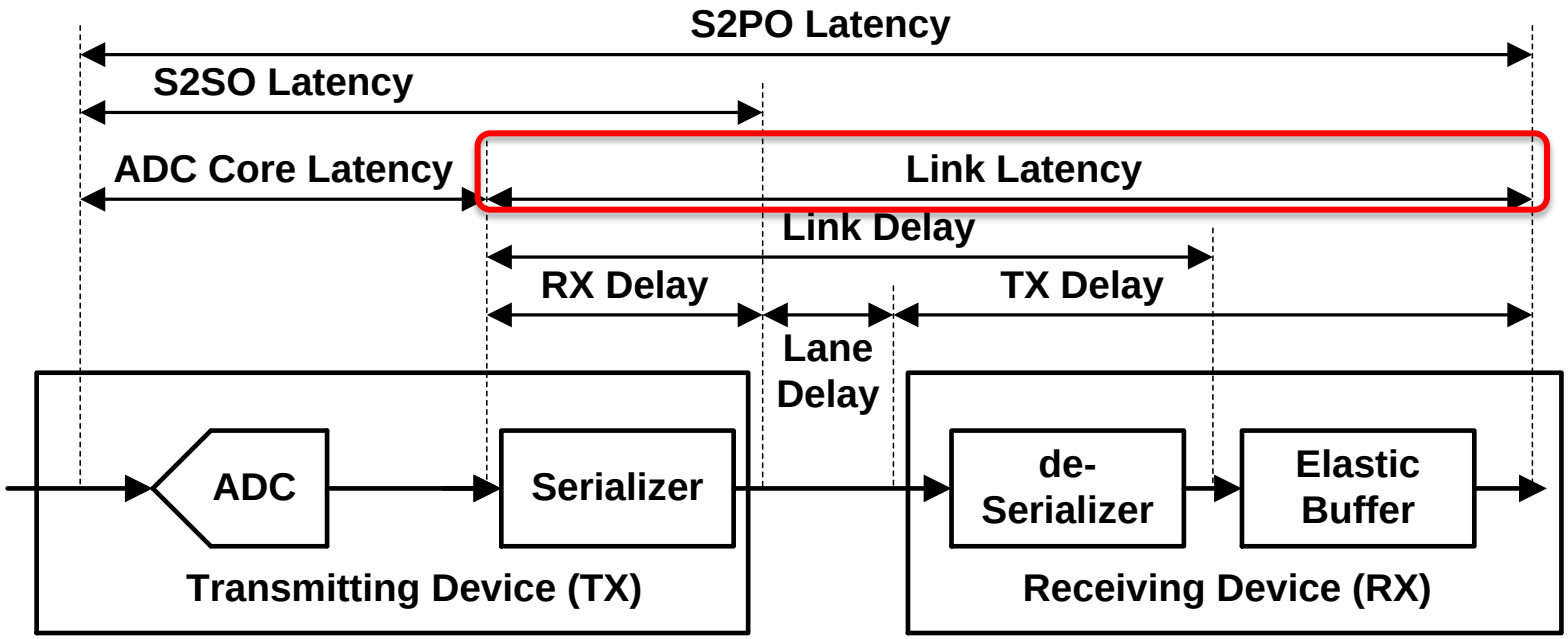
Latency in a JESD204B Link

What is Latency?

- Latency is defined as the total time (in seconds or clock cycles) it takes a signal to travel from Point A to Point B
- For Example:
  - Point A might be the input to the ADC
  - Point B might be the output of the DAC
- In a JESD204B link:
  - Point A is the input to the JESD204B transmitter
  - Point B is the output of the JESD204B receiver's elastic buffer

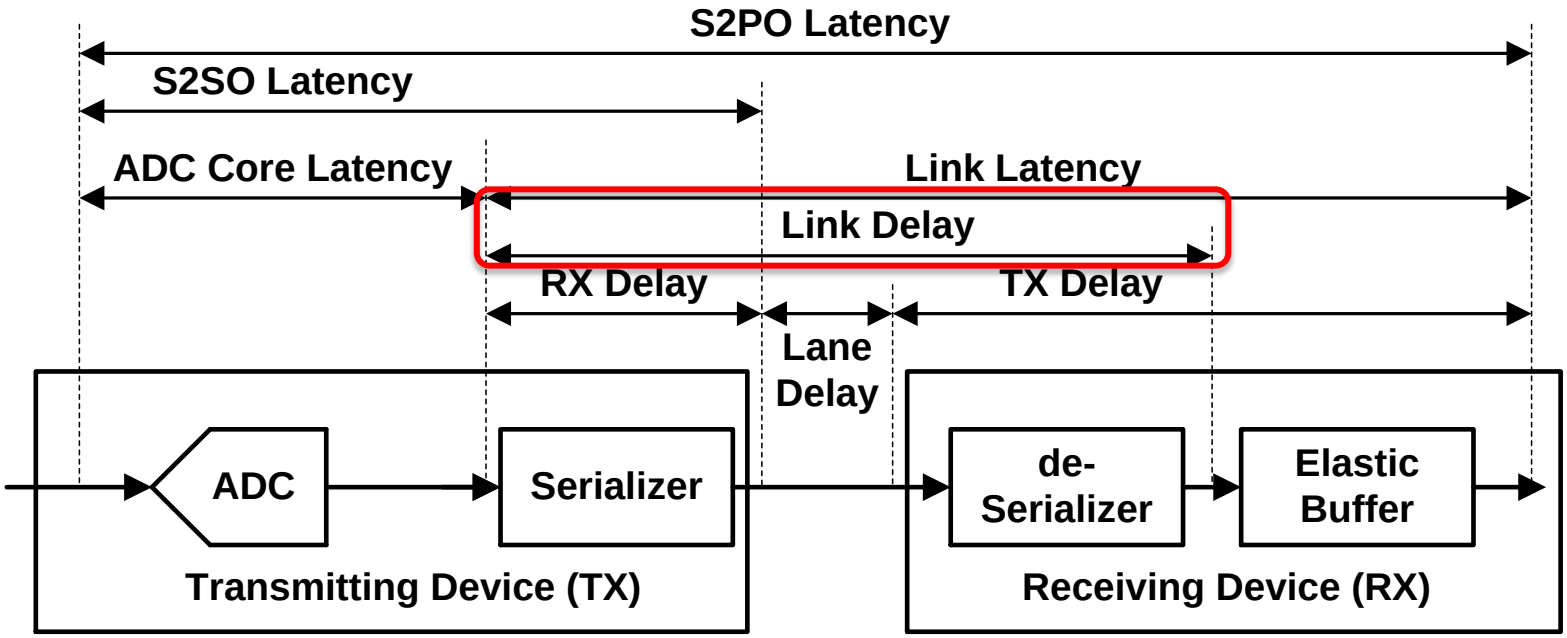
Latency Definitions

Link Latency — the latency from when the sampled parallel data is input to the serializer at the transmitter (ADC/FPGA) until the same data is available in parallel form at the output of the elastic buffer in the receiver (FPGA/DAC)



Latency Definitions

Link Delay — delay from when the sampled parallel data is input to the serializer at the transmitter (ADC/FGPA) until the same data is presented at the input to the elastic buffer in the receiver (FPGA/DAC)



Factors That Influence Latency or Delay

TX/RX Device Dependent
Link Layer Digital Implementation Delays
(De-)Serializer Implementation Delays
Internal SYSREF Delays
Data Converter Core Latency
Signal Path Processing (i.e. DDC)
Signal Path Buffering

Clock Device Dependent
Device Clock Launch Alignment
SYSREF Launch Alignment
SYSREF Pulse Characteristics

PCB Dependent
Data Channel Propagation Delay
Device Clock Propagation Delay
SYSREF Propagation Delay

PVT Dependent
Process
Voltage Supplies
Temperature

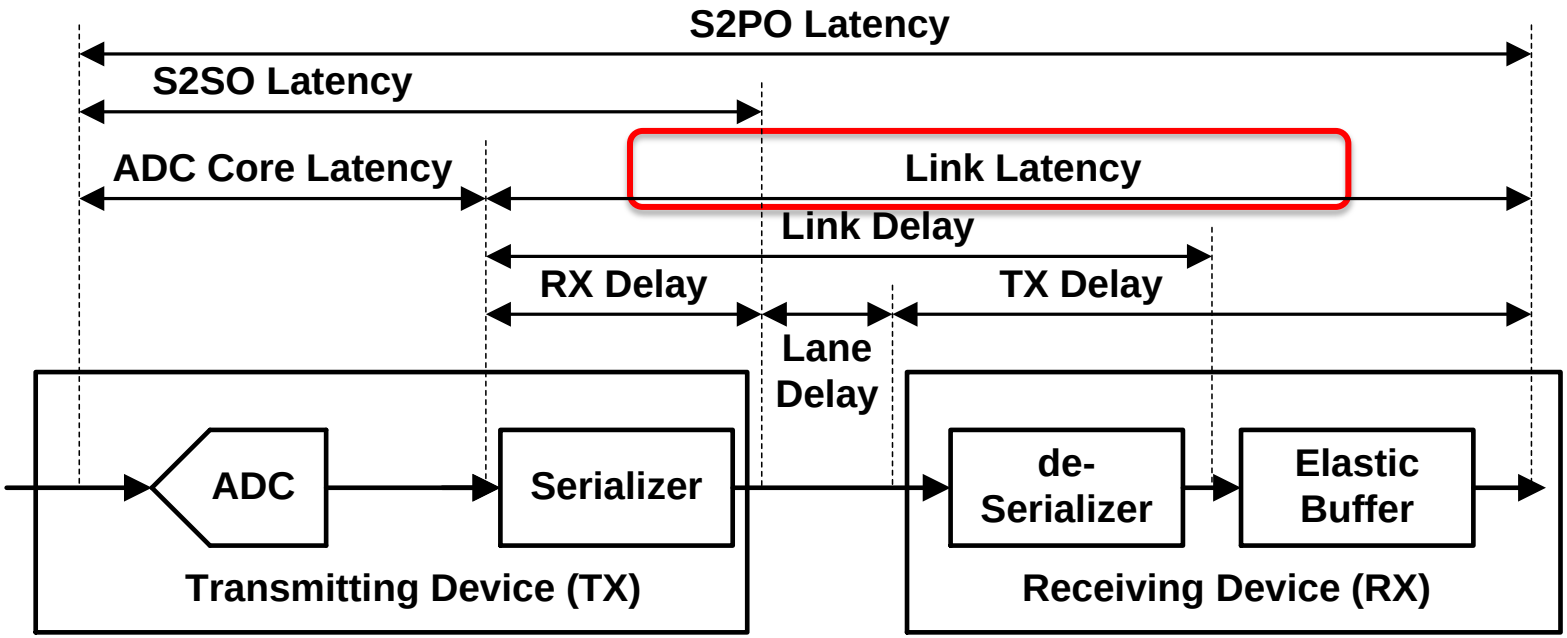
Deterministic Latency Definition

Deterministic Latency (DL) Definition

- **Wikipedia**: ”A **deterministic system** is a system in which no randomness is involved in the development of future states of the system. A deterministic model will thus always produce the **same output** from a given **starting condition or initial state**.”
  → The change in the state is known and constant (repeatable across trials)
- **JESD204B Standard** (abbr.): Latency from the frame-based data input at the TX to the frame-based data output at the RX. Latency should be programmable and repeatable over power cycles and re-sync events provided timing requirements are met.
- Knowing the exact latency is usually not as important as it being constant

Deterministic Latency (DL) Definition

- Deterministic latency in he JESD204 standard refers to the link latency and does not refer to individual delays in the link

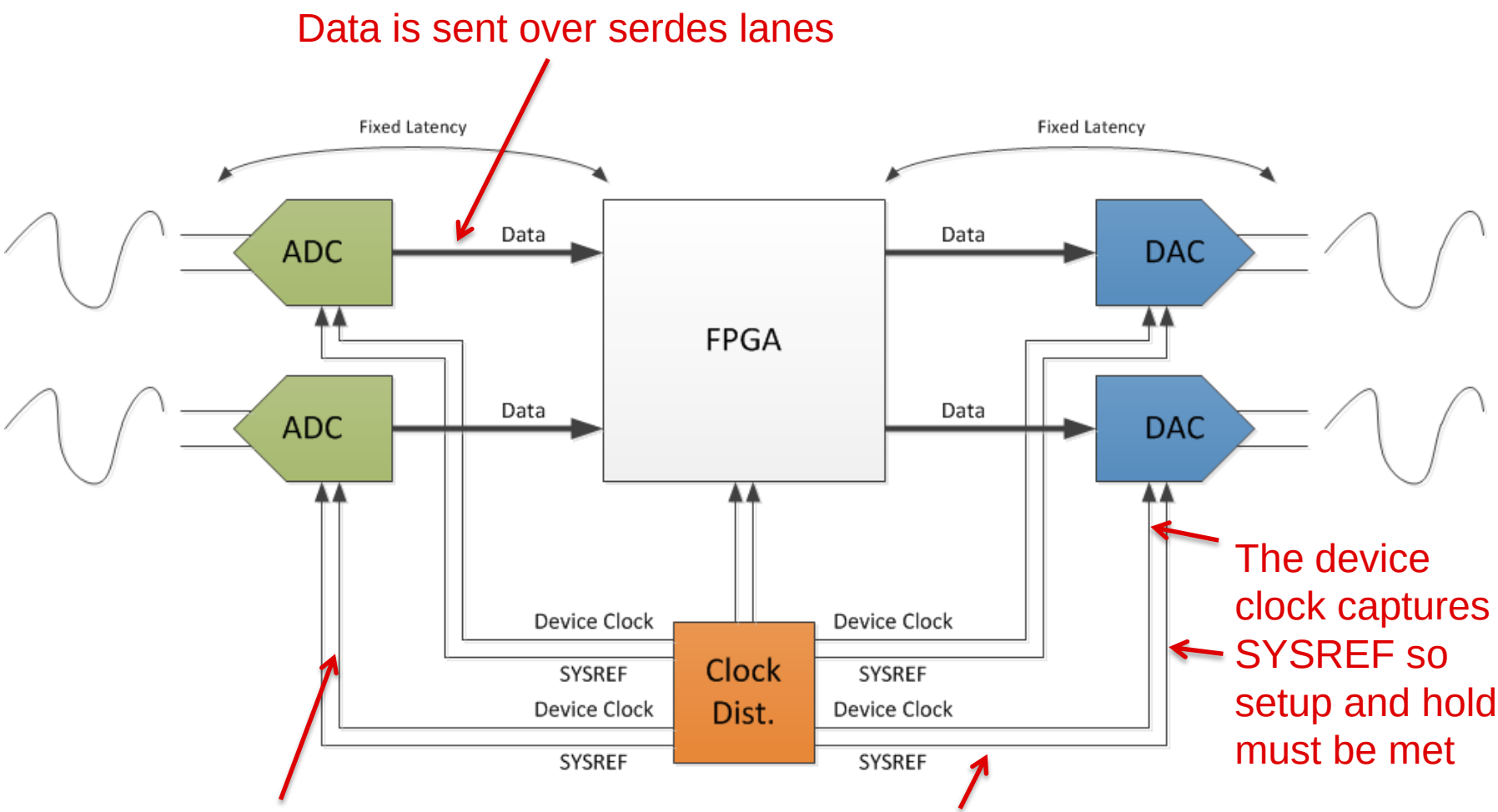


Systems that Require DL

- Applications sensitive to latency
  - Digital pre-distortion (DPD) control loops
  - Automatic gain control loops (AGC)
  - Defensive counter measures

- Any system that requires multi-device synchronization
  - Multi-antenna communications systems
  - Phased array radar
  - Magnetic Resonance Imaging (MRI)

Example: Multi-Device Synchronization



JESD204B Features that Enable DL

- (Time Reference) Low freq. time reference local to each device, synchronized deterministically to other devices in system

Local Multi-Frame Clock (LMFC)

- (Alignment Detection) TX→RX initialization pattern with embedded TX time reference is used by RX to detect reference alignment

Initial Lane Alignment (ILA) Sequence

- (Delay Adjustment) Adjustable delay compensation at RX

RX Elastic Buffer

Link Initialization Sequence to Achieve DL

1. Time synchronization signals are sent to all devices to align LMFCs

2. All TX's send ILA sequence aligned to TX LMFC

3. RX analyzes data alignment and adjusts elastic buffer for each lane independently to align data of all lanes

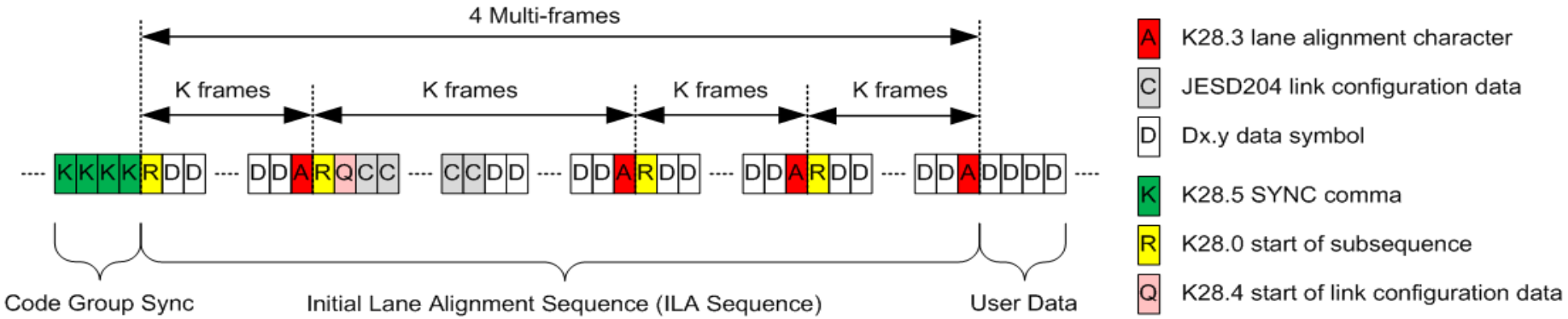
Time Synchronization Signals

- JESD204B defines 3 “subclasses”, 2 of which support DL
- 2 mechanisms to synchronize the local time references (LMFC)

Subclass	Mechanism for Deterministic Latency
Subclass 0	No support for deterministic latency (backward compatible with JESD204A).
Subclass 1	“SYSREF” signal is used to align LMFCs within all TX and RX devices.
Subclass 2	“SYNC” signal is used to align LMFCs, eliminating the need for “SYSREF”. LMFC is aligned based on when the SYNC signal is received from each data converter device. Complex timing means that this will only work below 500 MSPS.

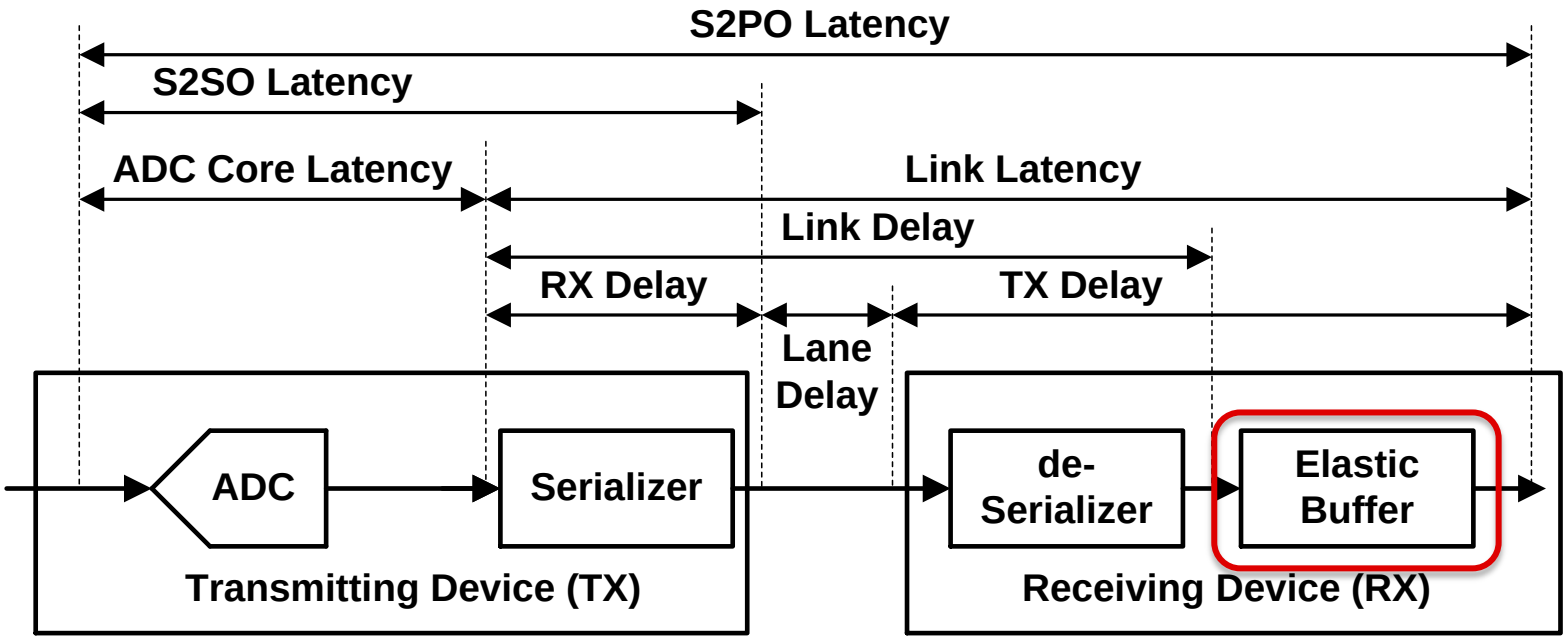
Initial Lane Alignment (ILA) Sequence

- Transmitters send ILA on all lanes starting on an LMFC “boundary”

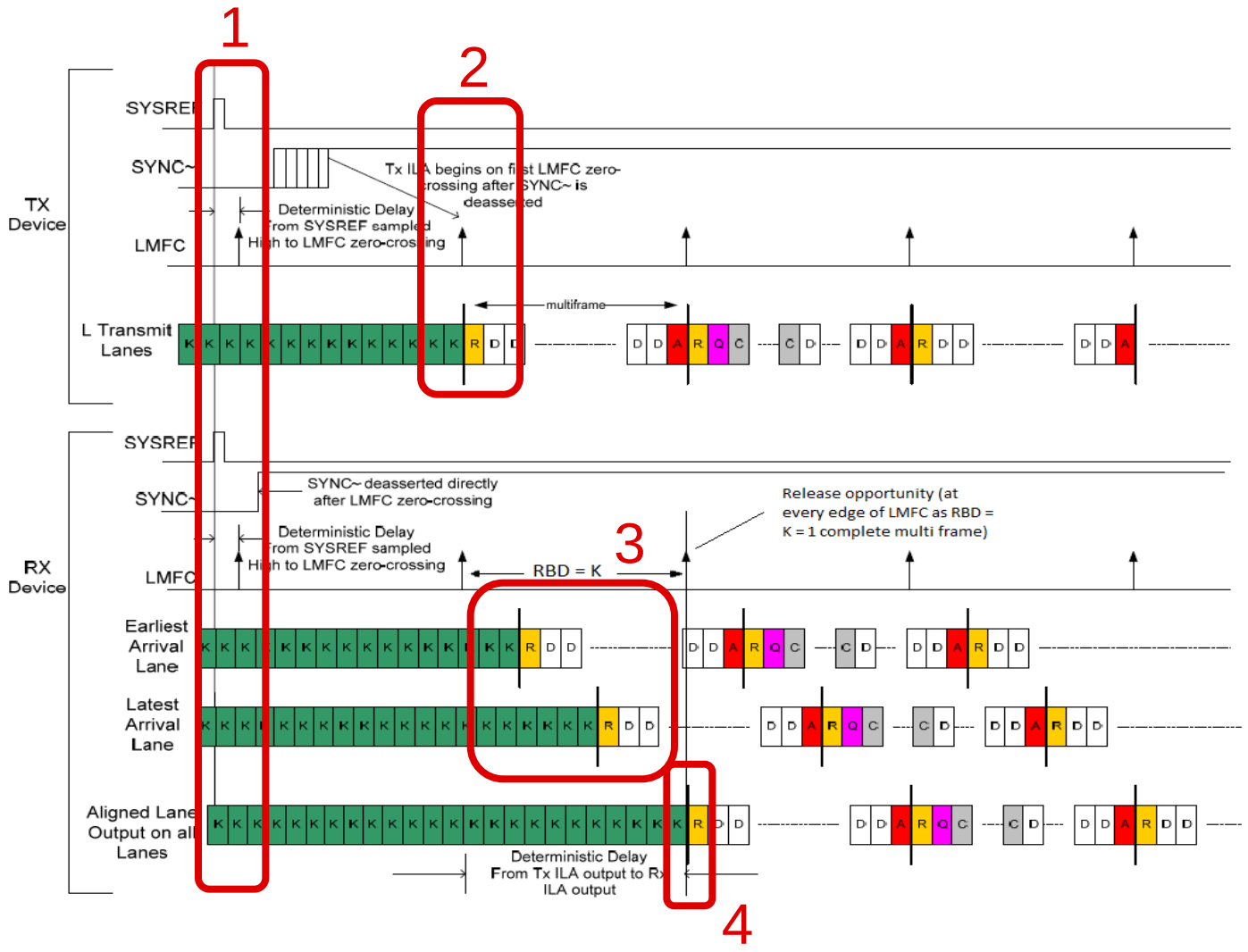


- The ILA contains /A/ and /R/ characters that indicate the multi-frame boundaries
- /A/ and /R/ are the alignment markers used to determine the data and time alignment and adjust the elastic buffer depth

Delay Compensation with Elastic Buffer



Deterministic Latency Visual



1. SYSREF is used to align LMFCs

2. After SYNC is received, all lanes send ILA sequence on next LMFC boundary

3. Each lane starts buffering it's data when it receives the /R/ character

4. All lanes are released on the next LMFC edge and are now aligned

Guaranteeing Deterministic Latency

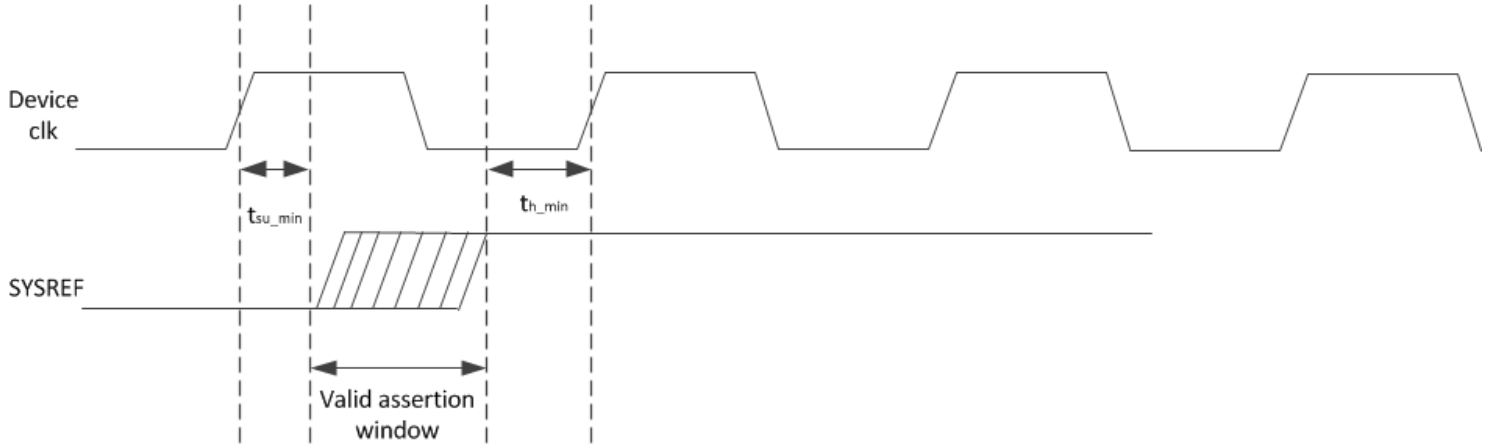
Requirements to Guarantee DL

1. The LMFCs in each device must have deterministic alignment every time the system starts or is re-synchronized

2. Data on all lanes must arrive before the RX data release point occurs
   - Max total link delay < LMFC period (T_{LMFC})
   - RBD setting must set release point to a time after all lanes have arrived

1. Align the LMFCs in Each Device

- The LMFCs must be aligned in each device
  - In reality, the LMFCs are misaligned but the phase difference must be deterministic
- SYSREF must meet setup and hold times relative to device clocks (Subclass 1)



- SYNC~ must meet setup and hold times relative to device clocks (Subclass 2)

2. Release Point Occurs After Data Arrives

- The standard requires: max(link delay) < T_{LMFC}
- Example: Serial Rate (SR)=10 Gb/s, F=2, K=32. What is LMFC period?
  - T_{LMFC} = 10*F*K/SR = 10*2*32/10e9 = 64ns (32 frame clock cycles)
- The default release point is on the next LMFC boundary

2. Release Point Occurs After Data Arrives

- The elastic buffer release point can be shifted from the LMFC rising edge by using the RBD parameter
- RBD is defined as a shift in the elastic buffer release point from the LMFC boundary by “RBD” frame periods
  - 1 < RBD < K
  - RBD = K corresponds to the release point at the next RX LMFC boundary
  - RBD = K-4 shifts the release point to 4 frame cycles *before* the next RX LMFC boundary
- Modifying RBD can be used to:
  - Release the buffer earlier to achieve minimum latency
  - Shift the release point away from a time window of link delay uncertainty

Excessive Link Delay

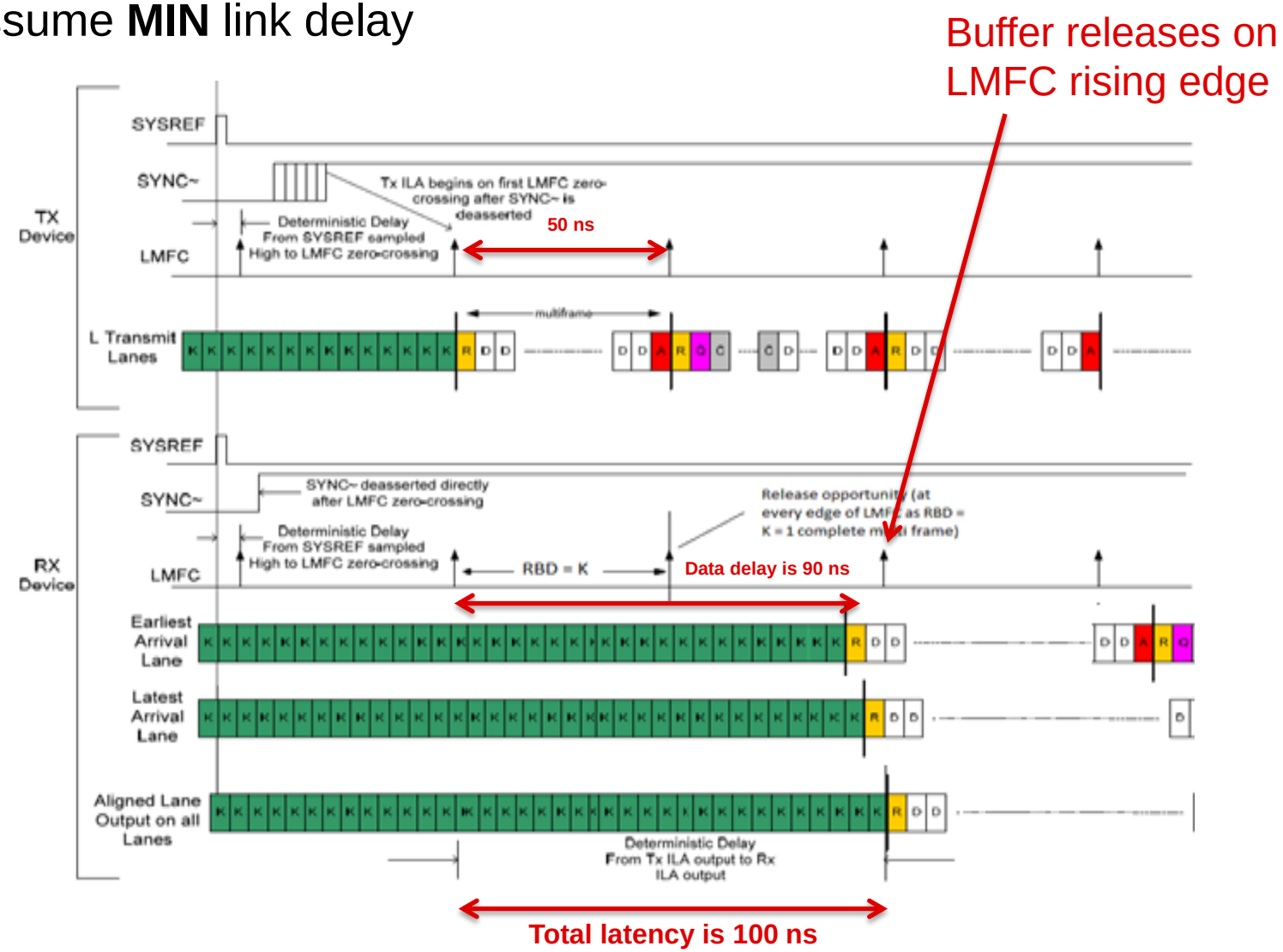
- Link delay > T_{LMFC} is a violation of requirement #2 but is common with today's devices
  - Not considered in standard
- DL can still be guaranteed if release point avoids time windows of link delay uncertainty

Example: Excessive Link Delay

- Design Goal: Set RBD to avoid delay windows of uncertainty and successfully achieve deterministic latency in the case of excessive link delay
- The LMFC period is 50 ns
- The link delay is 100 ns +/- 10 ns
  - Min link delay = 90 ns
  - Max link delay = 110 ns
- First assume the buffer release point is set to the LMFC boundary

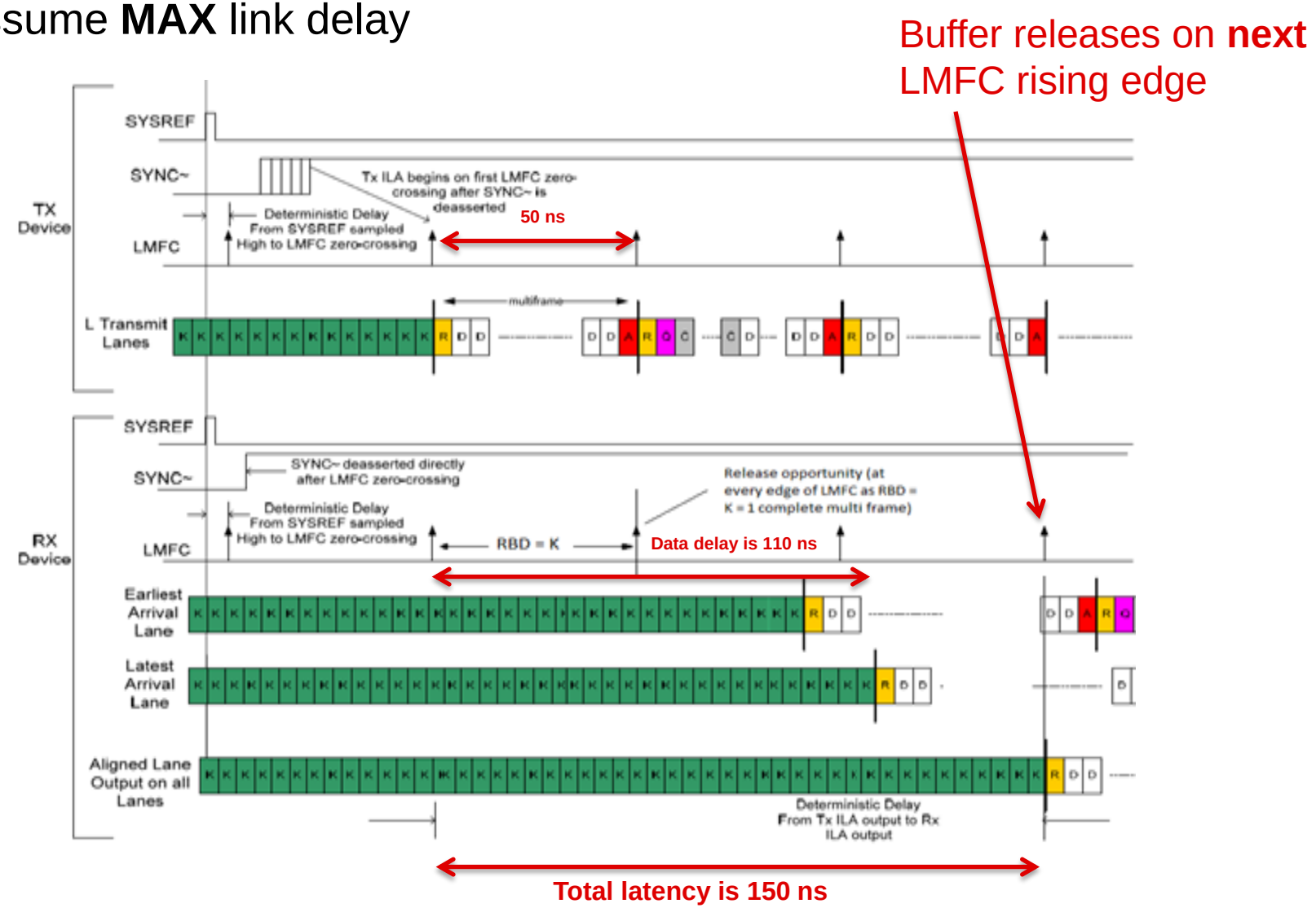
Example: Excessive Link Delay

- Assume **MIN** link delay



Example: Excessive Link Delay

- Assume **MAX** link delay



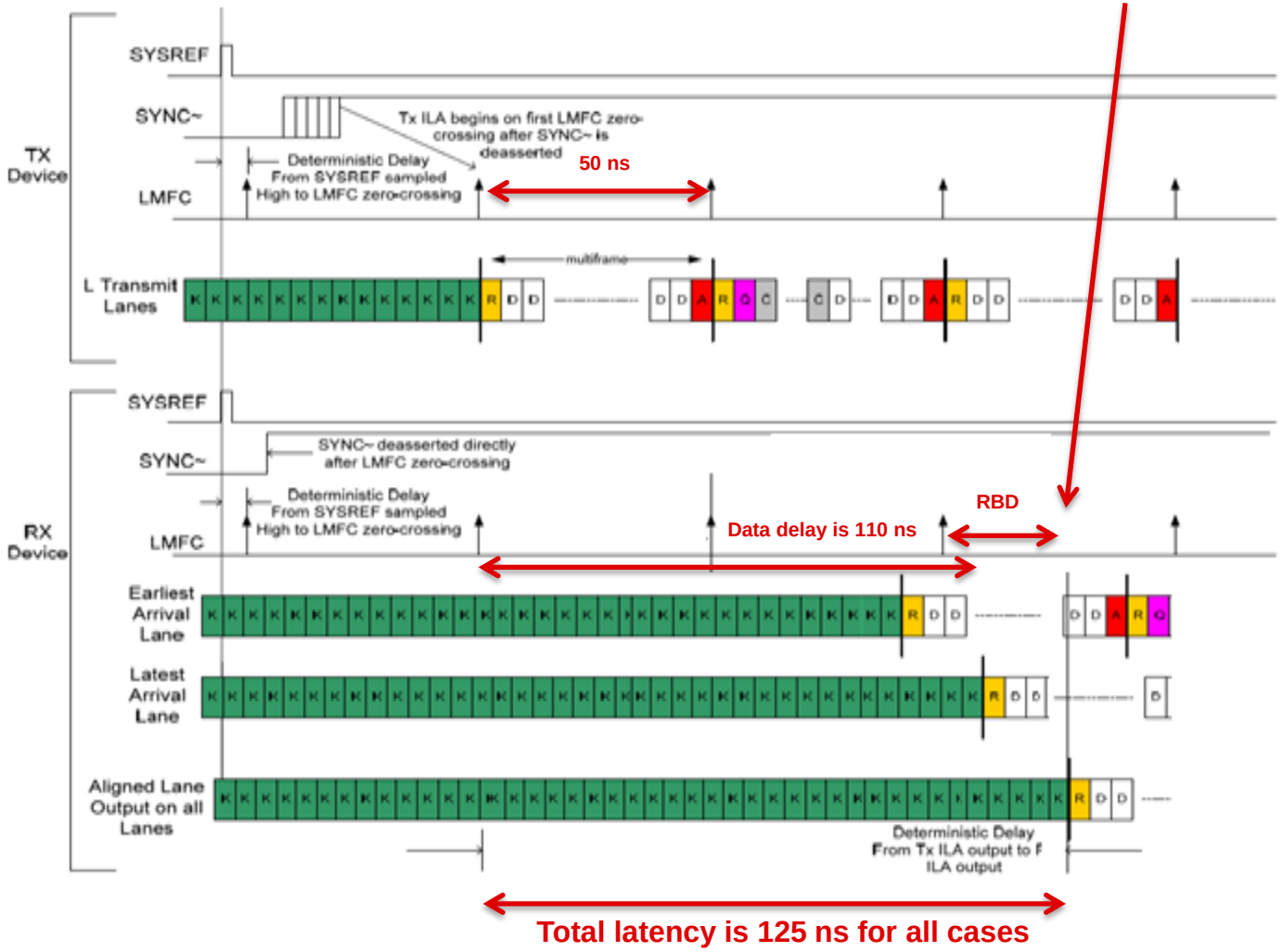
Example: Excessive Link Delay

- In this example, the latency IS NOT deterministic because it is not consistent from startup to startup
- How do we avoid this scenario?
  1. Calculate the delay window of uncertainty by finding the minimum and maximum expected link delay
  2. Choose a release point that occurs before the minimum delay and after the maximum delay

Use RBD to shift the release point

Set RBD ≠ K

Release Point occurs “RBD” frame cycles after the LMFC boundary



Designing for Deterministic Latency

Design Process for Deterministic Latency

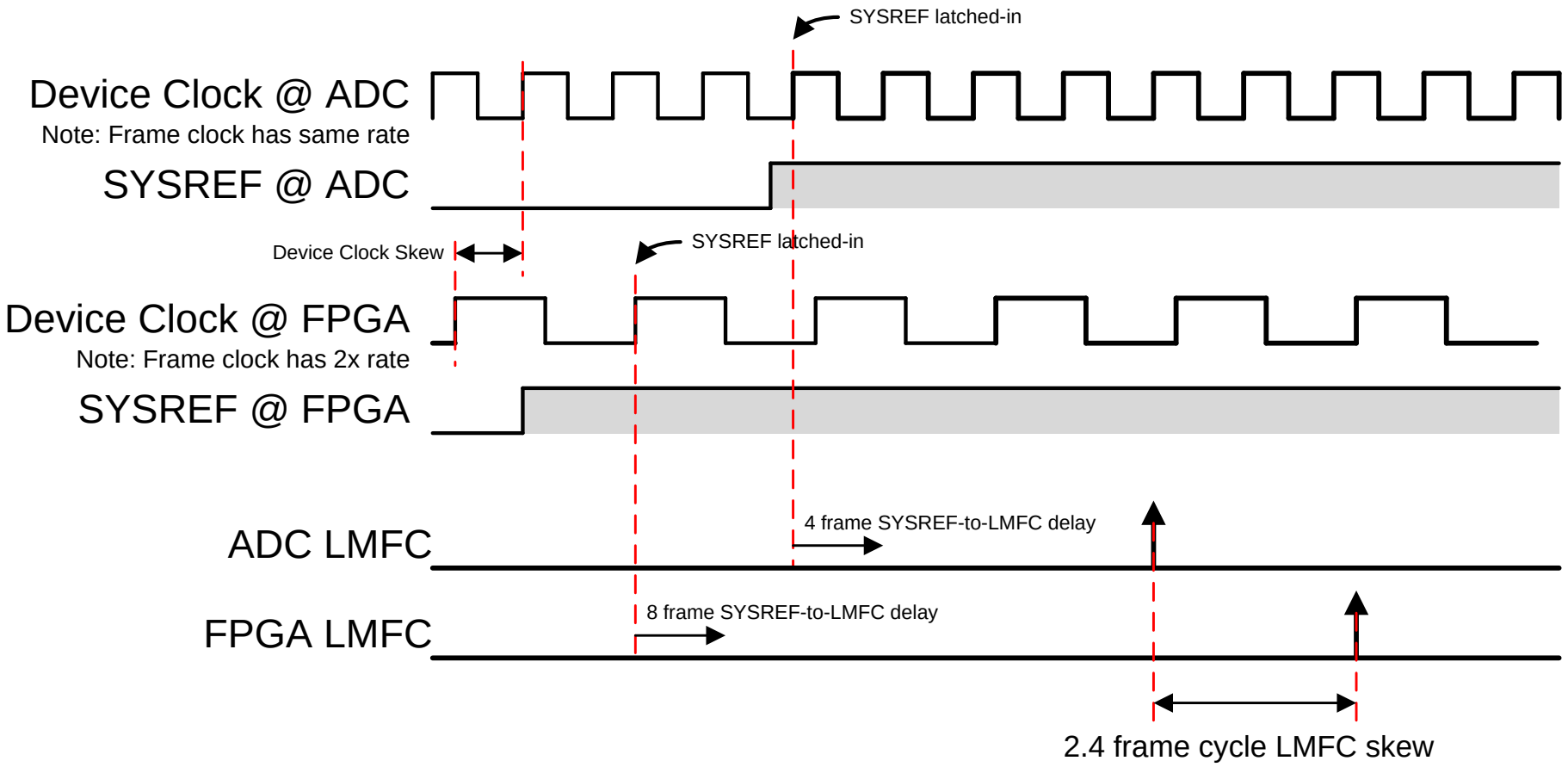
1. Determine Alignment of LMFCs
2. Calculate expected link delay (with variation) and window of uncertainty
3. Choose release point that avoids delay window with margin

Step 1: Determine Alignment of LMFCs

- Things to consider
  - Propagation delay of SYSREF and device clocks across board
  - Purposefully added delays to SYSREF, such as analog delays or dynamic digital delays (like in LMK04828)
  - Delays from SYSREF input pins to resetting of LMFC (internal to devices)

Step 1: Determine Alignment of LMFCs

- Example of calculating LMFC alignments



Step 1: Determine Alignment of LMFCs

- Example SYSREF to LMFC boundary for DAC38J84

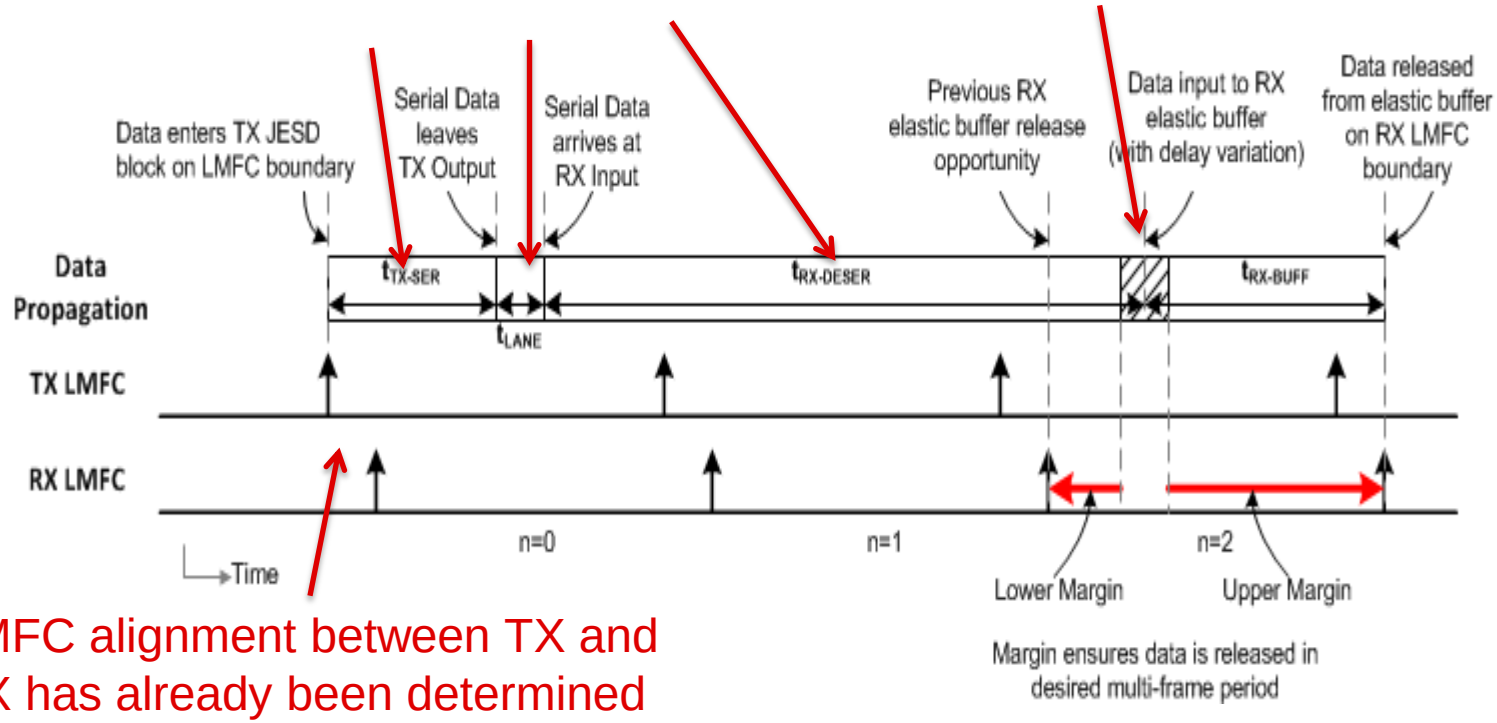
- SYSREF pin to LMFC boundary latency in terms of DACCLK

LMF	1x	2x	4x	8x	16x
841	16	24	40	80	160
442	10	16	24	40	80
244	N/A	10	16	28	40
148	N/A	N/A	11	16	28
821	24	40	80	160	N/A
421	16	24	40	80	160
222	10	16	24	40	80
124	N/A	10	16	28	40

Step 2: Calculate Link Delay

These delays will come from the datasheet or need to be measured or calculated

Variations occur due to device variances (specified in datasheet) or due to PVT effects

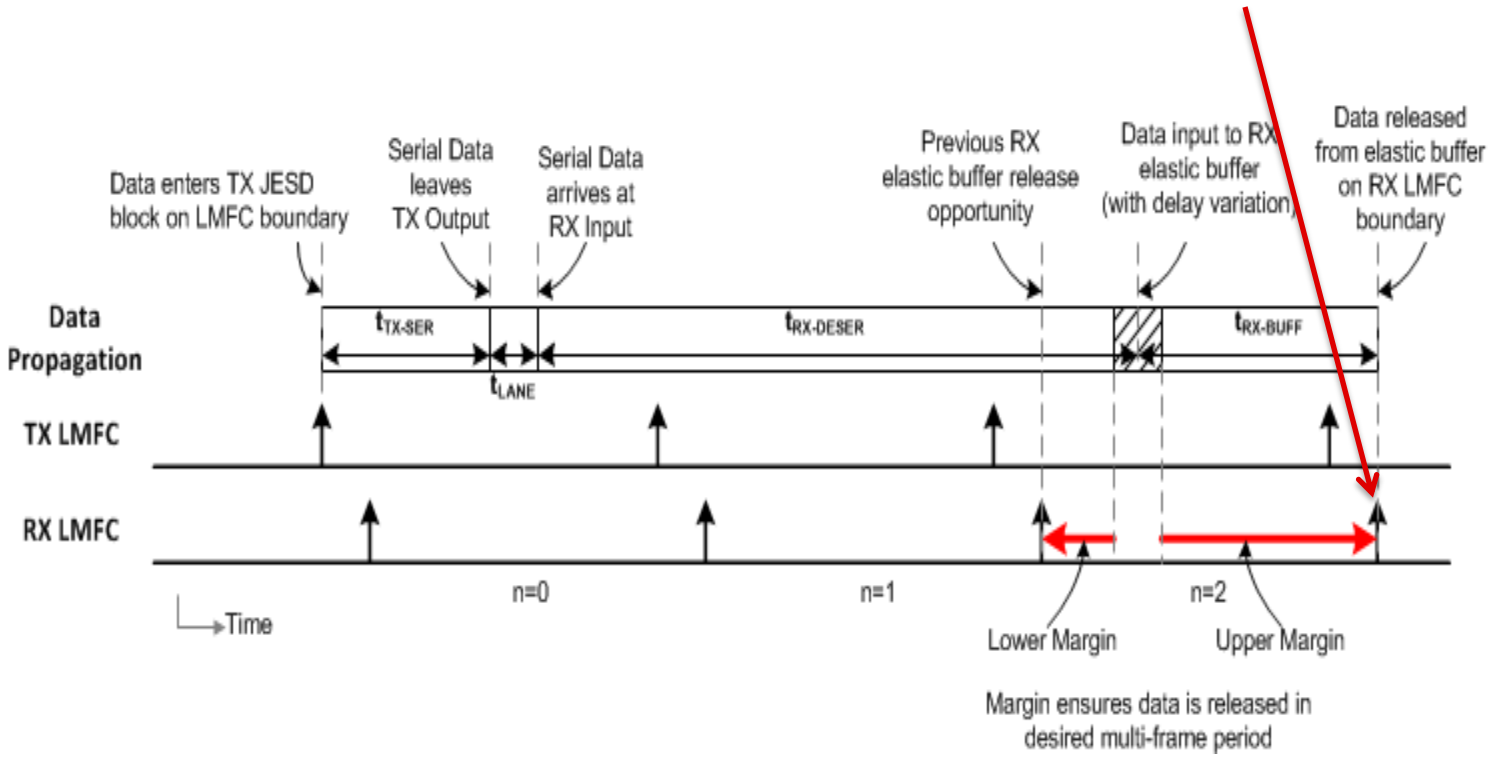


LMFC alignment between TX and RX has already been determined

Total Link Delay = $t_{TX\_SER} + t_{LANE} + t_{RX\_DESER}$ +/- $t_{VARIATION}$

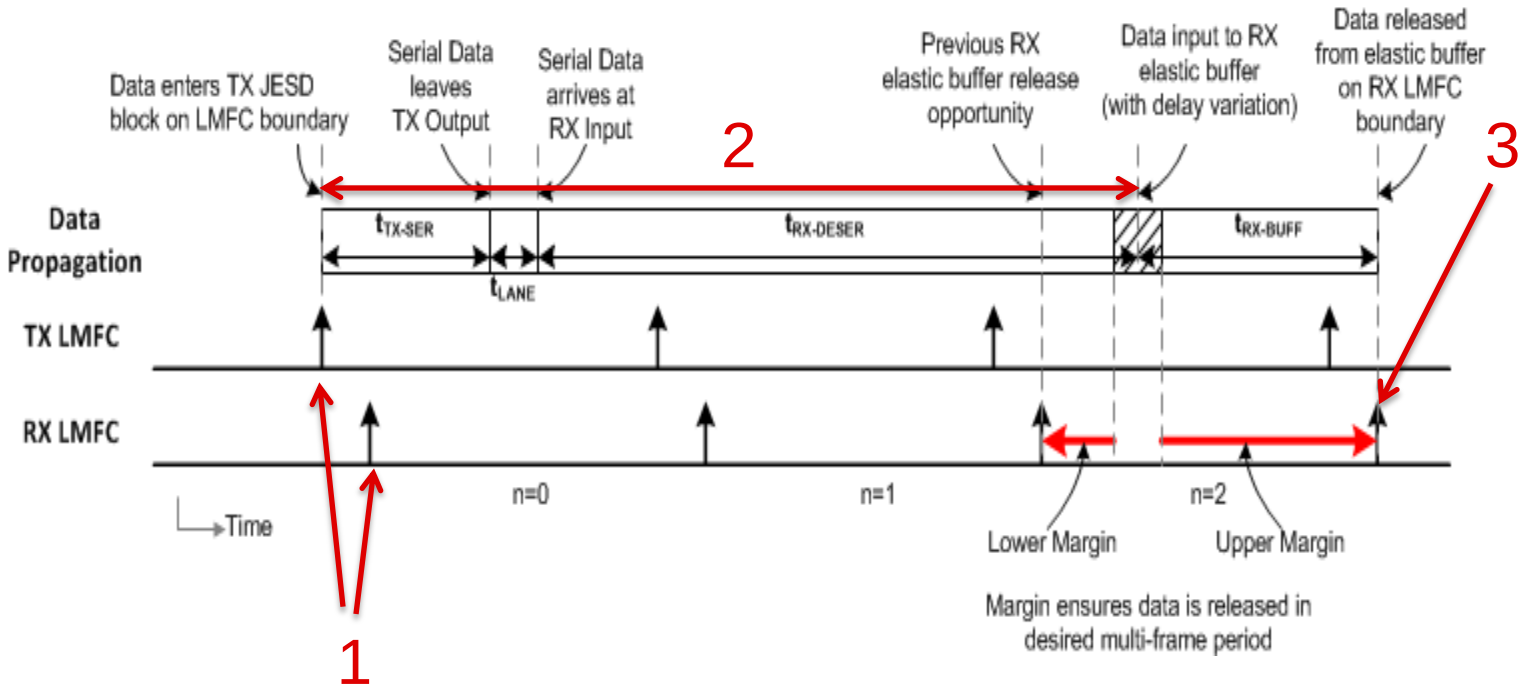
Step 3: Choose Buffer Release Point

Choose release point that guarantees enough margin around the expected lane arrival



Design Process Summary

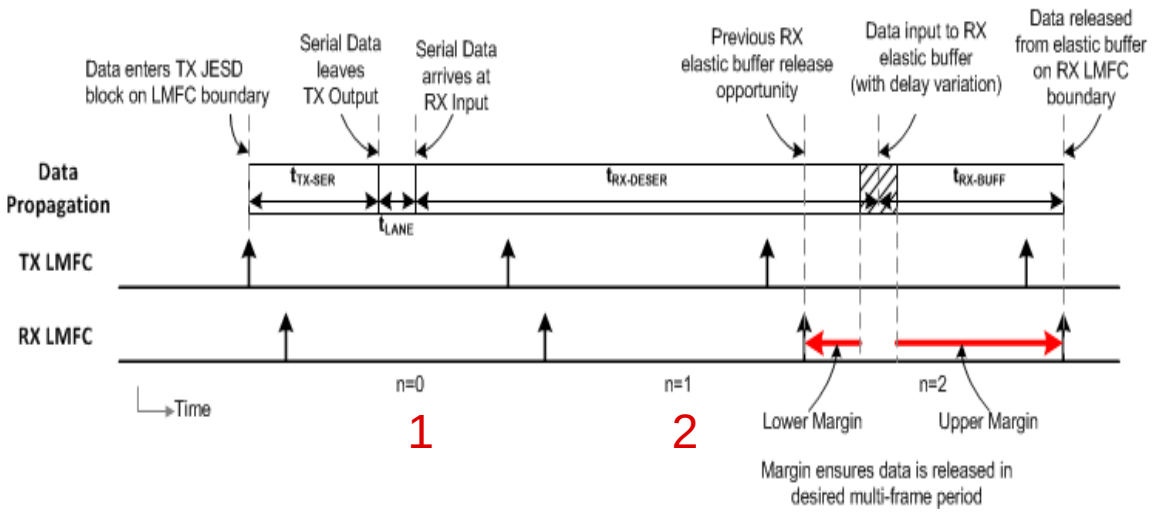
1. Determined LMFC alignment between TX and RX
2. Calculated total link delay
3. Determined the appropriate buffer release point



Total Link Latency

- The total link latency can be calculated using the following formula
- “n” is the number of whole RX multi-frames traversed for the case where the total link delay exceeds one LMFC cycle

$$\text{Link Latency} = (n * K + RBD) * T_{FRAME} + (t_{RX\_LMFC} - t_{TX\_LMFC})$$



n = 2

Add ADC or DAC latency for Total Latency

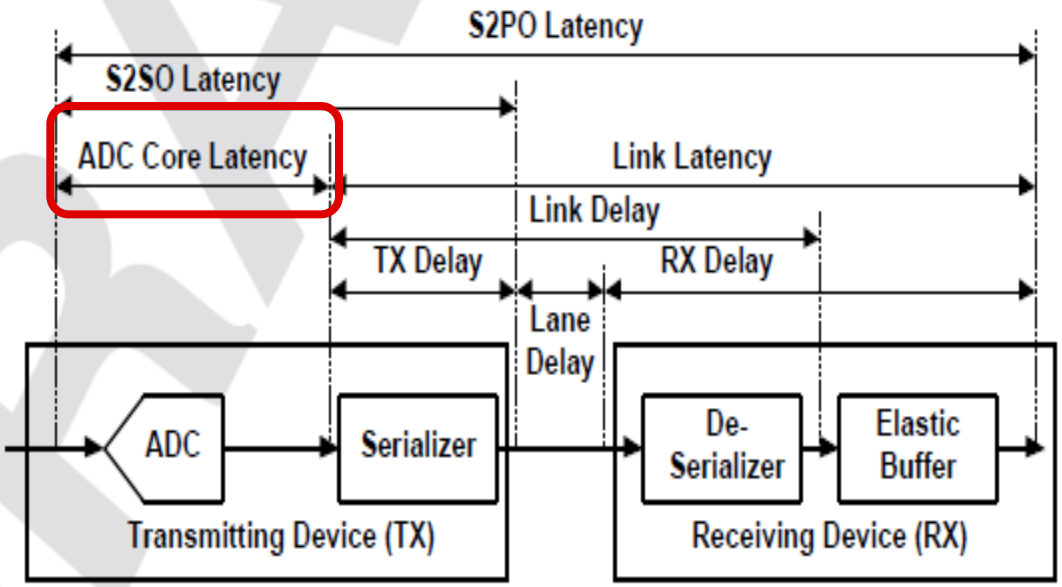
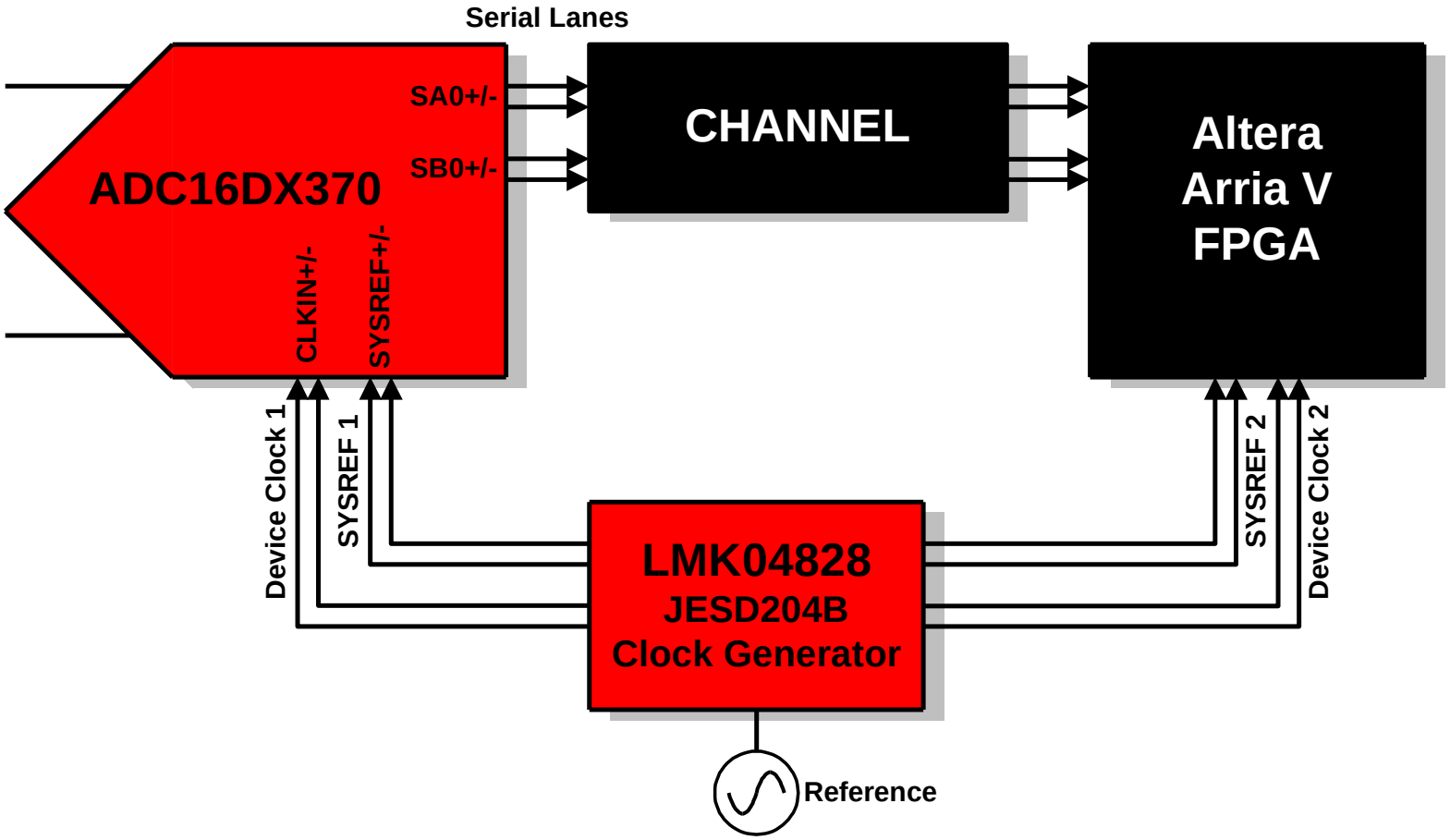


Figure 2. Block Diagram of Simplified Latencies in a System Using the LM97937

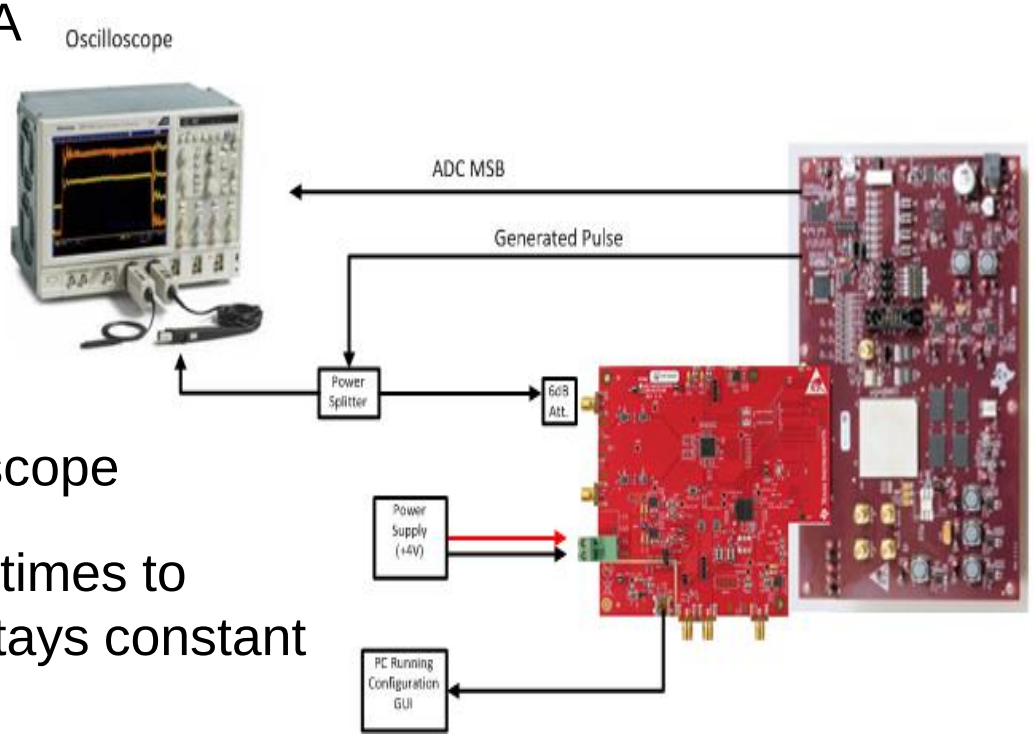
Verifying Deterministic Latency

Example System Diagram



Deterministic Latency Test Setup

1. Generate a pulse with FPGA
2. Capture FPGA pulse with ADC
3. Output ADC's MSB from FPGA
4. Observe relative timing on scope
5. Power up the system many times to confirm the relative timing stays constant

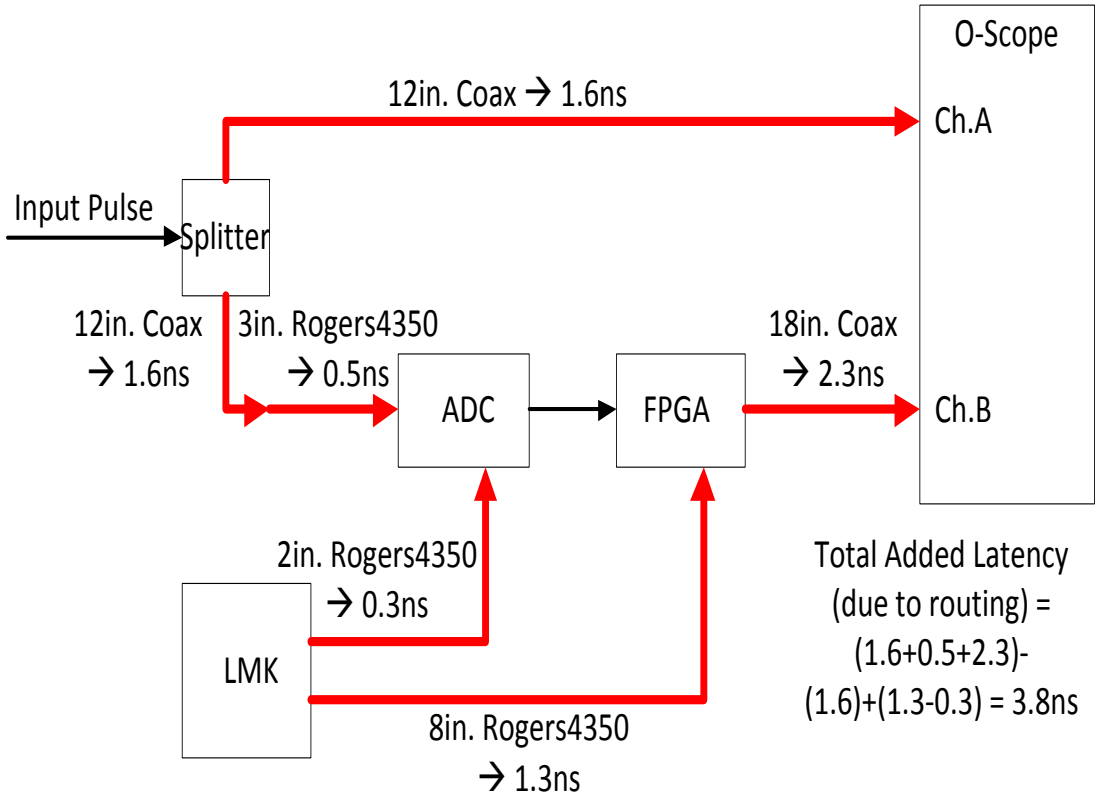


Device Setup for Test

- ADC = ADC16DX370 (16-bit, dual channel, 370 MSPS)
  - Device clock = 368.64 MHz (2.713 ns)
- JESD204B Parameters
  - L = 2, M = 2, F = 2, S = 1, K = 32
  - Frame cycle = 10 * F / Linerate = 10 * 1 / 7372.8 Mbps = 2.713 ns
  - LMFC cycle = Frame cycle * K = 2.713 ns * 32 = 86.82 ns
- FPGA
  - Device clock = 92.16 MHz (~10.85 ns)

Additional Delays in System

- Account for non-device related delays in calculations



Expected Latency (Calculation)

- Per the previous slides, the latency is calculated as

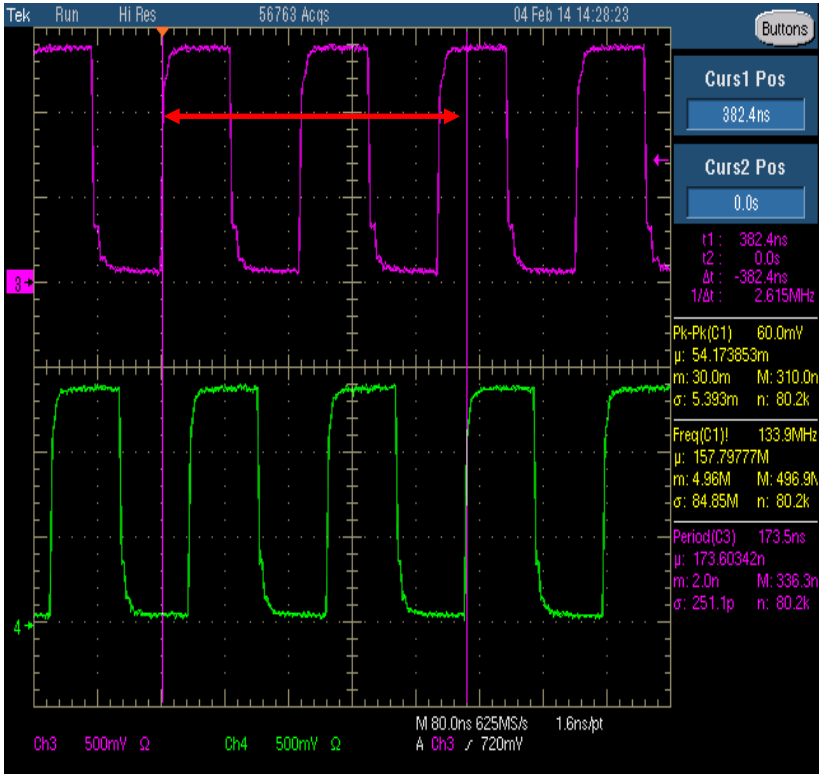
$$\text{Link Latency} = (n * K + RBD) * T_{FRAME} + (t_{RX\_LMFC} - t_{TX\_LMFC})$$

- For this experiment the following parameters apply
  - All units in Frame clock cycles
  - t_{RX_LMFC} = 28, t_{TX_LMFC} = 3.5, n = 2, K = 32, RBD=28
  - Link Latency = 116.5 frame clock cycles
- The following also extend the latency
  - ADC16DX370 core latency = +12.5
  - DEVCLK routing skew and MSB output routing delay = +1.4
  - SYSREF/DEVCLK sampling skew = +1.5
  - Additional receiver processing delays
    - +3 rx_tdata release delay (for earliest sample in the 4-sample set output each period of 92.5MHz clock. This delay may instead be +4)
    - +4 latching MSBs before output (at Fs/4 rate)
- Total Calculated Latency = 116.5 + 12.5 + 1.4 + 1.5 + 7 = **138.9 cycles**

Measured Latency

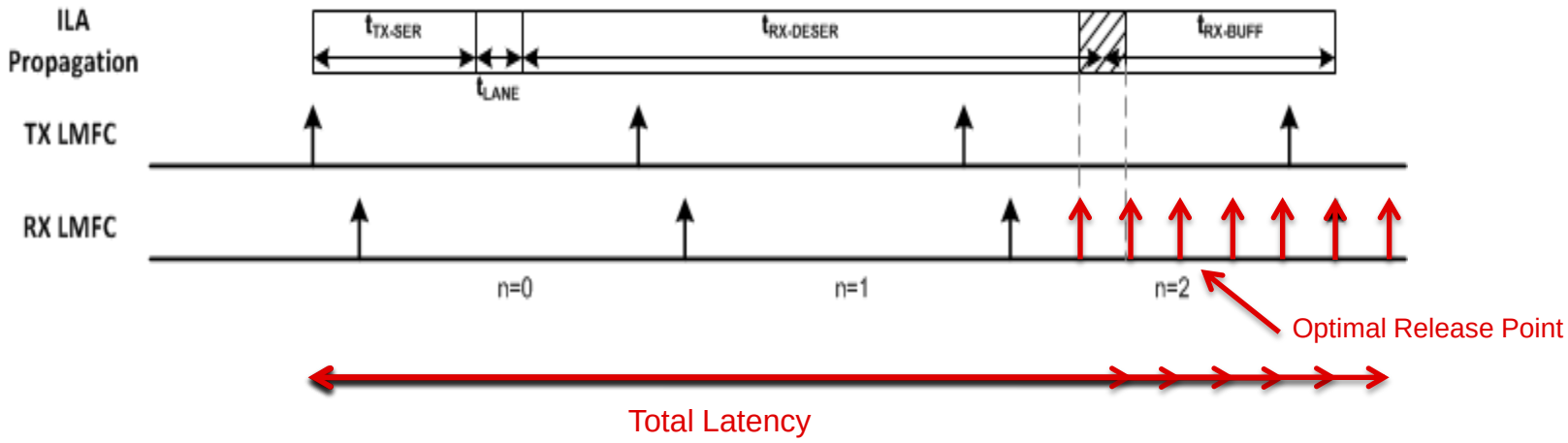
- Calculated latency for this setup is 138.9 frame cycles
- Measured latency is 379.6 ns / 2.7 ns = 139.9 cycles
- Note: A longer pulse width would remove ambiguity of input-to-output edge

Latency=379.6ns



Empirical Method to Determine Link Delay

1. Setup a test similar to the one shown to observe relative delays
2. Vary RBD until a 1 LMFC period latency jump is observed
3. Choose release point by taking the last RBD value before the latency jump was observed and add the expected latency variation to that value (plus extra margin)

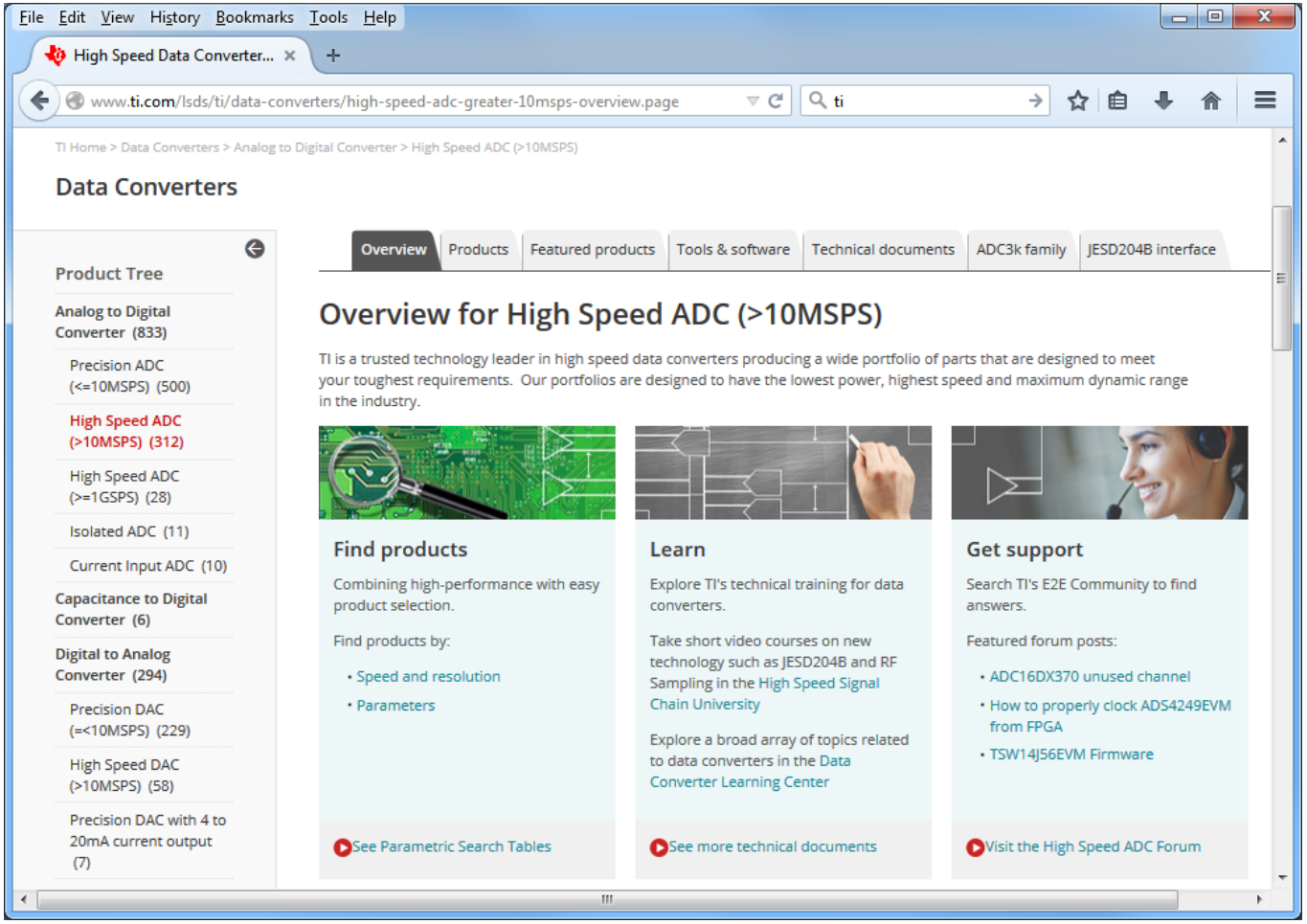


Summary

- Deterministic Latency (DL) refers to having a constant and known latency through the JESD204B link
- DL is enabled by the time reference (LMFC), alignment detection (ILA sequence) and delay adjustment (Elastic Buffer) features of the link
- Subclass 1 devices align the time reference using SYSREF, Subclass 2 device align using SYNCb
- The Elastic Buffer adjusts delay at the receiver to compensate for delay variation in other segments of the link
- RBD (Release Buffer Delay) is used to vary the buffer release moment to avoid link delay windows of uncertainty and to reduce the total link latency

More Educational Resources

www.ti.com/lsds/ti/data-converters/high-speed-adc-greater-10msps-jesd204b.page



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