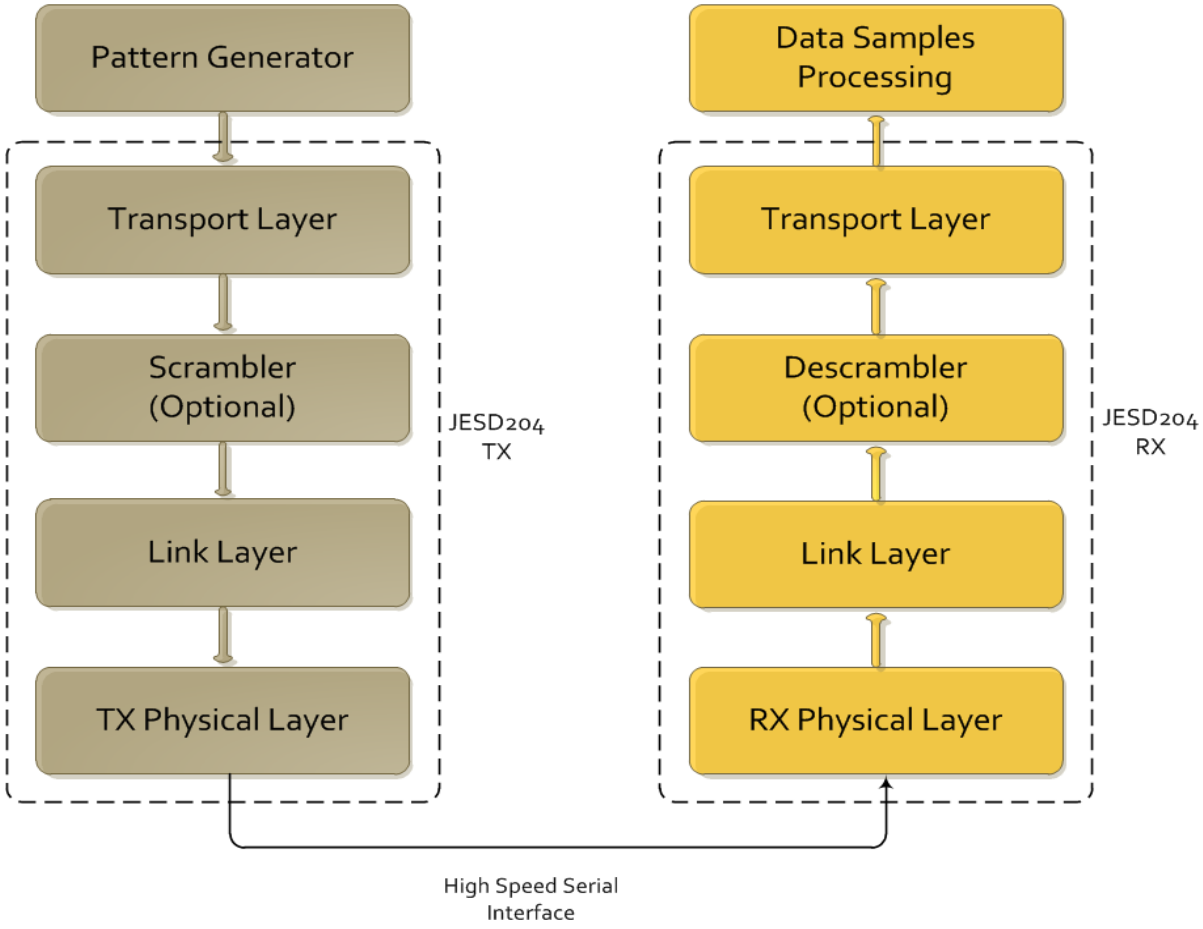
JESD204B
Transport and Data Link Layers

Texas Instruments High Speed Data Converter Training

Outline

- Transport Layer Details
- Link Layer Details

JESD204B Layers

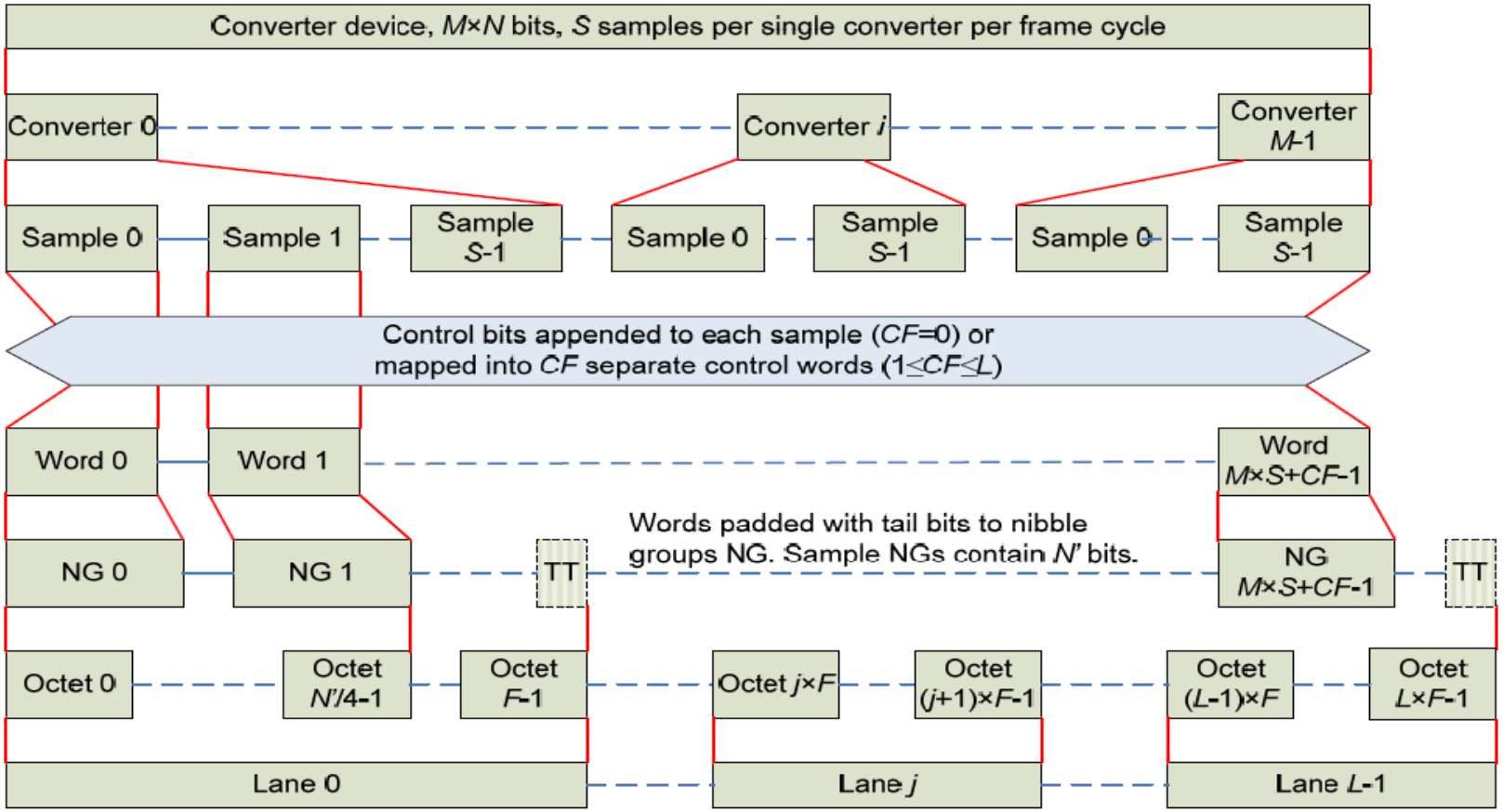


TRANSPORT LAYER

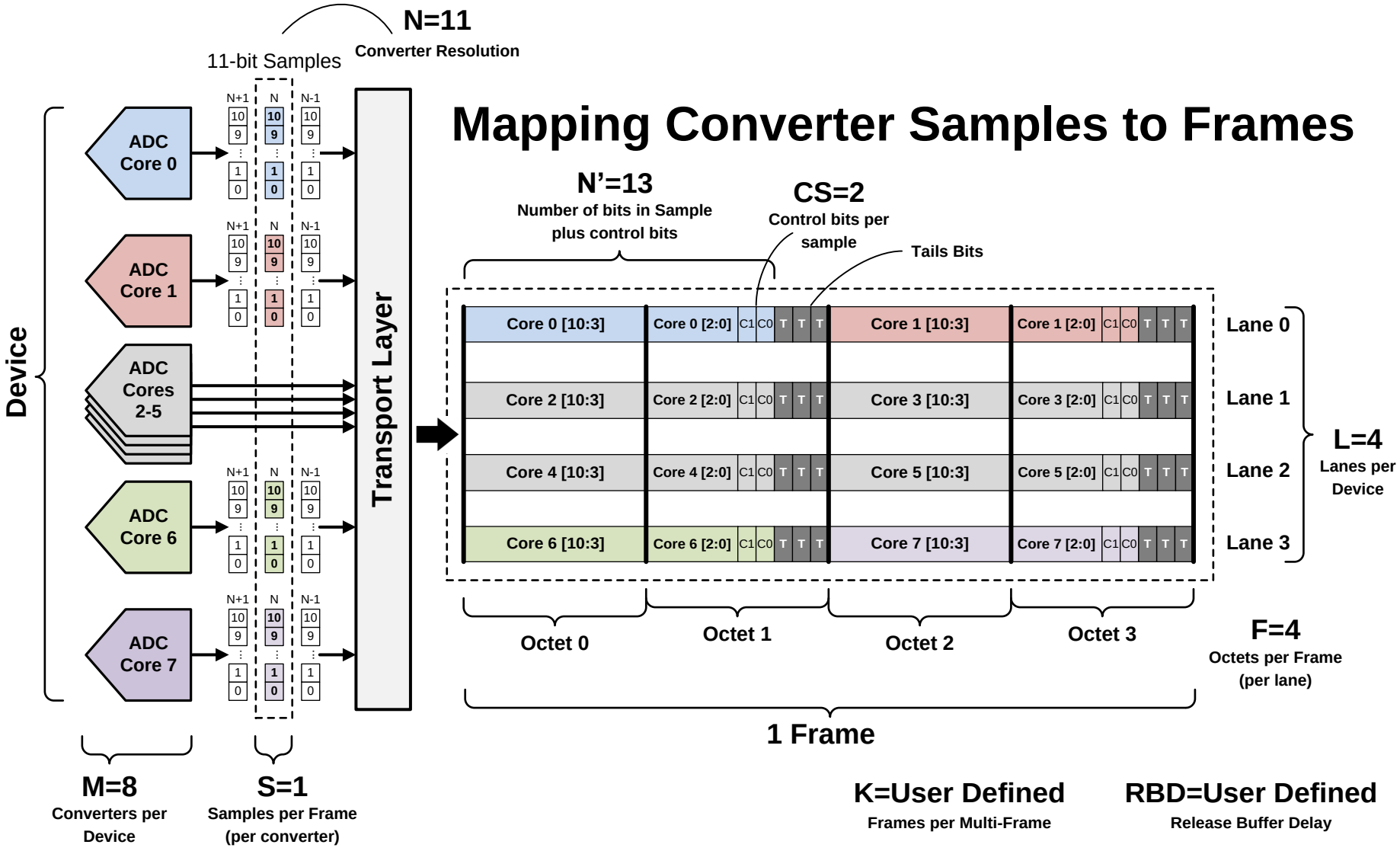
Transport Layer Overview

- Maps the data → octets → frames consisting of multiple octets
- Adds optional control bits to samples if needed
  - Control bits can be used to communicate status information, mark an inactive converter on the link or control receiver operation
- Adds tail bits if needed to create ‘full’ octets
- Distinguishes the possible combinations of device/links/lanes/etc.
  - Single converter connected to single lane link
  - Single converter connected to multiple lanes link
  - Multiple converters in a converter device connected to a single lane link
  - Multiple converters in a converter device connected to multiple lanes link

Transport Layer Data Flow



Transport Layer (Example #1)



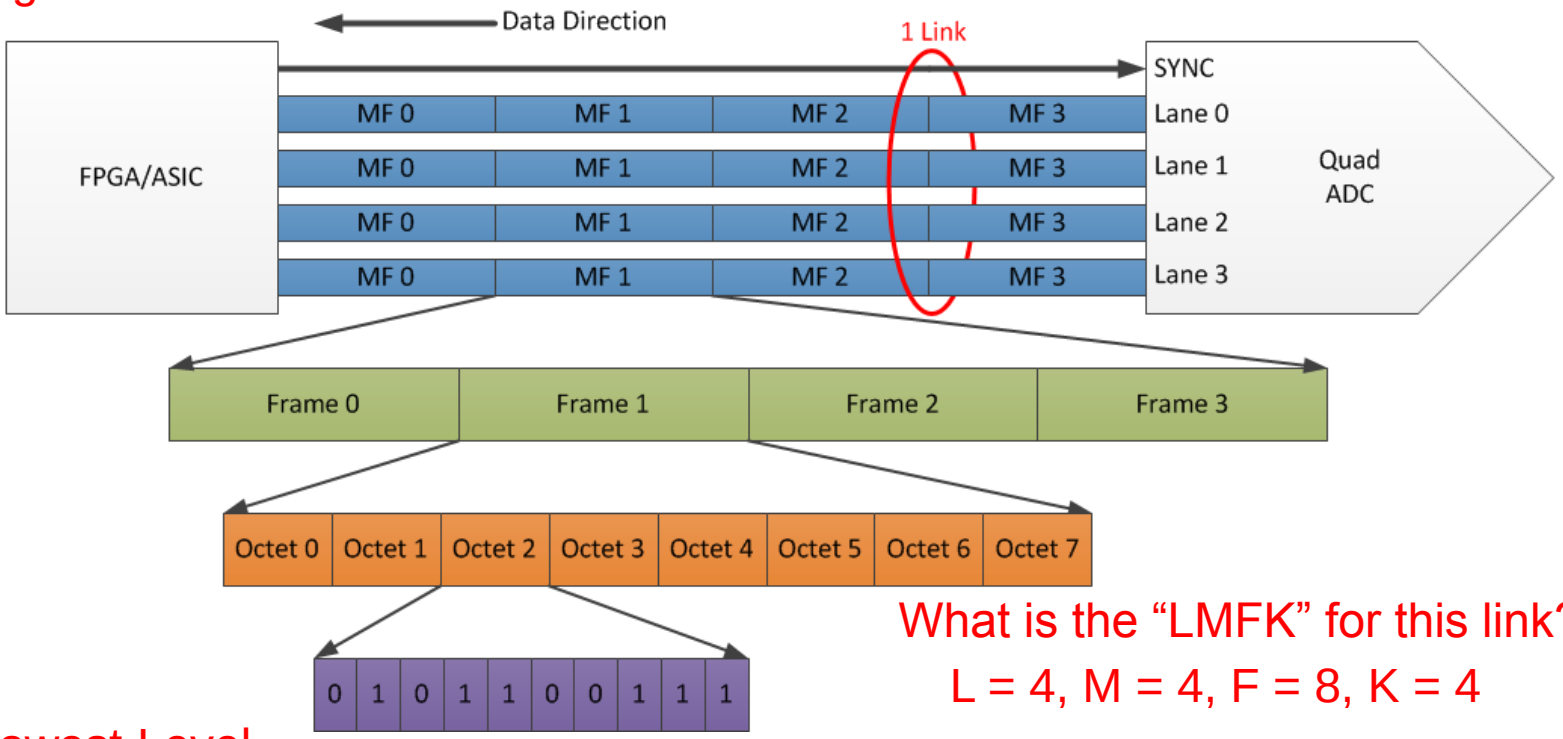
Transport Layer

- Some important parameters associated with transport layer are:
  - **L** **Number of lanes in a link**
  - **M** **Number of converters per device**
  - **F** **Number of octets per frame**
  - **S** **Number of samples per converter per frame clock cycle**
  - K # of frames per multiframe
  - CF Number of control words per frame clock cycle per link
  - N Converter Resolution
  - N’ Total number of bits per sample

- Control bits can either be appended after the LSB of every sample or all the bits for different samples can be sent together in CF number of frames.

Example #2 (16b Quad ADC)

Highest Level



Lowest Level

What is the “LMFK” for this link?

L = 4, M = 4, F = 8, K = 4

What is “S”?

S = 4

LINK LAYER

Link Layer Functions

- 8b/10b Encoding
- Link Synchronization
  - Code group synchronization
  - Initial frame synchronization
  - Initial lane synchronization
  - Link re-initialization
- Link Monitoring
  - Special alignment character insertion
  - Error Reporting
- SYNC~ signal combining
- Test Modes

Link Layer: 8b/10b Encoding

- Encodes 8-bit “octets” into 10-bit symbols
- Octet to symbol mapping depends on running disparity (RD)
- Coding provides many bit-transitions to enable CDR techniques
- DC balancing enables AC coupling

5b/6b code

Input		RD = −1	RD = +1	Input		RD = −1	RD = +1
	EDCBA	abcdei			EDCBA	abcdei	
D.00	00000	100111	011000	D.16	10000	011011	100100
D.01	00001	011101	100010	D.17	10001	100011	
D.02	00010	101101	010010	D.18	10010	010011	
D.03	00011	110001		D.19	10011	110010	
D.04	00100	110101	001010	D.20	10100	001011	
D.05	00101	101001		D.21	10101	101010	
D.06	00110	011001		D.22	10110	011010	
D.07	00111	111000	000111	D.23 †	10111	111010	000101
D.08	01000	111001	000110	D.24	11000	110011	001100
D.09	01001	100101		D.25	11001	100110	
D.10	01010	010101		D.26	11010	010110	
D.11	01011	110100		D.27 †	11011	110110	001001
D.12	01100	001101		D.28	11100	001110	
D.13	01101	101100		D.29 †	11101	101110	010001
D.14	01110	011100		D.30 †	11110	011110	100001
D.15	01111	010111	101000	D.31	11111	101011	010100
				K.28	11100	001111	110000

3b/4b code

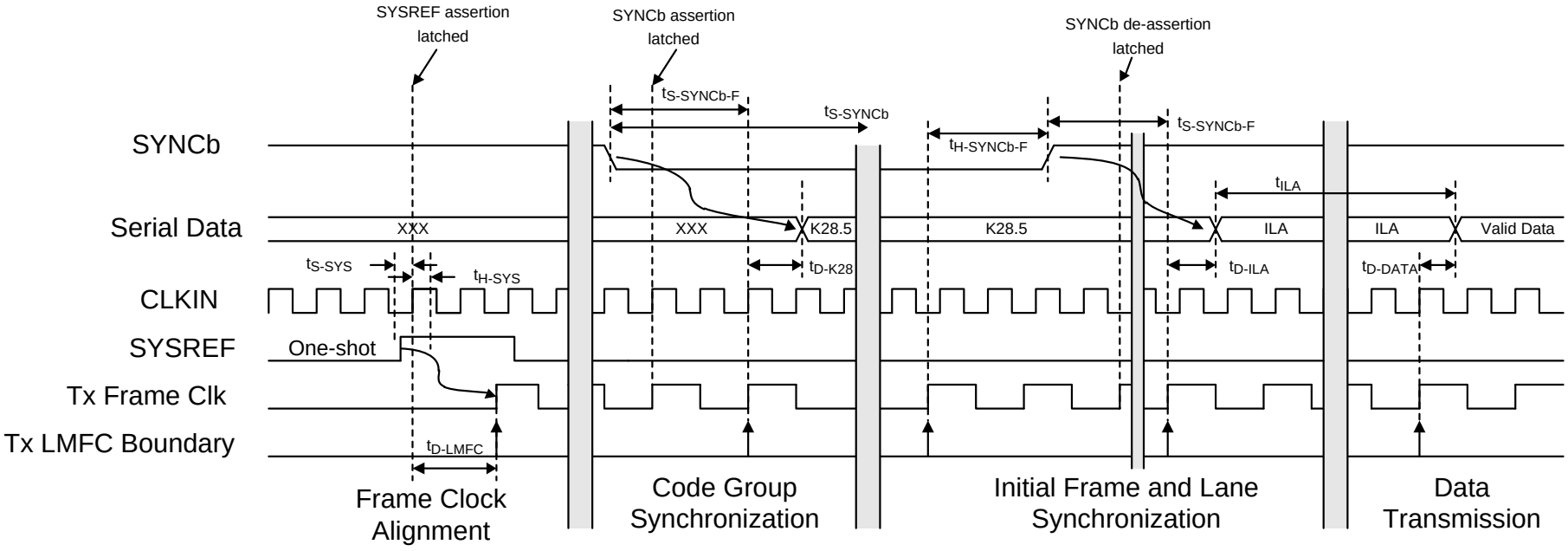
Input		RD = −1	RD = +1	Input		RD = −1	RD = +1
	HGF	fghj			HGF	fghj	
D.x.0	000	1011	0100	K.x.0	000	1011	0100
D.x.1	001	1001		K.x.1 ‡	001	0110	1001
D.x.2	010	0101		K.x.2 ‡	010	1010	0101
D.x.3	011	1100	0011	K.x.3 ‡	011	1100	0011
D.x.4	100	1101	0010	K.x.4	100	1101	0010
D.x.5	101	1010		K.x.5 ‡	101	0101	1010
D.x.6	110	0110		K.x.6 ‡	110	1001	0110
D.x.P7 †	111	1110	0001				
D.x.A7 †	111	0111	1000	K.x.7 †	111	0111	1000

Control symbols

Input				RD = −1	RD = +1
	DEC	HEX	HGF EDCBA	abcdei fghj	abcdei fghj
K.28.0	28	1C	000 11100	001111 0100	110000 1011
K.28.1 †	60	3C	001 11100	001111 1001	110000 0110
K.28.2	92	5C	010 11100	001111 0101	110000 1010
K.28.3	124	7C	011 11100	001111 0011	110000 1100
K.28.4	156	9C	100 11100	001111 0010	110000 1101
K.28.5 †	188	BC	101 11100	001111 1010	110000 0101
K.28.6	220	DC	110 11100	001111 0110	110000 1001
K.28.7 ‡	252	FC	111 11100	001111 1000	110000 0111
K.23.7	247	F7	111 10111	111010 1000	000101 0111
K.27.7	251	FB	111 11011	110110 1000	001001 0111
K.29.7	253	FD	111 11101	101110 1000	010001 0111
K.30.7	254	FE	111 11110	011110 1000	100001 0111

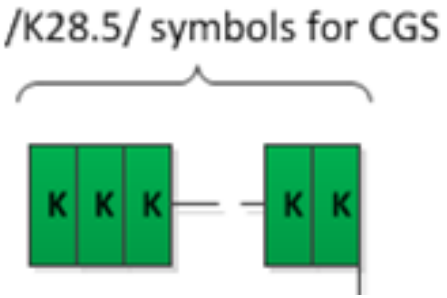
Link Layer: Link Establishment

- Link Establishment accomplishes TX and RX synchronization
  - Code Group Synchronization (CGS)
  - Initial Frame Synchronization
  - Initial Lane Synchronization



Link Layer: Code Group Synchronization

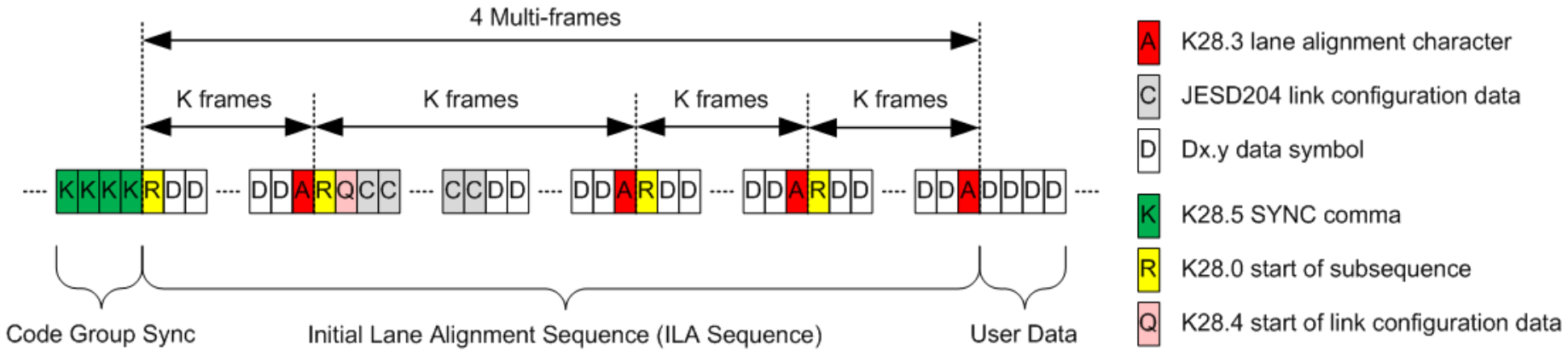
- During CGS, the RX aligns with the 10-bit symbol boundary of the transmitted symbols
- Synchronization Procedure:
  1. Receiver generates synchronization request by asserting SYNC~ signal
  2. In response, transmitter sends K28.5 comma symbols
  3. After receiving 4x K28.5 symbols on all lanes, the RX de-asserts SYNC~
  4. RX aligns frame boundary to next non-K28.5 symbol (Initial Frame Synchronization)



- If link has multiple lanes, then SYNC~ signal for all lanes in a link must be combined and presented simultaneously to the transmitter

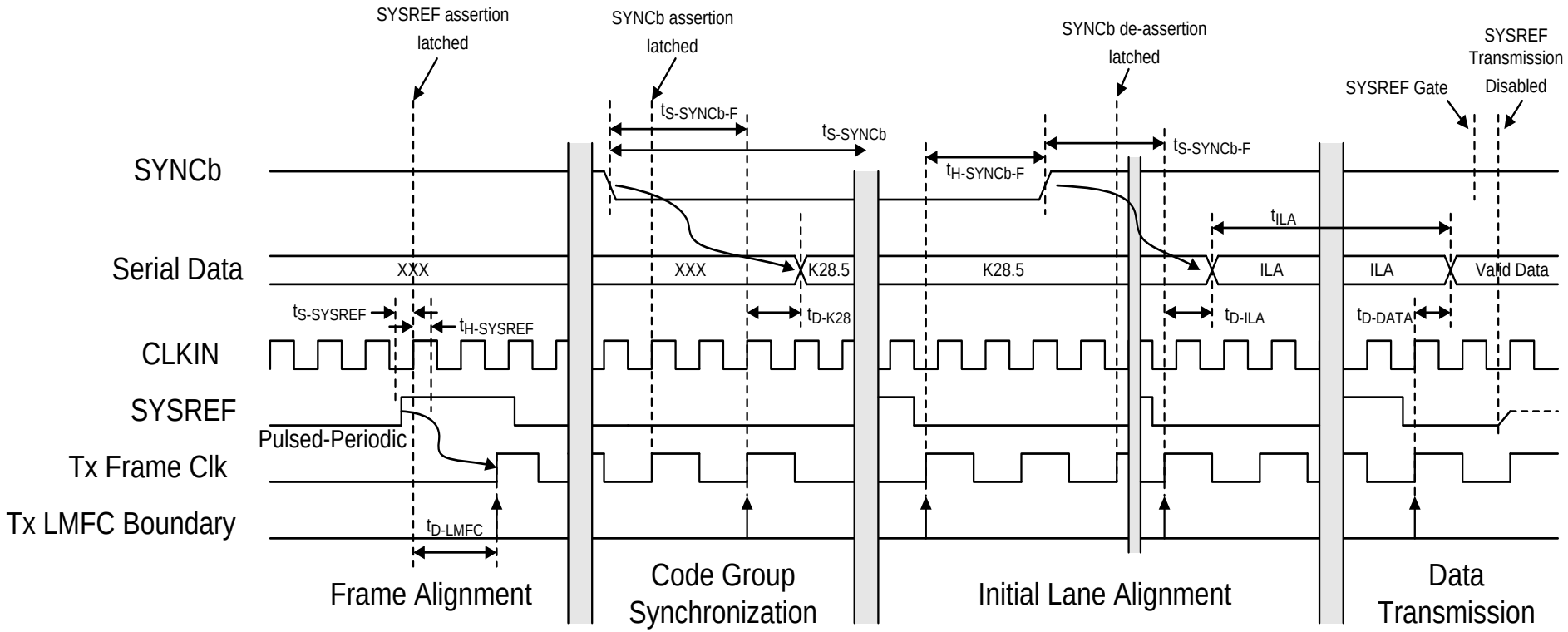
Link Layer: Initial Lane Synchronization

- Lanes are synchronized using initial lane alignment (ILA) sequence
- TX transmits ILA on next multi-frame boundary following CGS



- ILA is 4 multi-frames minimum, containing configuration parameters and alignment symbols (A)
- ILA is never scrambled, even if scrambling is enabled
- ILA information may be verified by the Rx, or it can be ignored if the Rx already expects a certain format

JESD204B Link Establishment



Link Layer: Frame Alignment Monitoring

- Transmitter sends out user data after ILA sequence
- Alignment characters are inserted into data stream in special conditions to re-check alignment
  - If last octet in 2 successive frame are equal → transmitter replaces latter octet with K28.7 symbol (scrambling disabled)
  - If last octet of a multi-frame is equal to last octet in previous frame → replace latter octet with K28.3 symbol
- Receiver “undoes” the special character replacement
- Receiver will re-align it’s frame clock to alignment characters under certain conditions
- **Texas Instruments** converter devices support both the monitoring and correction of lane alignments

Error Reporting

- Standard lists the following errors to be detected by each receiver.
  - 8B/10B disparity error
  - 8B/10B not-in-table code error
  - Control character in wrong position
  - Code Group Synchronization error

- Texas Instruments JESD204B DAC core also generates RX errors
  - Multiframe alignment error
  - Frame alignment error
  - Elastic buffer overflow (indicative of bad RBD value)
  - Link configuration error (TX and RX parameters do not match)
  - Some of the errors can be made to retrigger the synchronization request as specified by setting the corresponding bit in sync_req_ena configuration parameter

JESD204B Link Errors

- Elastic Buffer Overflow
  - Occurs when any of the RX lane buffers overflow before all the buffers have received their first non-/K28.5/ character
- Link Configuration mismatch
  - Occurs when the link configuration data sent in the 2nd multi-frame during ILA does not much the programmed RX configuration
- Frame alignment error
  - Occurs when /A/=/K28.3/ alignment char found but not at end of frame
- Multi-frame alignment error
  - Occurs when /F/=/K28.7/ alignment char found, but not at end of multi-frame
- 8b/10b disparity error
  - Occurs when received character is not consistent with running disparity
- 8b/10b not in table
  - Received 10-bit character is not found in the 8b/10b character table

Link Re-Initialization

- Under certain error conditions data receiver will request re-initialization of the link by asserting SYNC~
- Upon receiving the SYNC~ request, the transmitter device will start sending /K/ (K28.5) symbols
- A transmitter may also request re-initialization of the link by moving its state machine to the SYNC state and emitting a stream of /K/ symbols
- Minimum duration of SYNC~ request is defined by the standard to ensure a sufficiently long stream of /K/ symbols

Link Layer Test Modes

- Link layer test modes consist of predetermined sequences of 8b/10b characters that are transmitted in all frames and on all lanes of a multi-point link
- Link layer test characters are specified as if injected directly to the 8b/10b encoder and are never scrambled
- Link layer test modes required by JESD204B standard
  - Continuous /D21.5/ : high frequency pattern useful for random jitter (RJ) or receiver eye mask testing
  - Continuous /K28.5/ : medium frequency pattern useful for deterministic jitter (DJ) testing
  - Repeated ILA sequence
  - One of the following
    - Continuous sequence of modified random pattern (modified RPAT)
    - Continuous sequence of a scrambled jitter pattern (JSPAT)

Link Layer Test Modes

- All receiver devices must be able to verify the following:
  - A continuous sequence of /K28.5/ symbols for CGS
- Most devices must also support a CGS sequence followed by repeated ILA sequence
- All RX devices must also have the capability to suppress error reports due to a missing ILA
  - This feature enables BER measurements using standard test equipment which output 8b/10b encoded test patterns after initial synchronization with a K28.5 sequence
  - Most of the bit errors will lead to running disparity or not-in-table errors which will be evident by the RX asserting the SYNC~ interface
  - This allows the SYNC~ assertion to be used as a relatively accurate method for BER determination
- Additional test modes may be included in the TX physical layer

SYNC~ Signal Combining

- For a multi-lane link between an RX and TX device, the synchronization requests of all receivers are combined and presented simultaneously to the TX device.
- On multi-point links (one TX to multiple RX or multiple TX to one RX) the synchronization requests may be combined but it is not mandatory

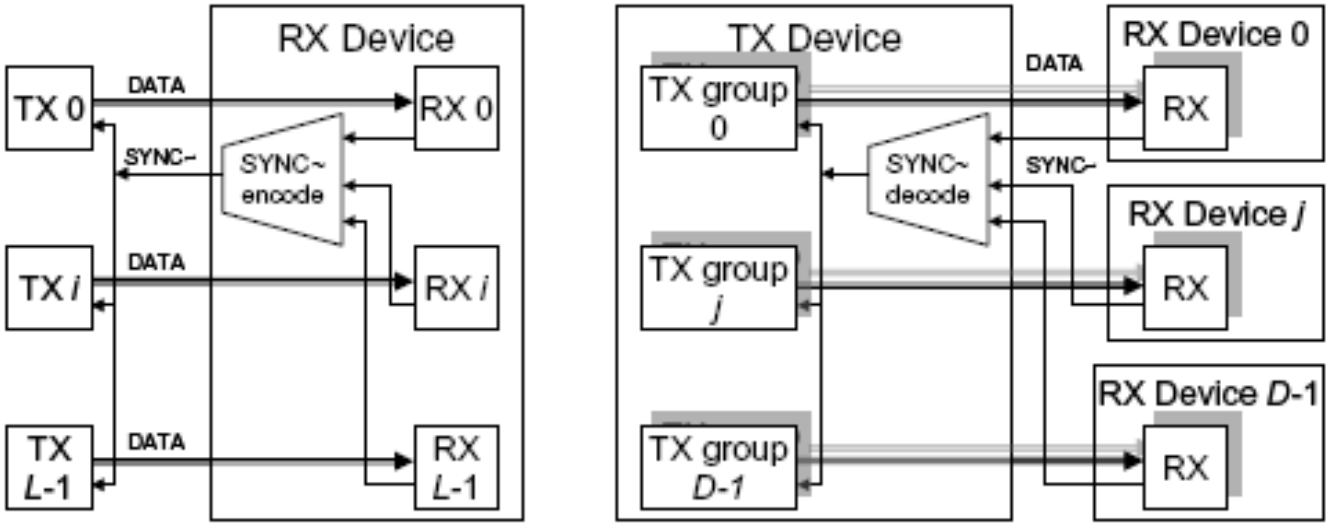


Figure 33 — Examples of SYNC~ signal combination

SYNC~ Signal Combining (cont'd)

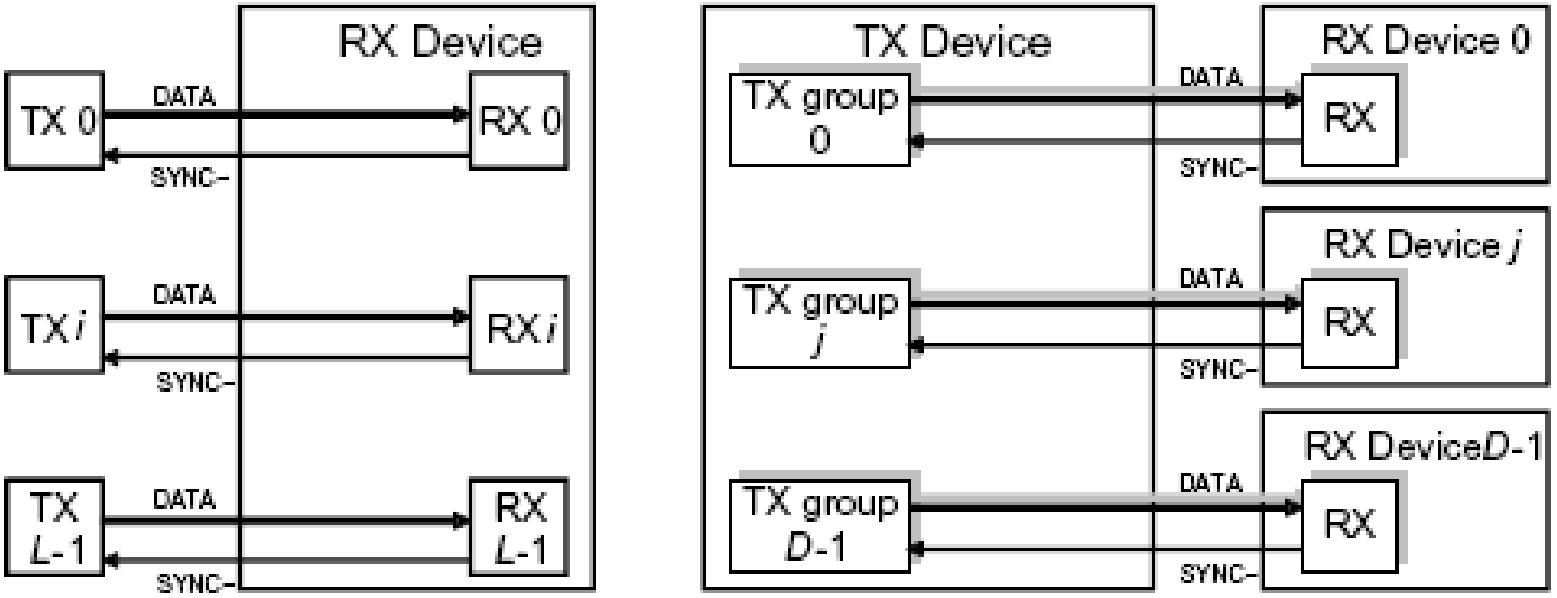


Figure 34 — Examples of non-combined SYNC~ signaling

Summary

- Transport Layer defines the mapping of data → octets → frames and is summarized by the transport layer parameters (LMFS, etc.)

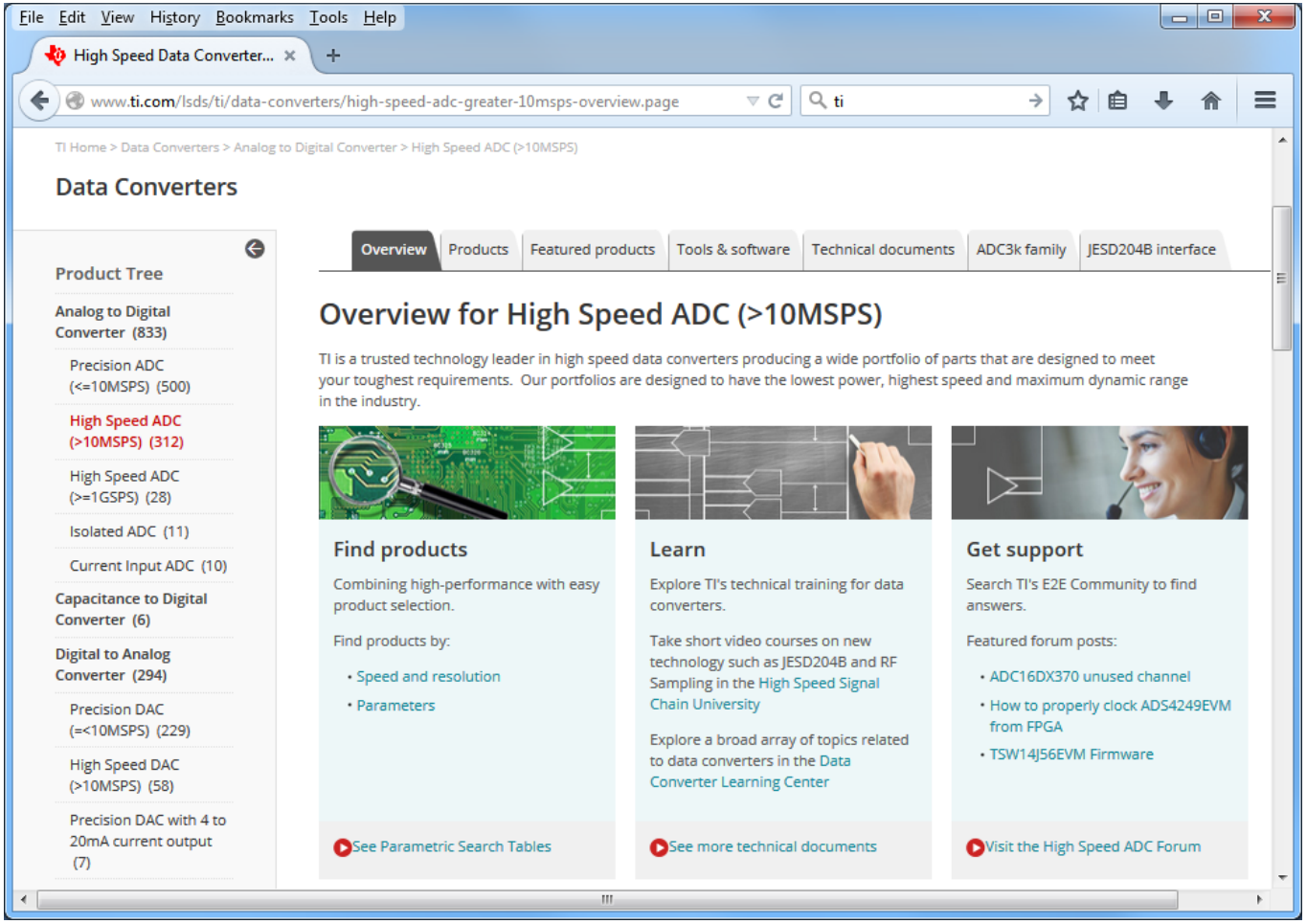
- Link Layout primarily consists of definitions for 8b/10b encoding, Link Synchronization and Link Monitoring

- The link synchronization sequence includes
  - Code group synchronization (CGS)
  - Initial frame synchronization
  - Initial lane synchronization (ILA)

- A variety of link errors are detected which may be reported over the SYNC~ interface or may trigger link re-synchronization

More Educational Resources

www.ti.com/lsds/ti/data-converters/high-speed-adc-greater-10msps-jesd204b.page



IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265