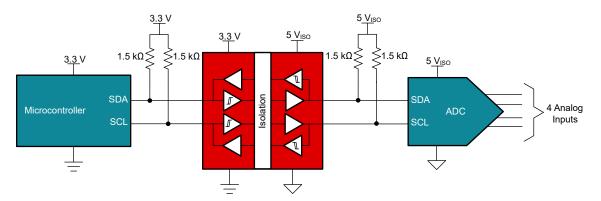
Product Overview Isolating I2C Signals





Example I2C Isolation Block Diagram

- Prevents DC and unwanted AC currents between controller devices and peripheral ICs
- · Allows signal transfer between controller devices and peripheral ICs
- · Protects low voltage parts in a system from high voltage circuits
- · Diminishes the effect of ground potential differences
- [FAQ] Why is the logic LOW level output voltage, VOL1, up to 0.8 V on Side 1 of the ISO1540/ISO1541 and ISO1640/ISO1641 bidirectional I2C isolators?
- [FAQ] ISO1640: Why are the maximum load capacitance and load current ratings for Side 1 of the ISO1640/ ISO1641 less than Side 2?
- I2C Bus Pullup Resistor Calculation
- Top 6 design questions about I2C Isolators
- How do Isolated I2C Buffers with Hot-Swap Capability and IEC ESD Improve Isolated I2C?
- Digital Isolator Design Guide

Need additional assistance? Ask our engineers a question on the *TI E2E™ Isolation Support Forum*

Part Number	AEC-Q100	Voltage Range	Data Rate	Bidirectional SCL Communication	Features
ISO1640		3.0 – 5.5 V (Side 1) 2.25 – 5.5 V (Side 2)	Standard Mode (0 to 100 kbps) Fast Mode (0 to 400 kbps) Fast-Mode Plus (0 to 1 Mbps) High-Speed Mode (0 to 3.4 Mbps)	√	High CMTI
ISO1640-Q1	1			√	Reinforced Isolation (ISO164xDW) Basic Isolation (ISO164xBD) Hot-Swappable I2C Connections Enhanced EMC
ISO1641					
ISO1643				1	Two additional unidirectional GPIO channels supporting up to 50Mbps
ESD Protection	Channel Count	Working Voltage	Clamping Voltage	Capacitance	IEC 61000-4-2 IEC 61000-4-5 Rating
TPD1E05U06	1	5.5 V	10 V	0.5 pF	12 kV 2.5 A
TPD2E2U06	2	5.5 V	9.7 V	1.5 pF	25 kV 5.5 A

For additional device options, browse the online parametric search tools for Isolated I2C Transceivers, Non-Isolated I2C Transceivers, and ESD Protection Devices.

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