Control Loop Design
SEPIC Preregulator Example

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Summary:

The control loop design approach from previous Unitrode Seminars is used to achieve optimized preregulator performance. Techniques for input current sensing and control are discussed — the usual methods don't work with the SEPIC topology. A small-signal model of the SEPIC preregulator is derived, including the coupled inductor used for ripple current steering.

Design Example

The SEPIC converter topology is more complex than the simple boost or flyback circuits most often used as high power factor preregulators. Accordingly, control loop problems are also more complex. Fortunately, in any high power factor preregulator application, the current loop control design is simplified because there is never a right half-plane zero associated with input current control, and because the very low bandwidth voltage control loop required to minimize line current distortion does not contribute to instability problems.

The specific control loop design example used in this paper is taken from a separate topic in this Seminar Manual.[1] The power circuit parameters are:

Switching frequency, fs:	100kHz
Coupled inductors, *L1, L2*:	2 mH
Leakage inductance, *LL*:	0.2 mH
Coupling capacitor, *Cc*:	0.5 µF
Sense transresistance, *Rs*:	0.2Ω
PWM sawtooth, p-p, *Vs*:	5 V
Output voltage, *Vo*:	200 V
Max. avg. power output:	200 W
Input voltage range, rms:	80-250 V

SEPIC Preregulator Control Loop

Design Approach

Overall current loop gain is optimized to achieve highest possible gain and bandwidth consistent with (a) Nyquist stability criteria for adequate phase margin at the 0 dB gain crossover frequency, *fc*, and (b) the unique requirements of a switched system to prevent subharmonic instability at 1/2 the switching frequency. The strategy to assure subharmonic stability is to match the worst-case slopes of the two input waveforms at the inputs of the PWM comparator during the OFF time of the power switch. This design approach has been the subject of previous Unitrode Seminars,[2] and will be demonstrated in this specific application. Graphic presentation using Bode plots helps provide clarity and discipline to the design process.

A two-loop system is used to control the high power factor (HPF) preregulator. The power circuit is contained within the inner current control loop, which is designed to complement the characteristics of the power circuit topology used. Outside of the properly optimized current loop, the specific topology inside the loop is not discernable. The closed current loop is programmed by a combination of output voltage feedback and fast and slow line voltage feedforward to achieve high power factor and output voltage regulation. The most sophisticated embodiment of these techniques to date is incorporated in the UC1854A control IC.

Power Circuit Gain

The coupled-inductor SEPIC converter power circuit is shown in Figure 1. In a high power factor preregulator, it is necessary to sense and control the input current. The first thing that is required in the current control loop design process is to plot the

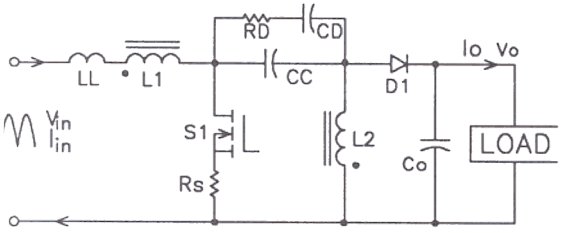

Fig 1. - SEPIC Power Circuit

small-signal gain vs. frequency of the power circuit (including the pulse width modulator). This requires a small-signal model of the specific topology. The model of the control-to-input current characteristic of the coupled-inductor SEPIC converter is developed in Appendix I at the end of this paper. The result, given in Equation 1, is the gain from the control output of the current amplifier to the voltage across the current sense resistor.

$$(1) \qquad \frac{v_{SR}}{v_{CA}} = \frac{R_S}{V_S} \frac{(I_{IN}+I_O) - jV_O/X_{L2}}{1-(f/f_R)^2}$$

where $R_S = V_{SR}/I_{IN}$, V_S is the p-p sawtooth voltage input to the PWM, $(I_{IN}+I_O)$ is the total current through the coupled inductor windings, V_O is the output voltage, and X_{L2} is the reactance of coupled inductor winding $L1$ or $L2$.

Except for the $1-(f/f_R)^2$ term in the denominator, The SEPIC gain given in Eq. 1 is identical to a flyback HPF circuit, which is not difficult to deal with.[3] But the SEPIC characteristic is complicated by the fact that leakage inductance L_L and coupling capacitor C_C resonate, with high Q. (L_L and C_C are closely coupled at all times.) The resonant frequency, f_R, is typically 1/10 of the switching frequency, f_S. Unfortunately, at f_R an *additional* 180° phase lag is *suddenly* introduced. This phase lag from 3 active poles (one variable) forces a loop gain crossover frequency f_C well below f_R.

A dilemma now exists: if f_C is set well below f_R, the loop can be made stable at and below f_C, but there will be large shock-excited oscillations at resonant frequency f_R superimposed on the input current. There is not enough loop gain at f_R to damp the ringing. On the other hand, if enough loop gain is provided at f_R to damp the ringing, the loop cannot be made stable because of the additional 180° phase shift at f_R.

A good solution to this problem is to control *average switch current* I_{SW} instead of input current I_{IN}. Below the resonant frequency f_R, I_{SW} is identical to I_{IN}, so if f_C is below f_R, it doesn't matter which is controlled. The small-signal model of the SEPIC converter with I_{SW} controlled is given in Eq. 2, derived in a similar manner to Eq. 1 above.

$$(2) \qquad \frac{v_{SR}}{v_{CA}} = \frac{R_S}{V_S}[(I_{IN}+I_O) - jV_O/X_{L2}]$$

Note that Equations 1 and 2 are exactly the same except for the denominator expression $1-(f/f_R)^2$. Eq. 2 is the same as for a flyback preregulator.[3] Taking this approach, the current loop design is simplified, and I_{SW} will behave perfectly. But the L_L-C_C resonant effect is now outside of the current control loop, so the input current will still have intolerable ringing superimposed. A separate damping network C_D and R_D in shunt with C_C takes care of this problem, independent of the current loop.

An additional major advantage of sensing average switch current instead of I_{IN} is that a current transformer (CT) can be used for current sensing. The discontinuous switch current waveform provides time for the CT to reset. The expense and power loss of a sense resistor is eliminated. Average CMC is necessary because peak switch current does not correlate with average. Peak switch current limiting is also needed for control during start-up and severe overload. The peak and average switch current information are both obtained from one current transformer.

Eq. 2 for power circuit gain (including PWM) with I_{SW} controlled is plotted in Fig. 2 using the values from page 1. The gain plotted is from the current amplifier output, v_{CA}, to the voltage across the current sense resistor, v_{RS}. At light loads, the $I_{IN}+I_O$ terms in Eq. 2 are negligible. Using the values of this example the power circuit gain is:

$$(3) \qquad \frac{v_{SR}}{v_{CA}} = \frac{-jR_S V_O}{V_S X_{L2}} = \frac{-j\,0.2\times200}{5\times2\pi\times.002} = \frac{-j637}{f}$$

Thus, at light load, a single pole is active over the entire range (solid line). A zero which varies

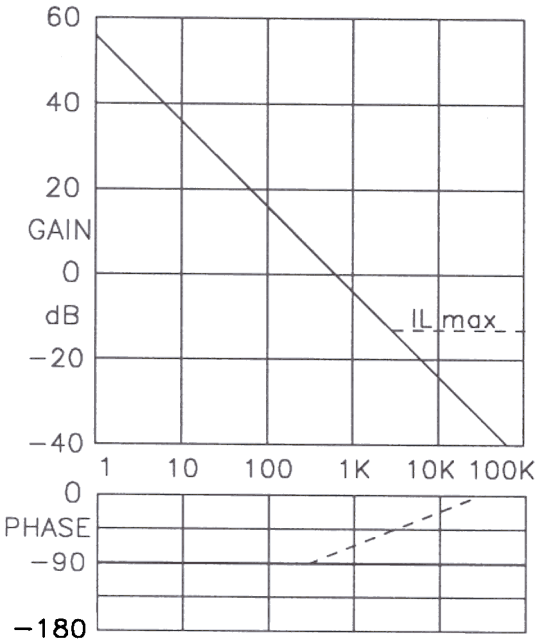

Fig 2. - Power Circuit Gain v_{RS}/v_{CA}

according to total coupled inductor current ($I_{IN}+I_O$) is indicated by the dash line. The lowest zero frequency is shown, at maximum inductor current. This occurs at *peak* low line voltage (113V) and full power (P_{pk} = 200W). I_{IN} = 400W/113V = 3.5A, I_O = 400W/200V = 2A, for a total 5.5A max. inductor current. The gain above this zero is fixed:

$$(4)\quad \frac{v_{SR}}{v_{CA}} = \frac{R_S(I_{IN}+I_O)}{V_S} = \frac{0.2\times 5.5}{5} = .22$$

Current Amplifier Gain

The current amplifier complements the power circuit gain characteristic to complete the overall current loop. Figure 3 shows the current amplifier and PWM comparator added to the SEPIC power circuit for average current mode control of switch current. Current sense resistor *Rs* represents a "transresistance" which translates switch current into a voltage input to the current amplifier. In this case, *Rs* = 0.2Ω translates 5 Amps into 1 Volt. But an *Rs* of 0.2Ω could also be a CT with 1:100 ratio and secondary load of 20Ω, which also translates 5 Amps into 1 Volt (but with much less power loss).

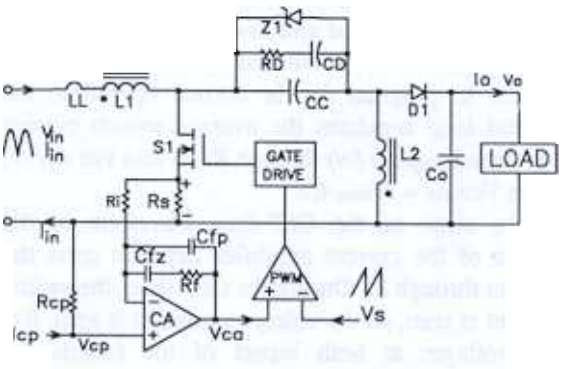

Fig 3. - Average CMC of Switch Current

The best approach to designing the current amplifier (CA) compensation network is to start at the switching frequency, using the slope matching technique to assure subharmonic stability. Then work down to lower frequencies to achieve the highest possible crossover frequency with adequate phase margin.

Slope matching: With fixed frequency PWM operation, the switch turns on at each clock pulse. The switch turns off when the oscillator ramp and control signal waveforms converge at the input of the PWM comparator. Depending on the gain, the waveforms (during the OFF time) will then either (a) cross over, (b) track each other (slopes match), or (c) diverge. It can be shown graphically and mathematically that if the OFF-time control signal slope exceeds twice the oscillator ramp slope, the control loop may experience sub-harmonic oscillation, at half the switching frequency.

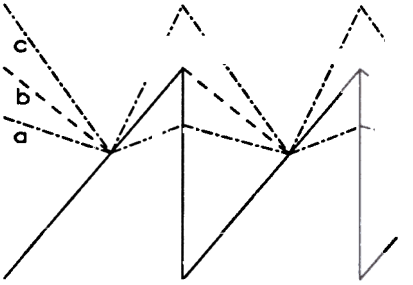

Fig 4. - PWM Comparator Input Waveforms

The easiest and most definite way to prevent this is to set the high frequency CA gain so the OFF-time slopes coincide under worst case conditions.

With the SEPIC converter, this is at maximum I_{IN}, occurring at full load and low line voltage peak.

Voltage V_{CP} is established by the outer control system to program I_{IN}. In normal operation, the current loop regulates the average switch current I_{SW} (which equals I_{IN}) through R_S so that $V_{RS} = V_{CP}$. Thus $V_{CPmax} = I_{INmax} \cdot R_S$.

The slope of the OFF-time waveform at the output of the current amplifier depends upon the current through R_i. During the OFF time, the switch current is zero, so the voltage across R_S is zero. But the voltages at both inputs of the functioning current amplifier are identical, equal to V_{CPmax}. So the maximum current through R_i (resulting in the maximum OFF-time slope at the comparator input) equals V_{CPmax}/R_i.

Calculate the OFF-time CA output slope :

$$\frac{dv_{CA}}{dt} = \frac{I_{Ri}}{C_{fp}} = \frac{V_{CPmax}}{R_i C_{fp}} = \frac{I_{INmax} R_S}{R_i C_{FP}}$$

Oscillator ramp slope :

$$dV_S/dt = V_S/T_S = V_S f_S$$

Equate the slopes :

$$\frac{I_{INmax} R_S}{R_i C_{FP}} = V_S f_S$$

Solve for C_{FP} :

$$C_{FP} = \frac{I_{INmax} R_S}{V_S f_S R_i}$$

Using the values from this example, and assuming R_i = 5K :

$$C_{FP} = \frac{3.5A \times 0.2\Omega}{5V \times 100K \times 5K} = 280 \text{ pF}$$

The high frequency CA integrator gain:

$$\text{CA gain} = \frac{-j}{2\pi f R_i C_{FP}} = \frac{-j\,114{,}000}{f}$$

High frequency loop gain (light load) is CA gain x Power circuit gain:

$$\text{Loop Gain} = \frac{-j\,637}{f} \frac{-j\,114{,}000}{f} = \frac{72 \times 10^6}{f^2}$$

CA gain and loop gain are entered in the Bode plot

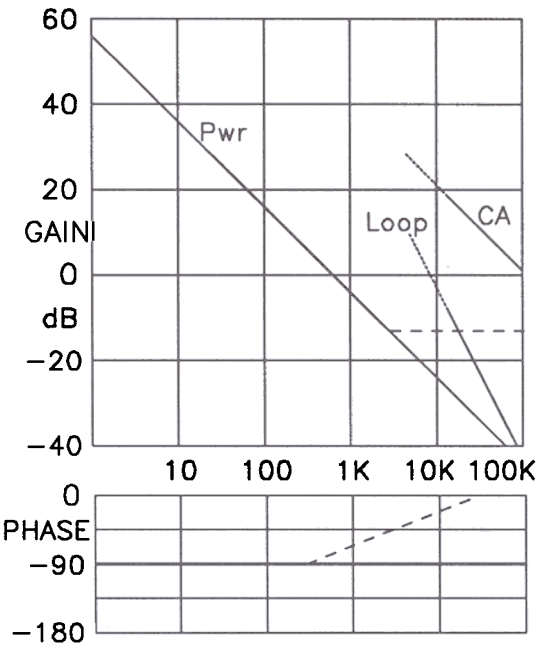

Fig 5. - Slope Matching Results Entered

of Fig. 5. (Loop gain is plotted above 50kHz for convenience although gain is not valid for a switched system.) Note that the CA gain crosses zero at ≈100kHz, easily satisfied by an amplifier bandwidth of only 500kHz.

It can be seen that the overall loop gain has two active poles where it crosses over at 0 dB gain, resulting in 180° excess phase lag and 0° phase margin at crossover. This is at the borderline of oscillation and is totally unacceptable.

The strategy to bring stability to this loop is to add a "phase bump" centered on the crossover frequency to flatten the gain characteristic and provide 45° phase margin at crossover. A zero at $f_C/2.5$ and a pole at $2.5f_C$ provides a -1 slope for a span of 2.5^2, or 6.25, centered on f_C. The crossover frequency is not yet determined, but with a -1 slope through crossover, the gain at $2.5f_C$ must equal 1/2.5, (-8dB). Inserting a gain of 0.4 in the high frequency loop gain expression and solving for f_P:

$$f_P = \left(\qquad \right)^{1/2} = 13.4 \text{ kHz}$$

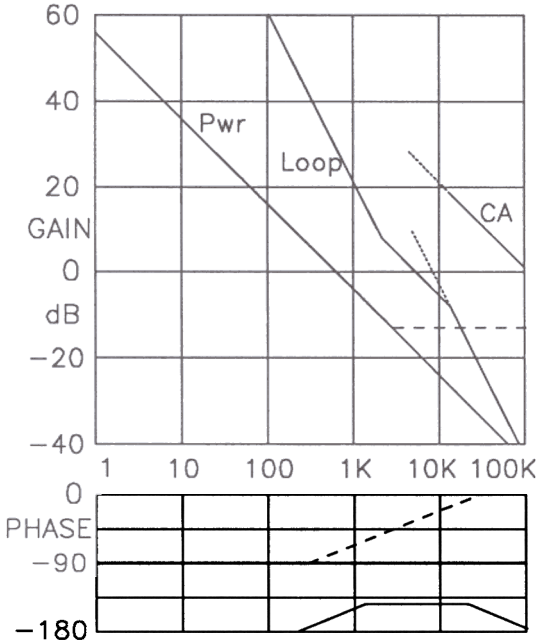

Fig 6. - Phase Bump Added to Loop Gain

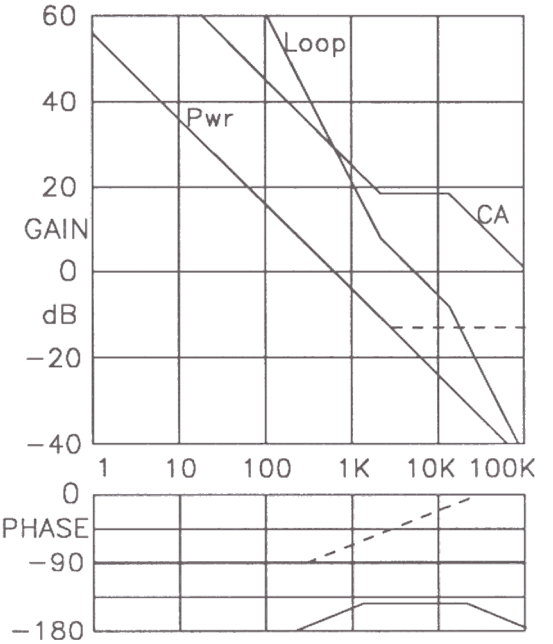

Fig 7. - Zero-Pole Pair Added to CA Gain

This result is plotted in Fig. 6. Crossover frequency *fc* is obviously *fp*/2.5 = 5.36kHz, and *fz* = *fc*/2.5 = 2.14 kHz, with a gain of 2.5 (+8dB). Phase margin is approximately 45°, although the straight lines of the Bode plot indicate 39°.

To achieve this result, the zero-pole pair at 2.14 kHz and 13.4 kHz are incorporated in the feedback network around the current amplifier. R_F and C_{FP} determine the pole frequency:

$$R_F = \frac{1}{2\pi f_{CP} C_{FP}} = 42K$$

Rather than calculate the value of C_{FZ} from the zero frequency (which is a little complicated), it is easier to observe that the CA gain below *fz* is a -1 slope, just like the gain above *fp*, but offset by a factor of 6.25, the span of the zero-pole pair. Therefore, the parallel combination of C_{FP} and C_{FZ} at low frequencies is 6.25 times C_{FP}. So C_{FZ} is 5.25 times C_{FP}, or 5.25·280pF = 1470pF.

The current amplifier is now defined and its gain characteristic is shown in Figure 7.

The final step in this process is to plot the overall loop gain and phase at maximum inductor current conditions, shown as the dash line in the power circuit plot. Figure 8 shows the operating extremes. Worst case for phase margin at crossover is with light load. (Worst case for subharmonic instability is at full load, but this was taken care of by slope matching.) Although the crossover frequency increases substantially at full load, the phase margin is more than adequate. Transient response will be little different over the load range because the loop gain characteristic below 3 kHz is fixed.

Component values: The values that were calculated for the current amplifier compensation network are summarized:

R_i	5K
R_f	42K
C_{FP}	280pF
C_{FZ}	1470pF

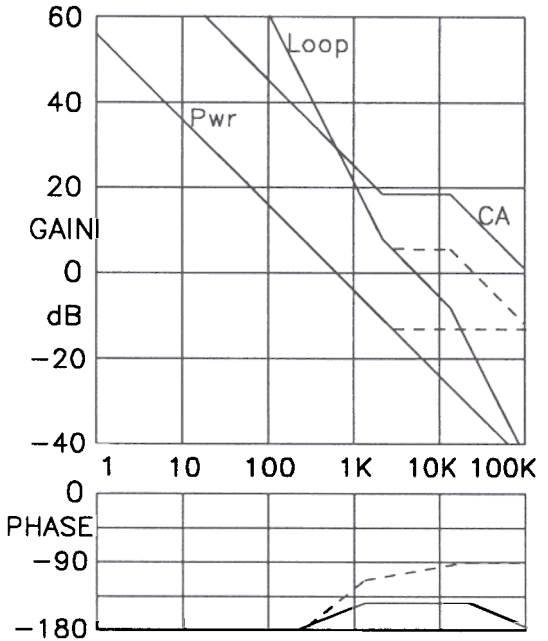

Fig 8. - Final Current Loop Definition

Peak Current Limiting:

Peak current limiting is necessary under start-up and extreme overload conditions. When *Vo* is low, the duty cycle becomes very small, resulting in very large peak/average current ratios. Average current limiting alone cannot prevent high peak currents from causing inductor saturation and impairment of switch and rectifier reliability. Peak current limiting is discussed in Reference [1].

Programming the Current:

Control circuitry external to the current loop programs the current level by means of the voltage V_{CP} applied to the reference input of the current amplifier. With a properly designed current loop, the resulting input current $I_{IN} = V_{CP}/Rs$. This is true *regardless of the power circuit topology within the current loop.* Thus in all cases, the closed current loop appears externally as a transconductance $1/Rs$. Techniques for power factor correction and output voltage regulation are generally applicable with any topology. A sophisticated approach to accomplish these goals using the UC1854 is discussed in [4].

References:

[1] L.H. Dixon, "High Power Factor Preregulator Using the SEPIC Converter," *Unitrode Seminar SEM900, Topic 6*, 1993

[2] L.H. Dixon, "Control Loop Design," *Unitrode Seminar SEM800*, 1991 (Reprinted as Topic C1 in SEM900)

[3] L.H. Dixon, "Average Current Mode Control of Switching Power Supplies," *Unitrode Seminar SEM700*, 1990 (Reprinted as Topic C1 in SEM800 and App. Note U-140 in the Unitrode Databook)

[4] L.H. Dixon, "High Power Factor Switching Preregulator Design Optimization," *Unitrode Seminar SEM700*, 1990 (Reprinted as Topic I3 in SEM800, SEM900)

Appendix I - Derivation of the Small-Signal Model

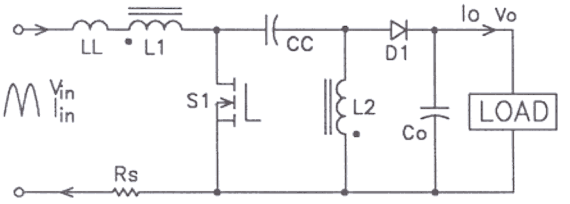

Fig. A1 - SEPIC Converter

BASIC RELATIONSHIPS:

L_1 and L_2 are coupled, with equal turns: $v_{L1} = v_{L2}$ L_L is leakage inductance.

V_O = Constant, V_{IN} = instantaneous rectified line, considered constant at high frequency.

$$D = V_O/(V_{IN}+V_O)$$
$$(1-D) = V_{IN}/(V_{IN}+V_O)$$

DC inductor voltages must equal zero, therefore:

$$V_C = V_{IN} \quad \text{and} \quad D = V_O/(V_C+V_O)$$

DC capacitor current must equal zero, therefore:

$$I_{IN} = I_{SW} \; ; \quad I_O = I_{L2}$$
$$I_O = (I_{IN}+I_{L2})(1-D) \; ; \quad (I_{IN}+I_{L2}) = I_O/(1-D)$$
$$I_{SW} = (I_{IN}+I_{L2})D \; ; \quad (I_{IN}+I_{L2}) = I_{SW}/D$$

DERIVATION:

DC Capacitor current must equal zero. By inspection:

$$I_C = I_{IN}(1-D) - I_{L2}D = 0$$
$$i_C = i_{IN}(1-D) - I_{IN}d - I_{L2}d - i_{L2}D$$
$$i_C = i_{IN} - (i_{IN}+i_{L2})D - (I_{IN}+I_{L2})d$$

(1) $$i_{IN} = (i_{IN}+i_{L2})D + (I_{IN}+I_{L2})d + i_C$$

Developing substitutes for the above terms:

L1 and L2 actually represent a single inductor, whose currents *collectively* determine the voltage across the coupled windings:

(2) $$(i_{IN}+i_{L2}) = -jv_{L2}/X_{L2} = -jv_{L1}/X_{L1}$$

$$V_{L2} = V_C D - V_O(1-D) = 0$$
$$v_{L2} = V_C d + v_C D + V_O d = (V_C+V_O)d + v_C D$$

(3) $$v_{L2} = V_O d/D + v_C D$$

Substitute (3) into (2) and multiply by D

(4) $$(i_{IN}+i_{L2})D = -jV_O d/X_{L2} - jv_C D^2/X_{L2}$$

Examine the ac voltages in the circuit mesh containing V_{IN}, L_L, L_1, C_C, and L_2.

Since $v_{L1} = v_{L2}$, and ac voltage across $V_{IN} = 0$,

(5) $$v_C = - v_{LL}$$

(6) $$v_C = - v_{LL} = -ji_{IN}X_{LL}$$

Substituting into (4):

$$(i_{IN}+i_{L2})D = -jV_O d/X_{L2} + j^2 i_{IN} D^2 X_{LL}/X_{L2}$$

(7) $$(i_{IN}+i_{L2})D = -jV_O d/X_{L2} - i_{IN} D^2 L_L/L_2$$

Since $v_{LL} = ji_{IN}X_{LL}$, and $v_C = -ji_C X_C$

from (5), $\therefore$ $ji_C X_C = ji_{IN}X_{LL}$

(8) $$i_C = i_{IN}X_{LL}/X_C = i_{IN}\omega^2 L_L C_C = i_{IN}(f/f_R)^2$$

Substituting (7) and (8) into (1):

(9) $$i_{IN} = -jV_O d/X_{L2} - i_{IN} D^2 L_L/L_2 + (I_{IN}+I_{L2})d + i_{IN}(f/f_R)^2$$

Rearranging:

$$i_{IN}(1 + D^2 L_L/L_2 - (f/f_R)^2) = ((I_{IN}+I_{L2}) - jV_O/X_{L2})d$$

(10) $$\frac{i_{IN}}{d} = \frac{(I_{IN}+I_O) - jV_O/X_{L2}}{1 + D^2 L_L/L2 - (f/f_R)^2}$$

Term $D^2L_L/L_2 << 1$, therefore negligible.

At resonance, gain becomes infinite, with sudden 180° phase shift.

If $v_{SR} = i_{IN}R_S$ and $d = v_{CA}/V_S$, then power circuit gain is:

(11) $$\frac{v_{SR}}{v_{CA}} = \frac{R_S}{V_S}\frac{(I_{IN}+I_O) - jV_O/X_{L2}}{1 - (f/f_R)^2}$$

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