

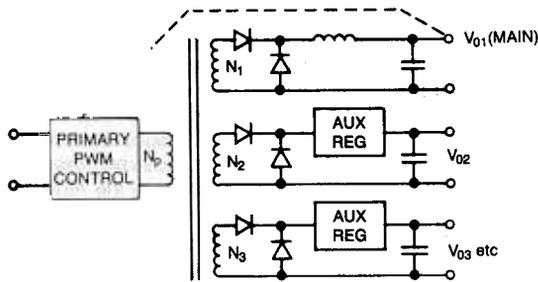
# **Magnetic Amplifier Control for Simple, Low-Cost, Secondary Regulation**

*by Bob Mammano*

**TOPIC 7**

# Magnetic Amplifier Control for Simple, Low-Cost, Secondary Regulation

Regulating multiple outputs of a switching power supply has always presented an additional challenge to the designer. With a single pulse-width modulated control system, how can the control loop be configured to keep all outputs in regulation when each may have varying loads? Although it is sometimes possible to average an error signal from each output — degrading the regulation on some outputs to improve on others — a more common approach, as shown in Figure 1, is to close the overall power supply loop to the output with the highest load current and opt for some form of auxiliary — or secondary — regulation for all the other outputs.



**Figure 1. A typical multiple output power supply architecture with overall control from one output.**

## Secondary Regulators

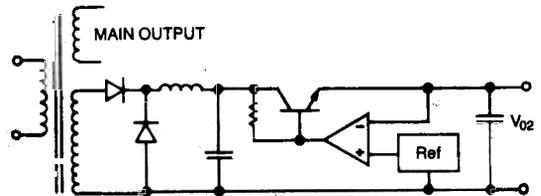
The problem with multiple outputs originates from the fact that the open-loop output impedance of each winding, rectifier, and filter set is not zero. Thus, if one assumes that the overall feedback loop holds the output of  $V_{01}$  constant, then the energy delivered to  $N_1$  must increase with increasing load on that output. This is accomplished by increasing the duty cycle on  $N_p$  which, of course, is seen by all the secondaries causing the unregulated outputs to rise.

Similarly, a changing load on one of the unregulated outputs will cause a direct change in that output as a function of its output impedance. Since the overall feedback loop is not sensing this output, no correction can take place. While these problems are minimized by closing the feedback loop on the highest power output, they aren't eliminated in any multiple output supply which sees varying loads. Using secondary regulators on each output other than the one controlled by the feedback loop is the usual solution. One additional benefit of these regulators, particularly as higher frequencies reduce the transformer turns, is to compensate for the fact that practical turns ratios may not match the ratio of output voltages.

Clearly, adding any form of regulator in series with an output adds additional complexity and power loss. The challenge is to minimize both. Before getting into mag amps, it is worth discussing some other commonly used solutions to this problem.

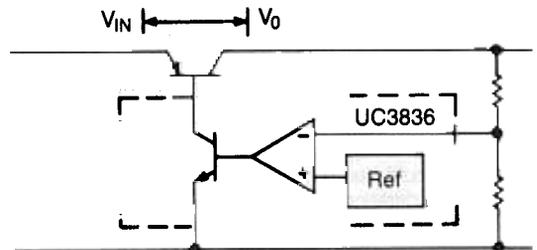
## Linear Regulators

Linear regulators usually trade efficiency for simplicity. There is always an added power loss equal to the input-output voltage differential across the regulator times the load current passing through it. Since these are DC regulators, a rectifier-filter must precede the regulator as shown in Figure 2. There are at least three reasons why the use of linear regulators may be an acceptable choice.



**Figure 2. Secondary regulation by means of a linear, DC regulator.**

1. Since our premise is that these regulators would be used on the lower power outputs, their power losses may be a small percentage of the overall power supply losses.
2. The fact that a secondary regulator needs only to compensate for the non-zero output impedances of the various outputs means that its input need not see a widely varying input voltage level.
3. There have been "high-efficiency" linear regulators introduced, such as the UC3836 shown in Figure 3, which allows the minimum input voltage to go down to less than 0.5 volts over the output voltage. With a low minimum ( $V_{IN} - V_O$ ), the average value can also be low, offering significant power savings.



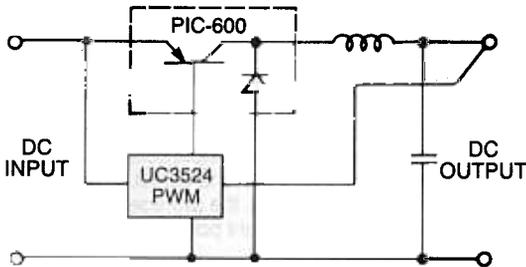
**Figure 3. The UC3836 provides a more efficient linear regulator by minimizing the minimum input-output differential.**

The advantages of a linear regulator are simplicity, good regulation unaffected by other parts of the power supply, and lowest output ripple and noise.

## Independent Switchers

A second type of commonly used secondary regulator is some kind of switching DC to DC converter — usually a buck regulator as shown in Figure 4. In the past, this approach was often used when load current levels made the power loss of a linear regulator unacceptable. The disadvantage of the complexity over a linear regulator has been minimized with the availability of several integrated circuit products. Figure 4, for example, shows the combination of a PIC-600 power stage and a UC3524 PWM controller, usable for load currents to 10 amps. An equally popular solution is Unitorde's L296 4-amp buck regulator. The obvious advantage of a switcher is potentially higher efficiency; however, there are also several disadvantages:

1. In their simplest form, these are generally DC to DC converters meaning that as an independent secondary regulator, an additional rectifier and LC filter would be needed at the input.
2. To alleviate the above problem, a pulse regulation technique could be used, but this introduces problems with frequency synchronization to the primary switching frequency.
3. This, in turn, can lead to another problem. Since most IC regulators use trailing-edge modulation, a primary side current mode controller can become confused with secondary switchers as the primary current waveform may not be monotonic.
4. And finally, the power losses of a switcher are not zero and making them insignificant to the total power supply efficiency may not be a trivial task.



**Figure 4. A secondary buck-type switching regulator is most easily implemented with a PIC-600 power module and an IC controller.**

There are at least two applications where some type of switcher would clearly be the best solution. One is where other considerations require something besides a step-down converter. For example, a higher voltage could be generated by using a boost configuration switching regulator.

A second usage for a switcher is for very low output voltages — 5 volts or less. Here the use of a BISYN® low-voltage, synchronous switch allows operation right off the secondary winding, eliminating both the rectifier diodes and the input LC filter. In this respect, a BISYN operates similar to a mag amp and can be a very efficient low-voltage secondary regulator.

## Magnetic Amplifiers

Although called a magnetic amplifier, this application really uses an inductive element as a controlled switch. A mag amp is a coil of wire wound on a core with a relatively square B-H characteristic. This gives the coil two operating modes: when unsaturated, the core causes the coil to act as a high inductance capable of supporting a large voltage with little or no current flow. When the core saturates, the impedance of the coil drops to near zero, allowing current to flow with negligible voltage drop. Thus a mag amp comes the closest yet to a true "ideal switch" with significant benefits to switching regulators.

Before discussing the details of mag amp design, there are a few overview statements to be made. First, this type of regulator is a pulse-width modulated down-switcher implemented with a magnetic switch rather than a transistor. It's a member of the buck regulator family and requires an output LC filter to convert its PWM output to DC. Instead of DC for an input, however, a mag amp works right off the rectangular waveform from the secondary winding of the power transformer. Its action is to delay the leading edge of this power pulse until the remainder of the pulse width is just that required to maintain the correct output voltage level. Like all buck regulators, it can only subtract from the incoming waveform, or, in other words, it can only lower the output voltage from what it would be with the regulator bypassed.

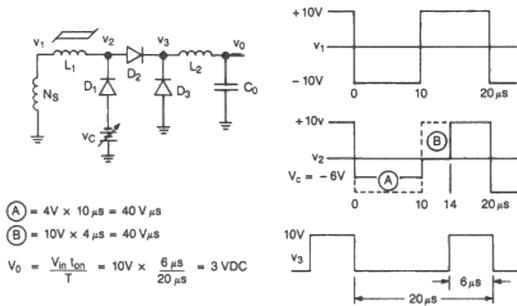
As a leading-edge modulator, a mag amp is particularly beneficial in current mode regulated power supplies as it insures that no matter how the individual output loading varies, the maximum peak current, as seen in the primary, always occurs as the pulse is terminated.

## Mag Amp Operation

Figure 5 shows a simplified schematic of a mag amp regulator and the corresponding waveforms. For this example, we will assume that  $N_s$  is a secondary winding driven from a square wave such that it provides a  $\pm 10$  volt waveform at  $v_1$ . At time  $t = 0$ ,  $v_1$  switches negative. Since the mag amp, L1, had been saturated, it had been delivering  $+10V$  to  $v_3$  prior to  $t = 0$  (ignoring diode drops). If we assume  $v_c = -6V$ , as defined by the control circuitry, when  $v_1$  goes to  $-10V$ , the mag amp now has 4 volts across it and reset current from  $v_c$  flows through D1 and the mag amp for the  $10 \mu\text{sec}$  that  $v_1$  is negative. This net 4 volts for  $10 \mu\text{sec}$  drives the mag amp core out of saturation and resets it by an amount equal to  $40V\text{-}\mu\text{sec}$ .

When  $t = 10 \mu\text{sec}$  and  $v_1$  switches back to  $+10V$ , the mag amp now acts as an inductor and prevents current from flowing, holding  $v_2$  at  $0V$ . This condition remains until the voltage across the core — now 10 volts — drives the core back into saturation. The important fact is that this takes the same  $40 \text{ volt-}\mu\text{sec}$  that was put into the core during reset.

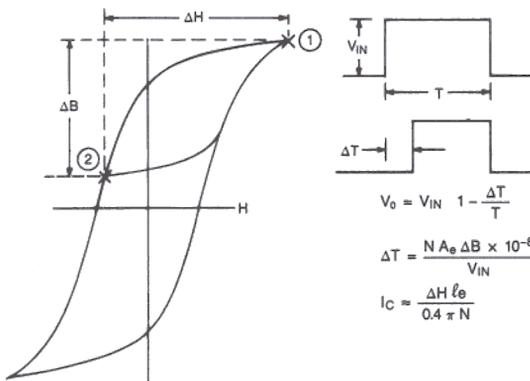
When the core saturates, its impedance drops to zero and  $v_1$  is applied to  $v_2$  delivering an output pulse but with the leading edge delayed by  $4 \mu\text{sec}$ .



**Figure 5. A simplified mag-amp regulator and characteristic waveforms.**

Figure 6 shows the operation of the mag amp core as it switches from saturation (point 1) to reset (point 2) and back to saturation. The equations are given in cgs units as:

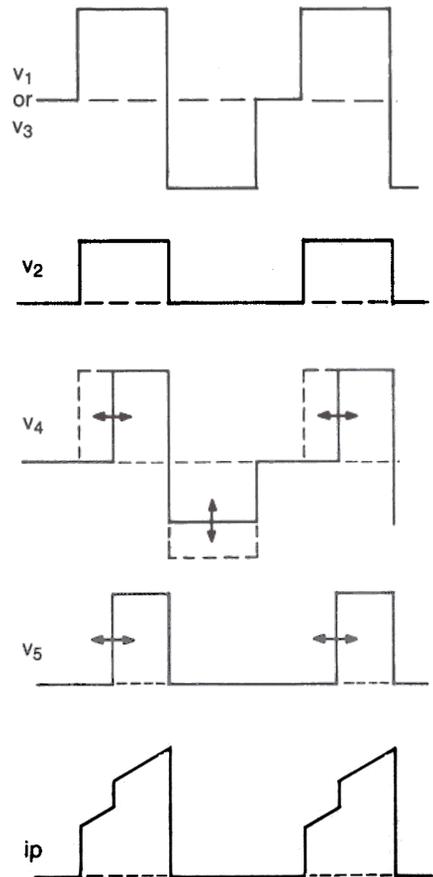
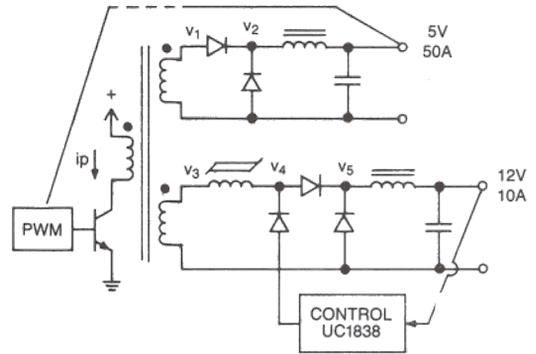
- N = mag amp coil turns
- Ae = core cross-section area, cm<sup>2</sup>
- ℓe = core magnetic path length, cm
- B = flux density, gauss
- H = magnetizing force, oersteds



**Figure 6. Operating on the B-H curve of the magnetic core.**

The significance of a mag amp is that reset is determined by the core and number of turns and not by the load current. Thus, a few milliamps can control many amps and the total power losses as a regulator are equal to the sum of the control energy, the core losses, and the winding I<sup>2</sup>R loss — each term very close to zero relative to the output power.

Figure 7 shows how a mag amp interrelates in a two-output forward converter illustrating the contribution of each output to primary current. Also shown is the use of the UC1838 as the mag amp control element.

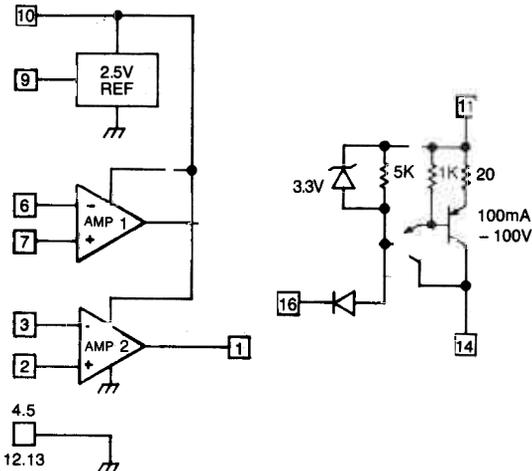


**Figure 7. Control waveforms for a typical two-output, secondary regulated, forward converter.**

## The UC1838 Mag Amp Controller

This IC has been designed specifically as a controller for mag amp switching regulators. Its block diagram of Figure 8 shows three functions:

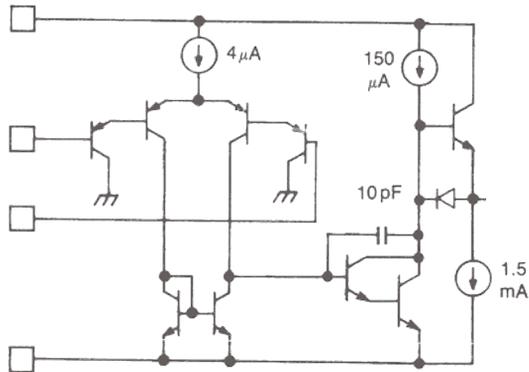
1. An independent, precision, 2.5V reference
2. Two identical operational amplifiers
3. A PNP output driver



**Figure 8. The block diagram of the UC1838 mag-amp control integrated circuit.**

The reference is a band gap design, internally trimmed to 1%, and capable of operating with a supply voltage of 4.5 to 40 volts. The op amps are identical with a structure as shown simplified in Figure 9. These have PNP inputs for a common mode input range down to slightly below ground, are internally unity-gain compensated for a bandwidth of 800 KHz, and have class A outputs with a 1.5mA current sink pull-down. The open-loop voltage gain is 120db to a single pole at 1 Hz with an additional phase lag of 15° at 1 MHz. Two op amps are included to provide several options. For example, if one is used to close the voltage feedback loop, the other can be dedicated to some protection function such as current limiting or over-voltage shutdown. Alternatively, if greater loop gain is required, the two amplifiers could be cascaded.

The PNP output driver can deliver up to 100 mA of reset current with a collector voltage swing of as much as 100V negative (within the limits of package power dissipation). Remembering that the mag amp will block more volt-seconds with greater reset, pulling the input of the driver low will attempt to reduce the output voltage of the regulator. Thus, there are two inputs, diode "OR"ed to turn-on the driver, turning-off the supply output. When operating as a current source, the response of this driver circuit is flat to one megahertz, at which point it has introduced 90° of phase shift.



**Figure 9. Simplified schematic of each of the operational amplifiers contained within the UC1838.**

Current limiting of the output driver is achieved by means of the 3.5V zener clamp (which is temperature compensated to match two  $V_{BE}$ 's) in conjunction with the 20Ω emitter resistor. Pin 11 of the driver can be connected to any convenient voltage source from 5DVC to the level used for Pin 10.

## Mag Amp Design Principles

One of the first tasks in a mag amp design is the selection of a core material. Technology enhancements in the field of magnetic materials have given the designer many choices while at the same time, have reduced the costs of what might have been ruled out as too expensive in the past. A comparison of several possible materials is given in Figure 10. Some considerations affecting the choices could be:

1. A lower  $B_{max}$  requires more turns — less important at higher frequencies.
2. Higher squareness ratios make better switches
3. Higher  $I_M$  requires more power from the control circuit
4. Ferrites are still the least expensive
5. Less is required of the mag amp if it only has to regulate and not shut down the output completely.

MATERIALS						
Trade Name	Composition	$B_{max}$ (kG)	Core Loss @ $B_{max}$	Squareness Ratio	Turns Req'd	$I_M$ (A)
Example: Similar Toroids, 1" O.D., 0.75" I.D., 0.25" High, 25KHz, 20V.						
Sq. Permalloy 80	79% Ni, 17% Fe	7	1.2W	0.9	19	0.04
Supermalloy	78% Ni, 17% Fe, 5% Mo	7	1.0W	0.55	19	0.03
Orthonal	50% Ni 50% Fe	14	7.2W	0.97	10	0.39
Sq. Metglass	Fe, B	16	7.6W	0.5	9	0.06
Power Ferrites	Mn, Zn	4.7	1.8W	0.4	11	0.1
Sq. Ferrite (Fair-Rite #83)	Mn	3.9	2.8W	0.9	13	0.4

**Figure 10. A comparison of several types of core materials available for mag-amp usage.**

In addition to selecting the core material, there are additional requirements to define, such as:

1. Regulator output voltage
2. Maximum output current
3. Input voltage waveform including limits for both voltage amplitude and pulse width
4. The maximum volt-seconds — called the “withstand Area,”  $\Lambda$  — which the mag amp will be expected to support.

With these basic facts, a designer can proceed as follows:

1. Select wire size based on output current. 400 Amp/cm<sup>2</sup> is a common design rule.

2. Determine core size based upon the area product:

$$A_w A_e = \frac{A_x \cdot \Lambda \cdot 10^8}{\Delta B \cdot K} \quad \text{where}$$

$A_w$  = Window area, cm<sup>2</sup>

$A_e$  = Effective core area, cm<sup>2</sup>

$A_x$  = Wire area, (one conductor) cm<sup>2</sup>

$\Lambda$  = Required withstand area, V-sec

$\Delta B$  = Flux excursion, gauss

$K$  = Fill factor  $\approx 0.1$  to  $0.3$

3. Calculate number of turns from

$$N = \frac{\Lambda \cdot 10^8}{\Delta B A_e}$$

4. Estimate control current from

$$I_c \approx \frac{H \ell_e}{0.4 \pi N} \quad \text{where}$$

$\ell_e$  = core path length, cm

$H$  is taken from manufacturer's curves. Note that it increases with frequency.

5. Check the temperature rise by calculating the sum of the core loss and winding loss and using

$$\Delta T \approx \frac{P \text{ watts}}{A \text{ (surface) cm}^2}^{0.8} \times 444^\circ\text{C}$$

6. Once the mag amp is defined, it can be used in the power supply to verify  $I_c$  and to determine the modulator gain so that the control requirements may be determined.

### Compensating the Mag Amp Control Loop

The mag amp output regulator is a buck-derived topology, and behaves exactly the same way with a simple exception. Its transfer function contains a delay function which results in additional phase delay which is proportional to frequency. This phenomenon will be considered in more detail later.

Figure 11 shows the entire regulator circuit, with the modulator, filter, and amplifier blocks identified. The amplifier, with its lead-lag network, is composed of the op-amp plus R1, R2, R3, C1, C2, and C3. The modulator, for the purpose of this discussion, includes the mag amp core, the two rectifier diodes, plus the reset driver circuit which is composed of D1, Q1, and R7.

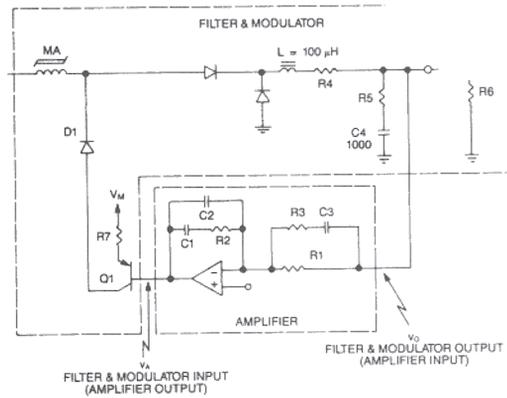


Figure 11. Schematic diagram of the regulator control loop.

The basic filter components are the output inductor (L) and filter capacitor (C4). R4 and R5 are the parasitic resistances of these components. The load resistor (R6) is also included, since it determines the damping of the filter.

The purpose of proper design of the control loop is to provide good regulation of the output voltage, not only from a dc standpoint, but in the transient case as well. This requires that the loop have adequate gain over as wide a bandwidth as practical, within reasonable economic constraints. These are the same objectives we find in all regulator designs, and the approach is also the same.

A straightforward method is to begin with the magnitude and phase response of the filter and modulator, usually by examining its Bode plot. Then we can choose a desired crossover frequency (the frequency at which the magnitude of the transfer function will cross unity gain), and design the amplifier network to provide adequate phase margin for stable operation.

Figure 12 shows a straight-line approximation of the filter response, ignoring parasitics. Note that the corner frequency is  $1 / (2 \pi \sqrt{LC})$ , or 316 Hz, and that the magnitude of the response “rolls off” at a slope of  $-40$  dB per decade above the corner frequency. Note also that the phase lag asymptotically approaches 180 degrees above the corner frequency.

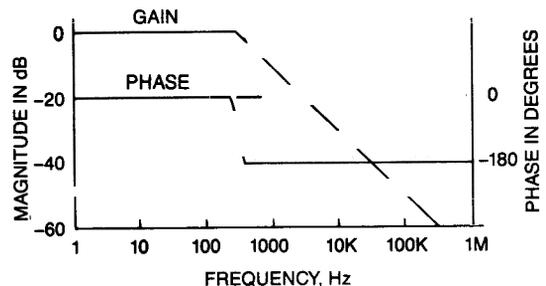
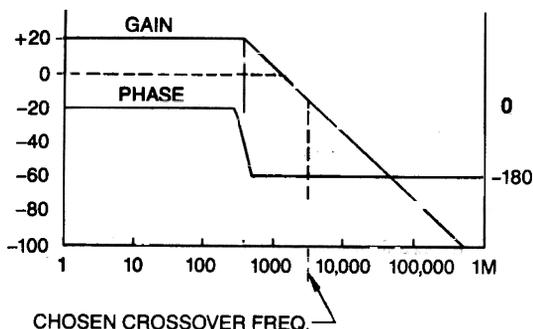


Figure 12. Output filter response.

Figure 13 shows the straight-line approximation of the combined response of the filter and modulator. With a modulator gain of 10, flat to frequencies well above the region of interest here, the magnitude plot has simply been shifted upward by 20 dB.

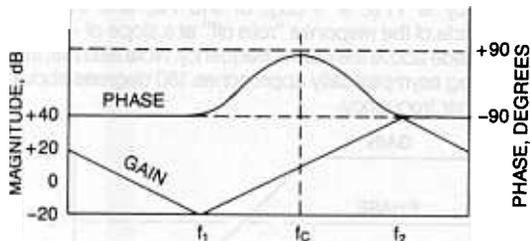


**Figure 13. Filter-modulator response.**

If we close the loop with an inverting error amplifier, introducing another 180 degrees of phase shift, and cross the unity gain axis above the corner frequency, we will have built an oscillator — unity gain and 360 degrees of phase shift.

An alternative, of course, is to close the loop in such a way as to cross the unity-gain axis at some frequency well below the corner frequency of the filter, before its phase lag has come into play. This is called “dominant pole” compensation. It will result in a stable system, but the transient response (the settling time after an abrupt change in the input or load) will be quite slow.

The amplifier network included in Figure 11 allows us to do a much better job, by adding a few inexpensive passive parts. It has the response shown in Figure 14. The phase shift is shown without the lag of 180 degrees inherent in the inversion. This is a legitimate simplification, provided that we use an overall lag of 180 degrees (not 360 degrees) as our criterion for loop oscillation.



**Figure 14. Amplifier response.**

The important point is that this circuit provides a phase “bump” — it can have nearly 90 degrees of phase boost at a chosen frequency, if we provide enough separation between the corner frequencies,  $f_1$  and  $f_2$ . This benefit is not free, however. As we ask for more boost (by increasing the separation between  $f_1$  and  $f_2$ ) we demand more gain-bandwidth of the amplifier.

### Additional Phase Shift of the Modulator

Using the usual time-averaging technique, we can justify the linear model of the filter and modulator. The modulator is represented by its dc gain,  $v_o/v_A$ , and a phase shift term which accounts for its time delay. This phase delay has two causes:

1. The output is produced after the reset is accomplished. We apply the reset during the “backswing” of the secondary voltage, and then the leading edge of the power pulse is delayed in accordance with the amount of reset which was applied.
2. The application of reset to the core is a function of the impedance of the reset circuit. In simple terms, the core has inductance during reset which, when combined with the impedance of the reset circuit, exhibits an L-R time constant. This contributes to a delay in the control function.

The sum of these two effects can be expressed as:

$$\phi_M = (2D + \alpha) \frac{\omega}{\omega_s}, \text{ where}$$

$\phi_M$  = Modulator phase shift

$D$  = Duty ratio of the “off” time

$\alpha$  = resetting impedance factor: = 0 for a current source, = 1 when resetting from a low-impedance source, and somewhere in between for an imperfect current source.

$\omega_s = 2\pi f_s$ , where  $f_s$  = the switching frequency.

When the unity-gain crossover frequency is placed at or above a significant fraction (10%) of the switching frequency, the resultant phase shift should not be neglected. Figure 15 illustrates this point. With  $\alpha = 0$ , we insert no phase delay which results from resetting from a voltage source (low impedance). The phase delay is minimized in the UC1838 by using a collector output to reset the mag amp.

The phase shift shown in Figure 15 is a result of both the impedance factor and duty ratio effects. In the case of resetting from a current source, the delay due to duty ratio is the more significant.

It is difficult to include this delay function in the transfer function of the filter and modulator. A simple way to handle the problem is to calculate the Bode plot of the filter/modulator transfer function without the delay function, and then modify the phase plot according to the modulator’s phase shift.

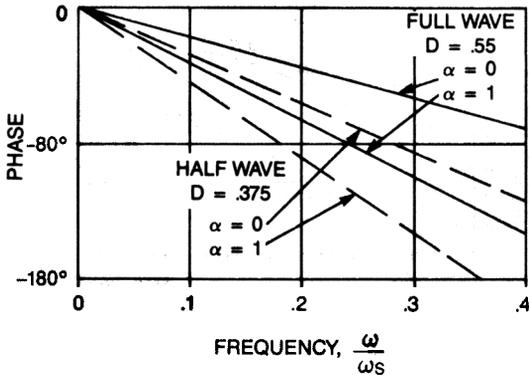


Figure 15. Mag-amp phase shift.

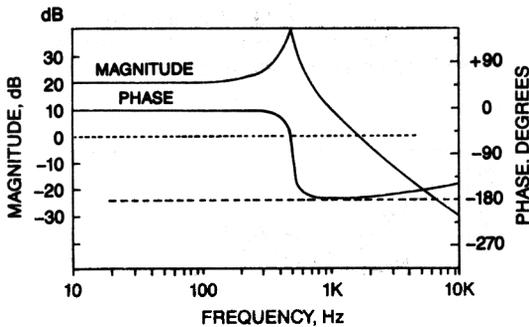


Figure 16. Filter-modulator response neglecting modulator phase shift.

### Design Example

As an example, consider a 10 V, 10 A output to be regulated with a mag amp. Assume that the output inductor has been chosen to be 100  $\mu$ H, and that the output capacitor is 1000  $\mu$ F. Each has .01 ohms of parasitic resistance, and the load resistor is 1 ohm.

We begin by plotting the response of the filter/modulator. In order to do this, we must determine the dc gain of the modulator. This can be done experimentally by applying a variable voltage,  $V_A$  to the base of Q1, adjusting it to set the output,  $V_O$ , to 10 V and then making a small change around the nominal value to determine the incremental gain. Assume that a 0.1 V change in  $V_A$  results in a 1 V change in the output; this gives a gain of 10. For a first look, the phase delay of the modulator is set at zero by choosing  $\alpha = 0$  and  $D = 0$ . The result is the plot of Figure 16. Note that the crossover frequency is approx. 1.6 KHz, at which the phase margin is only about 15 degrees.

Figure 17 illustrates the effect of phase shift, by setting  $\alpha = .2$  and  $D = .6$ . Note that the crossover frequency is unchanged, but that the phase margin is now approximately zero. The loop can be expected to oscillate.

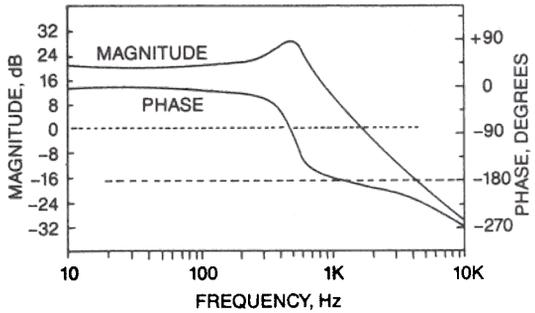


Figure 17. Filter-modulator response, with modulator's phase shift.

Dean Venable, in his paper, "The K Factor: A New Mathematical Tool for Stability Analysis and Synthesis," has derived a simple procedure for designing the amplifier network. In summary, the procedure is as follows:

1. *Make a Bode Plot of the Modulator.* This can be done with the use of a frequency response analyzer, or it can be calculated and plotted, either with the use of a simple straight-line approximation or with the use of one of the available computer analysis programs. Don't forget to include the effect of the filter capacitor's ESR (equivalent series resistance), using its minimum value, since this presents the worst case for loop stability. Also, include the modulator's phase shift.
2. *Choose a Crossover Frequency.* The objective, of course, is to make this as high as possible for best (fastest) transient response. The limiting condition on this choice is as follows: The amplifier can provide, as a theoretical maximum, 90 degrees of phase boost, or — stated another way — 180 degrees of boost from its inherent 90 degrees of phase lag. We will work with this latter convention, and assign it the symbol  $B_C$ , the boost at the crossover frequency. The required  $B_C$ , then is:

$$B_C = M - P - 90, \text{ where}$$

$M$  = Desired Phase Margin, and

$P$  = Filter & Modulator Phase Shift.

Examining this relationship, we can see that the Desired Phase Margin is  $M = B_C + P + 90$ ,

and hence if the filter-modulator phase shift is 180 degrees, the theoretical limit of phase margin is 90 degrees. Since an acceptable minimum phase margin for reasonable transient response is around 60 degrees, we deduce that we must choose a corner frequency below that at which the filter and modulator phase lag is:

$$P = M - B_C - 90, \text{ or } P = 60 - 180 - 90 = -210$$

To accomplish this we would have to separate the amplifier's two corner frequencies by infinity. A more practical case is to choose -190 degrees as a limit — maybe even less, since separating these frequencies (for more phase boost) may require an impractical amount of gain-bandwidth in the amplifier.

With this guideline in mind, we establish the criterion that:  
 $P > -190$  degrees.

Combining this with the earlier criterion of not trying to cross over at a frequency greater than one-tenth the switching frequency, we have:

$$f_c = .1 f_s,$$

— or —

$f_c$  = the frequency where the filter-modulator's phase shift has fallen to  $-190$  degrees.

Choose the result which yields the lower crossover frequency.

It is a coincidence in this design example that the filter-modulator phase shift is  $-190$  degrees at approximately 2 KHz, one-tenth the switching frequency. In this case, the choice of the crossover frequency is unanimous!

Dean Venable's "K Factor" is the ratio between the two corner frequencies,  $f_1$  and  $f_2$ :

$$K = f_2 / f_1$$

and, the two frequencies are centered geometrically about the crossover frequency. Therefore,  $f_1 = f_c / \sqrt{K}$ , and  $f_2 = f_c \sqrt{K}$ .

In this design example, we have chosen 2 KHz as our crossover frequency, where the modulator's phase lag is  $-190$  degrees, and wish to have 60 degrees of phase margin. The result is:

$$B_c = 60 - (-190) - 90 = 160 \text{ degrees}$$

3. **Determine the Required Amplifier Gain.** This one is simple! The amplifier must make up the loss of the filter and modulator at the chosen crossover frequency. In this example, the filter and modulator has approximately  $-3$  dB at the crossover frequency of 2 KHz, and hence the amplifier must have a gain of 1.41 (+3 dB) at 2 KHz.

With this information now at hand, we're ready to crank out the values of the amplifier components, as explained in Mr. Venable's paper:

$$K = (\tan [(B_c/4) + 45])^2$$

$$C_2 = 1 / (2 \pi f G R_1)$$

$$C_1 = C_2 (K - 1)$$

$$R_2 = \sqrt{K} / (2 \pi f C_1)$$

$$R_3 = R_1 / (K - 1)$$

$$C_3 = 1 / (2 \pi f \sqrt{K} R_3)$$

where  $f$  = crossover freq. in Hz, and  $G$  = amplifier gain at crossover (expressed as a ratio, not dB)

Figure 18 shows the response of this amplifier over the frequency range of interest.

Incidentally, the value for  $K$  is 130.65, and the corner frequencies are 175 Hz and 22,860 Hz.

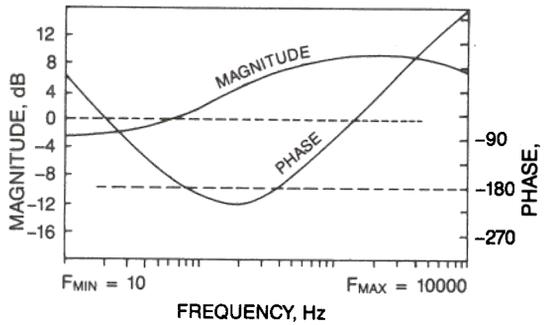


Figure 18. Compensated error amplifier response.

Combining the amplifier's response with the filter and modulator response results in the overall loop response, and this is shown in Figure 19. Note that the crossover frequency is 2 KHz, and that the phase shift is  $-120$  degrees (60 degrees of phase margin).

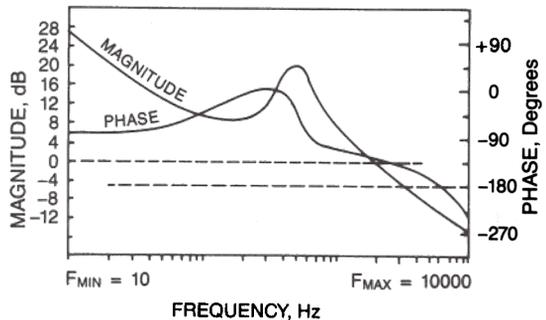


Figure 19. Overall regulator loop response.

### Check the Gain-Bandwidth Requirement for the Amplifier

To avoid disappointment, it is wise to check to see that the design does not require more gain-bandwidth than the amplifier can provide. This is fairly easy to do. We can simply calculate the gain-bandwidth product at  $f_2$ , since above this frequency the amplifier can be expected to be rolling off at the same  $-20$  dB/decade slope. The gain at  $f_2$  is:

$$G_{f_2} = \sqrt{K} G, \text{ and hence the required gain-bandwidth is:}$$

$$GBW = \sqrt{K} G f_2 = K G f \text{ since } f_2 = \sqrt{K} f$$

In this example the result is 368 KHz, well below the gain-bandwidth of the amplifier in the UC1838. If it had not been so, we would have had two choices: We could settle for a lower crossover frequency or less phase margin (not recommended), or add another amplifier in cascade with the one in the UC1838. The added amplifier would simply be designed as a non-inverting amplifier with modest gain and placed after the output of the existing amplifier. We might also examine the possibility of increasing the gain of the modulator by increasing the number of turns on the mag amp.

### Full-Wave Mag Amp Outputs

Although the examples thus far have explored the forward converter (a half-wave topology), mag amp output regulators also work well with half-bridge and full bridge converters (full-wave topologies). Two saturable reactors are required, as shown in Figure 20. Since the output current is shared by the two reactors, the cores can be smaller than the single core of a half-wave topology of the same power level.

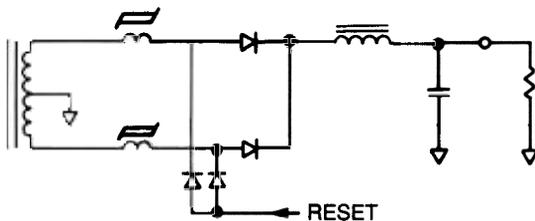


Figure 20. Full-wave output regulator.

### Converters with Multiple Mag Amp Outputs

There is no limit to the number of outputs which can be employed on a single converter, or even from a single secondary winding of the transformer. Recall, however, that the mag amp regulator is like a conventional buck regulator and can only provide voltages which are lower than that which would occur if the mag amp were not present.

Loop stability does not become complicated by the addition of more output regulators. The task is simply to stabilize each of the regulator control loops in the normal fashion.

### Interaction of the Mag Amp Loop with the Main Converter Control Loop

There are no surprises here. The output regulator behaves like a second converter (buck regulator) cascaded with the main converter. If both are stable when considered individually, they will not upset each other.

When considering the two circuits as a cascade, it is reasonable that if the output regulator responds quickly to a load transient, this perturbation will be presented to the main converter. The main loop will then deal with this if it senses the effect at the sensing point.

### Interaction with the Converter's Input Filter

Assuming the absence of current-mode control of the main converter, the only significant interaction of the mag amp outputs will be with the input filter. But this is not a problem if the filter is properly damped in accordance with the negative resistance presented by the input of the converter. A simple way to ensure stability is to determine the maximum-load negative input resistance of the converter at low frequency (the ratio of the change in input power to a small change in input voltages, squared), then damp the input filter so that the magnitude of its output impedance is always below this value.

### Continuous vs. Discontinuous Conduction of the Output Inductor

It is possible to operate the mag amp regulator with its output choke in the discontinuous mode, provided that the mag amp's winding is designed to reduce the pulse width accordingly. When this is done, the mag amp can reduce the pulse width to maintain output regulation even when the load current falls below the "critical" current of the output inductor. Transient response is affected just as it is in a simple buck regulator; it becomes poorer as the corner frequency falls.

### References

1. Mullett, Charles, "Design and Analysis of High Frequency Saturable-Core Magnetic Regulators," Powercon II, April 1984.
2. Venable, H. Dean, "The K Factor: A New Mathematical Tool for Stability Analysis and Synthesis," Proceeding of Powercon 10, March 1983.
3. Unitrode IC Corp. acknowledges and appreciates the support and guidance given by the Power Systems Group of the NCR Corporation, Lake Mary, Fla. in the development of the UC1838.

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