An Analytical Comparison of Alternative Control Techniques for Powering Next-Generation Microprocessors

By Rais Miftakhutdinov

ABSTRACT

The latest microprocessor roadmaps show not only ever-increasing performance and speed, but also the demand for higher currents with faster slew rates while maintaining tighter supply-voltage tolerances. This topic addresses these challenges by reviewing and comparing various control approaches for single- and multi-phase synchronous buck converters. An optimized hysteretic control algorithm is shown offering a significantly improved transient response, which is illustrated with a specific design example.

I. INTRODUCTION

An unprecedented push in semiconductor technology, especially microprocessors, set the new level of requirements for OEMs [1]. By the year 2005, 3.5-GHz processors having over 190 million transistors on chip will consume more then 160 W. The new 0.1-μM technology will drop the core-voltage of high-performance processors down to 1.2-V range, requiring up to 130-A current from the voltage regulator. Developing an efficient, low-cost power-delivery system for that type of load is one of the major problems to be solved.

Another problem relates to the high slew-rate current transients, exceeding 40,000 A/μs through the die when a processor abruptly changes its operation state. Obviously, special packaging, high-frequency decoupling, and a fast transient-response regulator must be used to keep the core-voltage tolerance within the required few percent.

Additionally, the latest mobile processors have implemented special power-saving technique called SpeedStep™, PowerNow™, and LongRun™ [15-17] trying to prolong battery life. In accordance to this technology, the microprocessor has different modes of operation; i.e., "performance," "battery" and "automatic." The idea is to decrease the clock frequency and core voltage at the battery mode, while keeping frequency and voltage higher at performance mode. In the automatic mode the processor continuously adjusts the clock frequency and voltage according to system demand. That means the microprocessor voltage regulator must be able to quickly change the output voltage on the basis of the control signals from the system or microprocessor.

The other power saving technique called "Intel Mobile Voltage Positioning" or IMVP, uses the droop-compensation approach usually associated with the extending of transient window. It also requires the negative core-voltage offset for some sleep-mode stages of the microprocessor [18]. This approach extends the battery life, because power dissipation of the microprocessor is inversely proportional to core voltage square. These new requirements must be counted during power-delivery system design.

A controller IC is a significant part of the microprocessor power supply: it integrates the described power-saving functions. Still, the main goal of controller is to provide an accurate output voltage at steady-state conditions and fastest response with minimum voltage tolerance at high slew-rate transients. The topic of this article explains the control-approach influence on transient and optimal power-delivery system design.

Review of available literature shows that usually the authors provide rule-of-thumb recommendations for selecting different components on the basis of transient parameters [5-7,13]. This topic discusses the transient in a power-delivery system as a whole, thereby suggesting more accurate design procedure. It includes the model selection, the derivation of transient equations in the time domain, the observation of transient waveforms, and the effect of different system parameters, including parasitics and controller characteristics. This approach defines the worst condition of transient, which is determined by the moment within the switching cycle in which the transient occurs. This condition is not described in the literature, although it influences component selection. This topic addresses the popular synchronous buck converter and the multi-phase (interleaved) topology based on it. The equations for a required number of output bulk capacitors are derived and an optimization procedure for the output filter design is suggested both for one- and multi-phase topologies.

The next section of the topic reviews and compares different control approaches most suitable for microprocessor power supplies. On the basis of the previous transient analysis, it first formulates a control algorithm for the best transient response. The next step explains how the limitations of actual controllers (such as delays, fixed on- or off-time, compensation bandwidth, and error-amplifier saturation) that might degrade the transient response. A review and comparison of control techniques shows that a hysteretic regulator is one of the most appropriate solutions for powering microprocessor-type loads having high slew-rate and amplitude transients.

A hysteretic controller and its modifications are described in the next section. Although a hysteretic regulator has been used in power electronics for a long time [28], earlier publications do not address modern applications and conditions. This analysis includes new equations for the switching-frequency calculation, both for the typical hysteretic control and for its modifications [26,30,33,34,40,42]. Finally, a design example and the optimization procedure are provided to implement the analysis results and to address important practical issues.

II. Transient Analysis

A. Power Distribution Model

The model selection for an analysis is always a tradeoff between practicality and accuracy of the results. Fig. 1 shows the power distribution system considered in the analysis.

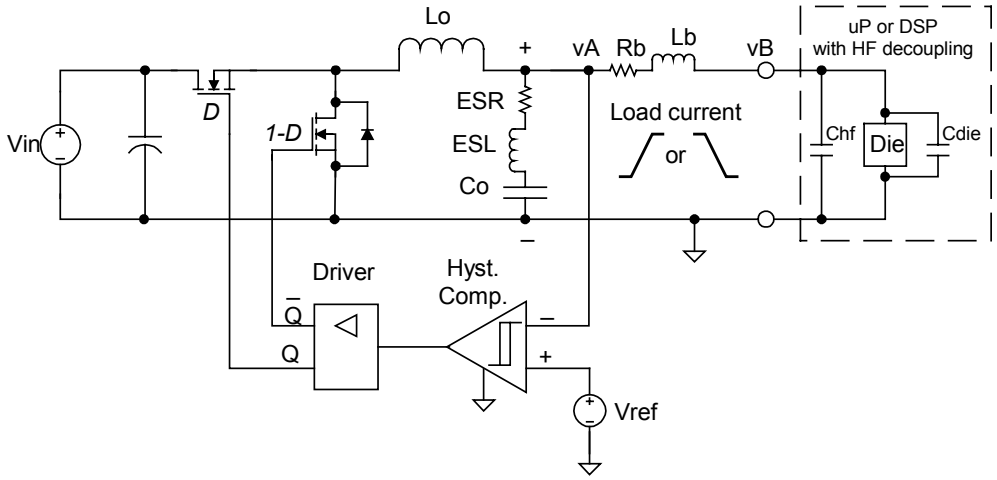


Fig. 1. Analyzed power-delivery system at load-current transients.

The model includes the synchronous buck converter, the output inductor L_O, the output bulk capacitor with parasitics, and the power supply traces between the bulk capacitor and the package or cartridge of the microprocessors. The output bulk capacitor is presented as a series connection of an equivalent ideal capacitor C_O, with equivalent series resistance ESR and equivalent series inductance ESL. The equivalent resistor R_B characterizes the resistive voltage drop through the supply paths and is the summarized resistance of the traces and the connectors. The equivalent inductor L_B characterizes the inductive voltage drop across the traces and connectors. The high-frequency decoupling capacitors on the die C_{DIE} and inside the package C_{Hf} are not included in the analysis, because usually the load-current slew-rate is specified at the package pins. Nevertheless, in situations when L_B and ESL are too high, it is important to decrease the slew-rate of current through the bulk capacitor C_O by adding the high-frequency decoupling capacitors around the package. This procedure is also described in the transient analysis section.The analyzed model is the lumped one, while in an actual power-delivery system the output capacitors and parasitics are distributed over the PCB board area. But results of the analysis using this model are confirmed by the measurements and sufficiently accurate for most applications. The same model of the power-delivery system is suggested in Intel's Power Distribution Guidelines [5-7]. The controller and the drive circuitry are assumed not to have any delays. They are able to maintain the on- or off-state of the related power switch during the transients as long as necessary to return the output voltage back to the steady-state level as soon as possible. In this case, the controller does not degrade the transient response, which is determined by passive components only. The hysteretic controller in Fig.1 includes the comparator with a hysteresis window, the reference voltage, and the drive circuitry with a complementary control of high- and low-side FETs. Fig. 1 is an example only, but it will be shown later that it is a good approximation of the ideal controller.

B. Analysis Approach

There are many publications where dc-to-dc buck converters for powering microprocessor are considered at load-current transients [19-24,26,30-34,37,40,42,44-46].

Computer simulation is one of the popular technique for the transient analysis [20]. It is a useful tool for design validation, but it does not reveal analytical relations among the parameters of a power-delivery system. Therefore, it is difficult to predict and find the optimal solution.

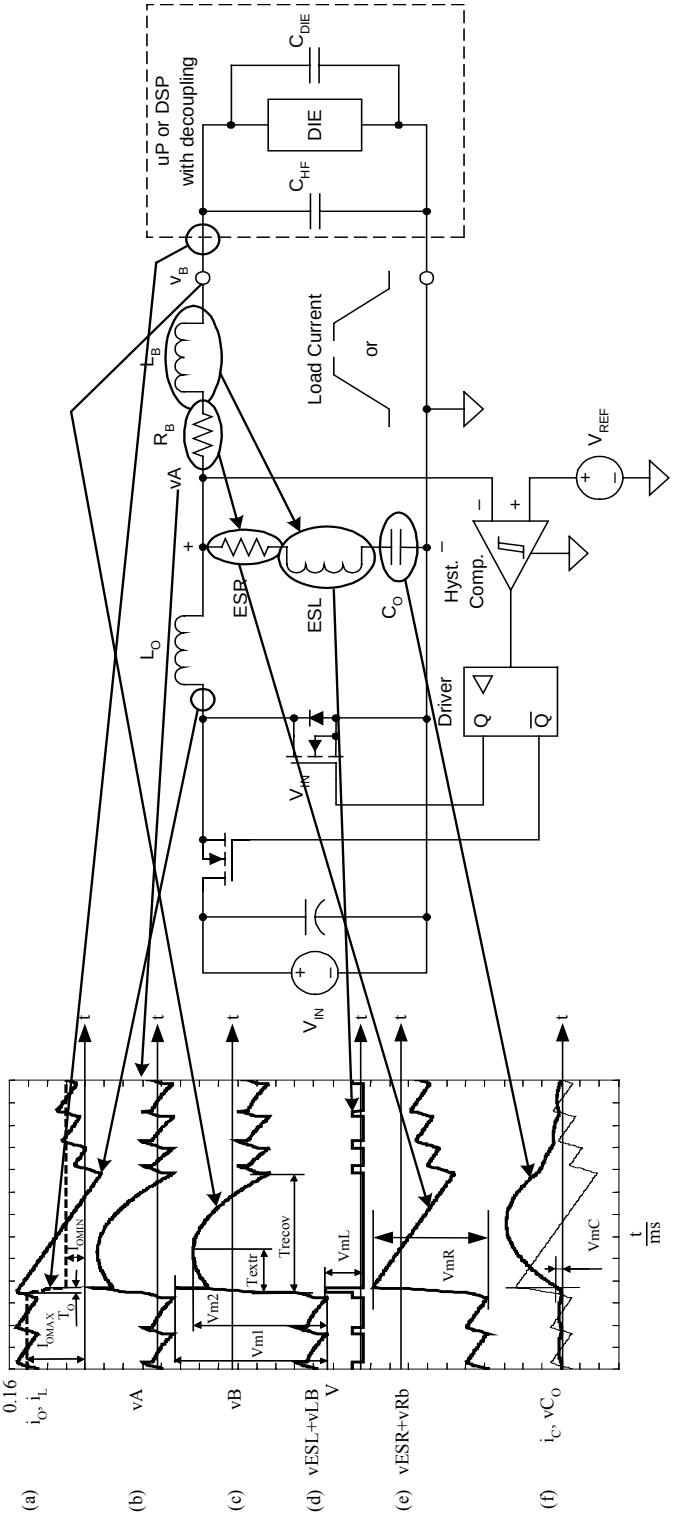
Small-signal analysis is another technique [21,22]. Some authors optimize the small-signal frequency characteristics—for example the output impedance [22]. However, this practice is questionable, because it applies the small-signal analysis to the large-signal transient process. This topic shows that small-signal analysis cannot explain the dependence of transient upon the moment within a switching cycle when it occurs.

Assuming that a load-current transient is a linear function of time, the equations are derived for the voltages and currents of all components of power-delivery system as a function of time before, during, and after the load-current transient. These equations are included in a MATHCAD-based software program to view the transient voltage and current waveforms. The same equations also characterize peak values of the transient. On the basis of these equations, the curves for selecting the optimal output filter and the minimum number of bulk capacitors selection are built [26,30,33,34,40,42].

C. Transient Waveforms and Experimental Verification

Fig. 2 shows the waveforms across the different elements of the model (Fig. 1) at the load-current step-down.

The output current changes between $I_{O(max)}$ and $I_{O(min)}$ (Fig. 2a) with a constant slew-rate. The step-up transient waveforms have the same stages and are qualitatively similar to a step-down, although they are described by different equations.



(a) Load-current and output inductor current transient waveforms.

(b) Transient-voltage waveform on the output of the dc-dc converter (point A in Fig. 1).

(c) Transient-voltage waveform on the microprocessor package pins (point B in Fig. 1).

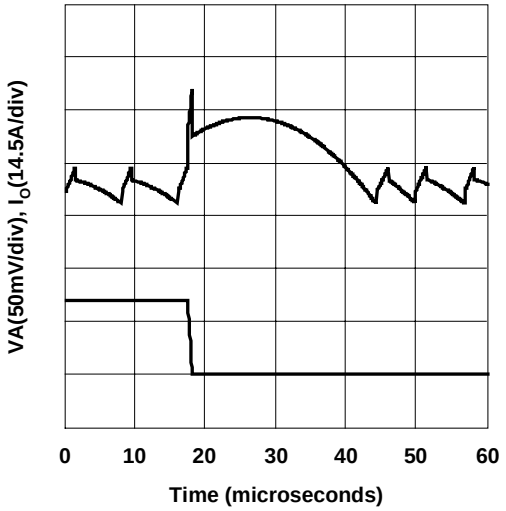
(d) Transient-voltage waveform at the inductive components of the model ESL and L_B.

(e) Transient-voltage waveform at the resistive components of the model ESR and R_B.

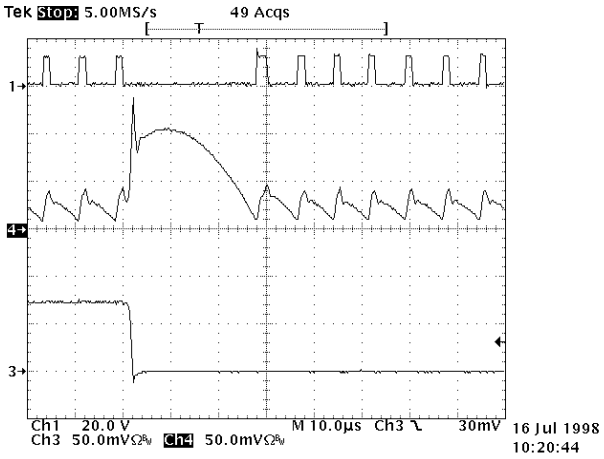
(f) Transient-voltage waveform and current on the-capacitor C_O.

Fig. 2. Waveforms through different elements of the model during load-current step-down transition.

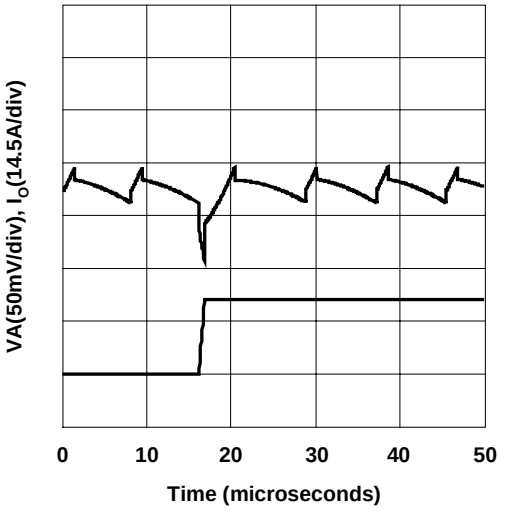
To verify the derived equations, the MATHCAD transient waveforms are compared with the measured ones under the same conditions. As shown in Fig. 3, the theoretical and measured waveforms are very close for the load-current step-down and step-up conditions. The comparison of analyzed waveforms, based on an ideal controller without delays, and measured waveforms, with the switching regulator based on the hysteretic controller TPS5210, shows that the hysteretic control, despite typical 250 ns delays does not degrade the transient characteristics significantly.



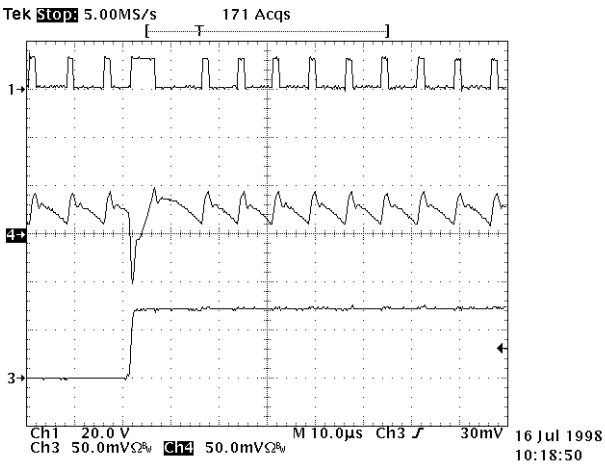
(a) Theory



(b) Measurement



(c) Theory



(d) Measurement

Fig. 3. Theoretical (a), (c) and measured (b), (d) waveforms at load-current step-down (a), (b) and step-up (c), (d)transitions. [The theoretical waveforms show the output voltage (top) and load-current (bottom) transients.The measured waveforms include V_{DS} voltage of the low-side FET (Ch1: 20V/div), output voltage (Ch4: 50mV/div) and load current (Ch3: 14.5A/div)].

D. The Two Extreme Values of a Transient

Fig. 4 shows typical load-current transient waveforms. The output-voltage waveform has two extreme values, V_M1 and V_M2.

For most applications the transient slew rate of the load current is much higher than the slew rate of the output-inductor current. Therefore, the first peak, V_M1, depends mainly on the parasitics of the output capacitor and supply path. The controller transient-response characteristics (Fig.5a) do not affect it significantly. The second peak, V_M2, depends on the resistive components ESR and R_B, the capacitive component C_O, the inductor value L_O and the converter characteristics, including the switching frequency and the type of control (Fig.5b).

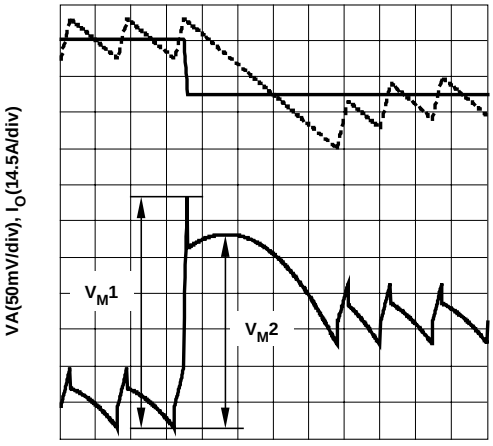
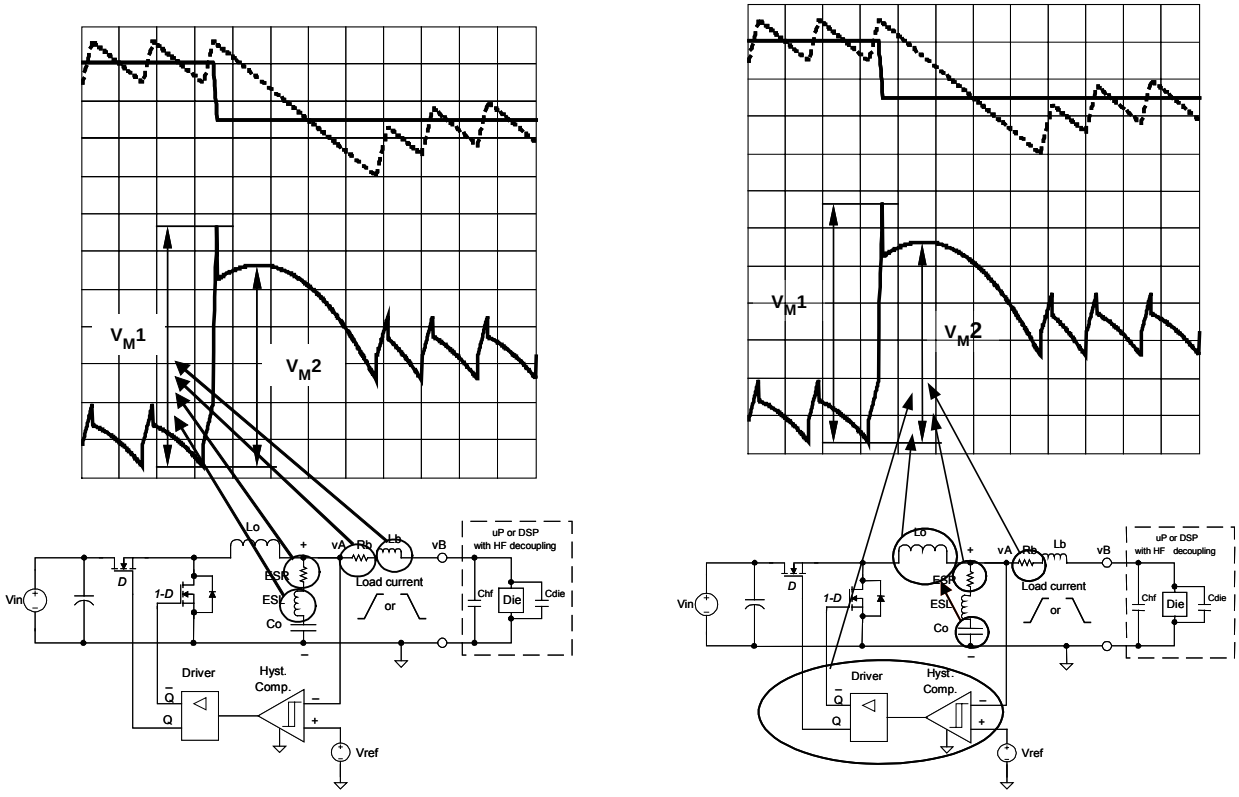


Fig. 4. Typical load-current transient waveforms.



(a) (b)

Fig. 5. Different parameters and their effect on peaks V_M1 and V_M2.

III. Impact of System Parameters on a Transient

A. Output Inductor Value

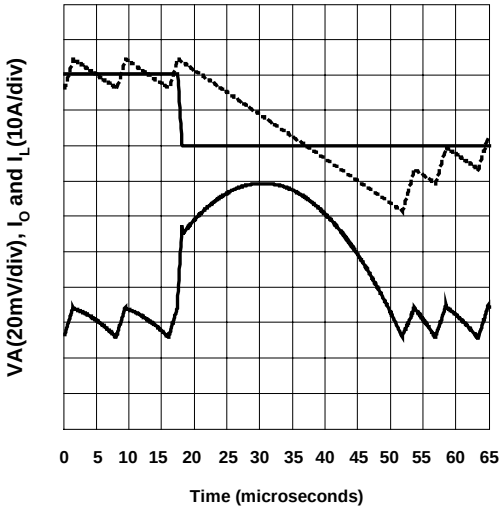
It could be thought, that the lower output inductor value enables better transient-response characteristics because of a faster inductor-current change to the new level after the load-current transient occurs.

In reality, the example in Fig. 6 shows that, after some optimal value (Fig. 6b), further decreasing of the inductor value increases the peak-to-peak transient amplitude because the output ripple rises significantly. As shown later, the optimal inductor value depends on the switching frequency and the characteristics of the output bulk capacitors.

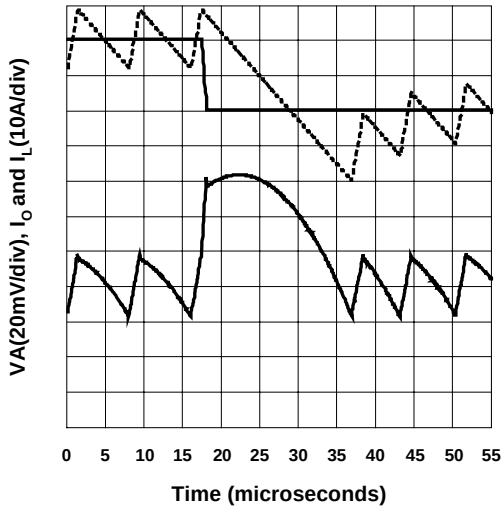
B. Dependence on Switching Cycle Position

The output-voltage transient response depends on where the load-current transient occurs within the switching cycle. If the load current steps down, the excessive energy stored in an output inductor is delivered to the output capacitor. The worst case for the step-down transition occurs if the transient takes place at the end of a conduction time of high-side FET, because the inductor current is at its maximum. At that moment the inductor stores the maximum energy, while the output ripple voltage also is at its maximum. So the effect of transient is most significant at that moment, causing greater output voltage spikes than at any other moment (Fig. 7).

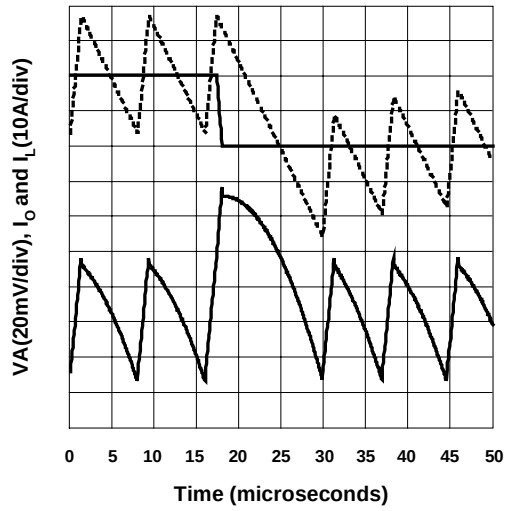
In contrast, the worst case for the step-up transition occurs if the transient happens at the end of the switching cycle, because the inductor current and output voltage ripple are at their minimum at that moment. Only the output capacitor supplies the load during the step-up transient, while the inductor must restore its energy and current to the new load-current level. This fact cannot be described with small-signal analysis, although the effect must be considered for reliable output filter selection.



(a) L_O = 1.6 µH $V_{O(max)}$ = 79 mV T_{RECOV} = 34 µs

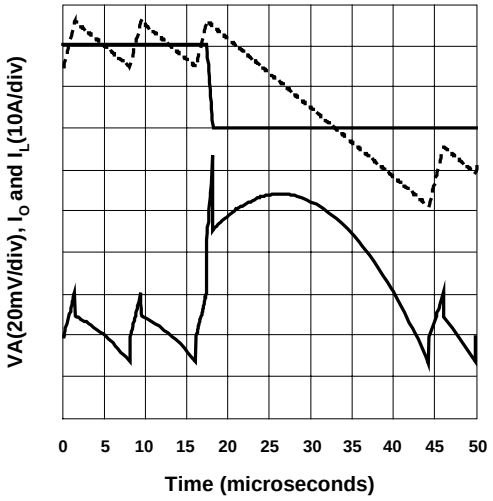


(b) L_O = 0.8 µH $V_{O(max)}$ = 62 mV T_{RECOV} = 19 µs

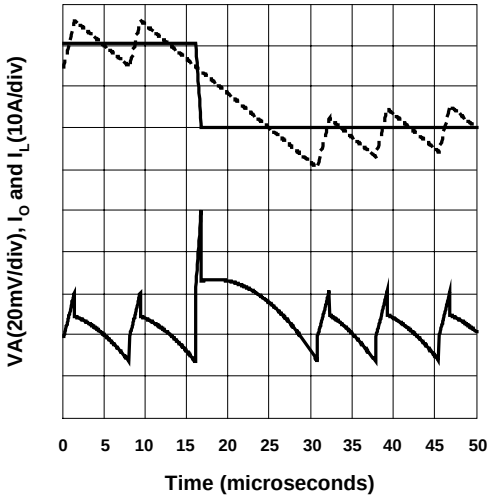


(c) L_O = 0.4 µH $V_{O(max)}$ = 72 mV T_{RECOV} = 12.5 µs

Fig. 6. Transient waveforms for different inductor values L_O.



(a) Worst case: Transient occurs at the end of the upper FETs conduction time.



(b) Best case: Transient occurs at the end of the switching cycle.

Fig. 7. Output voltage (bottom curve) and inductor current (dashed) waveforms for the different instants when the load-current (top, solid) step-down transition occurs.

IV. Equations for the Required Number of Capacitors

The peak values V_M1 and V_M2 for the worst-case step-down and step-up transients can be found with the derived equations. (See Appendix 1.) Assume that the output filter capacitors are connected in parallel and that each capacitor has the characteristics C_O1, ESR1 and ESL1. The number 1 after a parameter means that the parameter relates to one of many capacitors connected in parallel. The literature shows [33,34,42] that if ΔV_{REQ} is the maximum allowable peak-to-peak transient tolerance, then the required number of output bulk capacitors N1 and N2, to meet the conditions $V_M1 = \Delta V_{REQ}$ and $V_M2 = \Delta V_{REQ}$, respectively, can be found by equations (1) and (2):

where $KL = \Delta IL_{EQV}/\Delta I_O$ (3)

or

$$KL = \frac{V_{OUT} \cdot (1 - D \cdot n)}{L_{OEQV} \cdot \Delta I_O \cdot f_S \cdot n} \quad (4)$$

The parameter m depends on the type of transient. It is equal to:

$$m = 1 - n \cdot D \quad (5)$$

for the worst-case step-down transient and to:

$$m = \frac{D \cdot (1 - n \cdot D)}{n \cdot (1 - D)} \quad (6)$$

$$N1 = \frac{\frac{ESR1}{T_O} + ESR1 + \frac{T_O}{2C_O1} + \left(ESR1 + \frac{T_O}{2 \cdot C_O1}\right) \cdot \left(1 - \frac{T_O \cdot f_S \cdot n}{m}\right) \cdot KL}{\frac{\Delta V_{REQ}}{\Delta I_O} - \frac{L_B}{T_O} - R_B} \quad (1)$$

$$N2 = \frac{\frac{1}{2}\left[\frac{m}{C_O1 \cdot f_S \cdot n} - \frac{T_O}{C_O1} + \left(ESR1 + \frac{ESR1^2 \cdot C_O1 \cdot f_S \cdot n}{m} + \frac{m}{4 \cdot C_O1 \cdot f_S \cdot n}\right) \cdot KL + \frac{m}{C_O1 \cdot f_S \cdot N} \cdot \frac{1}{KL}\right]}{\frac{\Delta V_{REQ}}{\Delta I_O} - R_B} \quad (2)$$

for the worst-case step-up transient. The ΔIL_{EQV} is the peak-to-peak ripple portion of the output inductor current, Δ_{IO} is the load-current step, $D = V_{OUT}/V_{IN}$ is the duty cycle, $f_S = 1/T_S$ is the switching frequency, and T_S is the switching cycle. The number of channels in an interleaved (multi-phase) regulator is n. For the one-channel converter *n* = 1. Later discussion shows that, with some assumptions, the same transient analysis applies to the one- and multi-channel interleaved converters.

The second peak V_M2 exists only if the following condition is fulfilled:

$$\frac{m}{f_S \cdot n} \cdot \left(\frac{1}{KL} + \frac{1}{2} \right) - ESR \cdot C_O > T_O \qquad (7)$$

where T_O is the load-current transition time. If this condition is not fulfilled, only the first spike and Equation 1 must be considered. The other assumption of the analysis is that $T_O < D \cdot T_S$. This assumption does not restrict the analysis for most applications. Equations 1 and 2 can be used for the optimal output-filter design based on the optimization curves N1 = N1(f_S, $L_{O(eqv)}$, n) and N2 = N2(f_S, $L_{O(eqv)}$, n). But first, let us consider some simple but useful relations from these equations.

A. Influence of Supply-Path Parasitics

The voltage-transient waveforms on the converter output pins (point vA in Fig.1) and on the microprocessor package supply pins (point vB in Fig.1) are different because the supply-path resistance R_B and inductance L_B cause an additional voltage drop. If the output current step ΔI_O and slew-rate vI are defined as:

$$\Delta I_O = I_{O(max)} - I_{O(min)} \qquad (8)$$

$$vI_O = \frac{\Delta I_O}{T_O} \qquad (9)$$

then the additional voltage drop V_B of the supply paths is:

$$V_B = VR_B + VL_B = \Delta I_O \cdot R_B + vI_O \cdot L_B \qquad (10)$$

Assume that R_B = 1.5 mΩ; L_B = 1.0 nH; ΔI_O = 23.8 A; vI_O = 20 A/μs and $T_O = \Delta I_O/vI_O$ = 1.2 μs in accordance with the VRM 8.4 requirements [10]. Then the voltage drop through the supply path is:

$$V_B = 35.7 \text{ mV} + 20 \text{ mV} = 55.7 \text{ mV} \qquad (11)$$

For the 1.65-V output power supply, the voltage drop is almost 3.8%. This example shows why it is important to keep the output filter capacitors as close as possible to the microprocessor package to avoid a significant voltage drop due to supply path parasitics.

Let us consider the other example. The expression:

$$\left(\frac{\Delta V_{REQ}}{\Delta I_O} \right) - \left(\frac{L_B 1}{T_O} \right) - R_B 1$$

is the denominator of the Equation 1.

Obviously, the minimum number of bulk capacitors N1 can be calculated only if the following inequality is met:

$$\frac{\Delta V_{REQ}}{\Delta I_O} > \frac{L_B 1}{T_O} + R_B 1$$

Assume that ΔV_C = 96 mV for the previous example.

In this case $\Delta V_{REQ} / \Delta I_O$ = 4 mΩ. This is an important transient characteristic, let's call it Equivalent Transient Resistance (ETR). L_B/T_O = 0.84 mΩ. That means that the supply path parasitics L_B and R_B give us 4 mΩ/(4 – 0.84 – 1.5) mΩ. = 4/1.66 = 2.4 times number of capacitors increase.

B. Bulk Capacitor Parameters

The expression $\frac{ESL}{To} + ESR + \frac{To}{2 \cdot Co}$ is part of the numerator of the Equation 1 for N1. It characterizes the selected capacitor characteristics. For example, the aluminum electrolytic capacitor 6.3ZA1000 from Rubycon has ESL = 4.8 nH, ESR = 24 mΩ and C_O = 1000 μF. That gives us 4.8 nH/1.2 μs +24 mΩ +1.2 μs /(2•1000 μF) = (4+24+0.6) mΩ = 28.6 mΩ. After substituting 1.66 mΩ for denominator from the previous example: 28.6 mΩ /1.66 mΩ = 17.2

Roughly at least 17 capacitors must be used to meet the requirements. It will be shown later how this number can be reduced by additional high-frequency decoupling.

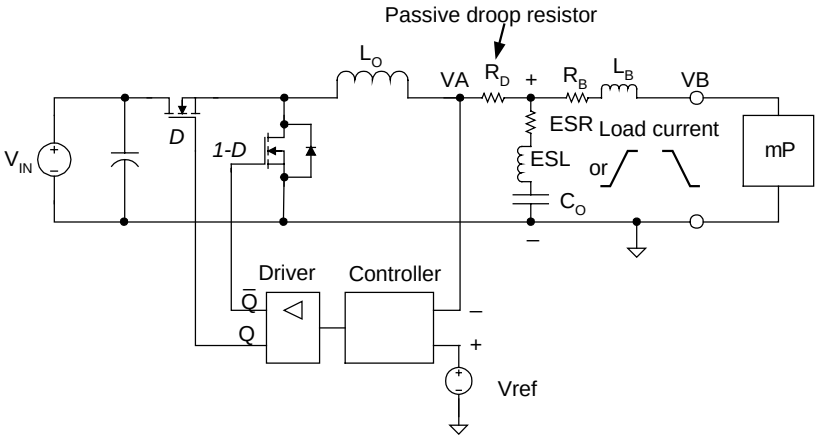
C. Active and Passive Droop Compensation

Equations 1 and 2 show that increasing ΔV_{REQ} can lower the required number of bulk capacitors. The droop compensation is an effective technique to increase ΔV_{REQ}. Droop compensation means that the dc output voltage of the converter is dependent on the load. It is set to the highest level within the specification window at no-load condition and to the lowest level at full-load. This approach degrades the static load regulation but increases the output-voltage dynamic tolerance by as much as twofold, thus reducing the number of bulk capacitors required. For the same output filter, this technique allows a decrease in peak-to-peak output-voltage transient response. Fig. 31 in the design-example section shows the output voltage budget with droop compensation.

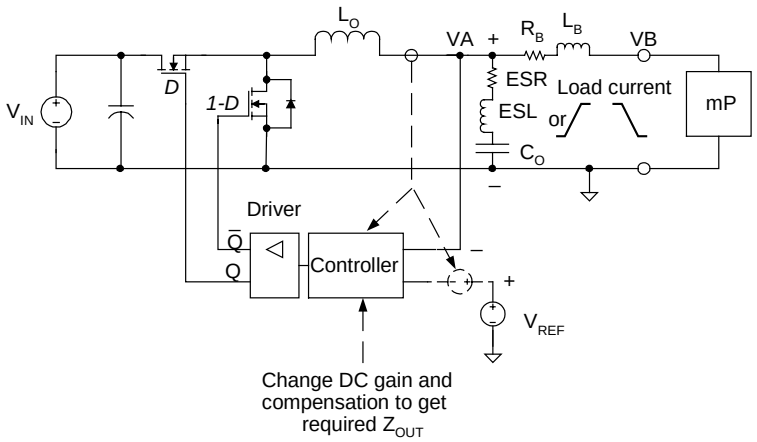
The popularity of droop compensation is confirmed by the fact that it has numerous names such as "Programmable Active Droop™," "Active Voltage Positioning," "Adaptive Voltage Positioning," "Summing-Mode Control," "Intel Mobile Voltage Positioning (IMVP)," etc.

There are two different approaches for a practical implementation of this idea. Fig. 9a shows the simplest way called "passive" droop compensation. The droop resistor R_D = ESR is inserted between the output capacitor and the output voltage sense point V_A. Passive droop is fast and naturally follows the load-current transient. This approach can be used probably with any type of control technique. The drawback is that it requires the additional resistor with power losses in it. The other approach, called "active" droop compensation, is shown in Fig. 9b. It can be implemented by adding an offset proportional to the output current, which is subtracted from the reference voltage, or by changing the dc gain and the compensation circuitry to get a desirable output impedance Z_{OUT} [22,37]. The main challenge here is that it must be accurate and fast enough to follow the transients having their own repetition frequency up to 100 kHz [8-11].

The transient waveforms with and without active droop compensation are shown in Fig. 10. One can see that without droop compensation (Fig. 10a) the output-voltage peak-to-peak amplitude is 146 mV and it exceeds the requirements, as shown by the cursors. With droop compensation (Fig. 10b), the peak-to-peak transient is only 78 mV, keeping the output voltage of the same regulator well within the requirements.

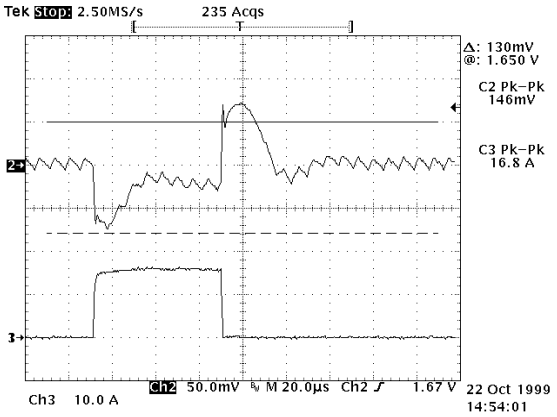


(a) Passive droop compensation

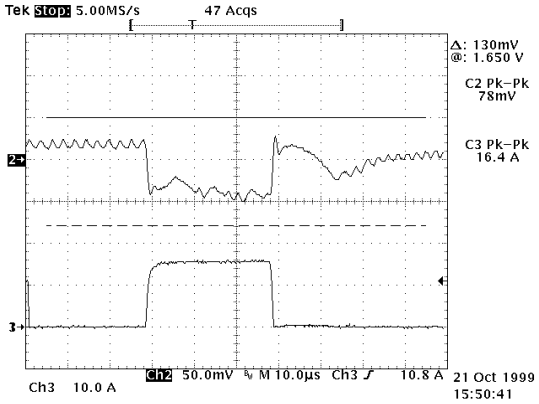


(b) Active droop compensation

Fig. 9. Passive (a) and active (b) droop compensation technique.



(a) Without droop compensation Vout p-p = 146 mV



(b) With droop compensation Vout p-p = 78 mV

Fig. 10. Active droop compensation technique. Channel 2 shows the output voltage (50 mV/div.), Channel 3 shows the load current (10 A/div.), and the cursors show the required limits for the output voltage.

D. Optimization Curves

Equations 1 and 2 for the required numbers of bulk capacitors N1 and N2 can be used to build optimization curves as a function of the output inductance L_O (Fig.11).

These curves are built for a step-down transient by using aluminum electrolytic capacitors with:

C_O = 1000 µF, ESR = 24 mΩ, ESL = 4.8 nH

with the following conditions:

V_{IN} = 5 V, V_{OUT} = 1.65 V, f_S = 100 kHz, ΔV_{OUT} dc = -80 mV / +40 mV, ΔV_{OUT} ac = -130 mV / +80 mV, $I_{O(max)}$ = 26 A, $I_{O(min)}$ = 2.2 A, ΔI_O = 23.8 A, ΔV_{REQ} = 96 mV,

vI_O = 20 A/µs, T_O = 1.19 µs, R_B = 1.5 mΩ, L_B = 1 nH.

The higher number of capacitors related to the curves N1 and N2 must be selected to meet the requirements—in this case for L_O = 2 µH, N1 = 20, while N2 is only 12. These values mean that the voltage drop associated with ESL and L_B is too high. The influence of ESL and L_B and the required number of bulk capacitors N1 can be decreased by placing the high-frequency decoupling capacitors very close to microprocessor pins.The equations for N1 and N2 can be drawn as a function of $T_O = \Delta I_O / vI_O$ for the selected inductance L_O = 2 µH and switching frequency f_S = 100 kHz (Fig.12).The graph shows that doubling T_O from 1.2 µs to 2.4 µs will decrease the number of bulk capacitors from 20 to 15. This transient time increase means that the slew-rate of the transient must be decreased from 20 A/µs to 10 A/µs. A solution by adding high-frequency ceramic decoupling capacitors is illustrated in Fig.13. For 15 electrolytic capacitors the total inductance is ESL1/15 + L_B = 4.8 nH/15 + 1 nH = 1.3 nH. The 805 1-µF ceramic capacitor has ESL1 = 2.6 nH including inductance of vias and traces. The equivalent inductance of four capacitors placed very close to the microprocessor is 2.6 nH/4 = 0.65 nH. Adding four high-frequency decoupling capacitors roughly halves the slew-rate, in accordance with the following equation:

vI_O new = $vI_O \cdot$ (0.65 nH/1.3 nH) = 20 A/µs · 0.5 = 10 A/µs.

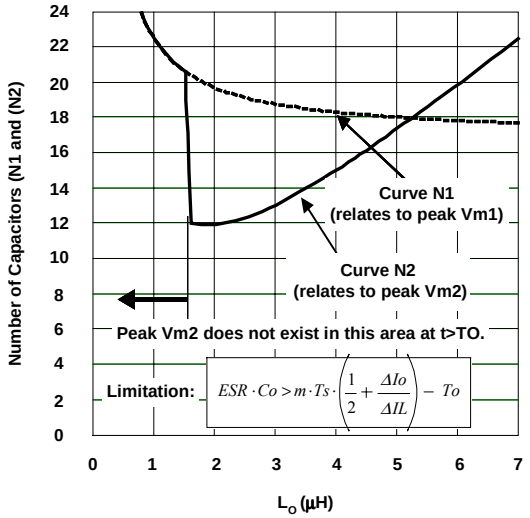


Fig. 11. Optimization curves for the required number of bulk capacitors based on the equations for N1 and N2.

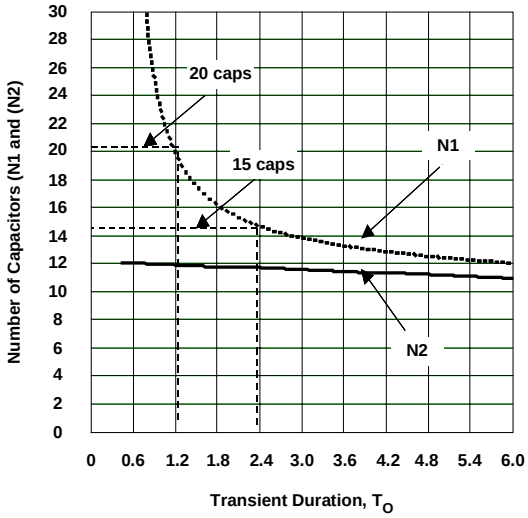


Fig. 12. Required number of bulk capacitors N1 and N2 as a function of the transient duration T_O.

This decrease in the slew rate means that adding four high-frequency ceramic capacitors close to the microprocessor pins decreases the number of bulk capacitors from 20 to 15. Fig. 12 shows that further decoupling does not give significant effect, although four more ceramic capacitors might save roughly two more bulk capacitors. The capacitance and ESR of the ceramic capacitors must be big enough to support the load until the bulk capacitors will take over the transient.

V. Transient Response of a Multi-Phase Interleaved Buck Converter

The interleaved synchronous buck converter becomes a popular solution to supply high-current microprocessors because of the lower input and output current ripple and the higher operating frequency of the input and output capacitors compared to the one-channel solution [42-46]. Interleaving also enables spreading of the components and the dissipated power over the PCB area, but it requires equal current-sharing between the channels. Different control approaches to achieve accurate current-sharing and fast transient response for interleaved microprocessor power supplies are suggested in the literature [44-46]. Meanwhile, outlining an optimal application area for the one-channel and interleaved solutions requires an analysis and output filter selection procedure for the interleaved regulator at high slew-rate load-current transients. Apparently the analysis and optimization procedure for the one-channel synchronous buck converter can be extended to the multi-phase interleaved synchronous buck converters.

The power-delivery system considered in the analysis appears in Fig. 14. The analyzed model includes the n-channel interleaved synchronous buck converter. Each channel of the model is similar to the one-phase solution analyzed earlier (Fig.1).

The converter operates in a phase-shifted manner at the steady state condition sharing the current equally between the channels. For the best response during the transients, all channels turn the high-side FETs simultaneously on at load-current step-up or off at step-down, thus allowing the fastest recovery and a minimum dynamic tolerance of the output voltage. The control signals do not have delays and the duty cycle covers all possible ranges from zero to one. When the output voltage returns to the nominal level after the transient, the channels resume phase-shifted operation with the same sequence they had before the transient. This ideal control algorithm for the best transient response is illustrated in Figs. 14 and 15.

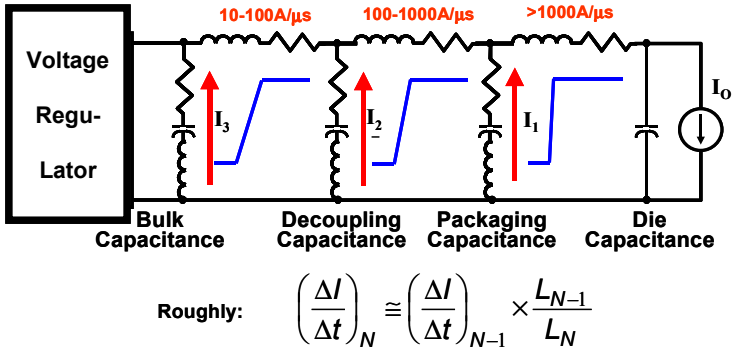


Fig. 13. How high-frequency decoupling decreases current slew-rate.

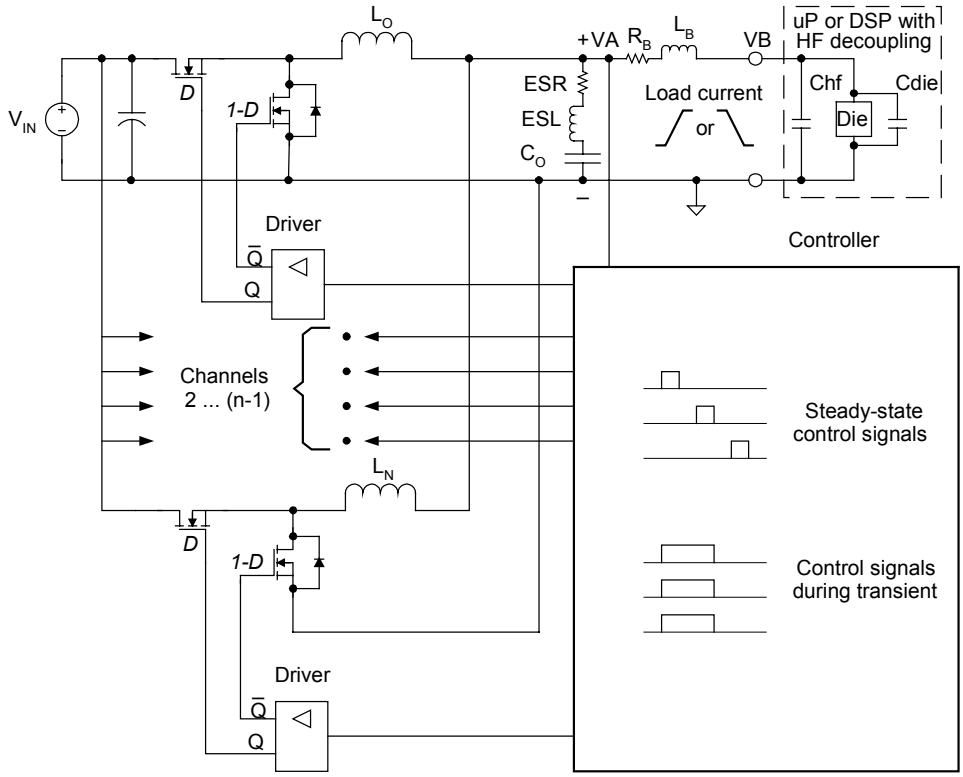


Fig. 14. Analyzed model of the interleaved synchronous buck converter.

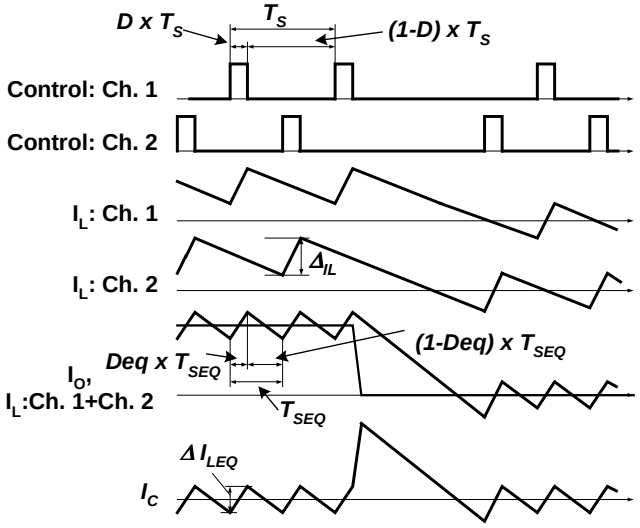


Fig. 15. Control signals, inductor currents through the each channel and summarized inductor, capacitor and load currents of interleaved buck converter at load-current step-down transient.

The analysis is based on the same approach described earlier for the one-channel synchronous buck converter. Assume that (1-D) > n·D, where n - number of channels and $D = V_{OUT}/V_{IN}$ - duty cycle of each channel. This condition is fulfilled for most microprocessor power supplies, for example, the popular 12-V input and 1.6-V output synchronous buck converters with four channels have D = 0.13, (1-D) = 0.87, n·D = 0.52, and thus 0.87 > 0.52. It can be shown that the summarized current through the inductors and output capacitor of an n-channel interleaved converter has the same waveforms as an equivalent one-channel converter with the following parameters:

$D_{EQV} = n \cdot D$, $f_{S(eqv)} = n \cdot f_S$, $T_{S(eqv)} = T_S/n$, $L_{O(eqv)} = L_O/n$, $V_{IN(eqv)} = V_{IN}/n$, $\Delta IL_{EQV} = \Delta IL \cdot (1-n \cdot D)/(1-D)$

where D is duty cycle, f_S is switching frequency, T_S is switching period, L_O is output inductor, V_{IN} is input voltage and ΔIL is peak-to-peak inductor-current ripple of each channel of the interleaved buck converter. D_{EQV}, $f_{S(eqv)}$, $T_{S(eqv)}$, $L_{O(eqv)}$, $V_{IN(eqv)}$, and ΔIL_{EQV} are duty cycle, switching frequency, switching period, output inductor, input voltage and peak-peak inductor-current ripple of the one-channel equivalent buck converter respectively. The waveforms in Fig.15 illustrate this statement.

During the transients, because all channels turn to the same state simultaneously in accordance with the proposed control algorithm, the interleaved converter can be considered a one-channel, which now has the same input voltage V_{IN} as the original interleaved one and the output inductor L_O/n. The consideration of the parameters of the equivalent one-channel converter helps to explain what kind of advantages to expect from the interleaved converter. Interleaving provides the same properties as the one-channel converter when operating at higher frequency, having higher duty cycle and lower input voltage and inductor value. But all this happens only if a good steady state and dynamic current sharing are provided between the channels.

In an ideal control circuit, the transient response of the interleaved converter is defined by the output-filter characteristics including the slew-rate of the inductor current. It is interesting that for the step-down transient when all low-side switches are turned on, the inductor-current slew rate equals $(V_{OUT} \cdot n)/L_O$ and has the same slew-rate as during the $(1-D_{EQV})$-part of the switching cycle. But for the step-up transient when all high-side switches are turned on, the slew-rate of the inductor current is $(n \cdot (V_{IN}-V_{OUT}))/L_O$, which is much higher than in steady state operation during the D_{EQV}-part of the switching cycle, where the slew-rate is only $(V_{IN}-V_{OUT} \cdot n)/L_O$.

The transient-response dependence on the position of the switching cycle in which the load-current transient occurs is the same as that of the one-channel converter. The difference is that the summarized currents through all the channels and the output voltage ripple cancellation effects must be considered, which is accomplished in this analysis by substituting an equivalent one-channel converter. Further analysis estimates the worst-case transient and compares the different type of output capacitors in the interleaved converter.

The example below illustrates how the number of channels and capacitor characteristics defines the number of required bulk capacitors N1 and N2 [42]. The following requirements are typical for a modern high-end microprocessor:

- V_{IN} = 12 V,
- V_{OUT} = 1.5V,
- $I_{O(max)}$ = 50 A,
- $I_{O(min)}$ = 0 A,
- ΔI_O = 50 A,
- ΔV_{REQ} = 100 mV,
- vI_O = 50 A/μs,
- R_B = 0.4 mΩ,
- L_B = 0.2 nH,
- f_S = 200 kHz.

Optimization curves are built for aluminum electrolytic, OS-CON, specialty polymer SP and ceramic capacitors. The required number of capacitors N2 and inductor value L_O at different switching frequencies for this application are shown in Table 1.

These numbers of capacitors relate to an ideal controller. The practical implementation might require some additional capacitors. But this analysis sets goals to achieve and shows relations between the number of capacitors and number of channels, switching frequency, inductor value, and capacitor and layout parasitics.

TABLE 1. OPTIMAL REGULATOR PARAMETERS FOR DIFFERENT TYPES OF CAPACITORS AND NUMBER OF CHANNELS

Type	Vendor	Part Number	F_S per ch lkHz	Parameters of each capacitor			Number of Capacitors for Different Numbers of Interleaved Channels / L_O per Channel			
				C_O 1μF	ESR 1mΩ	ESL 1nH	1 one Channel	2 two Channel	3 three Channel	4 four Channel
Aluminum Electrolytic	Rubycon	6.3ZA1000	200	1000	24	4.8	18/0.8μH	16/1.6μH	16/2.4μH	15/3.2μH
OS-CON	Sanyo	4SP820M	200	820	8	4.8	8/0.25μH	7/0.5μH	6/0.75μH	6/1.0μH
Specialty Polymer	Panasonic	eefcd0d101r	300	100	20	3.2	28/0.1μH	18/0.2μH	15/0.3μH	13/0.4μH
Ceramic, 1210	Murata	grm235y5v 226z10	400	22	20	0.5	60/0.05μH	30/0.1μH	20/0.15μH	16/0.2μH

The following is the summary of the comparison.

- The aluminum electrolytic and OS-CON capacitors require significant additional high frequency decoupling at slew-rate 50 A/μs because N1 >> N2.
- Interleaving for aluminum electrolytic and OS-CON capacitors does not significantly decrease the number of required output capacitors. Only the decrease in the input filter ripple needs to be considered as the result of interleaving.
- The 2-channel interleaving is optimal for the specialty-polymer capacitors. They require much lower high-frequency decoupling at 50 A/μs load-current slew-rate in comparison with the aluminum electrolytic capacitors.
- The most significant effect of interleaving relates to the solution with the ceramic capacitors. The required number of them drops almost inversely proportional to the number of interleaved channels. Ceramic capacitors do not require additional decoupling at 50 A/μs load-current slew-rate.

VI. CONTROL TECHNIQUES FOR POWERING LOW-VOLTAGE, HIGH SLEW-RATE LOAD

A. Review of Control Techniques for High-Slew Rate Load-Transient Applications

Different control approaches are considered in the literature [19-27,30,33,37,40,41,45,46] for the high-slew-rate load-current transient applications. Some solutions require additional circuitry, such as a power amplifier or switch, to regulate the output voltage if it exceeds some set points at the transients [23,25]. This approach complicates the design. Moreover, to avoid the interaction between the main and the additional control circuitry at normal operation, the output voltage set points of the additional circuitry have to be at least 2-3 percent different from the reference voltage of the main circuitry. This requirement causes some delay until the additional circuitry starts to control the output voltage when the transient occurs. The cost of this delay is the additional bulk capacitors in the output filter. The other potential problem results from the occurrence of the transients in the microprocessors with high repetitive frequency (up to 100 kHz most of their operation). That means that this additional circuitry could operate frequently and dissipate a significant amount of power, because it usually operates in the linear mode. Although these ideas are interesting and

may find their optimal application niche, this topic addresses only the control approaches that do not require additional switches or power amplifiers.

Let us review some basics of the control theory before considering and reviewing different control approaches. In control theory, any switching regulator with feedback loop includes a plant and a compensator. The plant in a switching regulator is its power stage, with at least two different states controlled by the switching function. The regulated output signal of this control system is the output voltage of the regulator. The compensator senses the output voltage and somehow changes the switching function to keep the output voltage within the required window. The power stage of the voltage regulator must include a low-pass filter, which is a second order L-C filter in the applications considered. There are many different disturbances, such as input voltage, temperature, aging, and load current that change the output voltage. But for the considered power-delivery system with a high-slew-rate transient type of load, the main disturbing factors is the load current and the slew-rate of the current transient. As discussed in the "Introduction" section above, the load-current transient step and its slew-rate for the considered type of load is much higher than in most generic applications. At the same time the required tolerance of the output voltage of the regulator is very tight. On the basis of this discussion the following main problems can be specified:

- The low-pass filter nature of the power stage means that the fast response to the load-current transients is limited and defined first of all by the power stage itself.
- The power stage with a fast response to the load-current transient might require high-slew rate current changes through its own components. At the same time the power stage must prevent the transient propagation outside the regulator without a significant increase of the input filter. These are contradictory requirements.
- The compensator senses the change of the output voltage when the load-current transient occurs. The tight tolerance requirements for the output voltage makes it even more difficult to separate the output voltage change caused by a load-current transient from noise.
- The direct sensing of the load current helps to avoid the additional delays. The load current must be sensed between the output capacitor and the microprocessor because the output inductor current or current through the power switch is not the actual load current.
- The ESR and ESL of the output capacitors and the supply path parasitics help to sense the load current and its changes because of the additional voltage drop. But the design goal is to avoid this voltage drop by selecting lower ESR and ESL capacitors and improving the layout. These are also contradictory requirements.
- The compensator cannot improve the dynamic characteristics of the power stage. Actually the compensator only degrades the transient response because of the delays and restrictions put by the compensator on the power stage.
- Some think that the compensator has no influence and that only the output capacitor characteristics define the response characteristics because the slew-rate of the transient is too high. That might be true if the output capacitance is so over-killed that any controller is fast enough to handle the transient. In reality, an output filter with minimum size (or cost) can be designed only by using a fast and optimal compensator (control approach). In other words, the sooner the controller starts to react on the transient, the better is the response, because the first spike can be suppressed by high- or mid-frequency decoupling.

This discussion suggests the desirability of first finding the optimal power stage, including the low-pass filters. (That attempt was made in the previous section.) After that, on the basis of the transient analysis, the control approach must be selected. The control approach must not significantly degrade the dynamic characteristics of the power stage and must provide some additional properties that increase the reliability and the robustness of the power-delivery system, for example, current limit, constant or variable switching frequency, and pulse-duration limitations.

There is a large variety of control techniques in power electronics. The control techniques reviewed and considered in the topic are selected on the basis of their current popularity in this application area or of their promising characteristics. These control approaches are voltage mode (Fig. 16), peak current mode (Fig. 17), average current mode (Fig. 18), V^2-mode (Fig. 20), and hysteretic (ripple) mode (Fig. 19). They can be divided in the following two groups:

- Control techniques that do not sense the load current or its changes directly, and so do not feed-forward or feed back this signal. This is group-control with a "slow" feedback loop, because it senses the disturbance caused by the load current indirectly and uses this signal in the main feedback loop. This group improves the dynamic response by increasing the unity-gain-frequency bandwidth of the voltage mode [20] or of different types of current-mode [21,36-39] control. Some authors have suggested an optimization of the small-signal characteristics for a minimum output impedance [22].

- The control techniques that does sense the output current transient directly or through the related change of the output voltage and uses this signal in a fast feedback loop or feed-forwards it to improve the transient response. The main examples of this group are hysteretic-mode [26, 29-33] and V^2 -mode [27,46] control techniques. This is group control with a "fast" feedback loop.

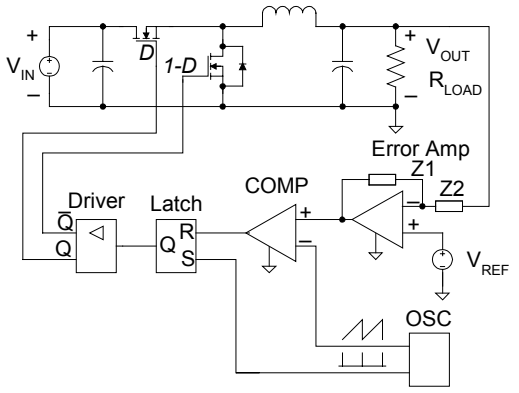


Fig. 16. Voltage mode control.

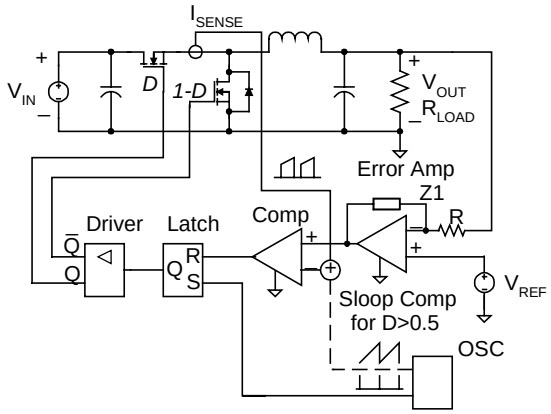


Fig. 17. Peak current mode control.

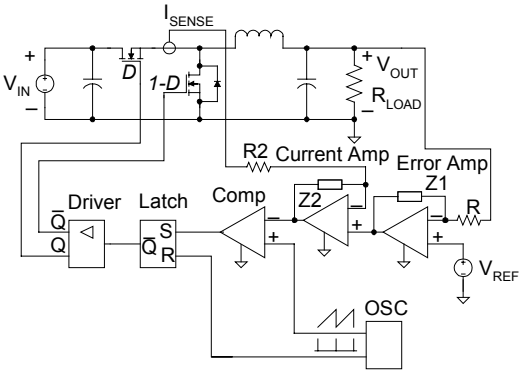


Fig. 18. Average current mode control.

B. Control with Slow Feedback Loop

This approach requires complicated feedback-loop-compensation circuitry for a stable converter operation at all conditions, including the wide range of the output capacitance that is usually specified by the requirements [11]. The unity-gain bandwidth must be at least a few times lower than the switching frequency, so the dynamic characteristics of the regulator are relatively slow. Using a small-signal model to

interpret and improve the large-signal transient response characteristics, as described in [20,22], is questionable. Although these controllers are very popular in most generic applications, their transient characteristics are worse than the controllers having direct load-current sensing and a fast load-current feedback loop.

C. Control with Fast Feedback Loop

The most popular implementation of the second approach is the hysteretic control and V^2 mode control. The hysteretic control (or two-state, bang-bang, ripple, free-running regulator, etc.) is the simplest control approach, which has been used for a long time [28]. This is probably the earliest controller or regulator. The hysteretic controller became the solution in the new applications that require the fast load-current transient response power supplies. This is a very simple solution that does not require the compensation circuitry and has the excellent dynamic characteristics. The examples of integrated circuit implementation of this approach for modern applications are available now from a few companies, including Texas Instruments (Fig. 19).

Unlike other control approaches, this controller does not have a slow feedback loop: it reacts on the load-current transient in the switching cycle where the transient occurs. Its transient response time depends only on delays in the hysteretic comparator and the drive circuitry. The high-frequency noise filter in the input of the comparator also adds some additional delay. Those delays depend mostly on the level of the selected technology, and so the hysteretic control is theoretically the fastest solution. The other advantage of the hysteretic controller is that its duty cycle covers the entire range from zero to one. It does not have the restrictions on the conduction interval of the power switches that most of the other control approaches have. This capability is very important to decrease the recovery time of the output voltage after a load-current transient.

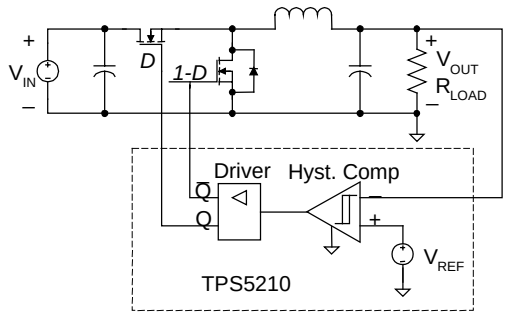


Fig. 19. Hysteretic control.

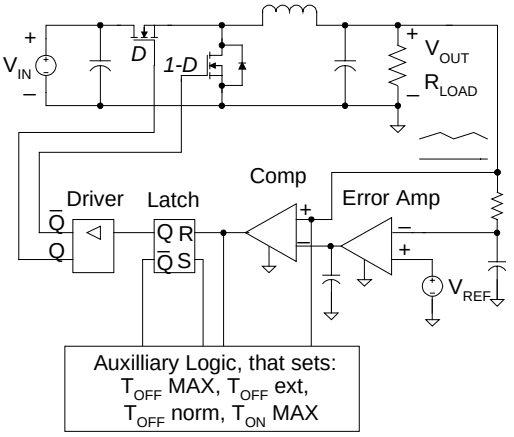


Fig. 20. One of the implementations of V^2 mode control.

The V^2 mode control also has very fast transient-response characteristics, but it has drawbacks in its original implementation (Fig. 20). This controller uses the output-voltage ripple as the ramp signal of the modulator. It is assumed that the voltage ripple of the output capacitor depends mostly on the ESR, while the part of ripple caused by the ESL and C_O is negligible. In this case the ripple is proportional to the inductor current ripple. At the transients, this voltage carries the information about the load-current change directly to the comparator, bypassing the slow main feedback loop. The V^2 mode control actually can be defined as the sort of hysteretic control having the additional error amplifier. This amplifier enables an increase of the hysteresis window of the comparator without degrading the accuracy of the output voltage.

On the other hand, the use of output ripple-voltage as the ramp signal causes the stability to depend greatly on the output capacitor parasitics. This dependence is especially problematic when using many high-frequency ceramic or film capacitors in parallel as the output filter. In this case, the equivalent output capacitor is almost ideal, because its parasitics are negligible and an output ripple has a parabolic waveform instead of a linear ramp. This ripple is also with an angle of $\pi/2$ out of phase with the output inductor current. Providing a stable operation in this situation might be a problem. Another possible problem is getting a reliable and predictable startup characteristic of the V^2 mode controller. The controller may require additional circuitry for the startup control only, as in the original implementation [Fig. 20]. To avoid these problems, the modifications of V^2 mode control superimpose the inductor-current ramp signal onto the input of a comparator [46].

There is another problem related to controllers that sense information about load current by using output capacitor's ESR: their frequency dependence from the output filter parasitics and its variation related to tolerances and variations of the capacitor characteristics. This problem could be solved by using the frequency synchronization or again, by superimposing an additional ramp signal to avoid dependence from the output filter [29,40,41]. It is useful to mention that the compensation of controllers with the slow feedback loops also depends on the output capacitor parasitic variations. Table 2 shows pros and cons of the discussed controllers for high-slew-rate load-current transient applications.

TABLE 2. COMPARISON OF CONTROL APPROACHES FOR HIGH SLEW-RATE TRANSIENT APPLICATIONS

	Hysteretic (ripple) control	V^2 mode control	Voltage mode control	Current mode control
Reaction time	150ns - 200ns (limited only by technology)		5 - 10 μs in best case, because of slow feedback loop	
ON/OFF time duration limitation	No limitation	Constant OFF time in practical implementation, that degrade transient response	Limited by switching cycle of internal oscillator in constant switching frequency implementation	
Duty cycle limitation	No limitation		Yes/No Depends on part	Yes

Apparently any control allows implementation of the passive or active droop-compensation techniques discussed in the transient analysis section [Fig. 9]. But the cost of the implementation might be different. For example the compensation circuitry of controllers with slow feedback loop could be designed with low load regulation for this purpose. The question is still how fast the active droop compensation is. Usually the droop compensation needs to complete its own transient within 1-2 μs to be ready for the next transient. The hysteretic controller requires an additional current sense amplifier for the active droop implementation.

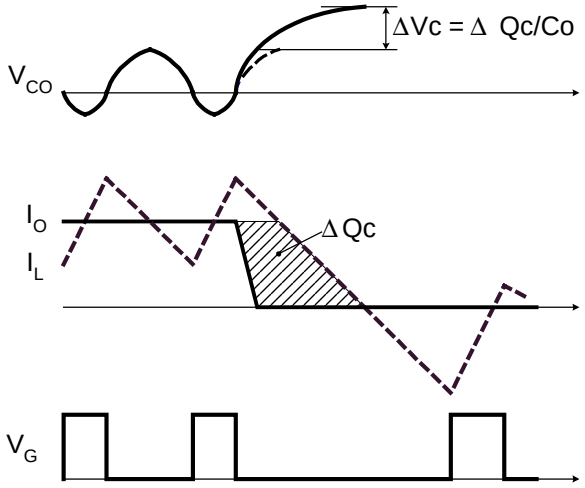
VII. EFFECT OF CONTROLLER LIMITATIONS ON THE TRANSIENT RESPONSE

The previous analysis assumed that the controller is ideal. The ideal controller does not have delays. It is able to maintain the on or off state of the respective power switches during a transient as long as necessary. As shown above, the controller parameters influence the second peak of the transient but have no effect on the first one (Fig. 5b). The real controllers do have delays and might have some restrictions on the duty cycle. For example, the constant on-time controller must complete its on-cycle for the high-side FET all the time, even when a transient occurs.

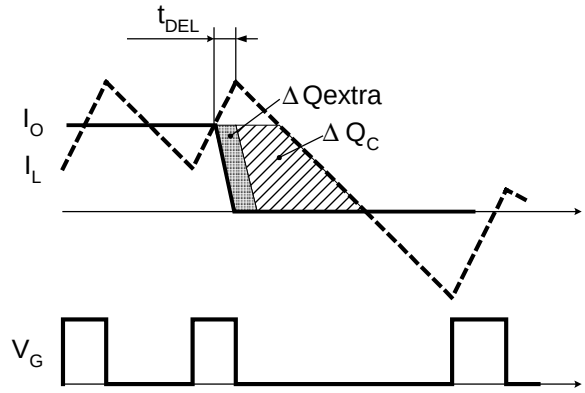
The same issue relates to the constant off-time control, but here the off-time cycle must be completed. The controllers with a trigger latch working at a constant frequency usually have restrictions on the maximum duty-cycle. Control approaches that do not have a fast feedback loop (which senses the load-current transient directly) require at least a few switching cycles until they start to change the duty cycle and to respond to a transient. This delay is caused by their low unity-gain bandwidth of the compensation circuitry compared to the switching frequency. Fig. 21 shows how the actual controller degrades the transient waveforms at a load-current step-down. The moment when the transient occurs is selected to get the worst-case conditions for each kind of controller.

The ideal controller in Fig. 21a does not have delays and duty-cycle restrictions. The capacitive portion of the output voltage vC_O gets the additional rise ΔV_C because the charge ΔQ_C is delivered to the output capacitor C_O (Fig. 1) by the inductor L_O. The delay t_{DEL} that any real controller has adds the extra charge ΔQ_{EXTRA} (Fig. 21b). This additional charge increases the second peak of the output-voltage transient waveform (Fig. 4) by $-\Delta Q_{EXTRA} / C_O$. The constant on-time controller (Fig. 21c) gets the extra-charge related to the delay and to the fixed on-time. The controller with a slow feedback loop (Fig. 21d) has even more extra charge and related voltage-soar than the previous controllers. This extra charge can have significant effect on the transient waveforms if the output filter has relatively low output-capacitance like, for instance, the ceramic capacitors in a high-frequency regulator. Actually the extra charge becomes more important in a low-size high-frequency solution. There the controller parameters could significantly affect the regulator cost and size.

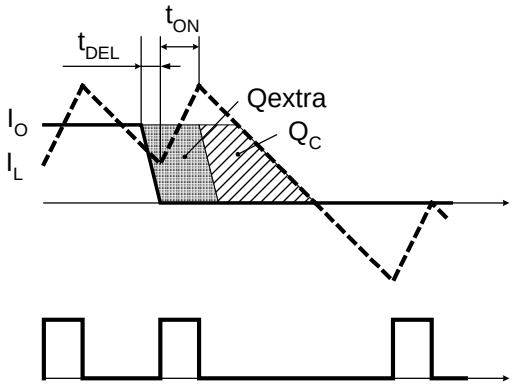
The control considerations in this section suggest that transient response makes the hysteretic controller is one of the best solutions for powering high slew-rate transient loads. The next section is dedicated to further analysis of this controller and some of its modifications.



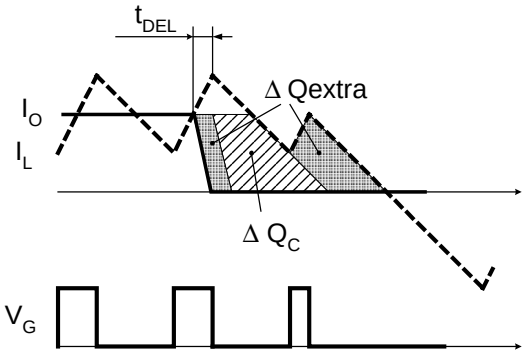
(a) “Ideal" controller. The moment of the transient is selected to get the worst-case condition.



(b) Controller with delays. The moment of the transient is shifted to the left to get the worst-case condition.



(c) Constant on-time controller with delays. The moment of the transient is shifted to the left because of delays and fixed on-time.



(d) Controller with delays and slow feedback loop.The additional on-cycle appears because of slow feedback loop.

Fig. 21. Impact of actual controller limitations on transient.

VIII. Modern Hysteretic (Ripple) Controller and its Modifications

A. Requirements for a Hysteretic Comparator

There are many examples of new requirements and technological achievements bringing new life to some old ideas and forgotten solutions. The hysteretic regulator is one of these examples. This regulator, based on a Schmidt trigger, was very popular in the 60s and early 70s. Unfortunately the simple scheme does not always mean easy analysis and design. Later, more sophisticated control approaches took over most applications by allowing fixed-frequency operation and more predictable design procedures. Nevertheless, the hysteretic control, which by control-theory definition belongs to the slide-mode control or a relay system, always has natural advantages such as fast transient-response. The engine of a modern hysteretic regulator is its comparator, which has a hysteresis window. The comparator is intended to keep the output voltage and ripple within the hysteresis window. In reality the ripple is always higher than the hysteresis window because of the delays. Another problem is that the switching frequency depends significantly on the power stage characteristics and the operation conditions.

Fast transient-response regulators are needed for powering devices such as modern, high slew-rate transient microprocessors, DSPs, and memory ICs. That need, and achievements in analog IC design technology, have made the hysteretic control interesting again. Modern hysteretic comparators have delays of only tens of nanoseconds, with a hysteresis window around 10-20 mV. This voltage is far from that of the old Schmidt triggers with hundreds of millivolts of hysteresis in a frequency range of a few kHz. The theoretical analysis of hysteretic regulators also must now take into account component and layout parasitics that cannot be avoided at or above a hundred kHz switching frequency and with extremely high slew-rate transients.

B. Switching Frequency of Hysteretic Regulator

Switching-frequency predictability of a hysteretic controller is important for a power-supply design. A simple and accurate method of determining the switching frequency is described below [26]. Assume that the input and output voltage ripple magnitudes are relatively negligible in comparison with the dc component. Also suppose that the time constant $L/(R_{DS(on)} + R_L)$ that includes the output inductor, L, the on-state resistance of the FET, $R_{DS(on)}$, and the inductor resistance, R_L, is high in comparison to the switching period. Assume the body-diode conduction time and switching-transition time are much shorter than the switching period. These assumptions are reasonable for high-efficiency regulators with low output- and input-voltage ripple. In such a case the output inductor current can be modeled as the sum of the dc component (equal to the output current I_O) and the ac linear ramp component, which flows through the output capacitor (Fig.22). The peak-to-peak value of the inductor current ΔI is equal to the following equation:

$$\Delta I = \frac{V_{IN} - I_O \cdot \left(R_{DS(on)} + R_L\right) - V_{OUT}}{L} \cdot D \cdot T_S \qquad (12)$$

where,

V_{IN} is the input voltage;

V_{OUT} is the output voltage;

T_S is the switching period;

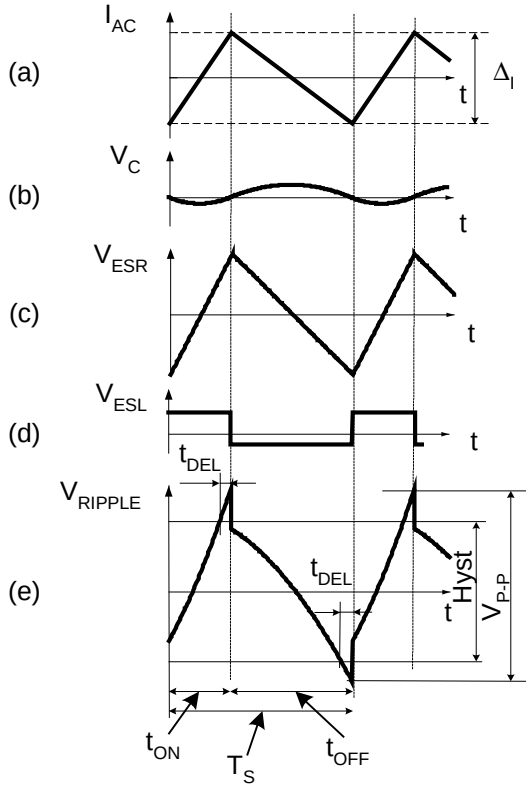
$$D = \frac{V_{OUT} + I_O \cdot (R_{DS(on)} + R_L)}{V_{IN}}$$

is the duty cycle which is defined as:

$D = t_{ON} / T_S$,

and t_{ON} is the on-time of the high-side FET.

The output capacitor can be modeled as the series connection of an ideal capacitor C_O and its ESR and ESL. The voltage waveforms across the each component of the output capacitor and the corresponding equations are shown in Fig. 22.



(a) Current waveform through the output capacitor

(b) Voltage ripple at the ideal capacitor with the initial value at the beginning of the high-side FET on-time.

High-side FET on:

$$V_C = \frac{\Delta I \cdot t^2}{2 \cdot C_O \cdot D \cdot T_S} - \frac{\Delta I \cdot t}{2 \cdot C_O}$$

High-side FET off

$$V_C = \frac{\Delta I \cdot t}{2 \cdot C_O} - \frac{\Delta I \cdot t^2}{2 \cdot C_O \cdot (1-D) \cdot T_S}$$

(c) Voltage waveform at the ESR

High-side FET on

$$V_{ESR} = ESR \cdot \left(\frac{\Delta I \cdot t}{D \cdot T_S} - \frac{\Delta I}{2} \right)$$

High-side FET off

$$V_{ESR} = ESR \cdot \left(\frac{\Delta I}{2} - \frac{\Delta I \cdot t}{(1-D) \cdot T_S} \right)$$

(d) Voltage waveform at the ESL

High-side FET on

$$V_{ESL} = \frac{ESL \Delta I}{D \cdot T_S}$$

High-side FET off

$$V_{ESL} = -\frac{ESL \cdot \Delta I}{(1-D) \cdot T_S}$$

(e) Summarized output voltage ripple waveform $V_{RIPPLE} = V_C + V_{ESR} + V_{ESL}$

Fig. 22. Voltage waveforms across each component of the output capacitor and the corresponding equations.(The time in each equation starts from zero at the beginning of the corresponding state.)

The output voltage ripple V_{p-p} is higher than the hysteresis window Hyst because of the delays t_{DEL}. Assume for simplicity that the delays for both switching moments are equal. The ideal capacitor voltage component has the same initial value during the switching cycles t_{ON} and (T_S-t_{ON}). (See Fig. 22.) In this case the voltage V_{p-p} is given by the following equation:

$$V_{p-p} = \frac{ESL}{L} \cdot V_{IN} + \Delta I \cdot ESR \qquad (13)$$

On the other hand the hysteresis window is equal to the difference between the peak-to-peak values of the V_{OUT} ripple V_{RIPPLE}, at the moments $t_{ON} - t_{DEL}$ and $t_{OFF} - t_{DEL}$:

$$Hyst = V_{RIPPLE}(t_{ON} - t_{DEL}) - V_{RIPPLE}(t_{OFF} - t_{DEL}) \qquad (14)$$

Substituting Equation 12 into the equations for V_C, V_{ESR} and V_{ESL} (Fig.22) and using Equations 13, 14 and 15, the following equation for the switching frequency, f_S, can be derived:

Equation 15 shows that the switching frequency strongly depends on the ESR and ESL. It is important that the ESL should meet the following condition:

$$ESL < (ESR \cdot t_{DEL} + Hyst \cdot L \cdot D / V_{OUT}) \cdot$$

If it does not, the voltage step at the ESL during switching exceeds the hysteresis window and the switching frequency becomes too high and uncontrollable.

In Equation 15 the switching frequency does not depend on the load current. This is because the synchronous regulator has only two states of operation during one switching period over the whole load-current range, including the no-load condition. In reality there is a weak dependence of the switching frequency on the load current because of the power losses and additional voltage drops at non-ideal components. Equation 15 should be sufficiently accurate for the first frequency evaluation at the beginning of a design. For a more precise frequency evaluation, one can use the equation that is shown in the Appendix 2, which includes the dependence on load current and static-loss resistances. Also, a detailed derivation of this equation is represented in the Appendix 2.

The theoretical prediction and the measurement results of the frequency for the evaluated power supply, under no load and 20-A load conditions, is given in Fig. 23.

Four Os-Con 820 µF, 4-V capacitors are used in this power supply. The measured values for the ESR and the ESL for the each capacitor are 8 mΩ and 4.8 nH respectively, using an impedance analyzer with lead-length error compensation. These values are divided by four because there are four capacitors in parallel. The other values substituted in Equation 15 are the following:

- L = 1.2 µH
- R_L = 11mΩ
- Hyst = 20.25 mV
- t_{DEL} = 570 ns

The theoretical results are a good approximation for measured results; the maximum difference is less than 7%.

The switching frequency was also measured with the four 10 µF ceramic capacitors. The results with and without ceramics are given in Fig. 24. For low input voltages, the switching frequencies are about the same. For the input voltage between 7 V and 11 V, the frequency is lower with the ceramics, because the resonant period between the ceramic and the OS-CON capacitors is close to the on-time of the converter. This resonance lengthens on-time; off-time must also increase to regulate V_{OUT} to the correct value thus lowering the switching frequency. Adding the decoupling ceramic capacitors decreases the ESL from 1.2 nH to 0.8 nH, consequently decreasing the switching frequency.

The theoretical output voltage waveform based on the derived equations is obtained using Mathcad software. These calculations are very close to the experimental waveforms (Fig. 25).

$$f_S = \frac{V_{OUT} \cdot (V_{IN} - V_{OUT}) \cdot \left(ESR - \frac{t_{DEL}}{C_O} \right)}{V_{IN} \cdot (V_{IN} \cdot ESR \cdot t_{DEL} + Hyst \cdot L - ESL \cdot V_{IN})} \quad (15)$$

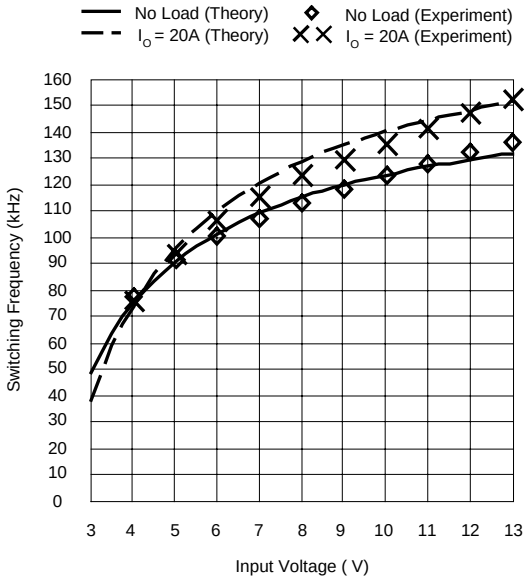


Fig. 23. Theoretical and measured switching frequency comparison at no-load and full-load conditions.

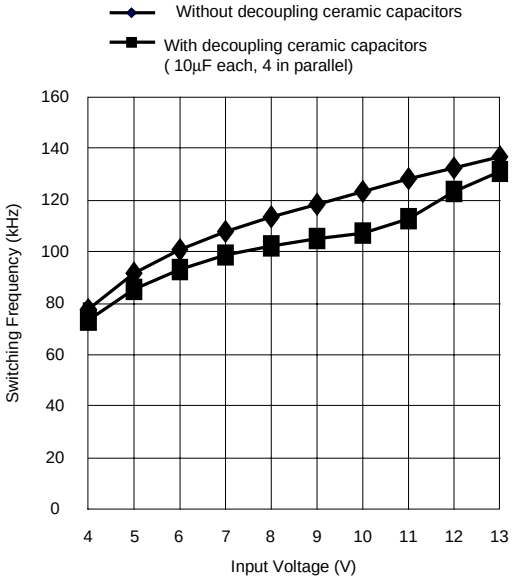
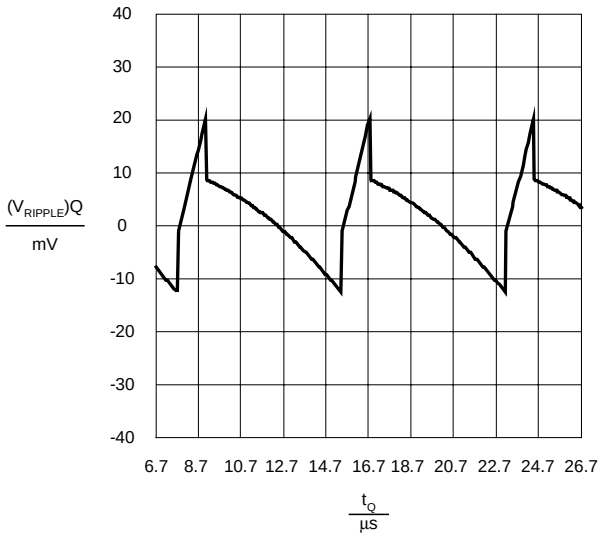
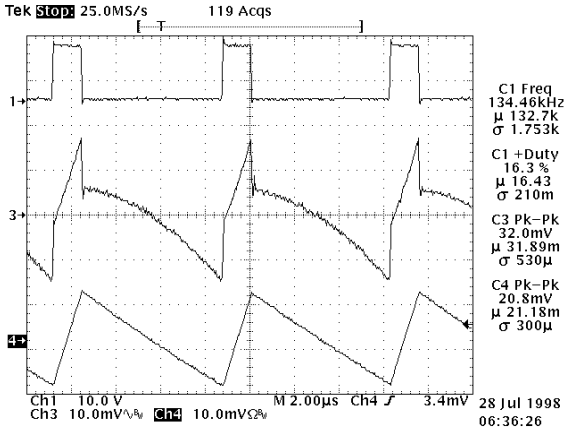


Fig. 24. Measured switching-frequency comparison with and without ceramic decoupling capacitors.



(a)



(b)

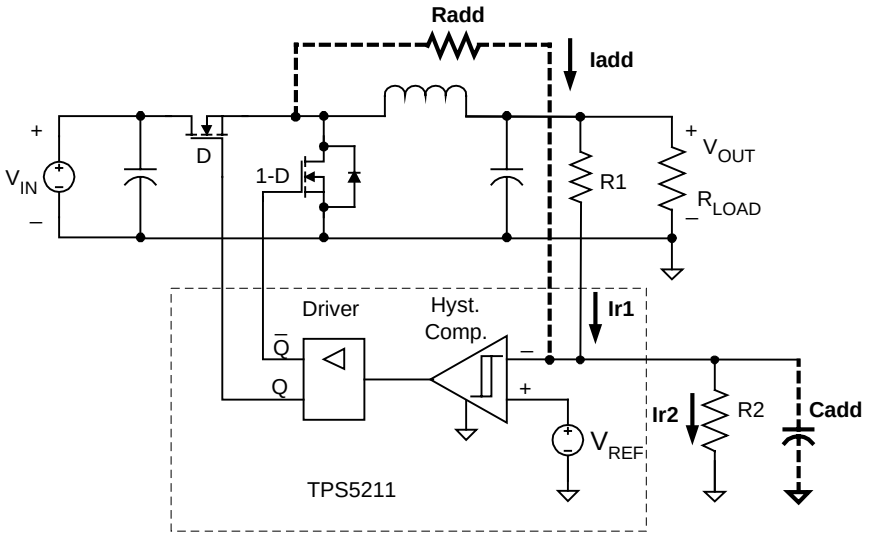
Fig. 25. Theoretical (a) and measured (b) output ripple waveforms.

C. Modified Hysteretic Regulator Invariable from Output Filter

The previous analysis shows that the switching frequency of a hysteretic controller in its typical implementation depends on the output-filter characteristics, including ESR and ESL of the output capacitor. This natural self-oscillating frequency of a hysteretic controller may be too low to take the full advantage of higher operating frequencies that allow using smaller output inductors and surface-mount low-ESR-output capacitors.

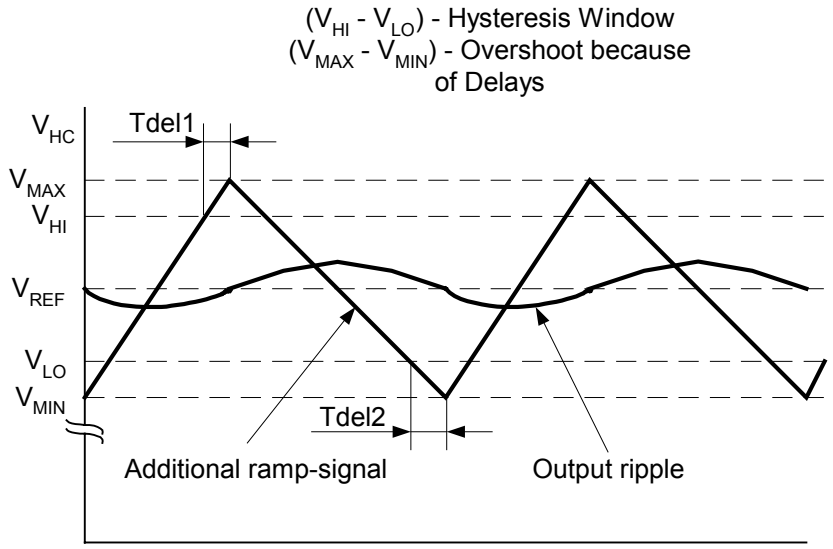
The suggested modified hysteretic controller includes a circuit that superimpose a ramp signal onto the sensed-output ripple voltage at the input of the hysteretic comparator [29,40,41]. At some level of this additional ramp, the hysteretic controller becomes invariable from the output-filter characteristics. The discussion below presents a few implementations of this modified controller, along with related equations for a switching frequency and an output voltage. The results of an analysis are compared with the measurements on the evaluation board. The additional circuit can be implemented with external components or integrated inside the hysteretic controller IC. Fig. 26a is a simplified diagram of a synchronous buck converter with a modified hysteretic controller.

The additional circuit R_{ADD}–C_{ADD} is added to the dc-to-dc regulator. The resistor R_{ADD} is connected between the input of the hysteresis comparator and the midpoint of the power switches. The capacitor C_{ADD} is connected between the same input of the comparator and ground. This circuit forms an additional ramp signal at the input of the hysteretic comparator. The two signals are summed at the input of the comparator—the ramp signal from the circuitry R_{ADD}–C_{ADD} and the signal from the output of the converter. (See Fig. 26b.)



(a)

Fig. 26. Synchronous buck converter with modified hysteretic control (a) and its comparator input waveforms (b).



(b)

Fig. 26. Synchronous buck converter with modified hysteretic control (a) and its comparator input waveforms (b).

By proper selection of R_{ADD} and C_{ADD} the amplitude of the additional ramp signal can be greater than the output ripple of the converter. As the result, the switching frequency becomes higher while the output ripple becomes lower. The switching frequency depends on R_{ADD} and C_{ADD}, and no longer depends on the output-filter characteristics. Assuming that the ripple at the capacitor C_{ADD} is small and so the currents I_{ADD}, I_R1 and I_R2 are constant within the intervals $D \cdot T_S$ and $(1\text{-}D) \cdot T_S$, the equation for a switching cycle T_S of the modified hysteretic controller can be derived as: (see below)

Equations 17 and 18 are charge and discharge currents of the capacitor C_{ADD} during the intervals $D \cdot T_S$ and $(1\text{-}D) \cdot T_S$ correspondingly. Equation 16 is accurate if the output ripple of the converter is much lower than the additional ramp (Fig. 26b). It means that the natural switching frequency of the converter, which is defined by the output filter parameters, is much lower than the switching frequency defined by the additional R_{ADD}–C_{ADD} circuit. The output voltage of the converter is defined by the following equation:

$$V_{OUT} = V_{REF} \cdot \left[1 + \frac{R1 \cdot R_{ADD}}{R2 \cdot (R1 + R_{ADD})} \right] \qquad (19)$$

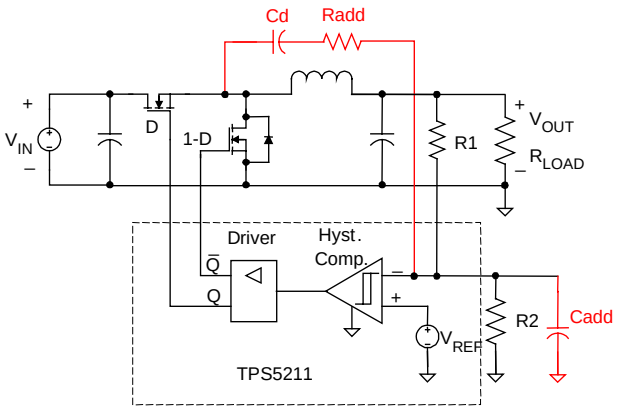
The output voltage V_{OUT} depends on the additional resistor R_{ADD}. To avoid this dependence, a decoupling capacitor C_D is added in series with R_{ADD} as shown in Fig. 27. The value of this capacitor must be much higher than C_{ADD}.

$$T_S = \frac{V_{IN} \cdot C_{ADD} \cdot Hyst}{R_{ADD} \cdot I_{CH} \cdot I_{DCH}} + T_{DELL} \cdot \left(1 + \frac{I_{CH}}{I_{DCH}} \right) + T_{DEL}2 \cdot \left(1 + \frac{I_{DCH}}{I_{CH}} \right) \qquad (16)$$

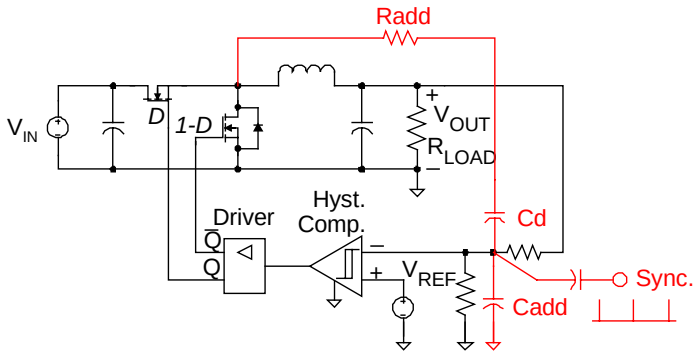
where $T_{DEL}1$ and $T_{DEL}2$ characterize the comparator and drive circuitry delays, and

$$I_{CH} = \frac{V_{IN} - V_{REF}}{R_{ADD}} + V_{REF} \cdot \left[\frac{R_{ADD}}{R2 \cdot (R_{ADD} + R1)} \right] - \frac{V_{REF}}{R2} \qquad (17)$$

$$I_{DCH} = V_{REF} \cdot \left[\frac{1}{R_{ADD}} + \frac{1}{R2} - \frac{R_{ADD}}{R2 \cdot (R_{ADD} + R1)} \right] \qquad (18)$$



(a)



(b)

Fig. 27. Modified hysteretic regulators with the decoupling capacitor C_D.(a) and the synchronized frequency (b).

With the decoupling capacitior C_D, the output voltage is defined as:

$$V_{OUT} = V_{REF} \cdot \left(1 + \frac{R1}{R2}\right) \qquad (20)$$

The voltage at the decoupling capacitor Cd is $V_{CD} = V_{OUT} - V_{REF}$, and the switching cycle of the converter is defined by the equation below.

The switching frequency does not depend on the output-capacitor characteristics, so high-frequency, low-cost ceramic or film capacitors can be used in this dc-to-dc converter, maintaining the same excellent load-current transient-response characteristics. The R_{ADD}–C_{ADD} circuit adds feed-forward properties to the controller improving the input-voltage step transient response.

To verify the analysis and assumptions, the switching frequency of the synchronous buck converter (Fig. 26a) was measured for 2-V, 1.65-V and 1.3-V output voltages and for the input voltage from 4 V up to 13 V. The comparison shows good correlation between the theory and experiment (Fig. 28). For this estimation the parameters of Equations 16-19 are the following:

- R_{ADD} = 49.9 kΩ
- R1 = 150 Ω
- R2 is open
- C_{ADD} = 1060 pF
- $T_{DEL}1$ = 240 ns
- $T_{DEL}2$ = 250 ns
- Hyst = 0.5% of V_{OUT}

$$T_S = \frac{V_{IN} \cdot C_{ADD} \cdot Hyst \cdot R_{ADD}}{V_{OUT} \cdot (V_{IN} - V_{OUT})} + T_{DEL}1 \cdot \frac{V_{IN}}{V_{OUT}} + TDEL2 \cdot \frac{V_{IN}}{V_{IN} - V_{OUT}} \qquad (21)$$

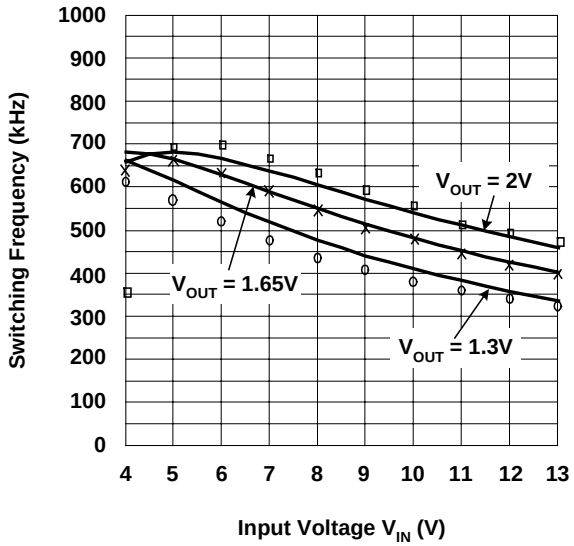
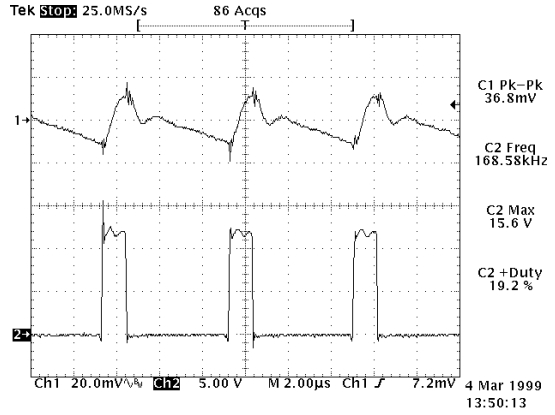


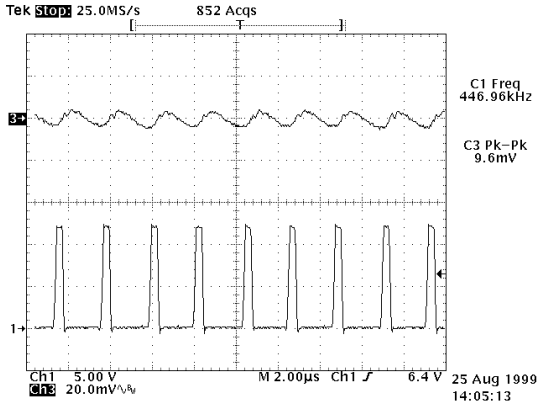
Fig. 28. Theoretical (solid) and measured (points) switching frequency.

In some electronic systems, switching frequency is important, if dc-to-dc converters have an externally synchronized switching frequency for parallel operation, interleaving, or avoiding a frequency range unacceptable to the system. Because the switching frequency of the modified hysteretic controller does not depend on the output-filter characteristics and has much lower variation, the dc-to-dc converters can be synchronized as it is shown in Fig. 27b. An external synchronization signal is applied to the input of a hysteretic comparator in this circuitry.

Fig. 29 shows the output-voltage ripple and the power-switches midpoint waveforms of the same dc-to-dc converter using a regular and modified hysteretic controller. The converter using the regular hysteretic controller (TPS5210 in this case) is optimized for low power losses and high efficiency and operates at 168 kHz, while the same converter using the modified hysteretic controller (TPS5211) operates at 450 kHz. While the hysteresis window has been set at the same level (20 mV for both controllers), the peak-to-peak output ripple is 36.8 mV for the TPS5210 and only 9.6 mV for the TPS5211. This example shows that the output ripple for a modified converter using the TPS5211 can be significantly lower than the hysteresis window.



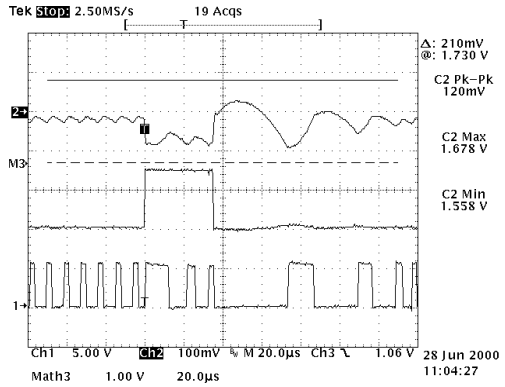
(a)



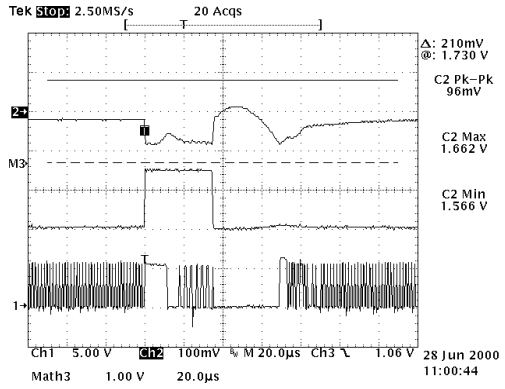
(b)

Fig. 29. Output voltage ripple and power switches midpoint waveforms of the same converter using the TPS5210 controller (a) and the TPS5211 with an external R_{ADD}-C_{ADD} circuit (b).

The waveforms shown in Fig. 30 illustrate the transient responses on 25-A load-current steps in accordance with Intel's VRM 8.4 requirements. The cursors show the limits for this test. Both tests are fulfilled on the same EVM with TPS5211 controller, except that the waveforms in Fig. 30a are shown for a regulator without a R_{ADD}–C_{ADD} circuit, while the additional circuit R_{ADD}–C_{ADD} has been added to increase the switching frequency in Fig. 30b. In both cases the peak-to-peak output voltage transient is well within the limits. It is 120 mV without (Fig. 30a) and 96 mV with R_{ADD} - C_{ADD} circuit (Fig. 30b). It is different because at a lower switching frequency the regulator has a higher ripple of the output voltage and a higher inductor current. In both cases the active droop compensation technique is used to reduce the number of output bulk capacitors.



(a) without R_{ADD} - C_{ADD} circuit



(b) with R_{ADD} - C_{ADD} circuit

Fig. 30. Output voltage transient response waveforms on 25-A load-current step with 30-A/µS slew-rate. [Ch.1: Drain-source voltage {5 V/div.}, Ch.2: Output voltage {100 mV/div.}, M.3: Load current {16 A/div.}].

D. Pros and Cons of the Hysteretic Control

Hysteretic controllers have excellent load-current transient-response characteristics compared to the other types of controllers (such as PWM voltage and current mode) with slow feedback loops. The controllers react on transients within the same cycle in which the transient occurs and keep the corresponding FET in on-state until the output voltage returns to the required dc level. Thus a minimum number of bulk output capacitors are required, saving total system cost.

The hysteretic control does not have a compensation circuitry that requires an accurate design in the whole input-voltage, output-voltage, temperature, and load-current range. The compensation can be complicated if the additional capacitors are added to the output of a voltage regulator around the microprocessor package.

The main problem of the hysteretic control relates to a predictable switching-frequency estimation and its dependence on the output-filter characteristics and the operation conditions. The switching frequency analysis in this topic addresses that issue. An alternative solution to the generic hysteretic control is the modified hysteretic control analyzed in this topic. In this case the switching frequency does not depend on the output-filter characteristics and can be fixed.

IX. Design Procedure and Example

The following step-by-step design procedure shows how to select the output capacitors, an inductor value, and a switching frequency that are best for a specific application. The typical dc-to-dc converter requirements for powering a notebook microprocessor are used as an example:

- V_{IN} = from 4.5 V up to 24 V
- V_{OUT} = 1.6 V
- $\Delta V_{OUT(dc)} = \pm 50$ mV
- $\Delta V_{OUT(ac)} = \pm 120$ mV
- $I_{O(max)} = 14.2$ A
- $I_{O(min)} = 0.3$ A
- $\Delta I_O = 13.9$ A
- $vI_O = 30$ A/µs
- $R_B = 0.4$ mΩ
- $L_B = 0.2$ nH

A. Definition of the Worst-Case Transient

The type of transient (load-current step-up or step-down) most important to optimize is selected. The transient caused by the load-current transition is complete when the inductor current reached the new steady-state current level. The inductor-current slew rate depends on the voltage applied to the inductor. This voltage is equal to V_{IN} - V_{OUT} during a load-current step-up, or to V_{OUT} during a load-current step-down. For most microprocessor and DSP applications, usually (V_{IN} - V_{OUT}) > V_{OUT} is applicable. This relationship means that the worst case is defined by the load-current step-down transition, because the lower voltage, V_{OUT}, lowers the inductor-current slew rate. In such a case the load-current step-down must be optimized first; then, after the output filter selection, the load-current step-up

transient must be verified to meet the requirements.

B. Maximum Peak-to-Peak Dynamic Tolerance

The accurate output voltage budget is estimated to determine the maximum dynamic output-voltage tolerance ΔV_{REQ}. The dynamic and static supply-voltage limits are compared with all potential tolerances, including set-point accuracy, time and temperature variation, and line-and-load regulation. Use the droop compensation and adjust the nominal output voltage to get the maximum possible ΔV_{REQ}.

Fig. 31 shows the output voltage budget calculation for this particular example. For the step-down transient, the required window is:

ΔV_{REQ} = 1,720 mV – 1,550 mV – 2 mV – 2·6 mV – 50 mV = 106 mV

For the step-up transient, it is:

ΔV_{REQ} = 1,650 mV – 1,480 mV – 2 mV – 2·6 mV – 50 mV = 106 mV

The required droop compensation is:

D_{ROOP} = 106 mV – 16 mV – (1,550 mV – 1,480 mV – 2 mV) = 22 mV

C. Output Bulk Capacitor and Inductor Selection

Equations 1 and 2 are used to build the optimization curves to show the required number of output bulk capacitors, N1 and N2. The 100-µF specialty polymer capacitor is selected for this design. It has ESR = 20 mΩ and ESL = 3.2 nH. The optimization curves N1 (dashed) and N2 (solid) as a function of the output inductance L_O and switching frequency f_S are shown in Fig. 32. The switching frequency 200 kHz is selected on the basis of the higher efficiency, although it requires 9 capacitors in comparison with only 7 of them at 300 kHz. The optimal value for the output inductor is around 0.6 µH.

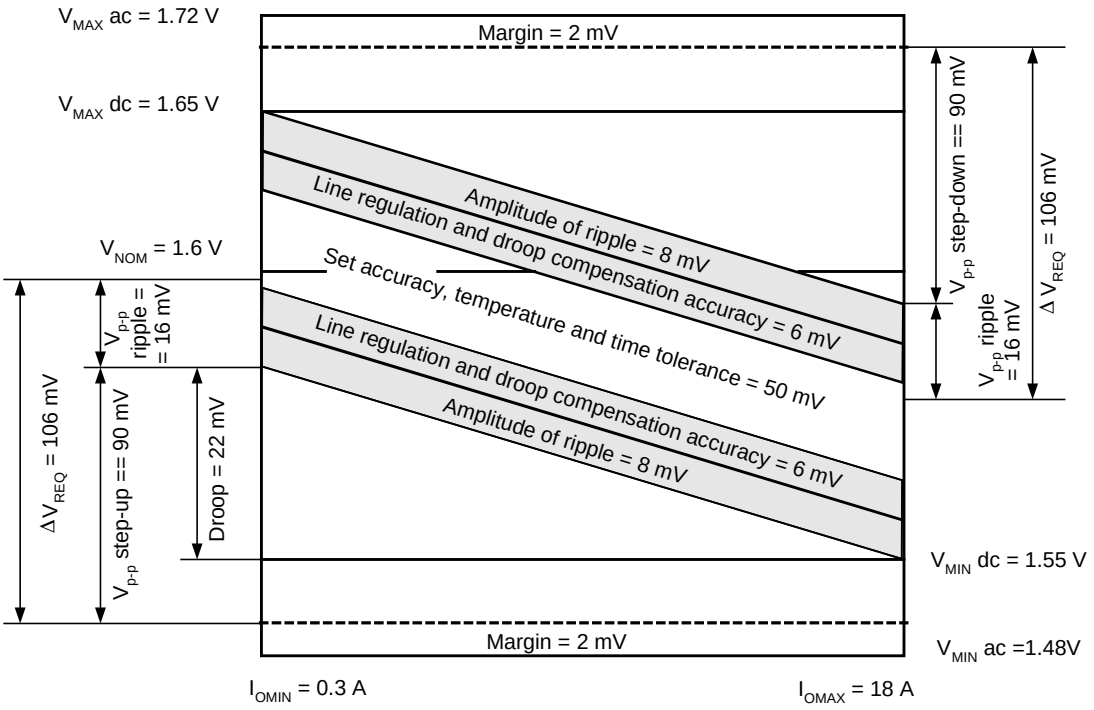


Fig. 31. Output voltage budget for notebook power supply (not scaled).

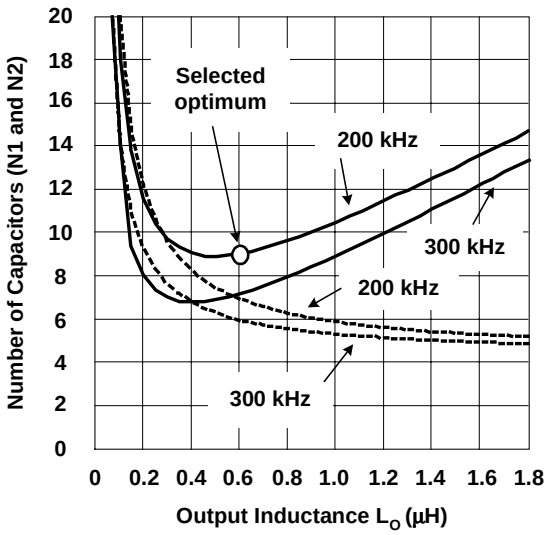


Fig. 32. Optimization curves N1 (dashed) and N2 (solid) as a function of output inductance L_O and switching frequency f_S.

D. Controller Selection

The modified hysteretic controller TPS5300 from Texas Instruments that is designed for the notebook dc-to-dc converters has been selected for this application. This controller implements SpeedStep™ technology for Intel's mobile Pentium III microprocessors. The functional block diagram of this controller is shown in Fig. 33. Below are its main features:

- A fast hysteresis comparator reacts to transient in 400-500 ns and does not have any restrictions on the duty cycle, thereby reducing the number of output bulk capacitors.
- The hysteretic control does not need feedback-loop compensation circuitry.
- External resistors set the hysteresis window as a percentage of the reference voltage.
- The high-bandwidth current sense amplifier enables the accurate overcurrent protection and active droop compensation.
- Internal 2-A gate drivers with bootstrap diode control the dead-time of power FETs to minimize power losses;
- Two linear regulator controllers provide additional 2.5-V CLK and 1.5-V I/O voltages.
- An adjustable, dynamic-VID code-change allows implementation of SpeedStep™ and PowerNow™ power-saving technologies.
- The additional features include the 5-bit VID code, VR_ON signal input, VGATE signal, OVP, UVLO and UVP protection.
- The soft-start circuitry brings the all voltages up at the same time.

E. Transient Waveforms

The excellent dynamic characteristics of hysteretic control are illustrated in Figs. 34 and 35.

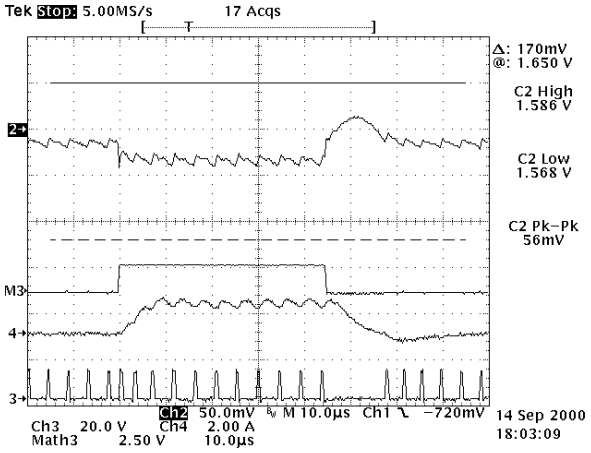


Fig. 34. The output voltage transient response (Ch.2) at V_{IN} = 12 V. The load current (M3) has 10-A step with slew rate of 30 A/µs. Ch. 4 - input current, Ch.3 - drain-source voltage of low-side FET

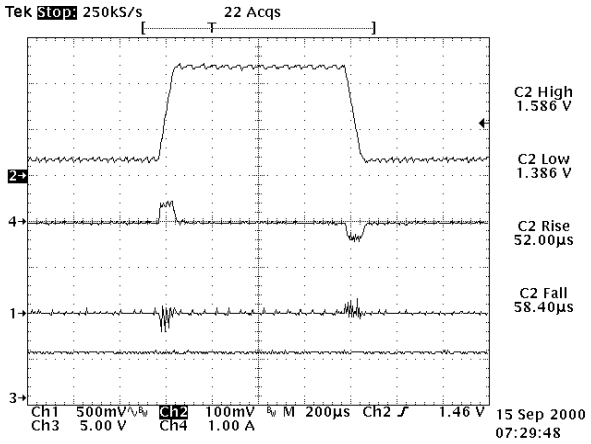


Fig. 35. The dynamic VID-code change waveforms from 1.35 V to 1.6 V and back at V_{IN} = 4.5 V and I_{OUT} = 10 A. Ch.2 - output voltage, Ch.4 input current, Ch.1- input voltage ripple, Ch. 3 - VGATE signal

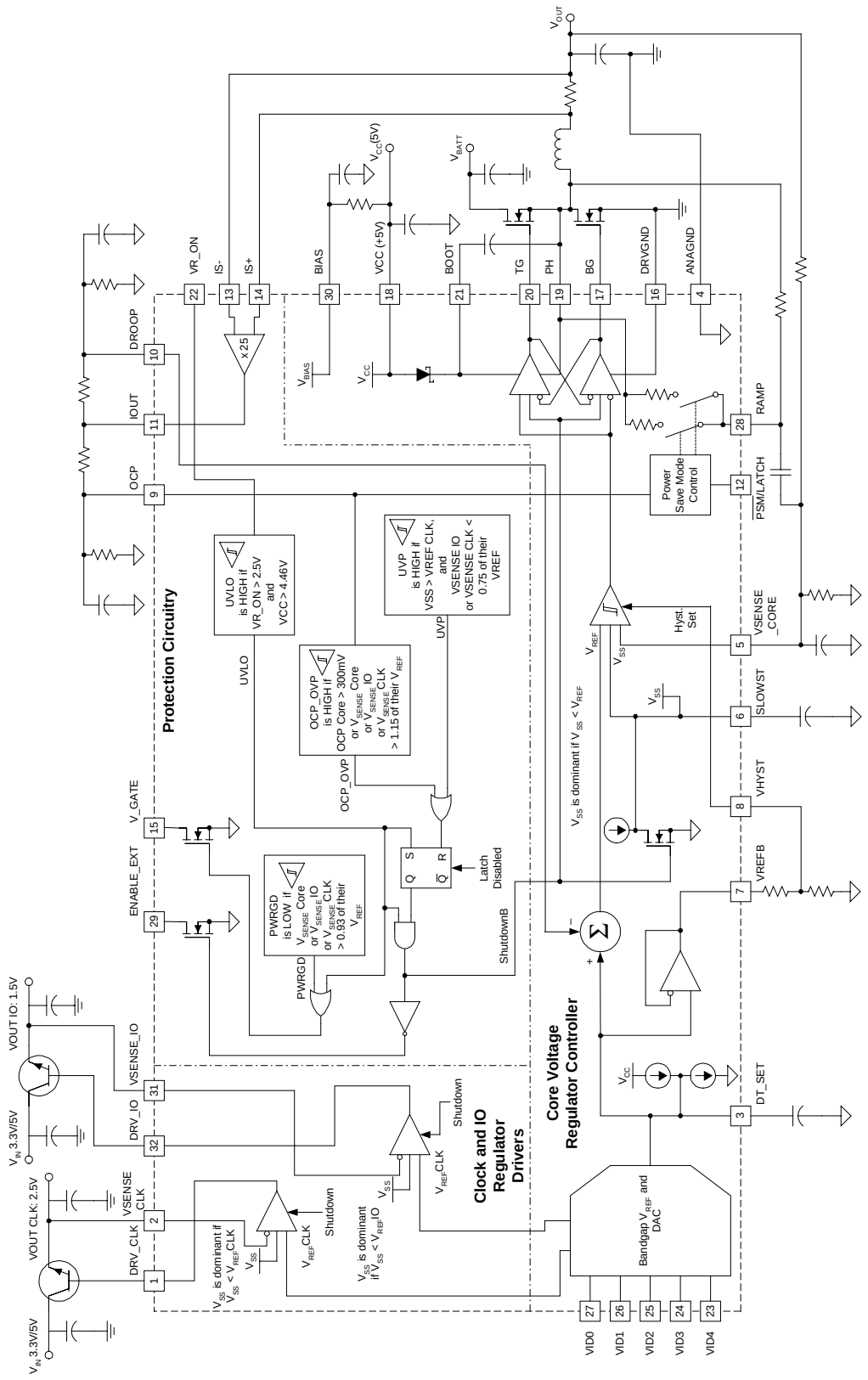


Fig. 33. The functional block diagram of modified hysteretic controller TPS5300 for notebook applications.

X. SUMMARY

The introduction of this topic discusses powering of modern low supply-voltage and high slew-rate transient loads (such as microprocessors, DSPs, and memory chips) and related problems.

The load-current transient analysis of one-phase, interleaved dc-to-dc buck converters with the ideal controller includes model selection, a description of an analysis approach, and confirmation of derived analytical equations by test results.

The optimization section discusses the best and worst conditions for the transients, which are not mentioned in previous literature. Those conditions depend on the instant when the load-current transition occurs relative to the switching cycle of a converter. This section discusses effects of the analyzed model parameters (including output-capacitor and supply-path parasitics and output-filter characteristics) and derives equations to determine the required number of bulk capacitors.

The proper control approach is important to meet tight static and dynamic tolerance requirements and decrease the number of expensive bulk capacitors for filtering. A review of different control solutions for the fast transient response dc-to-dc converters is presented in the paper. On the basis of this review, the fastest and simplest hysteretic control is selected for further analysis.

Renewed switching-frequency analysis of the classic hysteretic controller, including component parasitics, is presented. The modified hysteretic control invariable to the output-filter characteristics is suggested and analyzed.

Finally, an optimization procedure for minimum cost and size design by using the hysteretic controller in a synchronous buck converter is suggested. Appendixes 1 and 2 show the main equations used in this topic.

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Appendix A

MAIN EQUATIONS FOR THE LOAD CURRENT TRANSIENT WAVEFORMS

The following is the list of descriptions used during the analysis:

- V_{IN} - input voltage (Fig. 1);
- V_{OUT} - output voltage at point vA (Fig. 1);
- $D = V_{OUT}/V_{IN}$ - duty cycle (Fig. 1);
- L_O - output inductor of dc-dc synchronous buck converter (Fig. 1);
- C_O - ideal capacitance of output capacitor (Fig. 1);
- ESR - equivalent series resistance of output capacitor (Fig. 1);
- ESL - equivalent series inductance of output capacitor (Fig. 1);
- R_B - parasitic resistance of supply path (Fig. 1);
- L_B - parasitic inductance of supply path (Fig. 1);
- $I_{O(min)}$ - minimum output current during transient (Fig. 2a);
- $I_{O(max)}$ - maximum output current during transient (Fig. 2a);
- $\Delta I_O = (I_{O(max)} - I_{O(min)})$ - output current step during transient;
- T_O - output current transition duration (Fig. 2a);
- $vI_O = \Delta I_O/T_O$ - output current slew-rate;
- T_S - switching period;
- V_M1 - peak-to-peak transient voltage (Figs. 2c, 4) at point vB (Fig. 1) at the end of output current transition;
- V_M2 - peak-to-peak transient voltage (Figs. 2c, 4) at point vB (Fig. 1) inside T_{RECOV} interval;
- V_ML - peak to peak transient voltage because of ESL and L_B (Fig. 2d) at point vB (Fig. 1) at the end of output current transition;
- V_MR - peak to peak transient voltage because of ESR and R_B (Fig. 2e) at point B (Fig. 1) at the end of output current transition;
- V_MC - peak to peak transient voltage at C_O (Fig. 2f) at the end of output current transition;
- T_{RECOV} - time duration when the output voltage at point vA (Fig. 1) returns to its initial value after transient (Fig. 2c);
- T_{EXTR} - time duration (starting from the instant when the load-current transition occurs) when the voltage at point vB (Fig. 1) reaches the extreme V_M2 (Fig. 2c).

$$\Delta IL = \frac{V_{OUT} \cdot (1 - D) \cdot T_S}{L_O} \quad (1)$$

$$V_M1 = V_ML + V_MR + V_MC \quad (2)$$

$$V_M2 = V_M2R + V_M2C \quad (3)$$

$$V_ML = \frac{\Delta I_O}{T_O} \cdot (ESL + L_B) \quad (4)$$

Equations 5-9 describe the worst-case output current step-down transient (transition occurs at the end of upper FET conduction period)

$$V_M C = \frac{(\Delta IL + \Delta I_O)\cdot T_O}{2\cdot C_O} - \frac{\Delta IL\cdot {T_O}^2}{2\cdot C_O\cdot(1-D)\cdot T_S} \quad (6)$$

$$T_{EXTR} = (1-D)\cdot T_S\left(\frac{1}{2}+\frac{\Delta I_O}{\Delta IL}\right) - ESR\cdot C_O \quad (7)$$

Equations 10-14 describe the worst-case output current step-up transient (transition occurs at the end of switching cycle)

$$V_M R = \left(\Delta I_O + \Delta IL - \frac{\Delta IL\cdot T_O}{D\cdot T_S}\right)\cdot ESR + \Delta I_O\cdot R_B \quad (10)$$

$$V_M C = \frac{(\Delta IL + \Delta I_O)\cdot T_O}{2\cdot C_O} - \frac{\Delta IL\cdot {T_O}^2}{2\cdot C_O\cdot D\cdot T_S} \quad (11)$$

$$T_{EXTR} = D\cdot T_S\cdot\left(\frac{1}{2}+\frac{\Delta I_O}{\Delta IL}\right) - ESR\cdot C_O \quad (12)$$

$$V_M R = \left[\Delta I_O + \Delta IL - \frac{\Delta IL\cdot T_O}{(1-D)\cdot T_S}\right]\cdot ESR + \Delta I_O\cdot R_B \quad (5)$$

$$V_M 2R = ESR\cdot\left[\Delta I_O + \Delta IL - \frac{\Delta IL}{(1-D)\cdot T_S}\cdot T_O - \frac{\Delta IL}{(1-D)\cdot T_S}\cdot(T_{EXTR}-T_O)\right] + R_B\cdot\Delta I_O \quad (8)$$

$$V_M 2C = \frac{1}{C_O}\cdot\left[\begin{array}{l}\dfrac{\Delta IL\cdot T_O}{2}+\left[\dfrac{\Delta I_O}{T_O}-\dfrac{\Delta IL}{(1-D)T_S}\right]\cdot\dfrac{{T_O}^2}{2}+\left[\Delta I_O+\dfrac{\Delta IL}{2}-\dfrac{\Delta IL}{(1-D)\cdot T_S}\cdot T_O\right] \\ \cdot(T_{EXTR}-T_O)-\dfrac{\Delta IL}{(1-D)\cdot T_S}\cdot\dfrac{(T_{EXTR}-T_O)^2}{2}\end{array}\right] \quad (9)$$

$$V_M 2R = ESR\cdot\left[\Delta I_O + \Delta IL - \frac{\Delta IL}{D\cdot T_S}\cdot T_O - \frac{\Delta IL}{D\cdot T_S}\cdot(T_{EXTR}-T_O)\right] + R_B\cdot\Delta I_O \quad (13)$$

$$V_M 2C = \frac{1}{C_O}\cdot\left[\begin{array}{l}\dfrac{\Delta IL\cdot T_O}{2}+\left(\dfrac{\Delta I_O}{T_O}-\dfrac{\Delta IL}{D\cdot T_S}\right)\cdot\dfrac{{T_O}^2}{2}+\left(\Delta I_O+\dfrac{\Delta IL}{2}-\dfrac{\Delta IL}{D\cdot T_S}\cdot T_O\right)\cdot(T_{EXTR}-T_O) \\ -\dfrac{\Delta IL}{D\cdot T_S}\cdot\dfrac{(T_{EXTR}-T_O)^2}{2}\end{array}\right] \quad (14)$$

Appendix B

DERIVATION OF THE EQUATION FOR THE SWITCHING FREQUENCY

The following equation can be written in accordance with Fig. 22 (e):

$$Hyst = \Delta v_{ESL} + v_{ESR}(D \cdot T_S - t_{DEL}) - v_{ESR}(0) + v_C(D \cdot T_S - t_{DEL}) - \ldots$$
$$\ldots - (v_{ESR}(D \cdot T_S) + v_{ESR}((1-D) \cdot T_S - t_{DEL}) + v_C((1-D) \cdot T_S - t_{DEL}))$$

Substituting:

$$\Delta V_{ESL} = \frac{V_{IN} \cdot ESL}{L};$$

$$V_{ESR}(D \cdot T_S - t_{DEL}) - V_{ESR}(0) = \frac{\Delta I \cdot ESR \cdot (D \cdot T_S - t_{DEL})}{D \cdot T_S};$$

$$V_C(D \cdot T_S - t_{DEL}) = \frac{\Delta I}{2 \cdot C_O} \cdot \left(\frac{(D \cdot T_S - t_{DEL})^2}{D \cdot Ts} - (D \cdot T_S - t_{DEL}) \right);$$

$$V_{ESR}(D \cdot T_S) + V_{ESR}((1-D) \cdot T_S - t_{DEL}) = \frac{\Delta I \cdot ESR \cdot t_{DEL}}{(1-D) \cdot T_S},$$

$$V_C((1-D) \cdot T_S - t_{DEL}) = \frac{\Delta I}{2 \cdot C_O} \cdot \left(((1-D) \cdot T_S - t_{DEL}) - \frac{((1-D) \cdot T_S - t_{DEL})^2}{(1-D) \cdot T_S} \right)$$

and removing relatively small magnitude $t_{DEL}{}^2$, yields:

$$Hyst = \frac{V_{IN} \cdot ESL}{L} - \frac{\Delta I \cdot ESR \cdot t_{DEL}}{T_S \cdot D \cdot (1-D)} + \Delta I \cdot ESR - \frac{\Delta I \cdot t_{DEL}}{C_O}$$

After substituting:

$$\Delta I = \frac{V_{IN} - I_O \cdot (R_{DS(on)} + R_L) - V_{OUT}}{L} \cdot D \cdot T_S$$

and,

$$D = \frac{V_{OUT} + I_O \cdot (R_{DS(on)} + R_L)}{V_{IN}}$$

the following equation for the switching period can be derived:

$$T_S = \frac{V_{IN} \cdot (V_{IN} \cdot ESR \cdot t_{DEL} + Hyst \cdot L - V_{IN} \cdot ESL)}{(V_{IN} - I_O \cdot (R_{DS(on)} + R_L) - V_{OUT}) \cdot (V_{OUT} + I_O \cdot (R_{DS(on)} + R_L)) \cdot (ESR - t_{DEL} / C_O)}$$

For no load condition and for preliminary frequency prediction simplified equation might be used if to substitute:

$R_{DS(on)} + R_L = 0$ and $f_S = 1/T_S$.

This equation is:

$$f_S = \frac{V_{OUT} \cdot (V_{IN} - V_{OUT}) \cdot (ESR - t_{DEL} / C_O)}{V_{IN} \cdot (V_{IN} \cdot ESR \cdot t_{DEL} + Hyst \cdot L - ESL \cdot V_{IN})}$$

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Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265