Internal Compensation – Boon or Bane?

By Brian Shaffer

ABSTRACT

With the ever-increasing desire to reduce the complexity of DC/DC converters, designers are being encouraged to work with features that are being integrated within the control ICs. One such feature is the loop compensation circuitry, but with its inclusion in the controller, the power processing components now take on the dual role of both delivering input energy to the output load, and ensuring overall stability. Since this can occasionally present conflicts, knowledge of the limitations as well as the advantages of various internal compensation techniques is important to the user. In general, the use of internally compensated controllers is desirable in order to minimize design cycle time and board area.

I. INTRODUCTION

The control components of a DC/DC converter can be selected in a variety of methods. Some designers opt for the empirical approach; others take a more theoretical method. Whichever method is used, it must be included in the design cycle time. As a result, many IC manufacturers have included the compensation components within the control IC to speed up the design process. The inclusion of the compensation components within the control IC offers both advantages and disadvantages. This paper compares two internal voltage mode compensation techniques to the conventional external voltage-mode compensation technique. Voltage mode control seems to be the control method of choice for simple point-of-load DC/DC converters. With voltage mode control, the circuit implementation is simplified because no inductor current information is required and the efficiency is improved for the same reason. A listing of the three control techniques follows:

- Voltage mode with external poles and zeros
- Voltage mode with internal poles and zeros
- Voltage mode with internal gain limited error amplifier

Voltage mode with external poles and zeros is the most flexible, but requires the most amount of effort and skill to accomplish. *Voltage mode with internal poles and zeros* is less effort intensive, but also less flexible. *Voltage mode with gain limited error amplifier (E/A),* requires limited effort, and has limited flexibility, but can quite often get the job done well. Depending on the application and the design requirements, more than one of these methods may satisfy the design goals. It is up to the designer to select the most effective control method that meets the project's objectives. Obviously, satisfying the requirements with a controller from the third class of devices, yields the simplest solution in the least amount of time. The control methods listed can be applied to various converter topologies. For this paper the synchronous buck topology is presented as it is the topology of choice for the latest low voltage power hungry DSPs and micro-controllers.

II. TOPOLOGY OVERVIEW

The buck topology is a very well understood topology and the synchronous variant has the same AC and DC transfer functions as the continuous conduction mode, (CCM) model. Although the conventional buck topology has a discontinuous conduction mode of operation, the synchronous variant does not because of the bi-directional characteristic of the synchronous switch.

Fig. 1 shows the simplified schematic of a buck converter including the relevant parasitics. The control-to-output transfer function, Gpt(s)=Vo(t)/d(t), for the small-signal linearized model, is shown in equation (1).[1]

In order to discuss the advantages and disadvantages of each of the control topologies,

the open-loop transfer function is completed by determining the modulator gain and the compensator transfer function. The product of all three results in the complete open-loop transfer function.

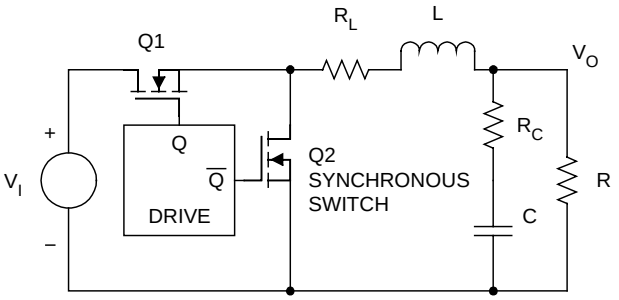

Fig. 1. Buck converter.

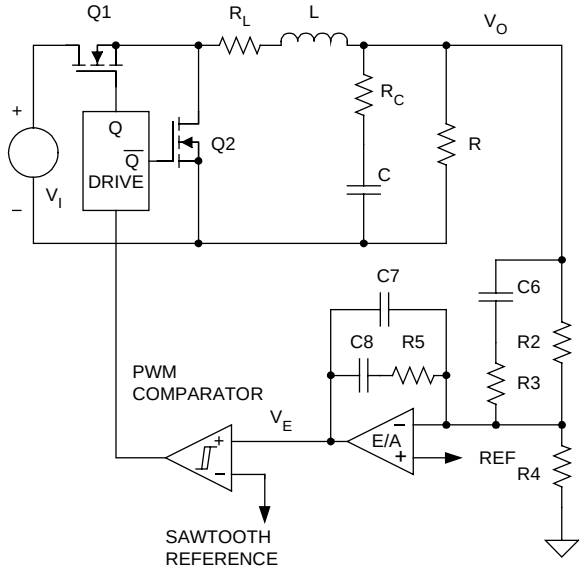

Fig. 2. Voltage-mode control implementation for synchronous buck converter with external pole-zero compensation.

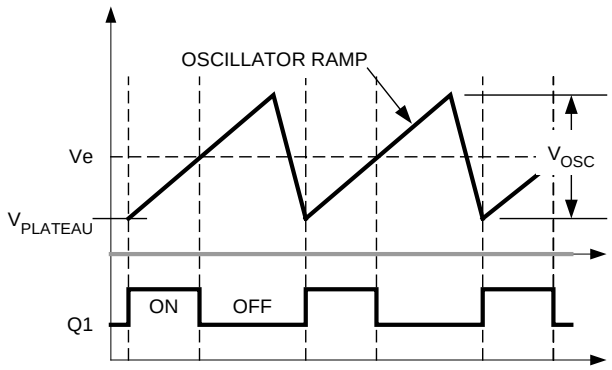

Fig. 3. Diagram of modulator operation.

Referring to Fig. 2 and 3, the modulator gain is determined by examining the operation of the PWM comparator, which generates the duty-cycle based on the error signal received from the E/A and the sawtooth waveform from the oscillator.

Fig. 3 shows that the modulator gain, Gmod(s) which is equal to d(t)/Ve(t), is given by $1/V_{OSC}$; where V_{OSC} is the peak-to-peak variation of the ramp signal. In voltage mode control the amplitude of the ramp signal is constant with operating point, which yields a constant modulator gain over all operating conditions.

The remaining portion of the open-loop transfer function is the compensator which is also called the error amplifier (E/A). This portion of the loop is presented in more detail for each of the compensation methods discussed.

$$G_{pt}(s) = Vin \cdot \left(\frac{R}{R + R_L}\right) \cdot \left[\frac{1 + R_C \cdot C}{1 + s \cdot \left[C \cdot \left(R_C + \frac{R \cdot R_L}{R + R_L}\right) + \frac{L}{R + R_L}\right] + s^2 \cdot L \cdot C \cdot \frac{R + R_C}{R + R_L}}\right] \quad (1)$$

III. CONTROL TECHNIQUES

A. Voltage Mode Control with External Poles and Zeros

In this method, the most control over the shape of the open-loop gain is obtained. The generic form of the Compensator is shown in Fig. 4.

The exact transfer function Hea(s) is shown in equation (2).

If the assumption is made that R2>>R3 and C8>>C7, then the exact transfer function can be simplified into equation (3).

Using the approximate solution yields a simple method for selecting the compensation components. The following method is described for a TPS54621 control IC from Texas Instruments, although the procedure would apply to most control ICs for buck-derived topologies, which utilize voltage mode control.

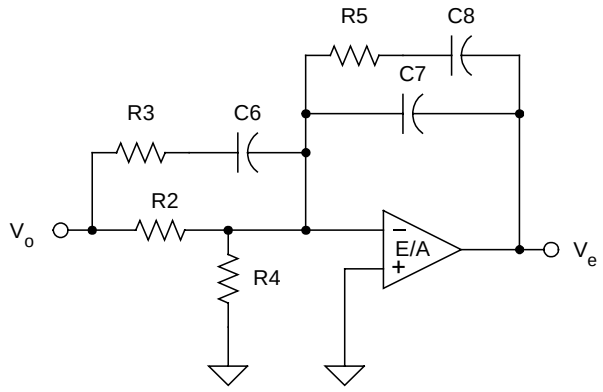

Fig. 4. Compensator for voltage mode control with external poles and zeros.

The following procedure [B] sets the crossover frequency, *fco*, to approximately 50kHz. If a lower crossover frequency were desired, the LC product of the output filter components would be increased, in order to decrease the break frequency of the output filter. The converse is also true. If a higher crossover frequency is desired, for improved transient response, then the LC product of the output filter could be reduced. The reasoning behind this first constraint is that it is desirable to limit the output filter break frequency to less than one tenth of the crossover frequency. By adhering to this constraint when selecting the output filter components, the phase shift of the output filter is compensated by the proper placement of the zeros in the compensation network.

B. Procedure for Selecting the External Compensation Components

1. Select output inductor, L, and output capacitor, C.

- $L > 5\mu H$
- $C > 220\mu F$

$$R_C < \frac{\Delta V_{p\_p} \cdot V_{in\_min} \cdot L \cdot f_S}{\left(V_{in\_min} - V_{OUT}\right) \cdot V_{OUT}}$$

- $R_C < 0.5\ \Omega$

  where ΔV_{p_p} = maximum allowable output voltage ripple.

2. Set R2 and R4 based on the desired output voltage. If the output voltage is 0.9V, R4 should be left open.

$R2 = 10k\Omega$

$$R4 = 10k\Omega \cdot \frac{V_{REF}}{V_{OUT} - V_{REF}}$$

$$H_{ea}(s) = \left(\frac{1}{s \cdot R2 \cdot (C8 + C7)}\right) \cdot \frac{(1 + s \cdot R5 \cdot C8) \cdot [1 + s \cdot C6 \cdot (R2 + R3)]}{\left[1 + s \cdot R5 \cdot \left(\frac{C8 \cdot C7}{C8 + C7}\right)\right] \cdot (1 + s \cdot R3 \cdot C6)} \tag{2}$$

$$H_{ea}(s) = \left(\frac{1}{s \cdot R2 \cdot (C8)}\right) \cdot \left[\frac{(1 + s \cdot R5 \cdot C8) \cdot (1 + s \cdot C6 \cdot R2)}{(1 + s \cdot R5 \cdot C7) \cdot (1 + s \cdot R3 \cdot C6)}\right] \tag{3}$$

3. Set the zero of C6 and R2 to approximately one-half a decade below the LC double pole to compensate for the phase loss.

$$C6 = \frac{\sqrt{L \cdot C}}{5000}$$

4. Set the pole of R3 and C6 to cancel the zero of the output capacitor and its R_C.

$$R3 = \frac{C \cdot R_C}{C6} = 5k\Omega \cdot \sqrt{C/L} \cdot R_C$$

5. Set C8 to determine the crossover frequency. Assume $R_C >> R_L$ and the component limits specified in Step 1.

$$C8 = 32nF \cdot \left(\frac{V_{IN}}{5V}\right) \cdot \left(\frac{50{,}000}{fco}\right) \cdot \left(1 + \frac{R3}{10k\Omega}\right)$$

6. Set the zero formed by R5 and C8 a decade below the LC double pole to avoid a conditional instability.

$$R5 = \frac{10 \cdot \sqrt{L \cdot C}}{C8} = \frac{C6}{C8} \cdot 50k\Omega$$

7. Set the pole formed by C7 and R5 a decade above the crossover frequency to boost the gain margin.

$$C7 = \frac{1}{2 \cdot \pi \cdot 10 \cdot f_{CO} \cdot R5} = \frac{0.32\mu F}{R5}$$

As can be seen from the above procedure, much consideration needs to be given to the selection of the compensation components. But, the benefits of external compensation are necessary in many high performance designs.

Another reason to consider this control scheme is the desire to have the lowest possible output ripple voltage and optimal transient response. In a fixed frequency converter, the output ripple voltage is predominantly a function of the equivalent series resistance of the output capacitor, R_C, and the value of the output inductor, L. For a given set of specifications, (input voltage, switching frequency, and output voltage), the size of the output inductor determines the amount of inductor ripple current. The amount of inductor ripple current is inversely proportional to the value of inductance. For this reason, it is desirable to have a very large amount of output inductance, but by doing so, the transient response is inhibited.

In the event of a large signal disturbance, a major factor in determining how fast the supply can respond is the slew rate of the output inductor, which is directly related to the value of output inductance. Hence, having a small value of output inductance is desirable for optimal transient response. Thus, there are two performance specifications that drive the value of output inductance in opposite directions. Ideally, a small value of output inductance is selected and reducing the equivalent series resistance of the output capacitor compensates for the increased ripple current. With this control method, more often than not, a stable solution can be found by varying the external compensation components. In the following two methods, restrictions imposed by the control ICs limits the ability to vary the output filter components. Although, in most practical cases, the restrictions imposed by the control ICs are not so restrictive as to preclude finding a viable solution.

In summary, the advantages of externally compensated control ICs include, 1) nearly unrestricted selection of power processing components, 2) possible improvement in output ripple voltage performance, 3) good line and load regulation, and 4) improved control over transient response. The disadvantages can be summarized as: 1) complexity of compensator design, 2) increased component count, 3) small increase in board area, 4) longer design cycle time.

B. Voltage Mode Control with Internal poles and Zeros

In this configuration, the error amplifier (E/A) output is typically not accessible from the outside of the IC, which means that the designer has no ability to shape the open-loop transfer function except with the proper selection of the power components. Fig. 5 shows one implementation of this control method used in the LM2673 control IC[2] from National Semiconductor Corp. The exact values of the internal poles and zeros vary because the inductor and capacitor values shown are not

constant. National Semiconductor Corp. has a patented approach to actively modify their values during operation. Typically this method results in lower bandwidth or reduced transient performance because the IC manufacturer has aprioristically decided upon the compensation components. This inevitably means that the manufacturer needed to be conservative in their assumptions in order to guarantee stability over the widest possible operating range.

With this method, no consideration needs to be given to the selection of the compensation components. The power processing components now take on the dual role of both delivering input energy to the output load, and ensuring overall stability. If the output inductor, the output capacitor and the output capacitor's equivalent series resistance is not selected properly, then the resultant poles and zeros will not produce a stable system when combined with the internally generated poles and zeros of the control IC. This new stability consideration can occasionally present a conflict with the design requirement of minimal output ripple and fast transient response. Another issue that may arise when using a controller with this configuration is that the manufacturer may not provide detailed characterization of the internally compensated E/A. The result is that designers are not able to perform theoretical stability analysis of the control loop for alternative power components. The designer is then restricted to empirical verification of loop stability for alternative power components or using the values suggested by the manufacturer. Although the designer may be somewhat limited, this method can produce acceptable results for less stringent requirements.

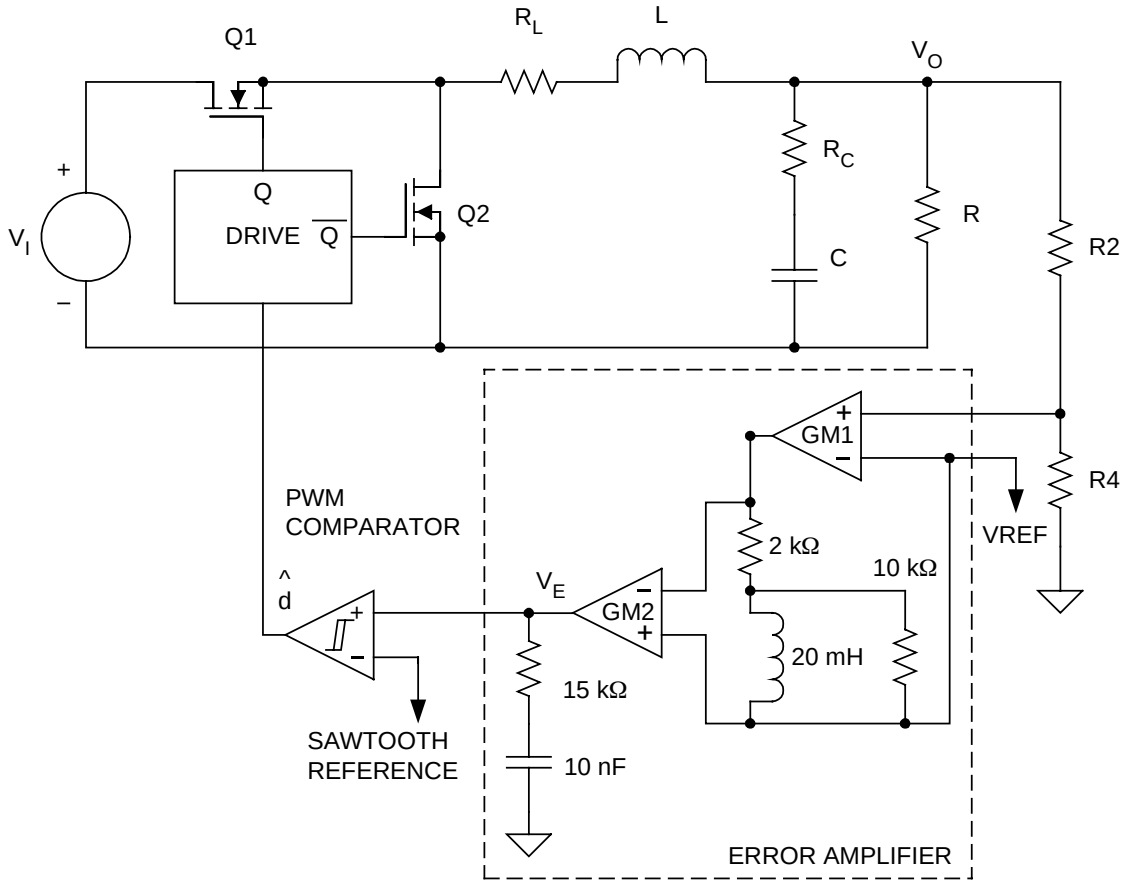

Fig. 5. Voltage-mode control implementation for synchronous buck converter with internal pole-zero compensation.

One important advantage of this compensation method is the presence of an internal integrator pole. By maintaining an integrator pole in the feedback path, the power supply has desirable regulation performance provided that the open-loop gain of the E/A is high. In Fig. 5, the gain blocks GM1 and GM2 are transconductance amplifiers. Their transfer functions are a function of their load impedance. For a transconductance amplifier the output voltage is equal to $V_{OF} \cdot G_m \cdot R_O$, where V_{OF} is equal to the differential input voltage across the amplifiers input terminals. G_m is the transconductance of the amplifier and R_O is the load impedance, which is typically a function of frequency. In this implementation the 10nF capacitor on the output of the second amplifier performs the integration function, by accumulating the charge associated with a DC signal.

In summary, the advantages of this method include, 1) simplified compensation design, 2) reduced component count, 3) shorter design cycle time, 4) reduced board area, and 5) good line and load regulation performance (internal integrator pole). The disadvantages of this method consist of, 1) non-optimized transient response, 2) restricted power train component selection, and 3) increased output ripple (Rc lower limit).

C. Voltage Mode with Internal Gain Limited Error Amplifier

In this third control technique, the open-loop gain of the internal error amplifier is limited to a preset value, for example 20 V/V, over a wide signal frequency range. Fig. 6 shows a typical implementation of gain-limited compensation. One such control IC that utilizes gain-limited compensation is the TPS54611 from Texas Instruments. The Bode plot for the E/A within the TPS54611 control IC is shown in Fig. 7. The plot shows that the E/A gain is approximately constant from DC to 150kHz; at which point the E/A has an internal pole reducing its susceptibility to switching noise. Because the E/A is gain limited all the way down to DC, the DC regulation of a circuit using this control technique is not as good as one that utilizes a method that increases gain for decreasing frequency. In the previous two methods the DC gain is limited only by the open-loop gain of the E/A, approximately 80dB.

One dominant term in determining the line regulation performance of a power supply, aside from the line regulation of its precision reference, is the DC gain of the E/A. The lack of which introduces an offset error at the input of

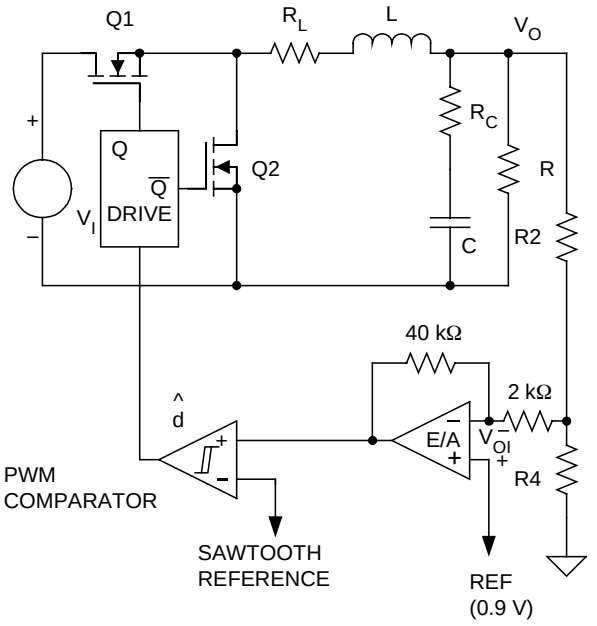

Fig. 6. Voltage-mode control implementation for synchronous buck converter with gain-limited E/A compensation.

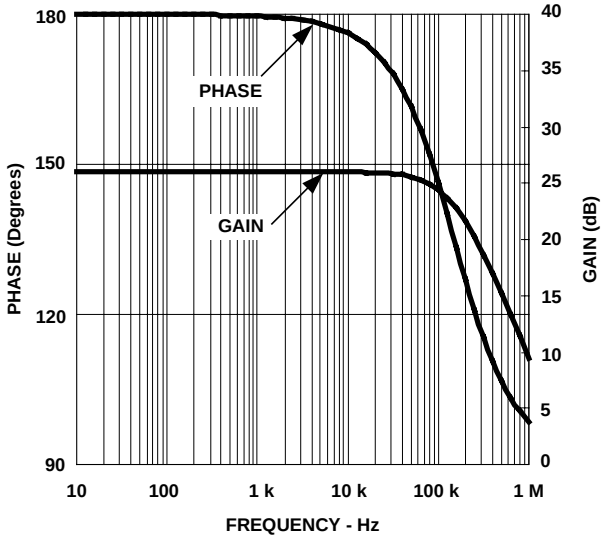

Fig. 7. TPS54611 Error amplifier gain and phase vs. frequency.

the E/A. Fig. 3 shows the operation of the modulator. In order for the E/A to control the duty-cycle over the entire input voltage range, the output of the E/A must vary around a nominal value. Consider an example where the nominal input voltage is 3.3V, the input voltage tolerance is ±10%, and the output voltage is 1.8 V. The plateau voltage is defined as 0.7 V, V_{OSC} is equal to 1 V peak-to-peak, and V_{REF} equal to 0.9 V. The E/A output, Ve_nom, has a nominal value of 1.2455 V.

$$V_{e\_nom} = V_{PLATEAU} + \frac{V_{OUT}}{V_{in\_nom}} \cdot V_{OSC}$$

The range over which the E/A output traverses as the input voltage varies from 2.97V to 3.63 V is 1.3061V to 1.1959V.

$$V_{e\_max} = V_{PLATEAU} + \frac{V_{OUT}}{V_{in\_min}} \cdot V_{OSC} = 1.3061$$

$$V_{e\_min} = V_{PLATEAU} + \frac{V_{OUT}}{V_{in\_max}} \cdot V_{OSC} = 1.1959$$

The E/A variation can be expressed in slightly a different way by only looking at the difference from the nominal value. In this way, it can be seen that the output of the E/A needs to vary by only +60.6mV and – 49.6mV around its nominal value. If a gain of 80dB is typical for the E/A, then the offset error introduced at its input terminals is only +6.1µV to –4.96µV.

$$V_{OFFSET} = \frac{\Delta V_e}{A_{ol}}$$

Since the reference is 0.9V, this induced offset error represents an error term of +0.000673% to -0.000551%. If the gain were only 26dB, then the induced offset error voltage would be increased to +3.03mV and –2.48mV, which represents an error of +0.337% and -0.276%. Thus, it can be seen that limiting the DC gain of the E/A adversely impacts the regulation performance of the power supply.

In most datasheets for internally compensated controllers, the IC manufacturer provides a graph showing the region of stability for the output capacitor's equivalent series resistance with a known output inductance and various amounts of output capacitance. One such chart is shown in Fig. 8. The x-axis lists various values of capacitance and the y-axis lists various amounts of equivalent series resistance. From this chart the proper amount of output capacitance and its equivalent series resistance can be selected that results in a stable design. The dashed line represents the minimum allowable equivalent series resistance that yields acceptable phase margin. The solid line represents the maximum allowable equivalent series resistance that yields a crossover frequency less than the maximum allowable. For this figure, the minimum allowable phase margin was set to 30º and the maximum allowable crossover frequency was set to 75kHz. For example, if an output inductance of 10µH and an output capacitance of 2720µF were used, then from Fig. 8, the capacitor's equivalent series resistance must be greater than 5.3mΩ and less than 35mΩ under all conditions.

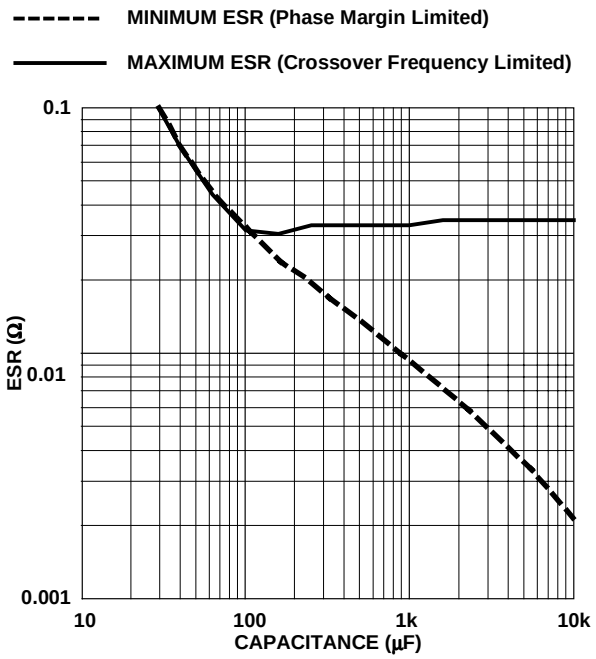

Fig. 8. Output capacitor R_C region of stability for various values of output capacitance for the TPS54611 controller, L=10µH.

It is imperative that the designer understands the AC characteristics of the output capacitors and verifies that the selected output capacitors are in agreement with the presented guidelines. If the IC manufacturer presents no guidelines, then the designer may use the information presented in this paper to determine the stability margins

for any combination of power processing components.

A beneficial aspect of this control method is the reduced amount of phase shift that is present in the feedback loop. Because the E/A has limited gain all the way down to DC, the typical integrator function has been eliminated and the 90º of phase shift associated with the integrator has been eliminated as well. This produces two benefits. First, it allows the E/A to respond more quickly to large-signal output errors because the relatively large integrator capacitor is not present and thus does not limit the slew-rate of the E/A output. Secondly, it makes the system easily stabilized because the total loop phase shift at frequencies less than one-tenth of the switching is only 180º as opposed to 270º if integral compensation were used. Because of the reduced phase shift, the ability to stabilize the loop with only the output capacitor's equivalent series resistance is realizable. If the zero associated with the output capacitance and its equivalent series resistance is close to the crossover frequency, then the associated phase boost stabilizes the system. The problem with this control method arises when the system calls for the lowest possible output ripple. As previously described, there is a lower limit to the output capacitor's equivalent series resistance and thus to the minimum value of output ripple that is theoretically achievable. However, in most practical applications this control method produces acceptable results.

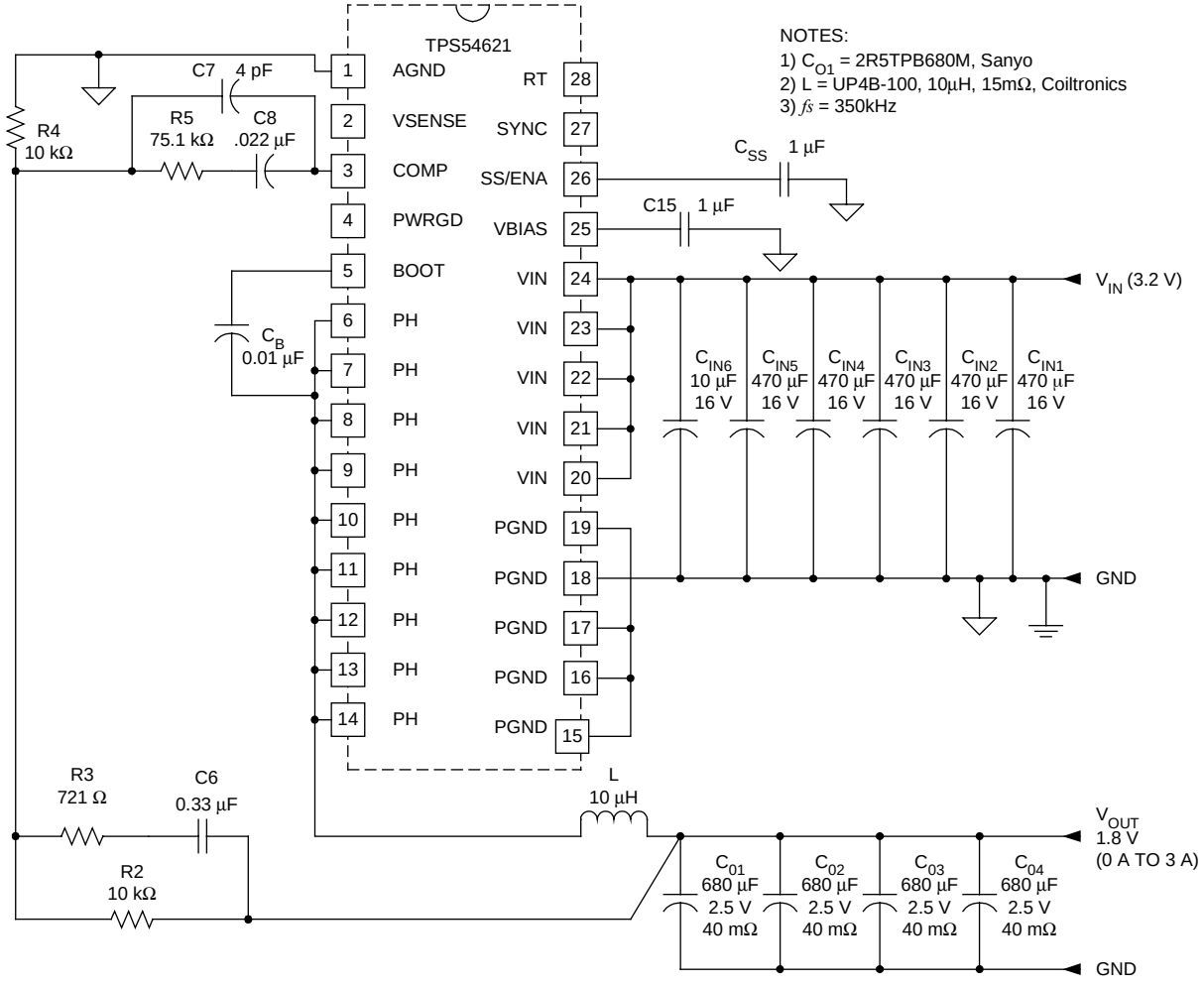

Fig. 9. Test circuit for external compensation.

In summary, the advantages of this method include, 1) simplified compensation design, 2) fast transient response (no integrator pole), 3) reduced component count, 4) shorter design cycle time, and 5) reduced board area. The disadvantages of this method consist of: 1) restricted power train component selection, 2) increased output ripple (R_C lower limit), and 3) reduced line and load regulation performance (limited gain at DC).

IV. Design Examples and Test Data

A. External Compensation

The schematic in Fig. 9, (previous page) is a typical application circuit for the TPS54621 Texas Instruments power supply IC. The compensation components were selected using the procedure outlined above, with V_{IN} = 3.2V and the other values as shown on the schematic. There are an additional five surface mount components used in this design as compared to an internally compensated design as shown in Fig. 15. Resistors Ri and Rf were not counted because they are typically internal to the IC.

The same PCB and controller were used to perform the testing and as a result, two resistors were used to duplicate the internal compensation network of a gain-limited E/A IC. The advantages of the five additional components can be seen in Fig. 10 and Fig. 11.

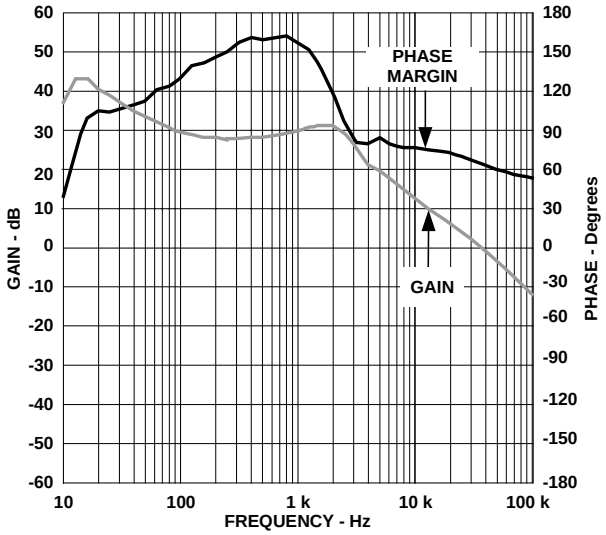

Fig. 10. Open-loop Bode plot for external compensation design, V_{IN}=3.2V, I_O=3.0A.

All the desirable attributes of an optimal Bode plot are shown in Fig. 10. It features increasing gain at low frequencies, providing good regulation performance. It features a high crossover frequency, resulting in reduced under and overshoot and fast settling times. It also exhibits excellent stability criteria given that it has a phase margin of approximately 65º and a gain margin of more than 10dB.

Fig. 11 shows the measured load transient response. As required for any precise measurements in a switching power supply circuit, low inductance probes were used for these measurements. The scope was also bandwidth limited to 20MHz. The peak deviation is measured as 36mV for 300ns, which quickly reduced to 22mV and the settling time is 28µs. This represents a peak deviation of 2% for 300ns and 1.2% for the remainder of the settling time. After reviewing the results for the other two control techniques, it becomes apparent that if optimal performance is required, the designer needs to consider a control IC that provides the flexibility for external compensation.

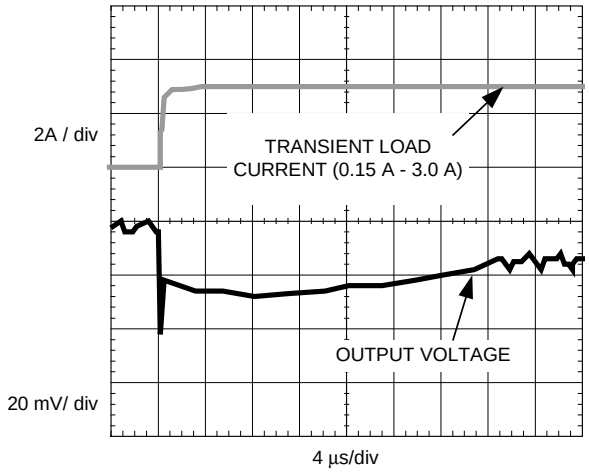

Fig. 11. Transient response for external compensation design, V_{IN} = 3.2V.

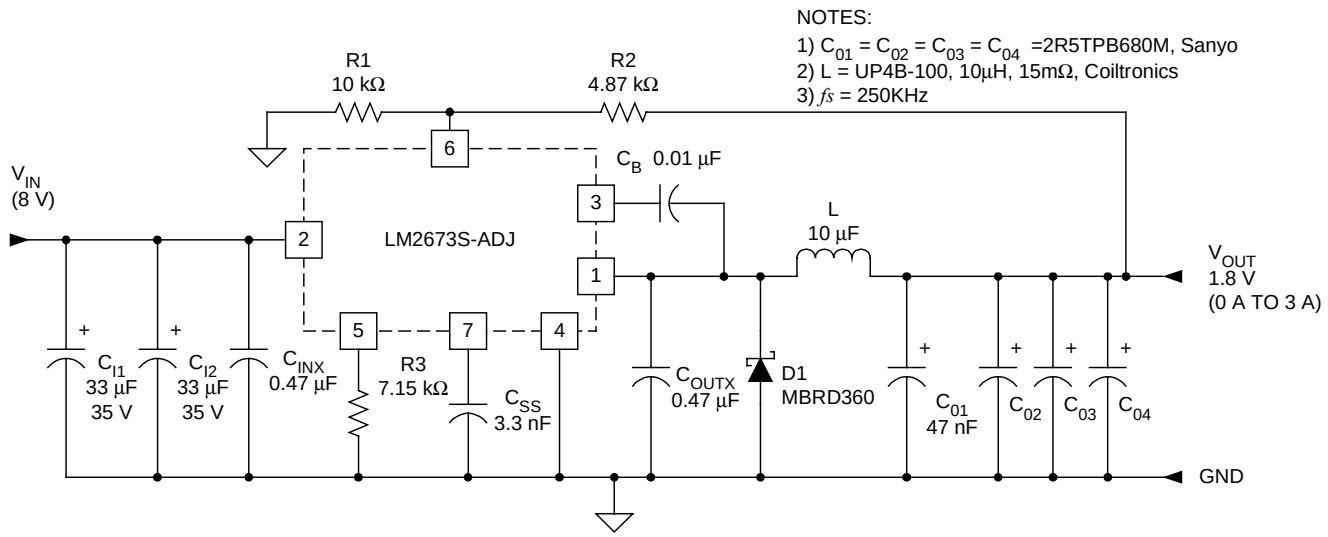

Fig. 12. Test circuit for internal pole-zero compensation.

B. Internal Compensation with Internal Poles and Zeros

In the following two circuit designs, the power processing components are set equal to the ones presented in the first circuit design where external compensation is used. Fig. 12 details the test circuit used for the LM2673S-ADJ controller, using internal pole-zero compensation. The details of the internal compensation are shown in Fig. 5. This technique has some desirable DC characteristics, but the AC characteristics typically are not be as good as the other two compensation methods being presented. Fig. 13 shows the open loop bode plot for the test circuit of Fig. 12.

The Bode plot reveals some of the issues that can arise from the necessity to deviate from the manufacturer's reference designs. The system is stable by a very small margin. While the phase margin is acceptable, around 72º, the gain margin is only 5dB, which is not desirable. A good rule of thumb is to set the gain margin to greater than 10dB. The gain margin is a measure of how much gain variation the system can withstand without becomming unstable. Gain variation can occur as a result of temperature variations and component tolerances.

One desirable aspect of this compensation scheme, as evident from the bode plot, is the increasing gain with decreasing frequency. As quantified in Section III. C*., Voltage Mode with Internal Gain Error Amplifier*, having a high system gain at DC results in good regulation performance. Examining the load transient response shown in Fig. 14, it becomes apparent that this compensation scheme does not provide reduced peak undershoot or reduced settling time. The peak deviation is measured as 96mV or 5.3% and the settling time is 575µs. The settling time is exceedingly long for a crossover frequency of 20kHz and this inconsistency demonstrates one of the major drawbacks of using internal pole-zero compensation. The IC manufacturer selects the size of the integrator capacitor and typically uses a large integrator capacitor to ensure stability over the widest combination of power processing components. But with a large integrator capacitor and limited E/A output current capability, the slew rate of the E/A output is limited which in turn limits the recovery time of the converter.

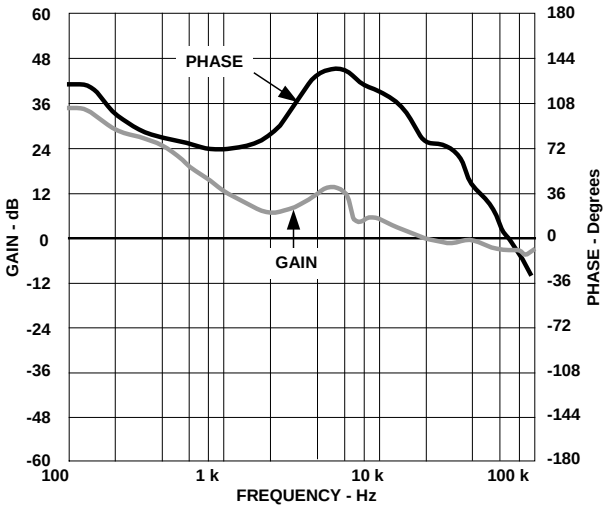

Fig. 13. Open-loop Bode plot for internal pole-zero compensation, V_{IN}=8.0V, I_O=3.0A.

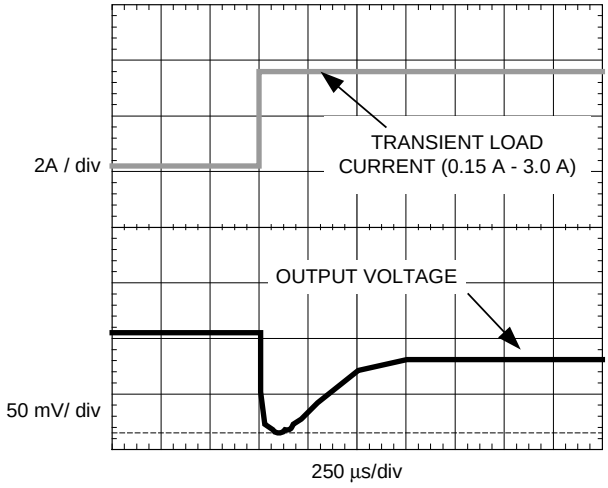

Fig. 14. Transient response for internal pole/ zero compensation, V_{IN} = 8.0V.

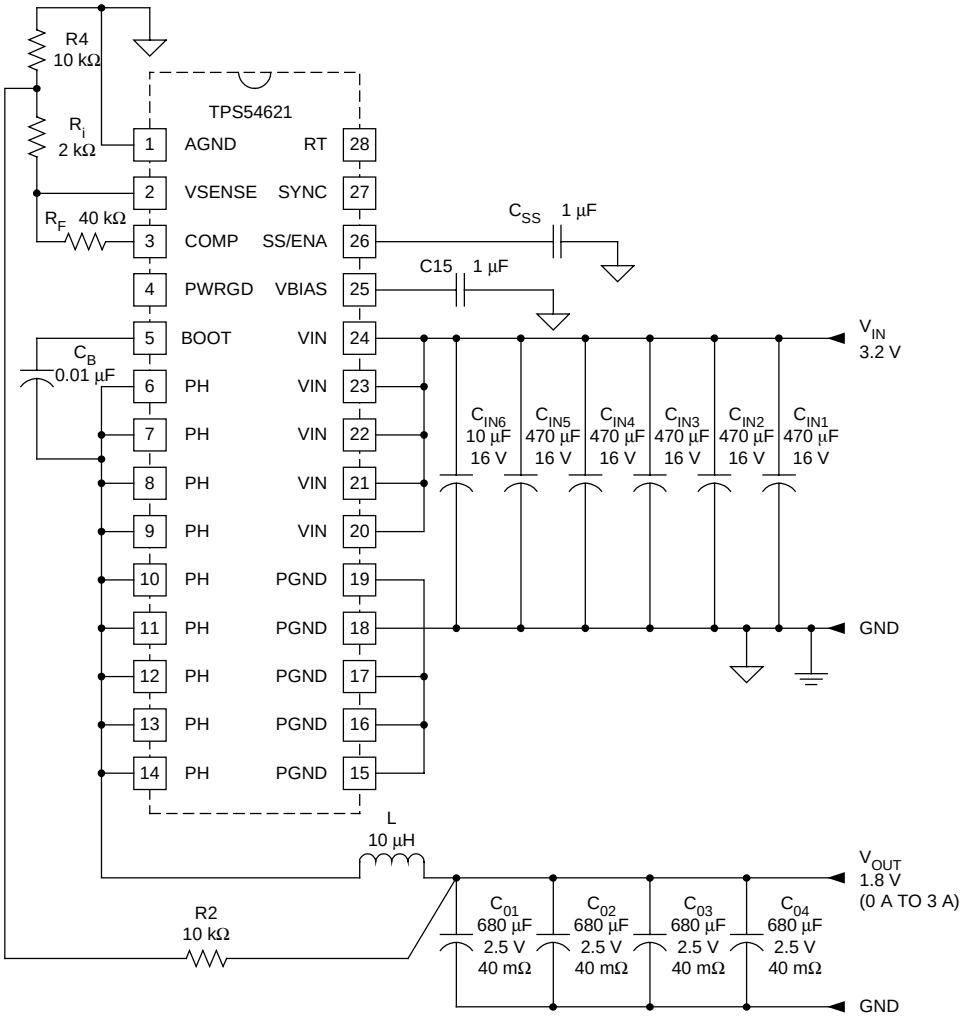

Fig. 15. Test circuit for internal gain limited E/A compensation.

C. Internal Compensation with Gain Limited Error Amplifier

The circuit used to demonstrate internal gain-limited compensation in Fig. 15 is identical to the one shown in Fig. 9, except that the external compensation components have been replaced by a resistor network which produces a constant gain of 20 V/V. The gain is constant from DC to 150kHz at which point the E/A has an internal pole which rolls off the gain at a negative 20dB per decade slope. By using the same power processing components the variations that different components and board layouts would have introduced are eliminated. The Bode plot in Fig. 16 demonstrates the effects of the gain-limited compensation. It shows that the gain is limited from 10Hz to 1KHz at which point it starts to roll-off at a negative 40 dB per decade slope. The output capacitor zero comes in at around 6 kHz and reduces the slope to negative 20 dB per decade. The output capacitor zero also increases the phase margin to a desirable 65º. The main drawback to this control method is that the regulation performance is worse than the other two methods described above. In most applications, the regulation performance is perfectly acceptable. In examining the transient response shown in Fig. 17, the peak deviation is measured as 33mV for 300ns, which quickly reduces to 22mV and the settling time is 60µs. This represents a peak deviation of 1.8% for 300ns and 1.2% for the remainder of the settling time. The fast settling time is partially a result of excluding an integrator capacitor in the compensation circuit. Where the externally compensated device has a bandwidth of 35kHz and a settling time of 28µs, the designer would expect to see a settling time of 3.5 times that or 100µs for this circuit, which has a bandwidth of only 10kHz. A comparison between the settling time of the internal pole-zero compensator and the settling time for the internal gain-limited E/A clearly reveals the benefits of the internal gain-limited E/A compensation. The internal pole-zero compensation has an equivalent bandwidth, but the settling time is almost 10 (575µs/60µs) times as long.

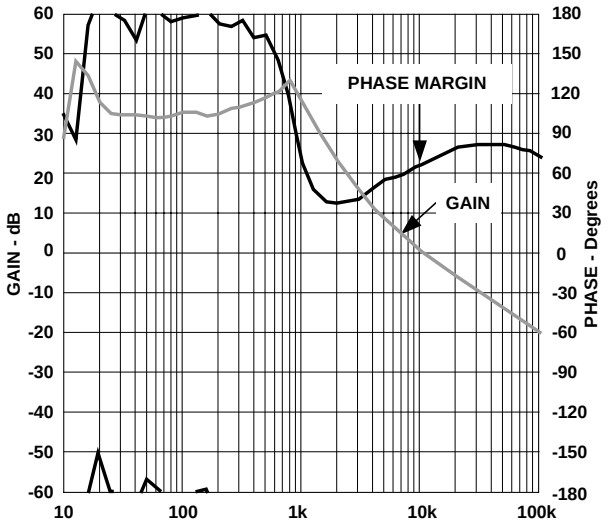

Fig. 16. Open-loop Bode plot for internal gain limited E/A compensation, V_{IN} = 3.2V, I_O = 3.0A.

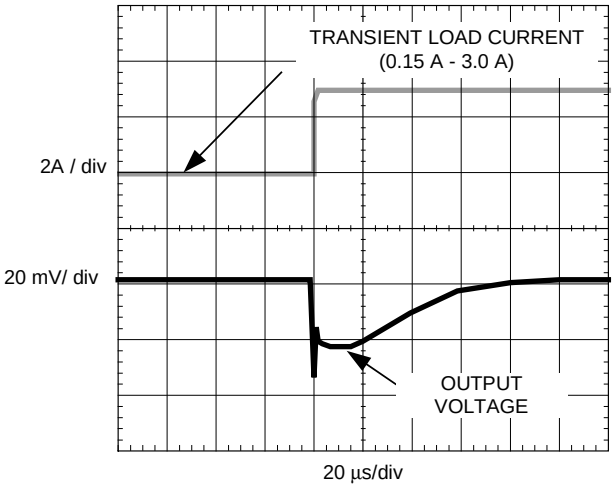

Fig. 17. Transient response for internal gain limited E/A compensation, V_{IN} = 3.2V.

V. SUMMARY

Two internally compensated voltage mode control techniques have been compared to the traditional externally compensated voltage mode control implementation. The advantages and disadvantages of each were identified. The use of internal compensation is desirable when the transient response requirements are not extremely stringent and design cycle time must be minimized. For higher performance designs, control ICs with external compensation provides the best performance at the cost of additional components, complexity and board space. Gain-limited internal compensation control ICs may offer the best trade-off between performance and simplicity. Gain-limited compensation provides very good transient response because the traditional integrator capacitor around the E/A is not present. The disadvantage is that the regulation specification is not ideal, but is acceptable for most practical applications.

VI. CONTROL TECHNIQUES COMPARISON SUMMARY

A. Voltage Mode with External Poles and Zeros

Advantages

- Nearly unrestricted selection of power train components
- Possible improvement in output ripple performance (no R_C limitations)
- Good line and load regulation
- Improved control over transient response characteristics

Disadvantages

- Complexity of compensator design
- Increased component count
- Small increase in board area
- Increased design cycle time

B. Voltage Mode with Internal Poles and Zeros

Advantages

- Simplified compensation design
- Reduced component count
- Shorter design cycle time
- Reduce board area
- Good line and load regulation

Disadvantages

- Non-optimized transient response
- Restricted power train component selection for stability
- Increased output ripple (R_C lower limit)

C. Voltage Mode with Internal Gain Limited E/A

Advantages

- Simplified compensation design
- Fast transient response (no integration capacitor)
- Reduced component count
- Short design cycle time
- Reduced board area

Disadvantages

- Restricted power train component selection for stability
- Increased output ripple (lower R_C limit)
- Reduced line and load regulation performance (limited DC gain)

REFERENCES

[1] Application Report, "*Understanding Buck Power Stages in Switchmode Power Supplies"*, TI Literature No. SLVA057.

[2] LM2673S-ADJ from National Semiconductor, Literature No. DS100913, August 2000.

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