Application Report
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# Loop Stability Analysis of Voltage Mode Buck Regulator With Different Output Capacitor Types – Continuous and Discontinuous Modes

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**ABSTRACT**

The buck dc/dc converter is probably the single most common voltage converter in use. Many design resources are available: application reports, text books, and many data sheets contain comprehensive design procedures for the continuous-conduction mode of operation. For discontinuous mode, however, the same solutions do not exist in a single-source, useful format.

The purpose of this application report is to provide a complete set of design equations for calculating the buck converter loop gain and phase in both continuous and discontinuous modes. Because most modern systems use more than one type of output capacitor, and because this can affect the power system stability, solutions are presented for up to three different types of capacitors.

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## 1 Introduction

In electronic circuits, the basic buck converter is not complicated (see Figure 1). The power section, or plant, consists of a pulse generator and a passive filter. These combine to convert an applied input voltage to a (lower) output voltage. The particular technique of using the pulse source and a reactive (nondissipative) output filter allows the transfer of energy with high efficiency. That is, little power is lost in the converter itself.

In order to regulate the output voltage, a voltage reference and an error amplifier are added to the circuit. These three basic blocks (the pulse generator, output filter, and error amplifier) combine to form a complete dc/dc converter (see Figure 1).

Other switch-mode converters are based on this buck topology. The forward converter, including single-transistor, half-bridge, and full-bridge topologies can all be represented by the same block diagram shown in Figure 1.

Implementing a modern buck converter can be accomplished in many ways, using different technologies. The error amplifier and voltage reference usually are integrated along with a voltage-controlled pulse generator, or modulator, into a monolithic integrated circuit (IC). The modulator's pulse output is buffered by power switches, which may be internal to the IC or external discrete devices. The output filter is almost always made up of an external inductor and capacitor(s).

The design of the circuit begins by selection of various operating parameters and component values, largely determined by the basic operating requirements, namely:

- Input voltage range
- Output voltage
- Output current range
- Operating frequency

By using these design requirements, the values of the filter components are determined, and the power switches are selected. As the method of choosing these parts and the operating frequency are well covered by most data sheets and many application reports (SLUP206)[1], it is not discussed in this document.

After selecting the main circuit components, the error amplifier and voltage reference must be added to provide output voltage regulation. The design of this compensator is described in several places, but usually only in specific terms, and only for specific operating conditions (continuous-conduction mode, with one type of output capacitor). Mathematical models for discontinuous-conduction mode, with several different capacitor types and parasitic losses, are unavailable.

This application report describes the design of the compensator for the voltage-mode buck converter, with solutions for complex filter structures and for operation in both the continuous- and discontinuous-conduction modes.

A step-by-step design procedure is also given, which can be used as a guideline for compensator design for any buck converter operating in the continuous and discontinuous modes.

Although the output filter can be infinitely complex (depending on the number and types of output capacitors, which are practically unlimited in variation), solutions are presented for some common designs (one, two, and three different types of output capacitor).

## 1.1 Stability Criteria

The control model of a buck converter can be represented by three basic blocks as shown in Figure 1.

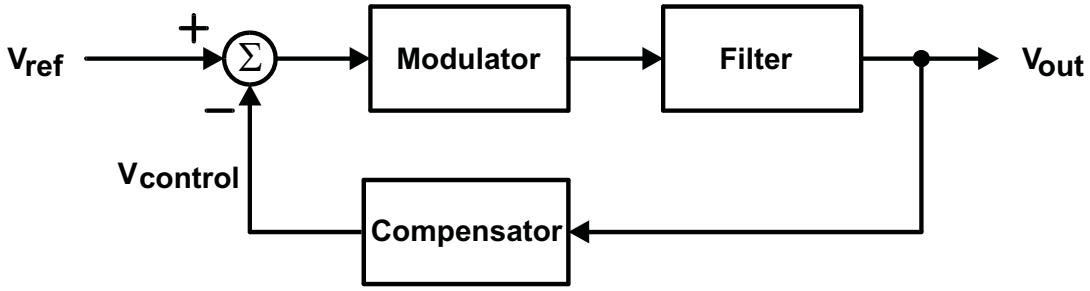



**Figure 1. Buck DC/DC Regulator Control Block Diagram**

The transfer function of the system shown in Figure 1 is

$$H_{system}(s) = \frac{V_{out}}{V_{ref}} = \frac{H_{\mathrm{mod}}(s) \cdot H_{Filter}(s)}{1 + H_{\mathrm{mod}}(s) \cdot H_{Filter}(s) \cdot H_{Compensator}(s)} = \frac{H_{\mathrm{mod}}(s) \cdot H_{Filter}(s)}{1 + H_{Loop}(s)} \quad (1)$$

The denominator of the system transfer function, 1 + $H_{Loop}$ (s), is the *characteristic equation* of the system, and $H_{Loop}$ (s) is the *loop gain* – the gain of the loop consisting of the modulator, filter, and compensator [3]. By inspection, it is clear that if $H_{Loop}$ (s) = –1, the transfer function of the system, $H_{Loop}$ (s) will become infinite – and that would be an unstable system.

The Nyquist criteria can be used to determine the stability of this system [4]. Because of the relative complexity of a typical buck converter, the most convenient way to analyze stability is by the use of graphical methods.

A special case of the Nyquist criteria can be applied by plotting the gain and phase of $H_{Loop}$ (s), and observing $\angle H_{Loop}(s)$ [the phase of $H_{Loop}$ (s)] when its magnitude is unity. This measure of the phase is the *phase margin*, and it is the difference between –180° and $\angle H_{Loop}(s) + 180°$. Mathematically, the phase margin is $\angle H_{Loop}(s)$., and a higher phase margin indicates a more stable control loop. A phase margin of 45° is usually taken as a minimum goal in power supply design, but any positive phase margin will result in a stable system.

The loop gain is the product of the transfer functions of each block in the loop:

$$H_{Loop}(s) = H_{\mathrm{mod}}(s) \cdot H_{Filter}(s) \cdot H_{Compensator}(s) \quad (2)$$

Each of these transfer functions must be determined in order to calculate $H_{Loop}$ (s). Therefore, each block is treated separately. Before doing this, the contents of each block is described in order to make clearer the comparison of the general block diagram to an actual schematic of a converter.

For this discussion, a generic schematic is used in order to avoid clutter and confusion. An actual circuit contains additional components, including an actual control integrated circuit (IC), but that level of detail is unnecessary for this discussion. Although some details are controller dependent, the concepts presented here are general. In a later example, it becomes clear how the controller properties affect the solution, and a list of controllers is presented along with their characteristics to aid in the calculations for specific designs.

For this derivation of the loop stability equations, the following block diagram represents a non-isolated buck converter (see Figure 2):

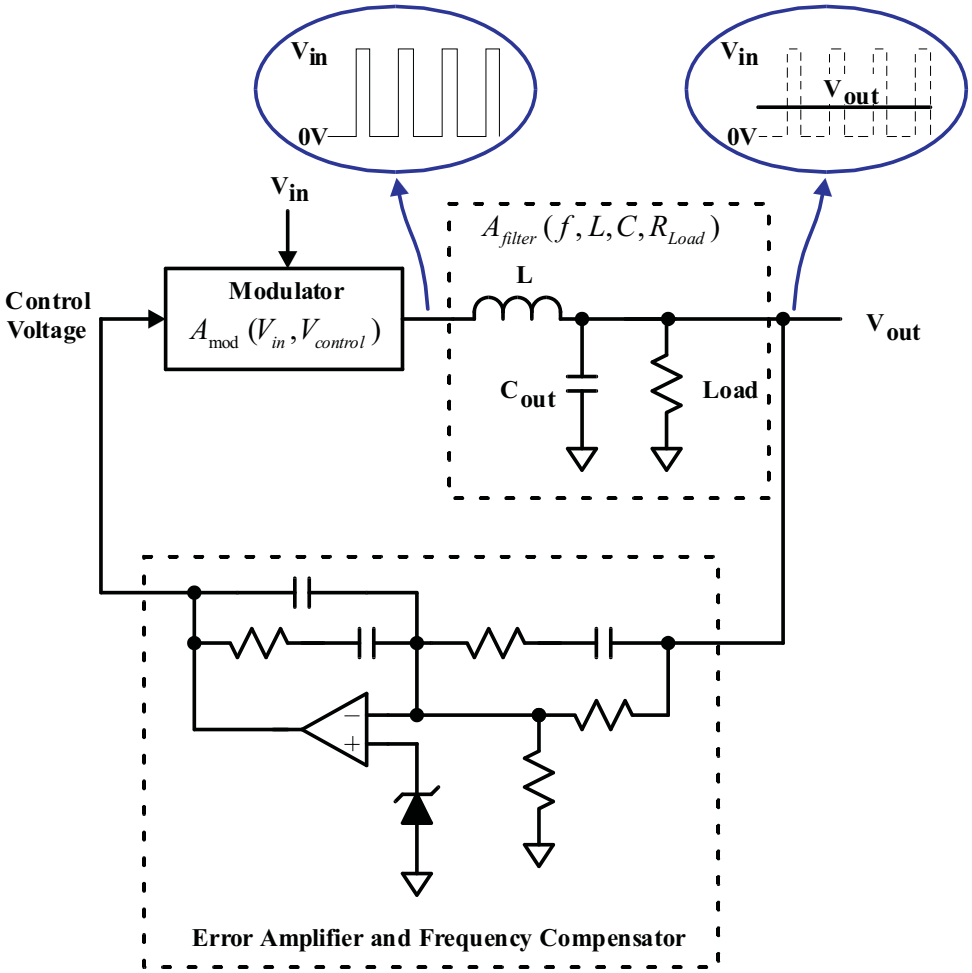



**Figure 2. Buck Converter Schematic**

## 1.2 Modulator

Of the three blocks that make up the buck converter, the modulator is the only one with no frequency dependence. The modulator is basically a voltage-controlled rectangle wave generator: In response to a control voltage, the modulator produces a repeating rectangular output waveform, with limits of 0 V and $V_{cc}$. This rectangle wave is produced by connecting the output to either the input voltage ($V_{cc}$) or to ground. The duty cycle of the output is defined as the time spent at $V_{cc}$ divided by the total period of the repetitive waveform. As such, $t_{on}$ is defined as the time that the output is connected to $V_{cc}$, $t_{off}$ is the time that the output is connected to ground, and the duty cycle is defined as $D = \frac{t_{on}}{t_{on} + t_{off}}$.

Internally, the most basic modulator consists of a voltage comparator and a sawtooth generator. These blocks are combined to produce the desired result as shown in Figure 3.

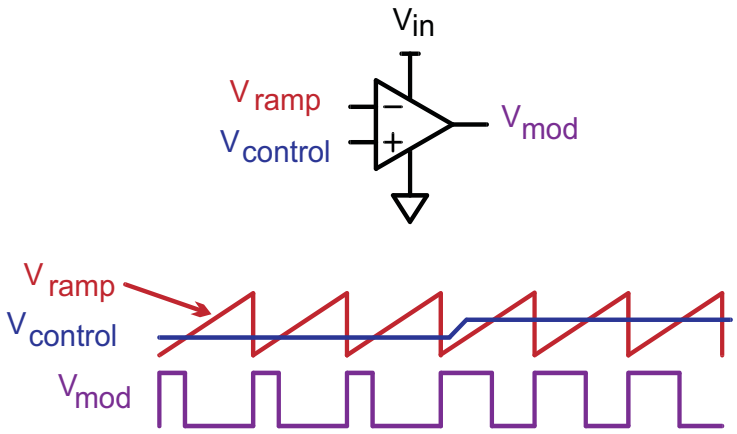



**Figure 3. Voltage Mode Modulator**

As the control voltage increases, the duty cycle of the output increases as well. When the control voltage equals (or is greater than) the peak voltage of the ramp signal, the output is continuously high. In other words, $t_{off}$ = 0 and the duty cycle is 1 (or 100%).

Conversely, if the control voltage is at or below the minimum of the ramp voltage, the output of the comparator is continuously low. This means that $t_{on}$ = 0 and the duty cycle is 0 (or 0%).

Notice that the frequency of the ramp signal determines the frequency of the modulator output, which is the switching frequency of the converter.

The modulator's output is a rectangle wave. This rectangle is averaged by the output filter and applied to the load as a dc voltage. The dc voltage is therefore the average of the rectangular pulse waveform, or

$$V_{out} = \frac{1}{T}\int_0^T v_{\mathrm{mod}}(t)dt = \frac{1}{T}\int_0^{t_{on}} V_{in}dt \tag{3}$$

Here, T is the period of repetitive pulse waveform ( $T = t_{on} + t_{off}$), so

$$V_{out} = \frac{V_{in} \cdot t_{on}}{t_{on} + t_{off}} = V_{in} \cdot D \tag{4}$$

In terms of the transfer function of the modulator, this is defined as the averaged value of the pulse train output divided by the control voltage input, or:

$$A_{\mathrm{mod}} = \frac{\Delta V_{out}}{\Delta V_{control}} \tag{5}$$

This refers to the change in output voltage as a result of a *change* in the control voltage. Remembering that the control voltage is bounded by the ramp voltage (which is considered a part of the modulator), and including the fact that the range of $V_{out}$ is 0V to $V_{in}$.

$$A_{\mathrm{mod}-CCM} = \frac{dV_{out}}{dV_{control}} = \frac{d}{dV_{control}}\left(V_{in}\frac{V_{control}}{V_{ramp}}\right) = \frac{V_{in}}{V_{ramp}} \quad (6)$$

This is the gain of the modulator. On a Bode plot, $A_{mod\text{-}CCM}$ is a constant gain and it causes no phase shift. In reality, this block has time delays, which cause phase shift. However, for the purpose of calculating the loop gain and phase, these phase shifts usually are not a problem.

## 1.3 Continuous- and Discontinuous-Mode Operation

When the inductor current is continuous in a buck converter, it is operating in the continuous-conduction mode, or CCM. Otherwise, the inductor current returns to zero during each cycle, and this is the discontinuous-conduction mode, or DCM.

In the block diagram of Figure 1, the filter and compensator blocks have linear transfer functions. The modulator, however, is nonlinear. The modulator responds to a continuous control voltage input and produces a pulse train output with the required duty cycle. At light loads, when the load current is below the critical current, the modulator may be commanded to produce pulses that are narrower than those required in CCM. This occurs when the modulator output is incapable of sinking current (the nonsynchronous power stage is one such structure). When the inductor current reaches zero, the modulator output disconnects from the output filter, and the voltage rises to $V_{out}$ until the next cycle begins and the input voltage is applied to the modulator output again. Figure 4 shows cases of CCM, the critical conduction point, and forced CCM, where the modulator is forced to sink current. This forced CCM is usually a characteristic of the controller IC being used and has some advantages over allowing the converter to revert to DCM.

Figure 5 shows the modulator output of a converter operating in DCM. When the inductor current reaches zero, the modulator output becomes high impedance, and this node can be seen floating up to $V_{out}$ until the next cycle starts.

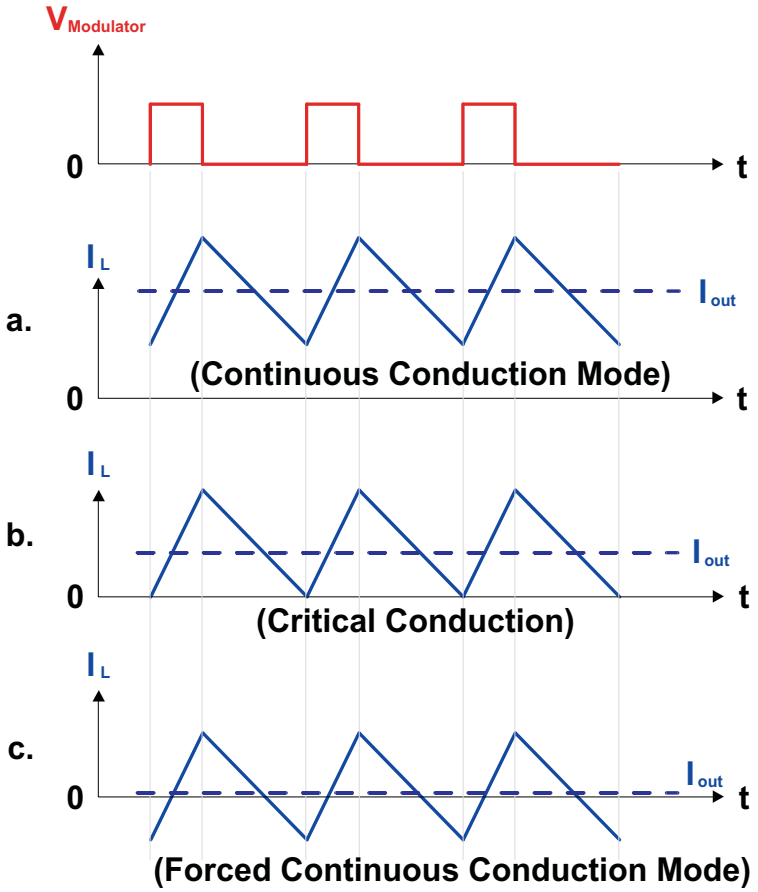



**Figure 4. Inductor Current in (a) CCM, (b) Critical Conduction Point, and in (c) Forced CCM**

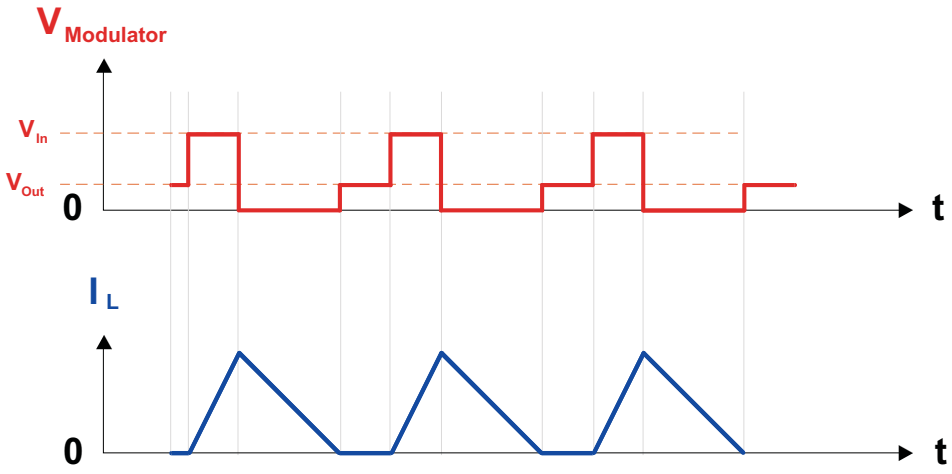



**Figure 5. Modulator Output and Inductor Current in DCM**

During the analysis of the loop stability, it is necessary to know if the converter is operating in CCM or DCM, or both (over a range of load current, the converter can enter both modes). If the controller operates in the forced PWM, forced CCM, or forced continuous mode (these all mean the same thing), then it always operates in CCM. Otherwise, the operating mode must always be known, so that the correct modulator gain and filter transfer functions are used.

The operating point that lies exactly at the threshold of DCM and CCM operation is usually referred to as the critical conduction point. At critical conduction, the dc output current is equal to half of the inductor's peak-to-peak ripple current:

$$Iout_{critical} = \frac{Inductor\ Ripple\ Current}{2} \approx \frac{(V_{in} - V_{out})\frac{V_{out}}{V_{in}}}{2Lf_{sw}} = \frac{V_{out}(V_{in} - V_{out})}{2V_{in}Lf_{sw}} \quad (7)$$

When $I_{out} < Iout_{critical}$, the converter operates in DCM (unless it is in forced PWM mode as previously described), and when $I_{out} \geq Iout_{critical}$ it operates in CCM.

## 1.4 DCM Modulator Gain

When the converter is operating in CCM, the duty cycle is approximately $D_{CCM} = \frac{V_{out}}{V_{in}}$. However, when the output current is below the critical current given in Equation 7, and when the converter is not in the forced PWM mode (that is, when the controller allows DCM), the duty cycle of the modulator reduces in order to maintain regulation. The modulator's duty cycle in DCM is given in SLVA057[2], and it includes the inductor series resistance $R_L$. Recognizing that $R_L$ << R in DCM, the modulator duty cycle is:

$$D_{DCM} = \sqrt{\frac{\frac{8Lf_{sw}}{R}}{\left(\frac{2V_{in}}{V_{out}} - 1\right)^2} - 1} \quad (8)$$

Where

$R_L$ is the load resistance
L is the value of the inductor
$V_{in}$ is the input voltage
$V_{out}$ is the output voltage
$f_{sw}$ is the regulator's switching frequency

Noting that $D_{DCM}$ is now a function of the load resistance R, it clearly also depends on the load current. This is in contrast to CCM, where the duty cycle depends only on $V_{in}$ and $V_{out}$. Figure 6 shows the duty cycle of a modulator, as the load current decreases and it transitions from CCM to DCM.

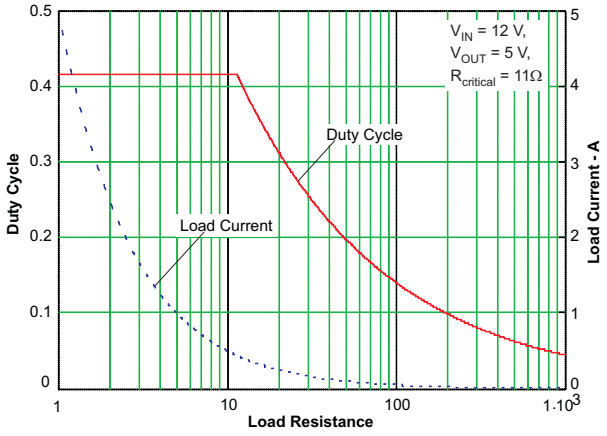



**Figure 6. Duty Cycle of a Modulator as Load Current Transitions Between CCM and DCM**

In DCM, the modulator does not produce a continuous pulse stream. It has three states: $V_{in}$, 0 V (ground), or open-circuit (high impedance), as shown in Figure 5. The transfer function of the modulator plus filter becomes more complicated than the CCM case. The modulator gain (the term *gain* is used loosely; see Appendix A for development) is:

$$A_{\mathrm{mod}-DCM} = \frac{d\,V_{out}}{d\,V_{control}} = \frac{2\,V_{out}\left(1-\frac{V_{out}}{V_{in}}\right)}{v_{ramp}\,D_{DCM}\left(2-\frac{V_{out}}{V_{in}}\right)} \tag{9}$$

Where:

$D_{DCM}$ is the duty cycle in DCM from Equation 8

Equation 9 is only valid in DCM, meaning that $R > \frac{V_{out}}{Iout_{critical}}$. Otherwise, the converter operates in CCM, and the modulator gain is given by Equation 6.

## 1.5 Output Filter

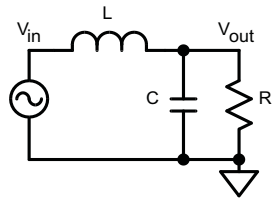
The modulator provides a pulse train, bounded by the input voltage, whose duty cycle is determined by an applied control voltage. The output filter performs the averaging function that converts this pulse train into the output voltage of the converter.

Because the goal of a dc/dc converter is to have high efficiency, the output filter consists of reactive components, which do not (to first order) dissipate any power. This filter operates as a low-pass filter in the frequency domain, suppressing the ac components of the modulator's pulse train. It is a simple second-order L-C section, terminated by the load resistance. Therefore, the load resistance is a critical component of the filter. It must be known in order to predict the filter's performance, the loop response, and the stability of the converter.

As described so far, the output filter is a simple second-order passive structure. Its transfer function now can be written and used in the stability calculations. However, some important caveats must be noted in order to attain useful and accurate results. These are addressed in the following paragraphs.

A discussion of the transfer function of the simple L-C filter, terminated by the load resistance R follows (see Figure 7).

a.




b.

$$H_{RLC}(s) = \frac{R}{R + sL + s^2RLC}$$

c.

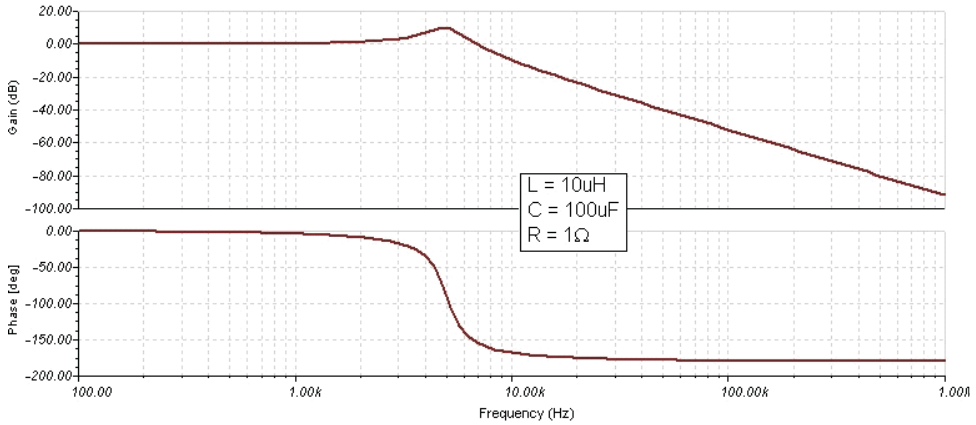
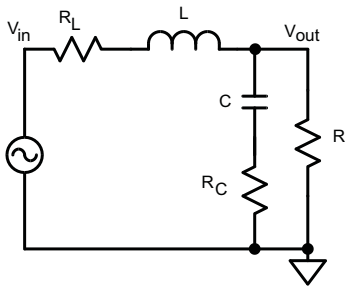



**Figure 7. Simplest LC Filter Schematic (a), Transfer Function (b), and Bode Plot (c).**

The cutoff frequency in this example (L = 10 µH, C = 100 µF, and R = 1 Ω) is approximately 5 kHz, and the ultimate phase shift settles at –180°, whereas the gain slope is –40 dB per decade of frequency increase above the LC cutoff frequency.

In many cases, parasitic effects of components are easily ignored and cause little consequence. To first order, capacitors and inductors have parasitic resistance, and these are included in this analysis, so that the filter transfer function is more accurate. Including some series resistance (usually referred to as ESR) in both the inductor and the output capacitor, results in this modified filter (the Bode plot has the lossless version superimposed for comparison, see Figure 8):

a.




b.

$$H_{Filter}(s) = \frac{1 + (C R_C)\, s}{1 + \frac{R_L}{R} + \left( \frac{L}{R} + R_C C + R_L C + \frac{R_L R_C C}{R} \right) s + \left( \frac{R + R_C}{R} \right) L C s^2}$$

c.

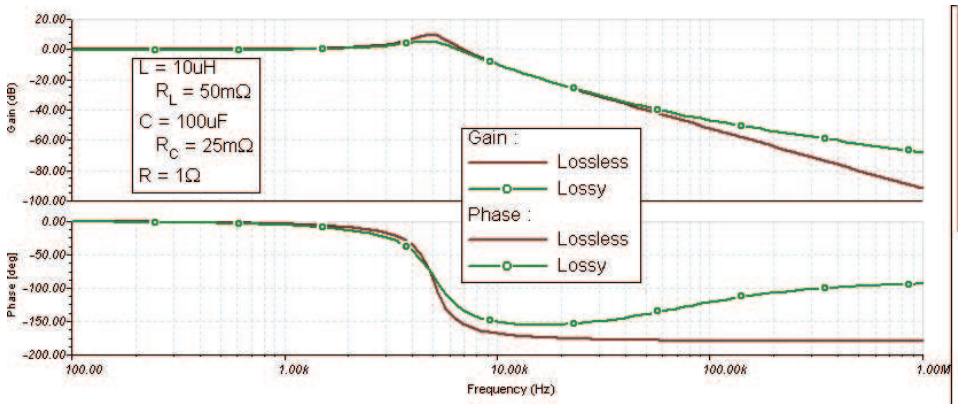
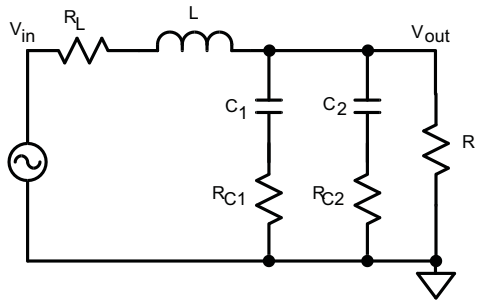



**Figure 8. Real LC Filter Schematic (a), Transfer Function (b), and Bode Plot (c)**

The effect of the parasitic resistances depends on their values relative to the other circuit values. Thus, it cannot be inferred from this discussion that a lossy filter creates an increasing phase and gain characteristic in all cases. The point is that the response of the filter can be changed, sometimes very dramatically, when these parasitics are included. The effect may be so subtle as to be insignificant. But the effect may be extremely dramatic, forcing design and component restrictions. Always consider the parasitics, and make an engineering judgment about whether to include them in calculations.

Complicating the filter design is the infinite number of load impedance structures. On a large board, three or four different types of output capacitors are possible, connected at various points in the power plane. The transfer function of the output filter with even two output capacitor types can become challenging (see Figure 9):

a.




b.

$$H_{Filter-CCM}(s) = \frac{1 + (R_{C1}C_1 + R_{C2}C_2)\,s + (R_{C2}C_2R_{C1}C_1)s^2}{1 + a_1 s + a_2 s^2 + a_3 s^3}$$

$$where \quad a_1 = \frac{L}{R} + (R_{C1}C_1 + R_{C2}C_2) + \frac{R_L}{R}(C_1 + C_2)$$

$$a_2 = \left[L(C_1 + C_2) + R_L C_1 C_2 (R_{C1} + R_{C2}) + R_{C2}R_{C1}C_2C_1\right] + \frac{L}{R}(R_{C1}C_1 + R_{C2}C_2)$$

$$a_3 = \frac{L}{R} C_1 C_2 \left[R(R_{C1} + R_{C2}) + R_{C1}R_{C2}\right]$$

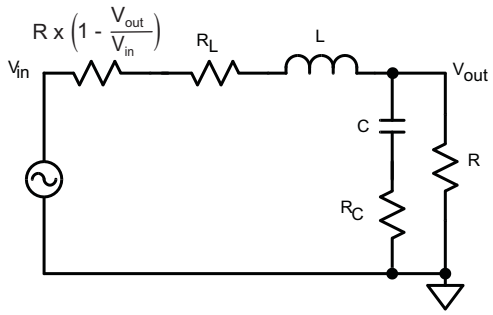
**Figure 9. Lossy Output Filter in CCM With Two Capacitor Types: Schematic (a) and Transfer Function (b)**

In order to model more complex output structures, the transfer function can be derived and used in the loop equations to calculate the gain and phase, which is the direction of this discussion. Appendix A contains transfer functions for filters with one, two, and three output capacitors, if equation-based solutions are desired. But it may be more convenient to use a SPICE (simulation program with integrated circuit emphasis) simulator to perform the loop analysis for more complicated structures.

## 1.6 Output Filter in Discontinuous Mode

In DCM, the output filter response changes because of the discontinuous nature of the modulator's driving impedance. In CCM, the modulator's output impedance is relatively low, but in DCM it is not. The equivalent circuit and transfer function of a lossy filter in DCM is shown in Figure 10.

a.




b.

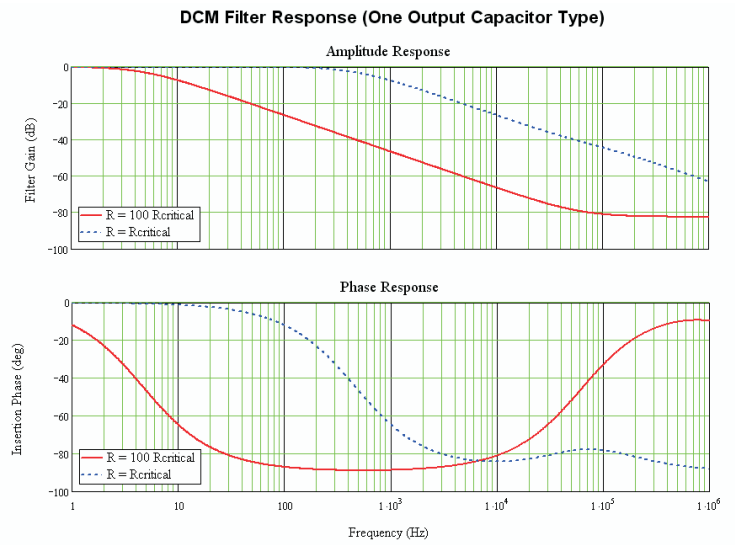
$$H_{Filter-DCM}(s) = \frac{1 + s \cdot R_C \cdot C}{1 + a_1 \cdot s + a_2 \cdot s^2}$$

where

$$a_1 = \frac{\frac{L}{R} + RC\left(1 - \frac{V_{out}}{V_{in}}\right) + C\left(R_C + R_L\right)}{2 - \frac{V_{out}}{V_{in}}}$$

$$a_2 = \frac{LC}{\left(2 - \frac{V_{out}}{V_{in}}\right)}$$

c.




$V_{in} = 25V$
$V_{out} = 5V$
$f = 300\,kHz$
$L = 10\,\mu H$
$R_L = 50\,m\Omega$
$C = 100\,\mu F$
$R_C = 25\,m\Omega$
$R_{critical} = 7.5\,\Omega$

**Figure 10. Lossy Filter in DCM: Schematic (a), Transfer Function (b), and Gain / Phase Characteristics for Two Values of Load Resistance (c)**

Appendix A gives transfer functions for DCM filters with one, two, and three output capacitors.

## 1.7 Compensator

The modulator and the output filter (including the load resistance) create the forward plant of the buck converter. These are the two stages that generate a dc output voltage from the dc input voltage. In order to close the loop, the output voltage is compared to a voltage reference, the error is amplified, and that error is applied to the modulator as its control voltage input. As the output voltage approaches the reference voltage, the error produced becomes small, and the system reaches a point of equilibrium: a temporary increase in $V_{out}$ creates a corresponding decrease in control voltage, which in turn drives the duty cycle of the modulator down, bringing the system back to a new point of equilibrium.

In order for this linear system to be stable, the loop phase delay must be less than 360° while the loop gain is above unity [ $|A_{Loop}(s)| \geq 1$, or $20\log|A_{Loop}(s)| \geq 0$ dB]. While the loop is stable for any phase shift less than 360°, a critically damped system (a reasonably fast loop response with minimal overshoot) will have a phase margin (defined as the difference between the actual loop phase delay and 360°) of about 60°. Any phase margin above zero degrees is technically stable, but lower values of phase margin are accompanied by more ringing in the loop after the loop is perturbed (by a change in Vin or Iout, for example). In power circuit design, 45° is often taken as a minimum goal for the phase margin.

As this is a negative feedback system, the error amplifier has a 180° phase shift (note the connections on the operational amplifier in Figure 2). That means that the plant (the modulator and output filter) in a critically damped system can only contribute another 120° of total phase shift, while the loop gain is above unity. Note that the modulator practically contributes no phase shift to the loop, but it does have gain. The output filter, being at least a second-order structure, can ultimately create at least 180° of phase shift. Of course, a second-order filter's phase shift reaches 180° only as its frequency approaches infinity — however, depending on the circuit values, it can reach the magic number of 120° quickly as it passes through its resonant frequency. In the examples given for the filter in Figure 7 and Figure 8, the insertion phase changes fast around the resonant frequency of the filter. Adding modulator gain to this passive filter increases the phase shift at the crossover (0 dB) frequency. This does not happen because the filter's insertion phase actually increases, but because the additional gain causes the crossover frequency to increase, as shown in Figure 11.

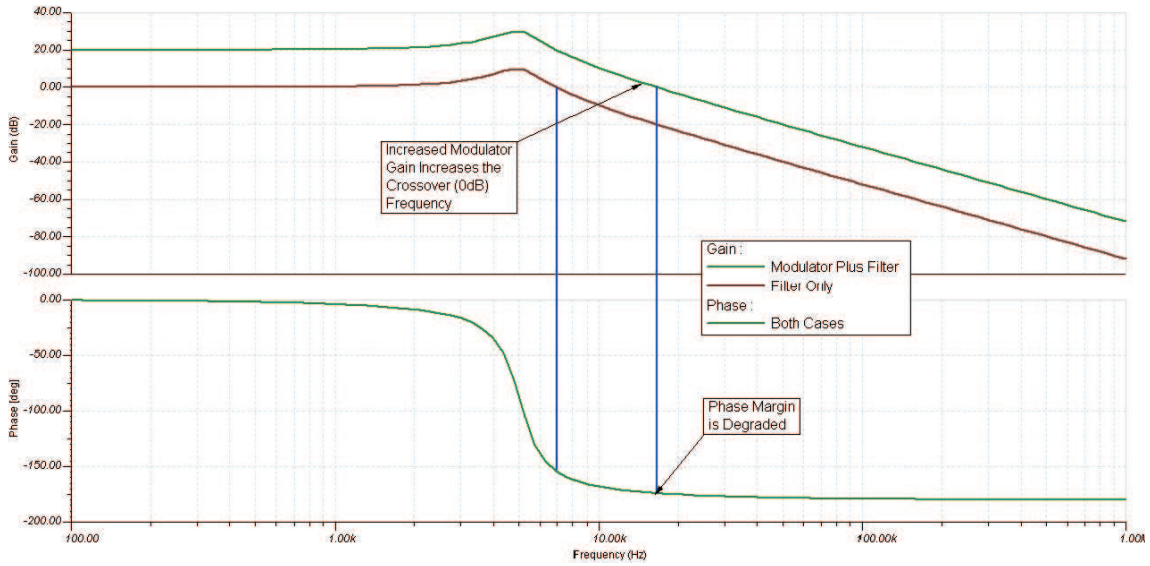
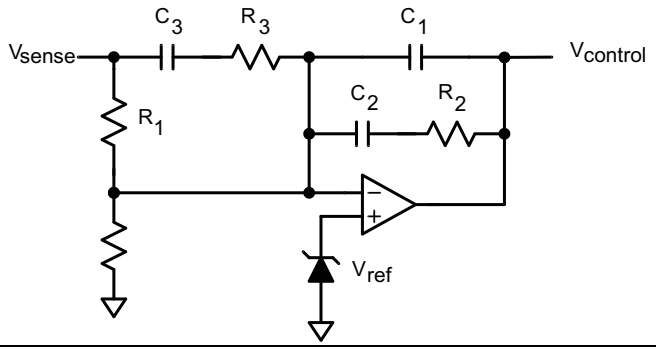



**Figure 11. Increasing Modulator Gain Raises Crossover Frequency and Reduces Phase Margin**

In order to close the loop on this converter, the error amplifier is inserted, as previously described, between the regulator output and the modulator control input. This allows the error amplifier to control the duty cycle of the modulator and hold the output voltage constant. Clearly, too much insertion phase is in the modulator/filter combination to achieve the desired phase margin for the closed loop. Therefore, the error amplifier is modified to shape the gain and phase of the loop so that the desired crossover frequency and phase margin can be achieved. The error amplifier is implemented using an operational amplifier in most cases. This building block can be used to provide the necessary compensation of gain and phase in the configuration shown in Figure 12.

a.




b.

$$H_{compensator}(s) = \frac{V_{control}}{V_{sense}} = \frac{H_{OL}(s)}{1 + H_{OL}(s)\beta(s)} \quad where$$

$$H_{OL}(s) = \frac{A_{DC}}{1 + \frac{s}{\varpi_{pole}}}$$

$$A_{DC} = Opamp\ DC\ Gain$$

$$\varpi_{pole} = 2\pi f_{pole} = Opamp\ Compensation\ Pole$$

$$\beta(s) = \frac{R_1 R_3 C_1 s\left(s + \frac{C_1 + C_2}{C_1 C_2 R_2}\right)\left(s + \frac{1}{R_3 C_3}\right)}{(R_1 + R_3)\left(s + \frac{1}{R_2 C_2}\right)\left(s + \frac{1}{(R_1 + R_3)C_3}\right)}$$

**Figure 12. Type 3 Compensator Schematic (a), and Transfer Function (b)**

The equations in Figure 12 require some explanation. The compensator is made up of an operational amplifier, configured as a complex filter by careful choice of the external passive components. As the operational amplifier is a part of the circuit, its characteristics may have some effect on the circuit's behavior, and this is why the basic operational amplifier parameters are included. The open-loop dc gain of the operational amplifier is represented by $A_{dc}$ and $\omega_{pole}$. $\omega_{pole}$ is the frequency of the operational amplifier's internal compensation pole. In the case of a discrete operational amplifier with its own data sheet, finding $\omega_{pole}$ is a matter of taking it from the open-loop frequency response. In a dc/dc controller, the error amplifier's open-loop response is usually not provided.

Another way to arrive at $\omega_{pole}$ is to use the operational amplifier's gain-bandwidth (GBW) and its dc voltage gain, $A_{dc}$, which are commonly given in a data sheet for a dc/dc converter:

$$\varpi_{pole} = 2\pi \frac{GBW}{A_{dc}} \tag{10}$$

The operational amplifier's open-loop gain should be higher than the desired compensator gain at all frequencies. Otherwise, the compensator response depends on the operational amplifier variations. In a dc/dc controller, the error amplifier gain is not well controlled (usually only a typical gain is specified); so, it is recommended to design the compensator to be relatively insensitive to variations in the error amplifier gain.

The modulator plus filter adds considerable phase delay, degrading the loop-phase margin, as has been shown. The compensator is designed to restore some loop phase, so that the overall loop phase margin meets our design goals, whatever they may be. The Type 3 compensator that is being discussed can provide two poles and two zeros in its transfer function. This is usually adequate for achieving critical damping (phase margin of about 60°), for example.

As may be expected, the circuit values interact with each other, and the location and behavior of the designed poles and zeros also affect each other. It is usually not practical (or necessary) to place the poles and zeros far enough apart that they do not interact. Fortunately, the desired response can usually still be obtained, sometimes with a little trial-and-error or judicious use of a SPICE simulator.

One possible response of this compensator is shown in Figure 13. The designed pole and zero locations are indicated, and in this case they are fairly easy to see in the actual response (the values were chosen for enough separation to see the inflections of each pole and zero). In a real-world design, the separation may not be so clear, but the overall goals for a stable system are usually still achievable.

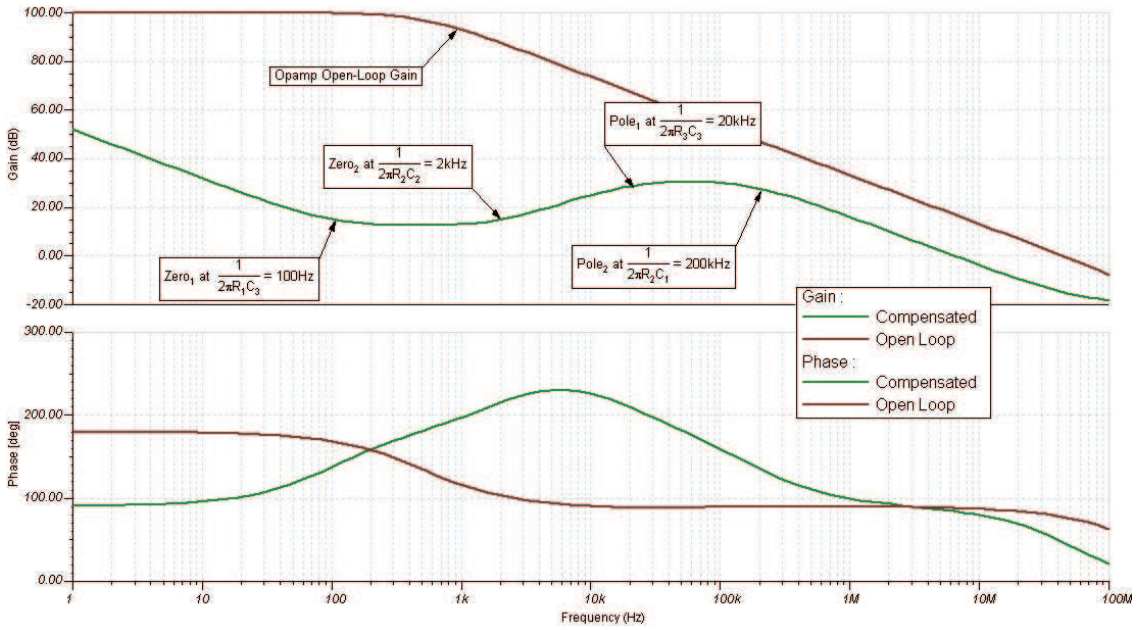



**Figure 13. An Example of a Type 3 Compensator Response**

## 1.8 A Design Example

One possible algorithm for placing the poles and zeros is demonstrated by an example. Besides deciding where to place the poles and zeros, the compensator gain also determines the crossover frequency of the loop. The crossover frequency selection is based on the switching frequency and the desired loop transient response. No attempt is made to define an optimum compensator, but the example used can be considered typical. In this case, the loop crossover is chosen to be near 20 kHz (that is, it is designed for 20 kHz, but a result that is reasonably close is acceptable, as errors due to interactions between the desired poles and zeros are expected). Only the CCM of operation is considered in order to design the compensator, but the DCM response for the final circuit is calculated.

The loop consists of the modulator, the output filter, and the compensator. The modulator's gain is a function of $V_{in}$ and $V_{ramp}$ when operating in CCM. The filter's transfer function is a function of the component values, including the load impedance. Although the selection of the filter components have not been discussed, they are mainly chosen based on dynamic issues in the circuit design. These choices and trade-offs are described well in most data sheets and several application reports (see SLUP206), and are not discussed in this document. Usually, the output inductor and capacitor(s) are decided before the compensator design is started.

This leaves the combined transfer function of the modulator and the output filter, and this response must be used to design the compensator. For example, the transfer function of the modulator and output filter of a design with a single type of output capacitor in CCM is given by:

$$H_{\mathrm{mod}+filter}(s) = H_{\mathrm{mod}-CCM}\, H_{Filter-CCM} = \frac{V_{in}}{V_{ramp}} \cdot \frac{1+(C\,R_C)\,s}{1+\frac{R_L}{R}+\left(\frac{L}{R}+R_C\,C+R_L\,C+\frac{R_L\,R_C\,C}{R}\right)s+\left(\frac{R+R_C}{R}\right)L\,C\,s^2} \quad (11)$$

For this design example, use the following parameters:

$V_{in}$ = 20 V
$V_{out}$ = 5 V
$I_{out}$ = 20 mA to 3 A
$f_{sw}$ = 300 kHz
L = 10 µH
$R_L$ = 25 mΩ
$C_{out}$ = 220 µF Electrolytic with $R_{C1}$ = 25 mΩ
plus 22 µF Ceramic with $R_{C2}$ = 5 mΩ
plus 50 × 0.1 µF Ceramics with 5 mΩ each, so $R_{C3}$ = 0.1 mΩ

Controller: TPS40200D, a nonsynchronous fixed frequency controller.

Controller Parameters (controller information is summarized in Table 1):

PWM Ramp Amplitude:

$$V_{ramp} = \frac{V_{cc}}{20} - 0.15V = 0.85V$$

Error Amplifier Open-Loop DC Gain: $A_{DC}$ = 10k

Error Amplifier Compensation Pole: 300 Hz

Feedback Reference Voltage: 0.696 V

**Step 1: Calculate the modulator gain using Equation 6:**

$$A_{\mathrm{mod}-CCM} = \frac{V_{cc}}{V_{ramp}} = \frac{20V}{0.85V} = 23.53 \quad \text{(or 27.4 dB)} \quad (12)$$

**Step 2: Calculate the Resistor Divider Values.**

Referring to Figure 12:

$$R_1 = R_{bottom}\left(\frac{V_{out}}{V_{ref}}-1\right) = 5.11k\left(\frac{5V}{0.696V}-1\right) = 31.6k \quad (13)$$

(5.11k was chosen for the closest match to standard 1% resistor values for the divider)

**Step 3: Calculate the filter's resonant frequency:**

$$f_{LC} = \frac{1}{2\pi\sqrt{L\cdot C_{out}}} = \frac{1}{2\pi\sqrt{10uH\cdot 247uF}} = 3.20\,kHz \quad (14)$$

**Step 4: Place the first zero slightly below the filter's resonant frequency:**

$$C_3 = \frac{1}{2\pi\cdot 0.9 f_{LC} R_1} = \frac{1}{1.8\pi f_{LC} R_1} = 1.75\,nF \text{ (use 1.8 nF)} \quad (15)$$

**Step 5: Place a pole at the crossover frequency:**

$$R_3 = \frac{1}{2\pi\, f_{crossover} C_3} = 4.42k \quad \text{(use 4.42 K)} \tag{16}$$

**Step 6: Calculate the required gain of the compensator at the desired crossover frequency:**

$$\left|H_{comp\_xover}\right| = \frac{1}{\left|\frac{V_{in}}{V_{ramp}} \cdot \frac{1+(C\,R_C)(j2\pi\ f_{crossover})}{1+\frac{R_L}{R}+(\frac{L}{R}+R_C\,C+R_L\,C+\frac{R_L\,R_C\,C}{R})(j2\pi\ f_{crossover})+\left(1+\frac{R_C}{R}\right)LC(j2\pi\ f_{crossover})^2}\right|}$$

$$= 1.35\,(or\ 2.61dB) \tag{17}$$

**Step 7: Set the gain of the compensator:**

$$R_2 = \left(R_1 \| R_3\right)\left|H_{comp\_xover}\right| = \left(31.6k \| 4.42k\right)\left(1.35\right) = 5.23k \quad \text{(use 5.23 k)} \tag{18}$$

**Step 8: Place a second zero just below the filter resonance:**

$$C_2 = \frac{1}{1.8\pi\, f_{LC} R_2} = \frac{1}{1.8\pi \cdot 3.02kHz \cdot 5.23k} = 10.56nF \quad \text{(use 10 nF)} \tag{19}$$

**Step 9: Place a second pole about a decade above the crossover frequency:**

$$C_1 = \frac{1}{2\pi \cdot 10 f_{crossover}\, R_2} = \frac{1}{20\pi \cdot 20kHz \cdot 5.23k} = 152\,pF \quad \text{(use 150 pF)} \tag{20}$$

**Step 10: Calculate or simulate the entire loop and adjust if necessary.**

The loop response can be calculated using Equation 21 through Equation 28.

$$H_{Loop}(s) = H_{\mathrm{mod}}(s) \cdot H_{Filter}(s) \cdot H_{Compensator}(s) \tag{21}$$

$$H_{\mathrm{mod}} = \begin{cases} \dfrac{V_{in}}{V_{ramp}} = \dfrac{20V}{0.85V} = 23.53 & (CCM\ or\ Forced\ CCM) \\ \dfrac{2V_{out}\left(1-\frac{V_{out}}{V_{in}}\right)}{v_{ramp}\, D_{DCM}\left(2-\frac{V_{out}}{V_{in}}\right)} & (DCM\ only) \end{cases} \tag{22}$$

$$\mathrm{H_{Filter}(s)} = \begin{cases} \text{See Transfer Functions for 3 Types of Output Capacitors} \\ \text{Given in Appendix A, Figure A5.} \end{cases} \tag{23}$$

$$H_{compensator}(s) = \frac{H_{OL}(s)}{1+H_{OL}(s)\beta(s)} \tag{24}$$

$$H_{OL}(s) = \frac{A_{DC}}{1 + \frac{s}{\varpi_{pole}}} \tag{25}$$

$$A_{DC} = Opamp\ DC\ Gain \tag{26}$$

$$\varpi_{pole} = 2\pi f_{pole} = Opamp\ Compensation\ Pole \tag{27}$$

$$\beta(s) = \frac{R_1 R_3 C_1 s\left(s + \frac{C_1 + C_2}{C_1 C_2 R_2}\right)\left(s + \frac{1}{R_3 C_3}\right)}{(R_1 + R_3)\left(s + \frac{1}{R_2 C_2}\right)\left(s + \frac{1}{(R_1 + R_3)C_3}\right)} \tag{28}$$

Following these steps results in the following final design (see Figure 14):

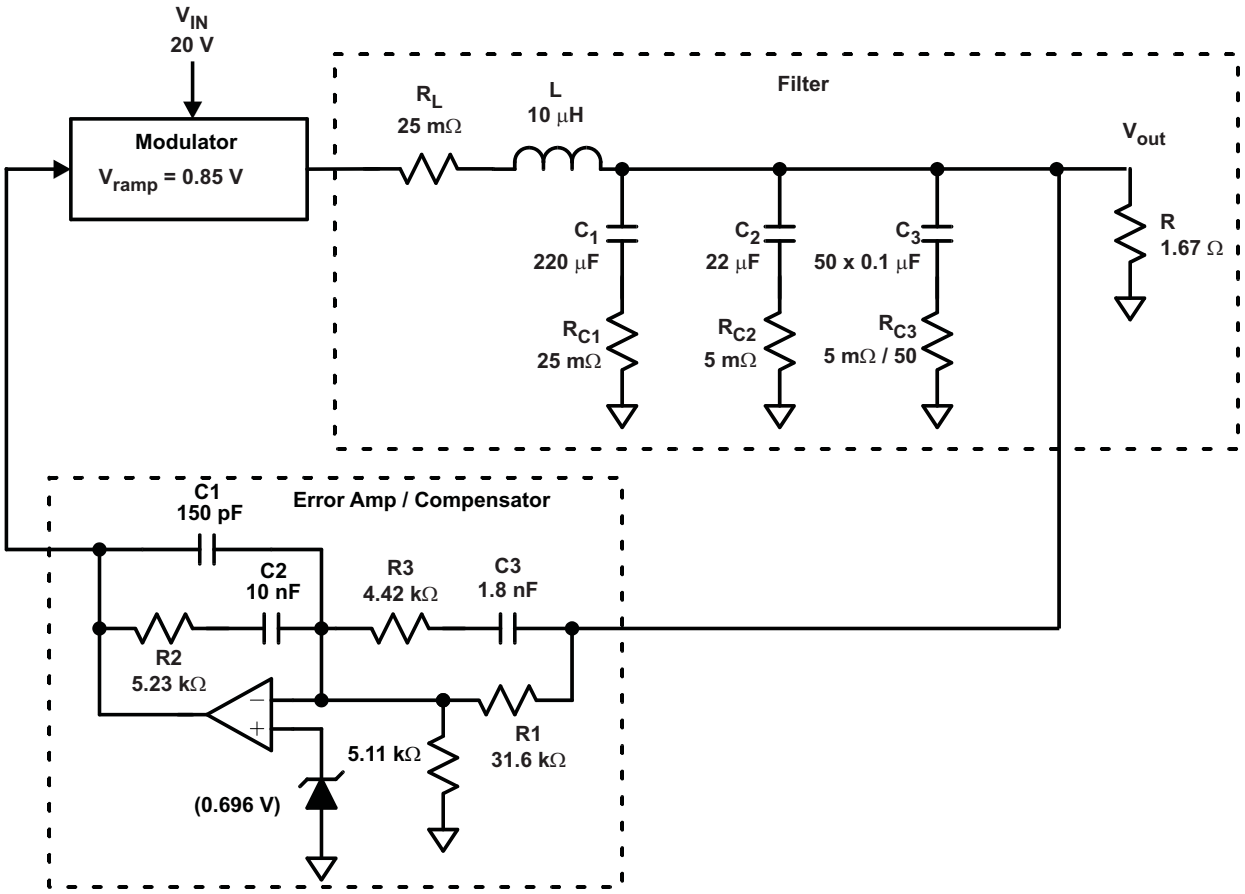



**Figure 14. Block Diagram of Example Design with Compensation.**

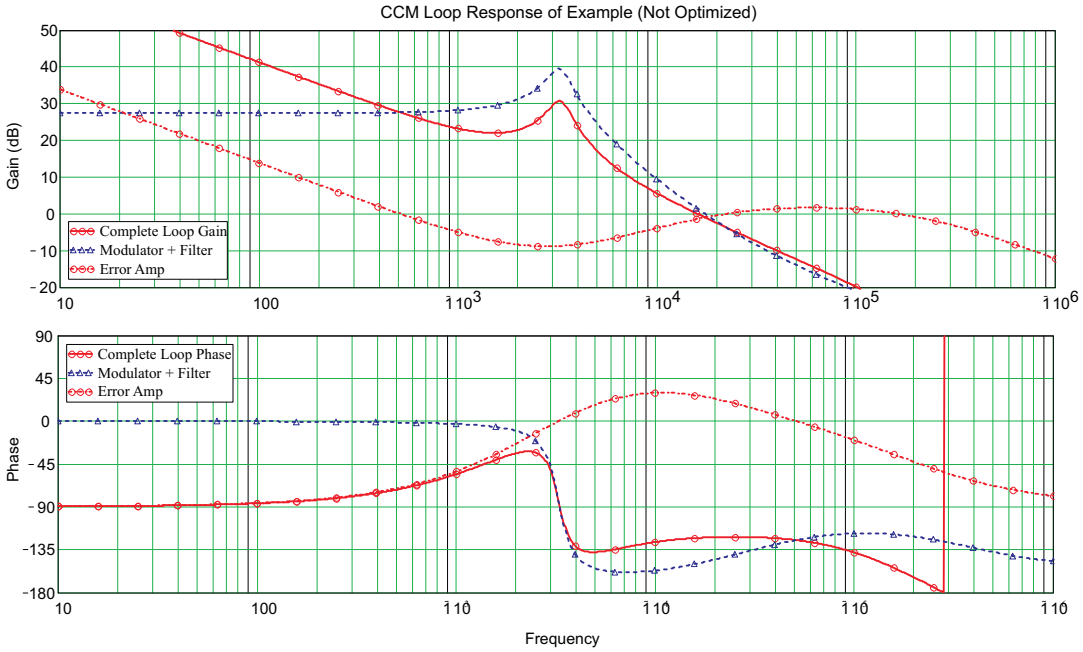



**Figure 15. Gain and Phase Response of Example Design. Crossover frequency is about 17kHz and the phase margin is about 60 degrees (as calculated, not optimized)**

The calculated gain and phase of the example circuit, with the closest standard component values to the calculated results, is shown in Figure 15. The crossover frequency is lower than the 20-kHz goal, and the loop phase margin is acceptable at about 60°.

The plots also show the contribution of the output filter and the error amplifier (including compensation).

Increasing the mid-band gain is one way to increase the crossover frequency, to achieve the goal of 20 kHz, if necessary (see Equation 18).

In this case, increasing R2 to 7.5k gives the following improved result (see Figure 16).

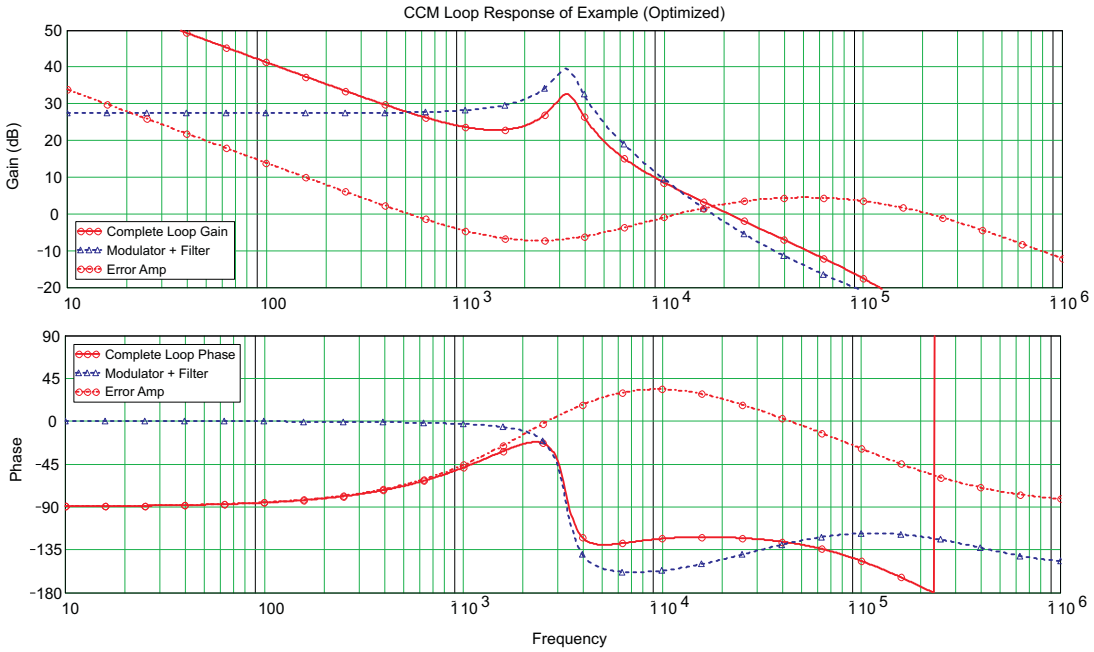



**Figure 16. Improving Loop Response by Changing R2 to 7.5k**

## 1.9 DCM Response of the Example Design

In DCM, the discontinuous nature of the modulator causes a damping of the output filter. The modulator gain is a function of the modulator duty cycle $D_{DCM}$, as well as the load resistance R (see Equation 7 and Equation 8). When the output current is at or above $Iout_{critical}$ (see Equation 6), the converter behaves according to the CCM equations previously used in this example. However, when the output current falls below $Iout_{critical}$, the frequency response is different because of this output filter damping effect. At the critical conduction point, the response abruptly changes, as shown in Figure 17(a). Figure 17(b) shows the response of the loop when the output current is at minimum, 20 mA.

Table 1 lists popular TI dc/dc controllers and converters, and gives the values for use in the design Equation 12 through Equation 28.

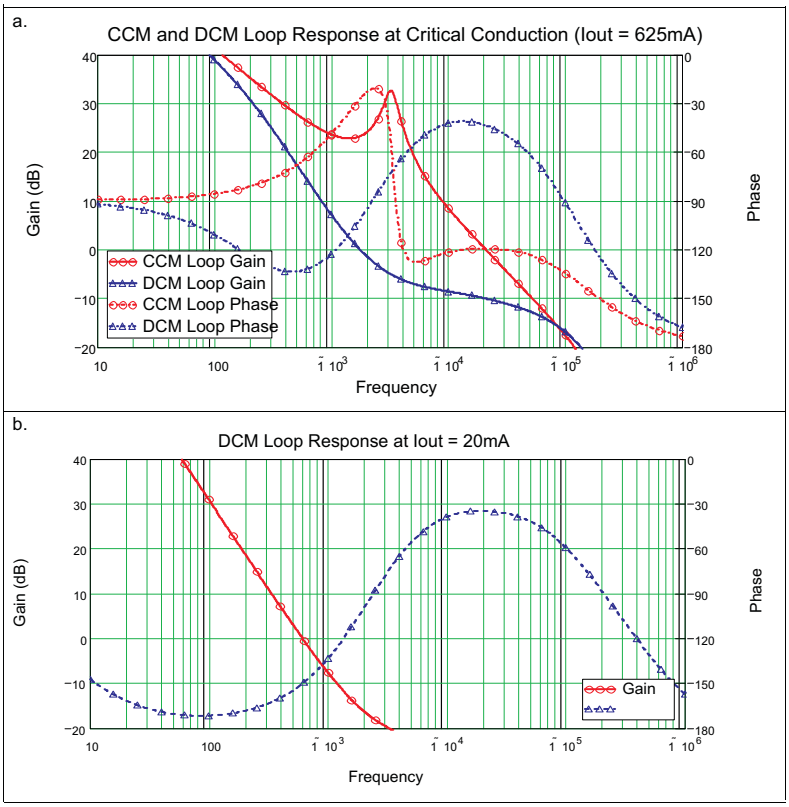



**Figure 17. Loop Response of the Design Example at Light Load.**
**(a) CCM and DCM Comparison at Critical Conduction;**
**(b) DCM Operation at Minimum Load Current of 20 mA**

## 2 Using a SPICE Simulator to Analyze Loop Stability

SPICE simulators are perfect for small-signal ac analysis of linear circuits, and that makes them perfect for calculating the loop gain and phase of a power supply.

The equations derived and presented in this document are useful for calculation using equation-based tools such as Mathcad™, Excel™, etc., but when the output filter becomes more complicated a SPICE-based solution makes the work much easier.

Figure 18 shows an example of using TINA [6] to perform the loop analysis for the CCM buck converter used in the preceding example. The advantage of using SPICE for this type of circuit becomes obvious, when comparing the SPICE schematic to the equations in Appendix A. However, SPICE does not design the compensator, so the design process given in Equation 12 through Equation 20 must still be followed.

TINA allows the use of embedded equations, in an Interpreter block. The Interpreter makes it convenient to perform some calculations based on circuit values and helps with documentation because the calculation results are a part of the schematic.

Because the design equations (for the modulator) are different in CCM and DCM, another TINA schematic is shown in Figure 19. This gives the solution for the DCM operation of the same circuit. Note that the DCM circuit is used only when the output current is less than the critical current (the calculations are included in both TINA circuits).

Using a SPICE simulator like TINA allows more complex output filter structures, including effects of distributed power planes, high-frequency filters, ferrites, and other complex load reactances.

These TINA circuits give good results compared to the calculations. Figure 20 shows a comparison between TINA and the calculated results for the example circuit in CCM.

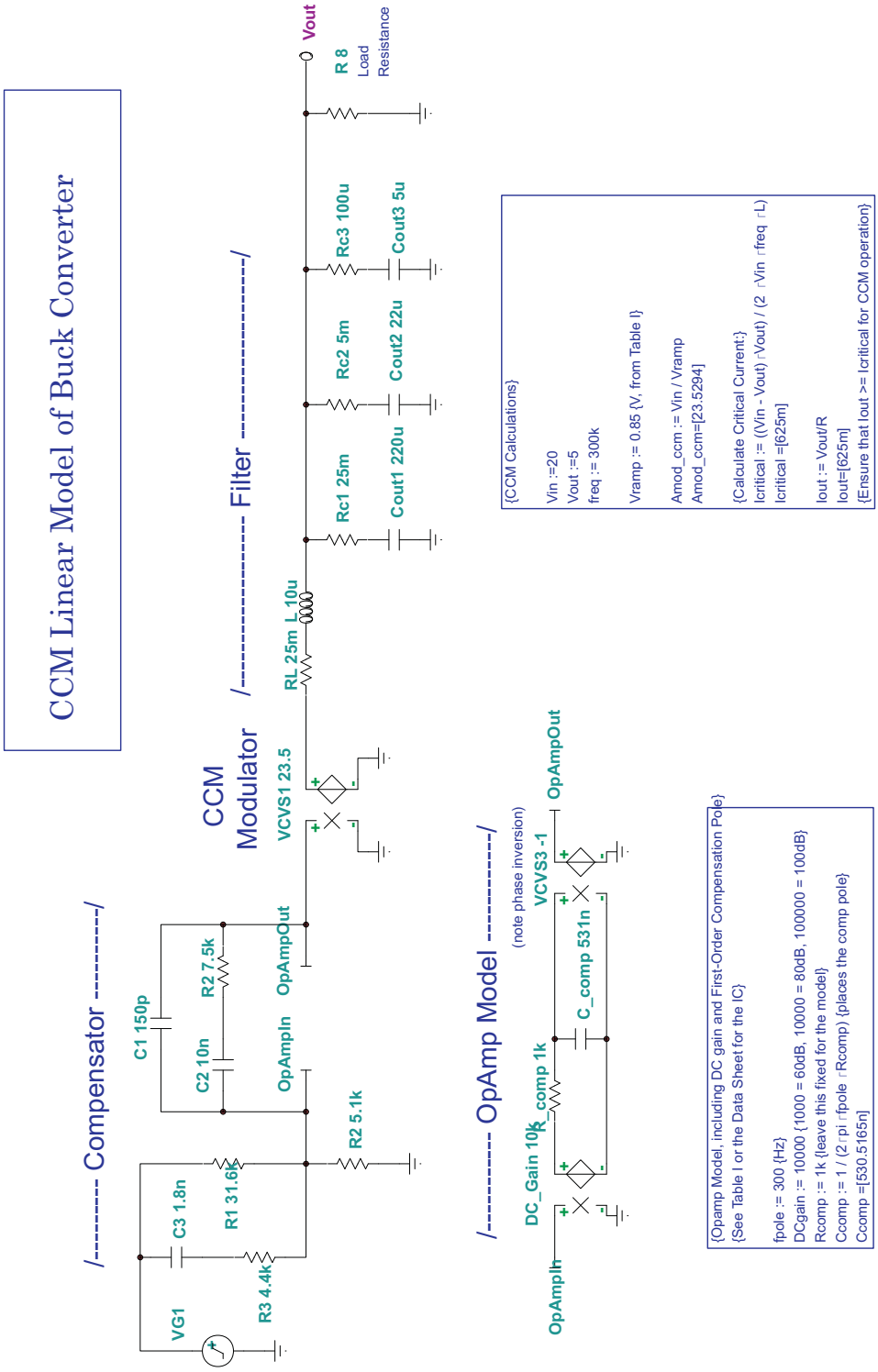



**Figure 18. TINA SPICE Simulation Schematic of the Example Circuit (CCM Version)**

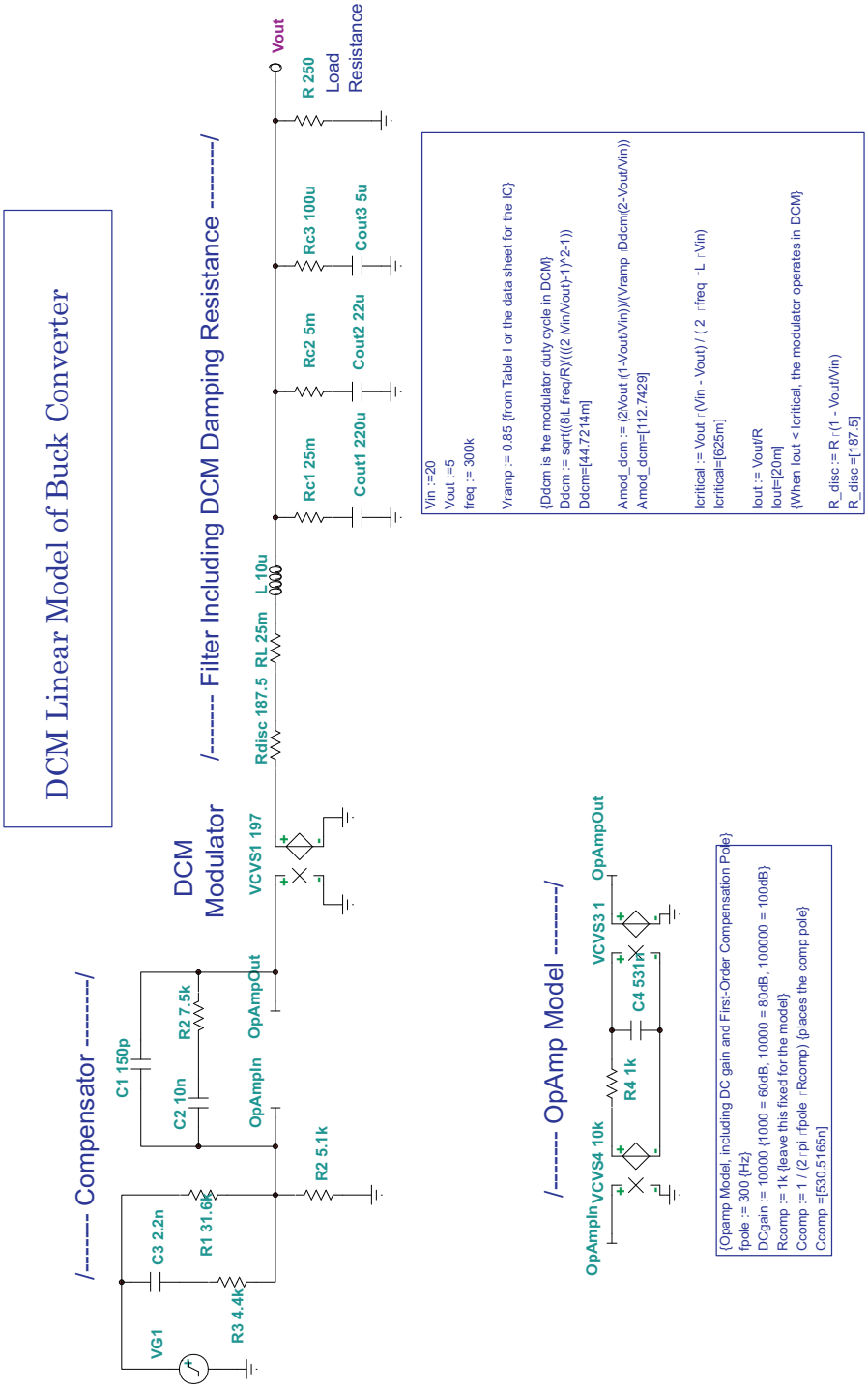



**Figure 19. TINA SPICE Simulation Schematic of the Example Circuit (DCM Version)**

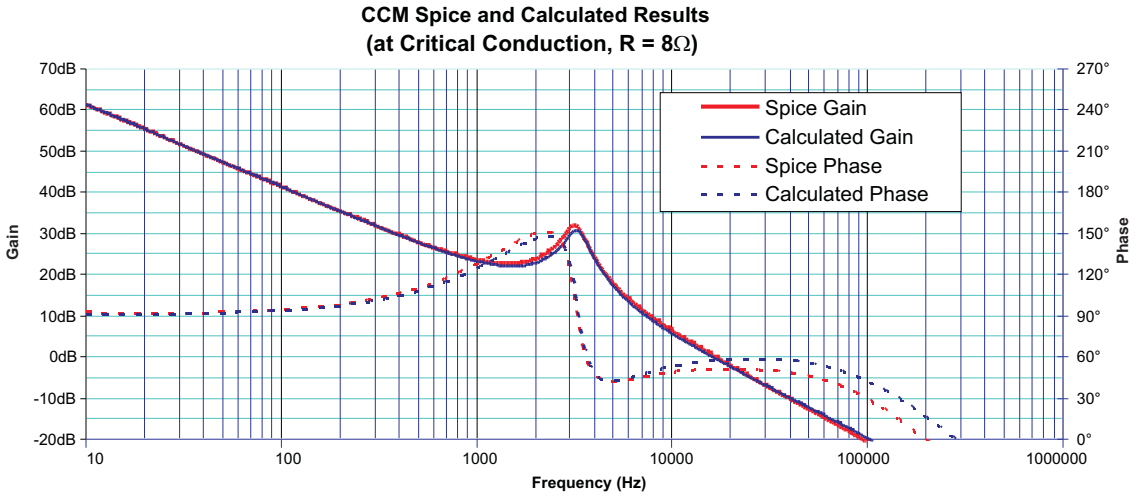



**Figure 20. Loop Gain and Phase for the Example Circuit, Using Both TINA (SPICE) and the Equations**

**Table 1. Design Parameters for Voltage Mode dc/dc Converters and Controllers**

| DEVICE | CCM ONLY | MODULATOR RAMP VOLTAGE | ERROR AMP DC VOLTAGE GAIN | ERROR AMP POLE | VOLTAGE REFERENCE |
|---|---|---|---|---|---|
| Equation Symbol → | — | $V_{ramp}$ | $A_{DC}$ | $\omega_{pole}$ | $V_{sense}$ |
| **Part numbers in *Bold Italic* are dual output converters.** | | | | | |
| TPS40000 | No | 0.93V | 18k | 550Hz | 0.700V |
| TPS40001 | Yes | 0.93V | 18k | 550Hz | 0.700V |
| TPS40002 | No | 0.93V | 18k | 550Hz | 0.700V |
| TPS40003 | Yes | 0.93V | 18k | 550Hz | 0.700V |
| TPS40004 | Yes | 0.93V | 18k | 550Hz | 0.700V |
| TPS40005 | Yes | 0.93V | 18k | 550Hz | 0.700V |
| TPS40007 | Yes | 0.93V | 18k | 550Hz | 0.700V |
| TPS40009 | Yes | 0.93V | 18k | 550Hz | 0.700V |
| TPS40020 | No | 0.93V | 18k | 550Hz | 0.690V |
| TPS40021 | Yes | 0.93V | 18k | 550Hz | 0.690V |
| TPS40040 | No | 0.87V | 18k | 550Hz | 0.600V |
| TPS40041 | Yes | 0.87V | 18k | 550Hz | 0.600V |
| TPS40050 | No | $2 \times \frac{V_{CC} - 3.48\ V}{V_{UVLO} - 3.48\ V}$ (1) | 10k | 500Hz | 0.700V |
| TPS40051 | Yes | | 10k | 500Hz | 0.700V |
| TPS40052 | Yes | | 10k | 500Hz | 0.700V |
| TPS40053 | Yes | | 10k | 500Hz | 0.700V |
| TPS40054 | No | | 10k | 500Hz | 0.700V |
| TPS40055 | Yes | | 10k | 500Hz | 0.700V |
| TPS40056 | Yes | | 10k | 500Hz | 0.700V |
| TPS40057 | Yes | | 10k | 500Hz | 0.700V |
| TPS40060 | No | | 10k | 1kHz | 0.700V |
| TPS40061 | Yes | | 10k | 1kHz | 0.700V |

(1) $V_{UVLO}$ is the programmed value of undervoltage lockout. See data sheet.

**Table 1. Design Parameters for Voltage Mode dc/dc Converters and Controllers (continued)**

| DEVICE | CCM ONLY | MODULATOR RAMP VOLTAGE | ERROR AMP DC VOLTAGE GAIN | ERROR AMP POLE | VOLTAGE REFERENCE |
|---|---|---|---|---|---|
| Equation Symbol → | — | $V_{ramp}$ | $A_{DC}$ | $\omega_{pole}$ | $V_{sense}$ |
| TPS40070 | No | $2 \times \frac{V_{CC} - 0.4\ V}{V_{UVLO} - 0.4\ V}$ (1) | 316 | 31kHz | 0.700V |
| TPS40071 | Yes | | 316 | 31kHz | 0.700V |
| TPS40074 | Yes | | 316 | 31kHz | 0.700V |
| TPS40075 | Yes | | 316 | 31kHz | 0.700V |
| TPS40077 | Yes | | 10k | 1kHz | 0.700V |
| TPS40100 | Yes | 0.5V | 10k | 500Hz | 0.690V |
| TPS40190 | Yes | 0.75V | 1k | 5kHz | 0.591V |
| TPS40192 | Yes | 0.75V | 1k | 5kHz | 0.591V |
| TPS40193 | Yes | 0.75V | 1k | 5kHz | 0.591V |
| TPS40195 | Yes | 1.0V | 1k | 10kHz | 0.591V |
| TPS40200 | No | (Vcc / 20) – 0.15V | 10k | 300Hz | 0.696V |
| TPS43000 | Pin Sel | 1V | ? | (GBW = 5MHz) | 0.800V |
| ***TPS51020*** | Pin Sel | $0..35V + 0.017 \times V_{CC}$ | 10k | 250Hz | 0.850V |
| ***TPS5124*** | No | 0.68V | 316 | 8kHz | 0.850V |
| TPS5410 | No | *Internally Compensated* (2) | | | 1.221V |
| TPS54110 | Yes | 1.0V | 316k | 16Hz | 0.891V |
| TPS5420 | No | *Internally Compensated* (2) | | | 1.221V |
| TPS5430 | No | *Internally Compensated* (2) | | | 1.221V |
| TPS54310 | Yes | 1.0V | 316k | 16Hz | 0.891V |
| TPS5431x | Yes | *Internally Compensated* (2) | | | See (3) |
| TPS5435x | Yes | $V_{CC}$ / 8 | 10k | 280Hz | 0.891V |
| TPS5450 | No | *Internally Compensated* (2) | | | 1.221V |
| TPS5455x | Yes | $V_{CC}$ / 8 | 10k | 280Hz | 0.891V |
| TPS54610 | Yes | 1.0V | 316k | 16Hz | 0.891V |
| TPS5461x | Yes | *Internally Compensated* (2) | | | See (3) |
| TPS54910 | Yes | 1.0V | 316k | 16Hz | 0.891V |
| TPS6211x | Pin Sel | *Internally Compensated* (2) | | | 1.153V |
| TPS54810 | Yes | 1.0V | 316k | 16Hz | 0.891V |
| TPS54972 | Yes | 1.0V | 316k | 16Hz | External |
| TPS54980 | Yes | 1.0V | 316k | 16Hz | 0.891V |
| TPS54672 | Yes | 1.0V | 316k | 16Hz | External |
| TPS54680 | Yes | 1.0V | 316k | 16Hz | 0.891V |
| TPS54010 | Yes | 1.0V | 316k | 16Hz | 0.891V |
| TPS6220x | No | *Internally Compensated* (2) | | | 0.500V |
| TPS6222x | No | *Internally Compensated* (2) | | | 0.500V |
| ***TPS6240x*** | Pin Sel | *Internally Compensated* (2) | | | 0.600V |
| TPS6210x | Pin Sel | 1.0V | 10k | 1kHz | 0.800V |
| TPS6230x | Pin Sel | *Internally Compensated* (2) | | | 0.400V |
| TPS6232x | Pin Sel | *Internally Compensated* (2) | | | 0.400V |
| TPS6200x | Pin Sel | *Internally Compensated* (2) | | | 0.450V |
| TPS6202x | Pin Sel | *Internally Compensated* (2) | | | 0.500V |
| ***TPS62420*** | Pin Sel | *Internally Compensated* (2) | | | 0.600V |

(2) internally compensated device. Refer to the data sheet for acceptable component values.
(3) Fixed output voltage versions, no external resistor divider is used.

**Table 1. Design Parameters for Voltage Mode dc/dc Converters and Controllers (continued)**

| DEVICE | CCM ONLY | MODULATOR RAMP VOLTAGE | ERROR AMP DC VOLTAGE GAIN | ERROR AMP POLE | VOLTAGE REFERENCE |
|---|---|---|---|---|---|
| Equation Symbol → | — | $V_{ramp}$ | $A_{DC}$ | $\omega_{pole}$ | $V_{sense}$ |
| TPS6205x | Pin Sel | *Internally Compensated* (4) | | | 0.500V |
| TPS62350 | Pin Sel | *Internally Compensated* (4) | | | Programmable |
| TPS6204x | Pin Sel | *Internally Compensated* (4) | | | 0.500V |

(4) internally compensated device. Refer to the data sheet for acceptable component values.

## 2.1 Conclusions

Stabilizing a buck converter is a complicated control loop problem. The compensation block of a buck dc/dc converter is required to provide an acceptable degree of stability to the regulator circuit. Design of the compensator is complicated by the variety of output filter designs possible in modern electronic systems. Solutions are presented for output filters with one, two, and three different types of capacitors (with different ESRs). A design example is presented which can be used as a template for analysis of any voltage mode buck converter. Because of the variety of integrated circuits available for buck converters, and the differences between them, a table is provided to summarize the data needed for the solutions presented. For other integrated circuits, this data can be taken from the data sheet.

## 2.2 Acknowledgments

Note that TINA, a SPICE simulator [6] was used to generate several plots, and also to provide transfer functions for the filter networks.

## 2.3 References

1. *Under the Hood of Low-Voltage DC/DC Converters* application report (SLUP206)
2. *Understanding Buck Power Stages in Switch Mode Power Supplies* application report (SLVA057)
3. Erickson, R, and Maksimovic, Dragan (2001). *Fundamentals of Power Electronics*. Assinippi Park, Massachusetts: Kluwer Academic Publishers.
4. Hale, F. J. (1973). *Introduction to Control System Analysis and Design*. New Jersey: Prentice-Hall, Inc.
5. Vorperion, V. (1990).Simplified Analysis of PWM Converters using the Model of the PWM Switch, part II: Discontinuous Conduction Mode. *IEEE Transactions on Aerospace and Electronic Systems*. 26, 497-505.
6. DesignSoft, Kft. (2007). TINA (Industrial Version 7.0) [Computer software]. New York: Freeman.

## Appendix A Filter Transfer Functions

This appendix gives the mathematical transfer functions as a function of frequency for some common configurations. The output filter consists of an inductor, with loss, plus one or more types of output capacitors. When different types of output capacitors are used, the response of the filter can be complex. Adding together the total capacitance, and assuming that the ESRs are all in parallel, although making the filter simpler, may not give an accurate solution. The ideal circuit model treats each capacitor separately, resulting in a more complex filter solution. The solutions for one-, two-, and three-output capacitor types are given in the following discussion to be used in the loop response calculations.

Vorperion [5] derives the modulator and output filter transfer functions in DCM. His results are presented in a form where the modulator and the output filter response are combined, and it may not be entirely clear where the effects of the modulator end, and the filter begins. It is more convenient to separate the effects of these two sections of the converter, so that the solution of the filter for CCM may be used to find the solution of the filter in DCM. This greatly reduces the effort required to deduce the correct model for DCM, given a solution for the CCM filter.

It may be unclear why the filter response is different in CCM versus DCM. The difference lies in the nature of the modulator's driving impedance. In CCM, the modulator's output impedance is comparatively low, as it is made up mostly of the power switch losses, which are usually quite low by design (compared to the filter impedance) at the switching frequency. In DCM, during a portion of each switching cycle, the modulator appears to have infinite impedance (both power switches are off). In this case, the average modulator output impedance may not be low enough to be negligible, when considering the filter response.

Vorperion's model of the modulator and output filter is:

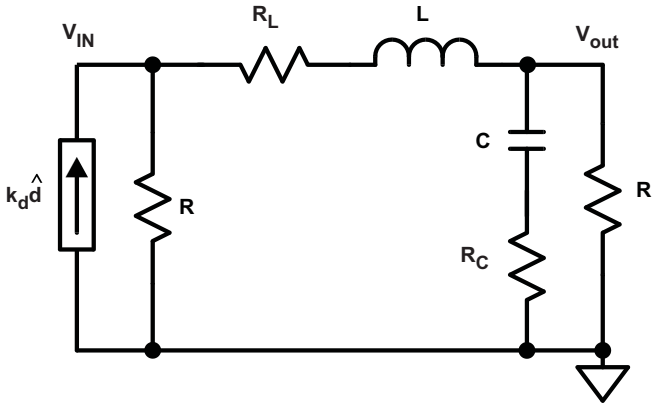



**Figure A-1. Vorperion's Model of the Modulator and Filter in DCM.**

The transfer function of this DCM model is given as:

$$\frac{\hat{v}_o}{\hat{d}} = H_d \frac{1 + s/s_{z1}}{1 + a_1 s + a_2 s^2} \tag{A-1}$$

$$H_d = \frac{2 I_o}{D} \cdot \frac{r R}{r + R + R_L} \tag{A-2}$$

$$r = R \cdot \left(1 - \frac{V_{out}}{V_{in}}\right) \tag{A-3}$$

$$k_d = \frac{2 I_o}{D} \tag{A-4}$$

$$I_o = \frac{V_{out}}{R} \tag{A-5}$$

$$s_{z1} = \frac{1}{R_{C1} C_1} \tag{A-6}$$

$$a_1 = \frac{L}{R_L + r + R} + C_1 \cdot \left[R_{C1} + R \| (r + R_L)\right] \tag{A-7}$$

$$a_2 = L C_1 \frac{R_{C1} + R}{R_L + r + R} \tag{A-8}$$

D = the duty cycle of the modulator

In order to separate Vorperion's result into a filter component and a modulator component, and show its relationship to the CCM case, start with the solution of the loss filter (the inductor and the capacitor each have a series resistance) in the CCM case (with an ideal voltage source):

$$\frac{\hat{v}_{out}}{\hat{v}_{in}} = H_{Filter}(s) = \frac{R + (R \cdot C \cdot R_C)s}{R + R_L + (L + R_C \cdot C \cdot R + R_L \cdot C \cdot R + R_L \cdot R_C \cdot C)s + (R + R_C) L C s^2} \tag{A-9}$$

Vorperion's model uses a current source. If this is converted to an ideal voltage source with resistance, the model becomes:

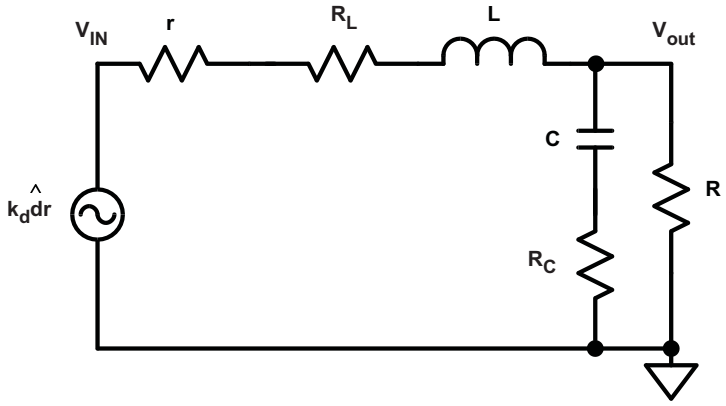



**Figure A-2. Vorperion's DCM Model With an Ideal Voltage Source**

This filter can be analyzed exactly as in the CCM case, exchanging $R_L$ for $R_L$ + r. Solving Vorperion's equation in Equation A-1 results in:

$$\frac{\hat{v}_{out}}{\hat{d}} = \frac{2 I_o r R}{D_{DCM} (R + r + R_L)} \cdot \frac{1 + C R_C s}{1 + \left(\frac{L + R_C C r + R_C C R + R_L R_C C + C R r + C R R_L}{R + r + R_L}\right)s + \left(\frac{(R + R_C) L C}{R + r + R_L}\right)s^2} \tag{A-10}$$

The second term in Equation A-10 is exactly the same result as the CCM filter response, after changing $R_L$ to $R_L$ + r. From this result it can be concluded that Vorperion's DCM result contains the CCM filter result, along with a frequency-independent term $\frac{2 I_o r}{D_{DCM}\left(2-\frac{V_{out}}{V_{in}}\right)}$

Vorperion's excitation is taken as the duty cycle of the modulator block, rather than the control voltage which is the input to the modulator. It is convenient at this point to modify Vorperion's result; refer to $v_c$, the error amplifier output and the input to the modulator. The conversion can be made in this way:

$$\frac{d V_{out}}{d D}=\frac{d V_{out}}{d\left(\frac{v_c}{v_{ramp}}\right)}=\frac{1}{\frac{1}{v_{ramp}}}\cdot\left(\frac{d V_{out}}{d v_c}\right)=v_{ramp}\cdot\frac{d V_{out}}{d v_c} \tag{A-11}$$

Therefore, in order to express Vorperion's result relative to the control voltage as an input rather than the duty cycle of the modulator, divide the result by $v_{ramp}$. Then Equation A-10 becomes:

$$\frac{\hat{v}_{out}}{\hat{v}_{control}}=\frac{2 I_o r R}{V_{ramp} D_{DCM}\left(R+r+R_L\right)}\cdot \frac{1+C R_C s}{1+\left(\frac{L+R_C C r+R_C C R+R_L R_C C+C R r+C R R_L}{R+r+R_L}\right)s+\left(\frac{(R+R_C) L C}{R+r+R_L}\right)s^2} \tag{A-12}$$

Now, Vorperion's result for the modulator plus filter has been separated into two components:

The second term of Equation A-12 can be obtained by knowledge of the transfer function of the passive output filter, making the substitution $R_L \rightarrow R_L$ + r, and then making the substitution for **r** given in Equation A-3.

The first term in Equation A-12 is frequency independent and can be treated as the modulator voltage gain, with its control input coming from the error amplifier. Although it may not be entirely accurate to call this the *modulator gain*, it serves the purpose in that it is the block between the error amplifier and the output filter, and it behaves as an ideal voltage source. Therefore, referring to this term is more of a mathematical convenience for the purposes of using the block diagram of the generalized buck converter shown in Figure A-3.

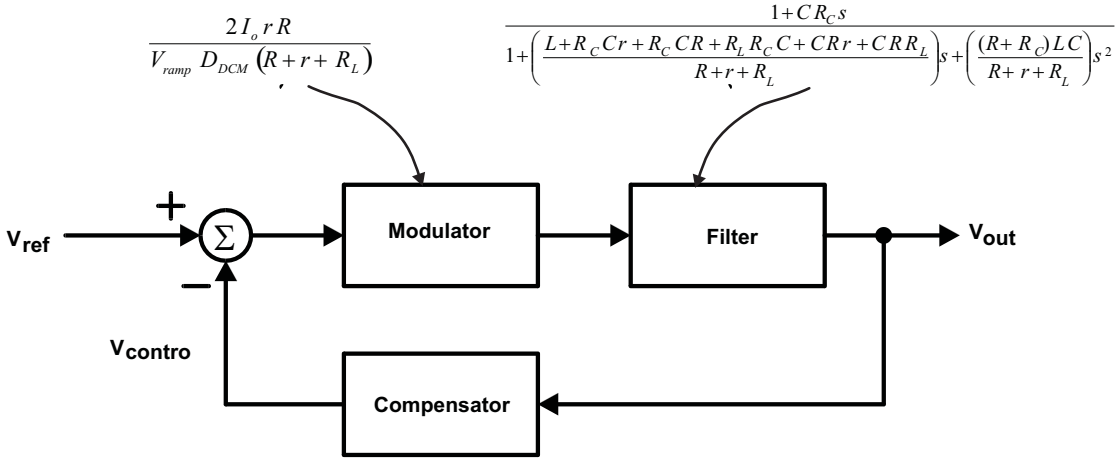



**Figure A-3. General Block Diagram of a Buck Converter With DCM Modulator and Filter Transfer Functions**

Another step of simplification can be made to Equation A-12. In DCM, the output (load) resistance is almost certainly much larger than the dc resistance of the inductor or the capacitor; that is, R >>$R_C$ and R >> $R_L$. Making this approximation, and also making a substitution for r as shown in Equation A-3, Equation A-12 reduces to:

$$\frac{\hat{v}_{out}}{\hat{v}_{control}} = \frac{2V_{out}\left(1-\frac{V_{out}}{V_{in}}\right)}{v_{ramp}\,D_{DCM}\left(2-\frac{V_{out}}{V_{in}}\right)} \cdot \frac{1+(C\,R_C)\,s}{1+\left[\frac{\frac{L}{R}+C\,R\left(1-\frac{V_{out}}{V_{in}}\right)+C\,(R_C+R_L)}{2-\frac{V_{out}}{V_{in}}}\right]s+\frac{L\,C}{2-\frac{V_{out}}{V_{in}}}s^2} \quad \text{(A-13)}$$

In CCM, the assumption that the parasitic resistances are much smaller than R may not be valid.

Equation A-13 is the complete transfer function of the modulator plus output filter for a DCM buck converter with a single type of output capacitor.

Although this discussion focuses on the output filter, note that the modulator in a DCM converter can be described by the first term in Equation A-13, namely:

$$A_{\mathrm{mod\_}DCM} = \frac{2V_{out}\left(1-\frac{V_{out}}{V_{in}}\right)}{v_{ramp}\,D_{DCM}\left(2-\frac{V_{out}}{V_{in}}\right)} \quad \text{(A-14)}$$

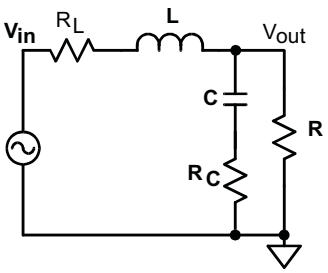
where $D_{DCM}$ is the duty cycle in DCM:

$$D_{DCM} = \sqrt{\frac{\frac{8L\,f_{sw}}{R}}{\left(\frac{2V_{in}}{V_{out}}-1\right)^2-1}} \quad \text{(A-15)}$$

This DCM modulator gain is frequency independent and applies to all voltage mode buck designs, regardless of the complexity of the output filter.

In the following examples of DCM and CCM filters, the results are obtained as previously described, including the simplifications resulting from R >> $R_C$ and R >> $R_L$ in DCM.

**a.**




**b.**

**CCM Filter Response**

$$H_{Filter-CCM}(s) = \frac{1 + (C R_C)\, s}{1 + \frac{R_L}{R} + \left( \frac{L}{R} + R_C\, C + R_L\, C + \frac{R_L\, R_C\, C}{R} \right) s + \left( \frac{R + R_C}{R} \right) L\, C\, s^2}$$

**c.**

**DCM Filter Response**

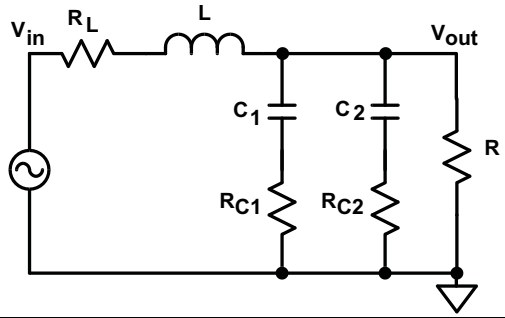
$$H_{Filter-DCM}(s) = \frac{1 + R_C\, C\, s}{1 + a_1\, s + \frac{L\, C}{2 - \frac{V_{out}}{V_{in}}} s^2}$$

where

$$a_1 = \frac{\frac{L}{R} + R\, C \left( 1 - \frac{V_{out}}{V_{in}} \right) + \left( R_C + R_L \right) C}{2 - \frac{V_{out}}{V_{in}}}$$

**Figure A-4. CCM and DCM Filter Transfer Functions for Filters with One Type of Output Capacitor**

**a.**




**b.**

**CCM Filter Response**

$$H_{Filter}(s) = \frac{1 + (R_{C1}C_1 + R_{C2}C_2)\,s + (R_{C2}C_2R_{C1}C_1)s^2}{1 + a_1 s + a_2 s^2 + a_3 s^3}$$

*where*

$$a_1 = \frac{L}{R} + (R_{C1}C_1 + R_{C2}C_2) + \frac{R_L}{R}(C_1 + C_2)$$

$$a_2 = \left[L(C_1 + C_2) + R_L C_1 C_2 (R_{C1} + R_{C2}) + R_{C2}R_{C1}C_2C_1\right] + \frac{L}{R}(R_{C1}C_1 + R_{C2}C_2)$$

$$a_3 = \frac{L}{R} C_1 C_2 \left[R(R_{C1} + R_{C2}) + R_{C1}R_{C2}\right]$$

**c.**

**DCM Filter Response**

$$H_{Filter}(s) = \frac{1 + (R_{C1}C_1 + R_{C2}C_2)\,s + R_{C2}C_2R_{C1}C_1R\,s^2}{1 + a_1 s + a_2 s^2 + a_3 s^3}$$

*where*

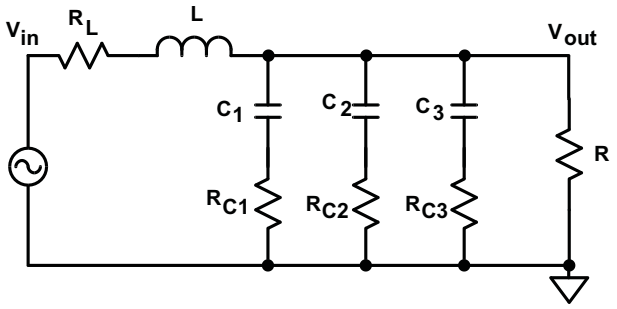
$$a_1 = \frac{R(C_1 + C_2)\left(1 - \frac{V_{out}}{V_{in}}\right) + \frac{L}{R} + (C_1R_{C1} + C_2R_{C2}) + \left(1 - \frac{V_{out}}{V_{in}}\right)(C_1R_{C1} + C_2R_{C2})}{2 - \frac{V_{out}}{V_{in}}}$$

$$a_2 = \frac{L(C_1(1 + R_{C1}) + C_2(1 + R_{C2})) + R_{C1}C_1R_{C2}C_2 + R\left(1 - \frac{V_{out}}{V_{in}}\right)C_1C_2(R_{C1} + R_{C2})}{2 - \frac{V_{out}}{V_{in}}}$$

$$a_3 = \frac{LC_1C_2\left[R(R_{C1} + R_{C2}) + R_{C1}R_{C2}\right]}{R\left(2 - \frac{V_{out}}{V_{in}}\right)}$$

**Figure A-5. CCM and DCM Filter Transfer Functions for Filters With Two Types of Output Capacitor**

**a.**




**b.**

**CCM Filter Response**

$$H_{filter-CCM} = \frac{1+\left(R_{C1}C_1 + R_{C2}C_2 + R_{C3}C_3\right)\cdot s + \left(R_{C2}C_2R_{C1}C_1 + R_{C3}C_3R_{C1}C_1 + R_{C3}C_3R_{C2}C_2\right)\cdot s^2 + R_{C3}C_3R_{C2}C_2R_{C1}C_1\, s^3}{1+a_1\cdot s + a_2\cdot s^2 + a_3\cdot s^3 + a_4\cdot s^4}$$

where:

$$a_1 = R_L\left(C_3 + C_2 + C_1\right) + \frac{L}{R} + \left(R_{C1}C_1 + R_{C2}C_2 + R_{C3}C_3\right)$$

$$a_2 = R_L\left(C_3R_{C2}C_2 + C_2R_{C1}C_1 + C_3R_{C1}C_1 + R_{C2}C_2C_1 + R_{C3}C_3C_1 + R_{C3}C_3C_2\right) + \\ + \left[L\left(C_1 + C_2 + C_3\right) + R_{C3}C_3R_{C1}C_1 + R_{C2}C_2R_{C1}C_1 + R_{C3}C_3R_{C2}C_2\right] + \frac{L}{R}\left(R_{C3}C_3 + R_{C1}C_1 + R_{C2}C_2\right)$$

$$a_3 = \frac{L}{R}\left[R_{C3}\,C_3\,R_{C1}\,C_1 + \left(C_3\,R_{C2}\,C_2 + C_2\,R_{C1}\,C_1 + C_3R_{C1}\,C_1 + R_{C2}\,C_2\,C_1 + R_{C3}\,C_3\,C_1 + R_{C3}\,C_3\,C_2\right)R + R_{C2}\,C_2\,R_{C1}\,C_1 + R_{C3}\,C_3\,R_{C2}\,C_2\right] \\ + R_L\left(C_3\,R_{C2}\,C_2\,R_{C1}\,C_1 + R_{C3}\,C_3\,R_{C2}\,C_2\,C_1 + R_{C3}\,C_3\,C_2\,R_{C1}\,C_1\right) + R_{C3}\,C_3\,R_{C2}\,C_2\,R_{C1}\,C_1$$

$$a_4 = \left(R_{C2}\,R_{C1} + R_{C3}\,R_{C1} + R_{C3}\,R_{C2} + \frac{R_{C3}\,R_{C2}\,R_{C1}}{R}\right)\cdot C_3\,C_2\,C_1\,L$$

**Figure A-6. CCM Filter Transfer Functions for Filters With Three Types of Output Capacitor (a, b)**

**c.**

**DCM Filter Response**

$$H_{filter-DCM} = \frac{1+\left(R_{C1}C_1 + R_{C2}C_2 + R_{C3}C_3\right)\cdot s + \left(R_{C2}C_2R_{C1}C_1 + R_{C3}C_3R_{C1}C_1 + R_{C3}C_3R_{C2}C_2\right)s^2 + R_{C3}C_3R_{C2}C_2R_{C1}C_1s^3}{1+\dfrac{a_1s + a_2s^2 + a_3s^3 + a_4s^4}{2-\dfrac{V_{out}}{V_{in}}}}$$

$$a_1 = \frac{L}{R} + \left(R_{C1}C_1 + R_{C2}C_2 + R_{C3}C_3\right) + \left(1-\frac{V_{out}}{V_{in}}\right)\left[R\left(C_3 + C_2 + C_1\right) + R_{C1}C_1 + R_{C2}C_2R_{C3}C_3\right]$$

$$a_2 = R\left(1-\frac{V_{out}}{V_{in}}\right)\left[C_3C_2\left(R_{C2}+R_{C3}\right) + C_2C_1\left(R_{C1}+R_{C2}\right) + C_3C_1\left(R_{C1}+R_{C3}\right)\right] + L\left(C_1+C_2+C_3\right) + \frac{L}{R}\left(R_{C3}C_3 + R_{C1}C_1 + R_{C2}C_2\right)$$
$$+ \left(R_{C3}C_3R_{C1}C_1 + R_{C2}C_2R_{C1}C_1 + R_{C3}C_3R_{C2}C_2\right)\left(2-\frac{V_{out}}{V_{in}}\right)$$

$$a_3 = L\left[C_3C_2\left(R_{C2}+R_{C3}\right) + C_2C_1\left(R_{C1}+R_{C2}\right) + C_3C_1\left(R_{C1}+R_{C3}\right)\right] + \left(2-\frac{V_{out}}{V_{in}}\right)C_1C_2C_3R_{C1}R_{C2}R_{C3}$$
$$+ R\left(1-\frac{V_{out}}{V_{in}}\right)C_1C_2C_3\left(R_{C1}R_{C2} + R_{C3}R_{C2} + R_{C3}R_{C1}\right)$$

$$a_4 = \left(R_{C2}R_{C1}R + R_{C3}R_{C1}R + R_{C3}R_{C2}R + R_{C3}R_{C2}R_{C1}\right)\cdot\frac{C_3C_2C_1L}{R}$$

**Figure A-7. DCM Filter Transfer Functions for Filters With Three Types of Output Capacitor (c)**

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