

XILINXPWR-082 EVM (HPA-082 board)
SWIFT™ (TPS54xxx series) DC/DC Converter-based Power Management Solution
Providing $I_{CCINT}=6A$ from $V_{IN}=5V$

SUPPORTS:

- Virtex-II Pro™ Design 2 (PR220) - <http://www-s.ti.com/sc/techlit/slva181.pdf>
- Spartan™-3 Design 4 (PR216) - <http://www-s.ti.com/sc/techlit/slva177.pdf>
 - o Requires resistor R7 be changed to 28.7kΩ to generate $V_{CCINT}=1.2V$
 - o RocketIO linear regulators (U4-U7) are not needed
- Virtex™-II Design 2 (PR219) - <http://www-s.ti.com/sc/techlit/slva180.pdf>
 - o Requires linear regulator U2 be changed to TPS79433 to provide V_{CCAUX}
 - o RocketIO linear regulators (U4-U7) are not needed

FEATURES:

- High efficiency minimizes heat
- Interchange SWIFT™ device to support 1.5 A to 9 A load currents
 - o 1.5A and 3A synchronous SWIFT devices are pin-pin compatible
 - o 6A, 8A, and 9A synchronous SWIFT devices are pin-pin compatible
- Use of the TPS54x10 adjustable devices allow
 - o use of smallest inductor and/or specific type of output capacitor
 - o flexibility to re-compensate as needed, depending on the bypass/decoupling capacitors used with the FPGA
- In-rush current (for charging decoupling caps and FPGA start-up) that places a demand on the input power supply is minimized by the use of optional
 - o Integrated soft-start configured with an capacitor to provide 10 ms rise time for V_{CCINT} and V_{CCO}
 - o Sequencing of V_{CCINT} , V_{CCAUX} , then V_{CCO} using PWRGD and ENABLE
- High UVLO trip point and integrated soft-start of the SWIFT™ devices eliminates the need for an external Supply Voltage Supervisor (SVS) to monitor the input rail.
- RocketIO™ powered by ultra- low noise, high PSRR (for rejecting noise at the input, preventing it from translating to the output) low dropout linear regulators (LDOs), TPS79xxx and TPS786xx. This series has been qualified by Xilinx to replace LT1963.
- Additional V_{CCO} rails easily added and sequenced (if desired) using the TPS54xxx PWRGD and ENABLE.
- The design meets Xilinx's V_{CCINT} and V_{CCO} start-up profile requirements, where applicable, including monotonic voltage ramp, in-rush current and power voltage ramp time requirements.

IMPORTANT WEB LINKS:

- Link to the TI home page for Xilinx FPGA power management solutions at <http://www.ti.com/xilinuxfpga> for more information and other reference designs.
- Link to datasheets at <http://focus.ti.com/lit/ds/symlink/TPS54610.pdf> and <http://focus.ti.com/lit/ds/symlink/tps79425.pdf>.
- Link to SWIFT™ design software tool at <http://focus.ti.com/docs/toolsw/folders/print/swift-sw.html> to assist further optimization/customization of design.

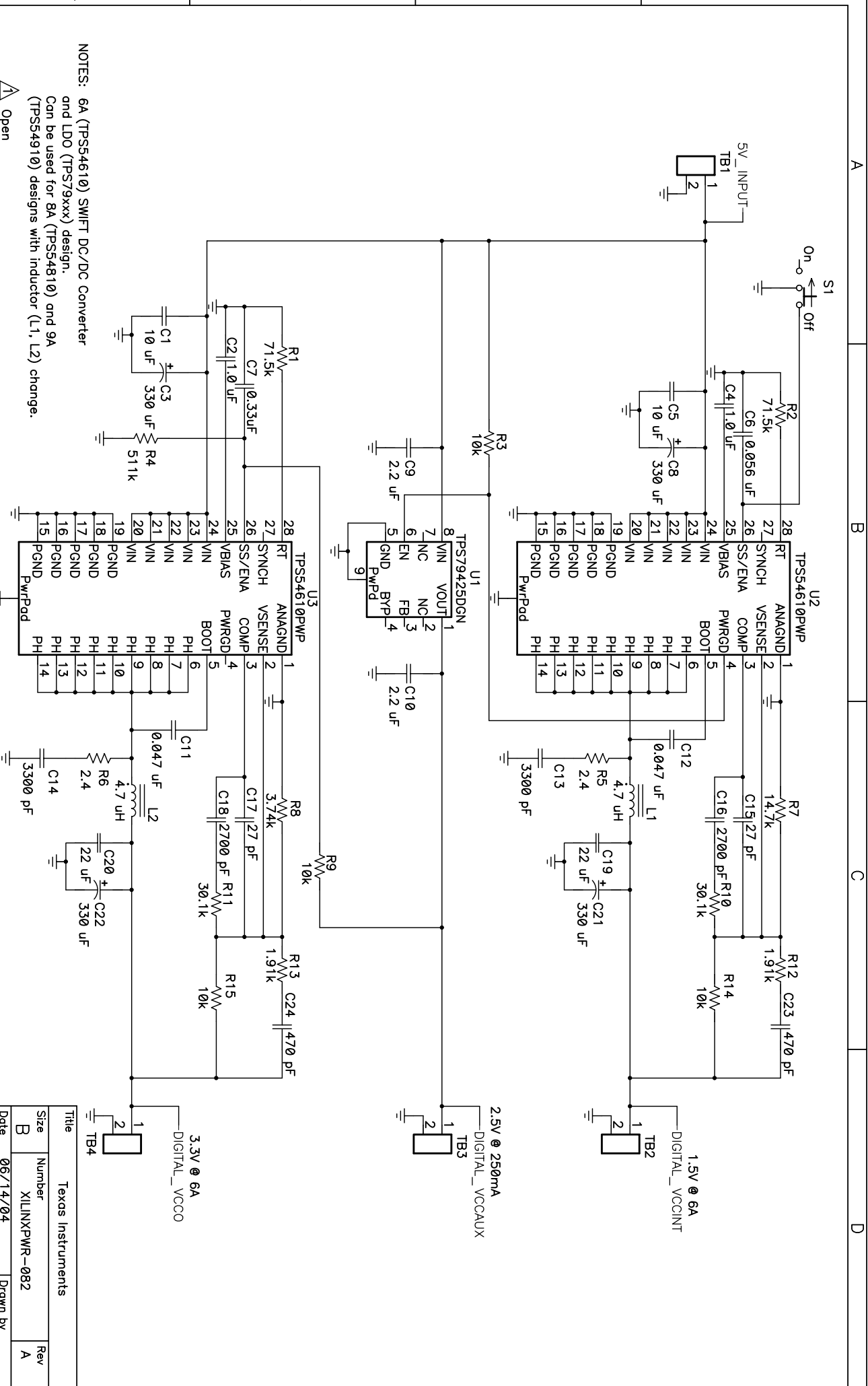
IMPLEMENTATION NOTES:

- **Sequencing:** Although Xilinx FPGAs **do NOT require it**, this reference design employs sequencing. This practice is consistent with good power supply design and prevents the input power supply from being pulled down due to supporting in-rush currents for charging large capacitive loads.
- **Additional Capacitance:**
 - o The TPS54610's have been compensated to allow for up to the following additional capacitance on each rail:
 - 12 uF in ceramics in parallel with
 - two 330 uF capacitors, each with ESR between 0.1 and 2 ohms.If more bypass capacitance or bulk capacitors with ESR outside the range above is used, each TPS54x10 control loop may need to be re-compensated using the SWIFT design software.
- **V_{CCAUX}:** V_{CCAUX} powers time-critical resources in the FPGA, including the Digital Clock Managers (DCMs). Therefore, this supply voltage is especially susceptible to power supply noise. V_{CCAUX} can share a power plane with V_{CCO}, but only if V_{CCO} does not have excessive noise. Changes in V_{CCAUX} voltage beyond 200 mV peak-to-peak should take place no faster than 10 mV per millisecond.
- **RocketIO:** When powering the RocketIO:
 - o A_{VCCAUTX}, V_{CCAUXRX}, A_{VTRX}, and A_{VTTX} may each be powered by their own linear regulator or by the same regulator if their voltages are the same. Keep power dissipation capability of the linear regulator package in mind.
 - o Select the appropriate TPS79xxx or TPS786xx based on the load current requirement, and the power dissipation capability of the package. In general, the lower the current rating, the lower the price of the linear regulator. Power dissipation of linear regulators is explained in TI Application Note SLVA118.
 - o For the TPS79x01 adjustable devices, size the feedback resistors according to the datasheet. These resistors are not populated on the schematic.
 - o All unused RocketIO transceivers must be connected to power (2.5V) and ground.
- **Modifications:**

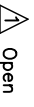
- Adapt for $V_{IN} = 3.3 \text{ V}$ by omitting U3.

QUESTIONS?

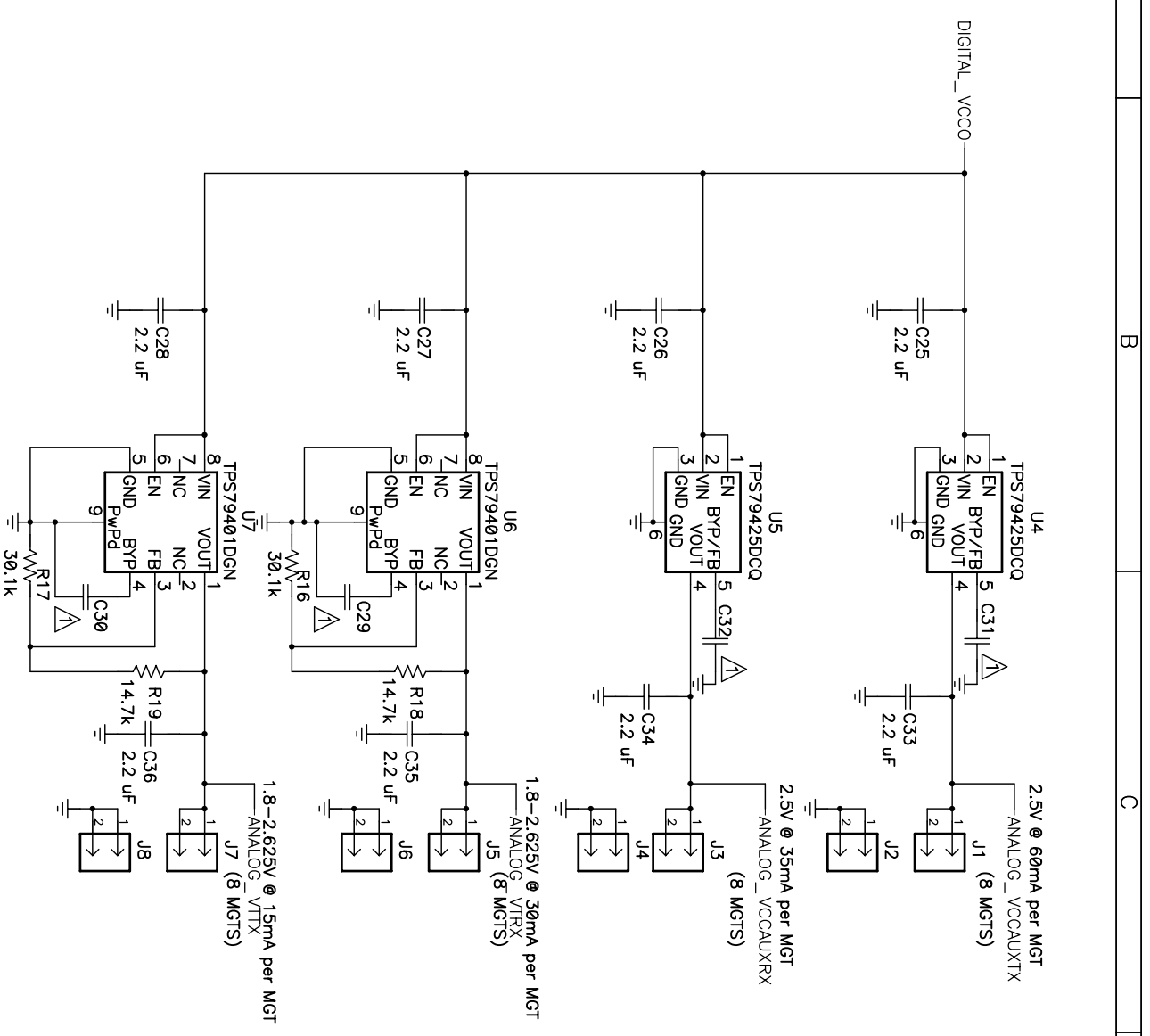
- Send an email to **fpgasupport@list.ti.com**



NOTES: 6A (TPS54610) SWIFT DC/DC Converter and LDO (TPS79xxx) design. Can be used for 8A (TPS54810) and 9A (TPS54910) designs with inductor (L1, L2) change.



Title		Texas Instruments	
Size	Number	XILINXPWR-082	
B			
Date	06/14/04	Drawn by	A
Filename hpd082a.sch		Sheet 1	of 2



Title			
Texas Instruments			
Size	Number	Rev	
B	XILINXPWR-082	A	
Date	06/14/04	Drawn by	
Filename	hpd0820a.sch	Sheet	2 of 2

Filename: HPA082A_bom.xls					
Date: 06/14/2004					
HPA082A BOM					
COUNT	RefDes	DESCRIPTION	SIZE	MFR	PART NUMBER
2	C1, C5	Capacitor, Ceramic, 10-uF, 6.3-V, X5R, 10%	805	muRata	GRM21BR60J106KE01
2	C11, C12	Capacitor, Ceramic, 0.047-uF, 25-V, X7R, 10%	603	muRata	GRM188R71E473KA01
2	C13, C14	Capacitor, Ceramic, 3300-pF, 50-V, X7R, 10%	603	muRata	GRM188R71H332KA01
2	C15, C17	Capacitor, Ceramic, 27-pF, 50-V, C0G, 5%	603	muRata	GRM1885C1H270JA01D
2	C16, C18	Capacitor, Ceramic, 2700-pF, 50-V, X7R, 10%	603	muRata	GRM188R71H272KA01D
2	C19, C20	Capacitor, Ceramic, 22-uF, 10-V, X5R, 10%	1210	muRata	GRM32ER61A226KA65
2	C2, C4	Capacitor, Ceramic, 1.0-uF, 6.3-V, X5R, 10%	603	muRata	GRM188R60J105KA01
2	C23, C24	Capacitor, Ceramic, 470-pF, 50-V, X7R, 10%	603	muRata	GRM188R71H471KA01
0	C29, C30, C31, C32	Capacitor, Ceramic, xxx-uF, vv-V	603		
4	C3, C8, C21, C22	Capacitor, Tantalum, 330-uF, 6.3-V, 600-milliohm, 20%	7343(D)	Vishay	293D337X96R3D2
1	C6	Capacitor, Ceramic, 0.056-uF, 16-V, X7R, 10%	603	muRata	GRM188R71C563KC01
1	C7	Capacitor, Ceramic, 0.33-uF, 10-V, X5R, 10%	603	muRata	GRM188R61A334KA61
10	C9, C10, C25, C26, C27, C28, C33, C34, C35, C36	Capacitor, Ceramic, 2.2-uF, 6.3-V, X5R, 10%	805	muRata	GRM21BR60J225KC01
8	J1 - J8	Header, 2-pin, 100mil spacing, (36-pin strip)	0.100 x 2	Sullins	PTC36SAAN
2	L1, L2	Inductor, SMT, 4.7-uH, 7.7-A, 12-milliohm	0.76x0.52	Coiltronics	UP3B-4R7
3	R1, R2, R9	Resistor, Chip, 71.5k-Ohms, 1/16-W, 1%	603	Std	Std
4	R10, R11, R16, R17	Resistor, Chip, 30.1k-Ohms, 1/16-W, 1%	603	Std	Std
2	R12, R13	Resistor, Chip, 1.91k-Ohms, 1/16-W, 1%	603	Std	Std
3	R3, R14, R15	Resistor, Chip, 10k-Ohms, 1/16-W, 1%	603	Std	Std
1	R4	Resistor, Chip, 511k-Ohms, 1/16-W, 1%	603	Std	Std
2	R5, R6	Resistor, Chip, 2.4-Ohms, 1/8-W, 1%	1206	Std	Std
3	R7, R18, R19	Resistor, Chip, 14.7k-Ohms, 1/16-W, 1%	603	Std	Std
1	R8	Resistor, Chip, 3.74k-Ohms, 1/16-W, 1%	603	Std	Std
1	S1	Switch, 1P2T, Slide, PC-mount, 200-mA	79900	E_Switch	EG1218
4	TB1 - TB4	Terminal Block, 2-pin, 15-A, 5.1mm	0.40 x 0.35	OST	ED1609
1	U1	IC, Utralow-Noise, High PSRR, Fast RF 250 mA, LDO Linear Regulators, 2.5V	MSOP 8	TI	TPS79425DGN

2	U2, U3	IC, IFET Power controller, Adj-V, 6-A	PWP28	TI	TPS54610PWP
2	U4, U5	IC, LDO Linear Regulator Ultralow-Noise High PSRR Fast RF, 500mA, 2.5V	SOT223-6	TI	TPS79425DCQ
2	U6, U7	IC, Utralow-Noise, High PSRR, Fast RF 250 mA, LDO Linear Regulators, Adj-V	MSOP-8	TI	TPS79401DGN
1	--	PCB, 3.6 In x 3.25 In x .062 In		Any	HPA082
Notes:					
	1. These assemblies are ESD sensitive, ESD precautions shall be observed.				
	2. These assemblies must be clean and free from flux and all contaminants.				
	Use of no clean flux is not acceptable.				
	3. These assemblies must comply with workmanship standards IPC-A-610 Class 2.				
	4. Ref designators marked with an asterisk (***) cannot be substituted.				
	All other components can be substituted with equivalent MFG's components.				

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