Design Considerations and Advances in Portable Power Battery Chargers

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Abstract

Battery-charger demands have changed from a simple stand-alone charger to an embedded charger and power source for the system. This topic provides some insight into the many new issues the designer should consider when designing either a linear or a switching regulator. Common transient issues caused by hot plugging/unplugging the adapter or system load during operation are presented. Problems and solutions surrounding use of a stand-alone charger to charge a battery with a system load in parallel are discussed along with the optimal solution for powering system loads.

I. Introduction

Providing power to a system is often regarded as a last-minute task, delegated to a systems person or an engineer with little power-supply design experience. This paper attempts to help the inexperienced power designer avoid many of the common mistakes made in portable power product design. Section II discusses the pros and cons of linear and switcher power conversion for a given application. A general theory of operation is followed by an explanation of a FET driver circuit, a current mirror circuit, and design considerations for component selection and layout. Section III highlights the potential hazards that may be caused by connecting and disconnecting active charger sources and loads. Typical application scenarios are modeled, simulated, and presented. Section IV explains the issues introduced when a system load is connected in parallel with a battery under charge. Several application "work-around" solutions are presented. Section V explores an alternative solution that avoids many of the pitfalls introduced when the system is connected in parallel with the battery.

II. Choosing Between a Linear and Switcher Battery Charger

There are two basic types of power conversions – a linear regulator and a switching regulator.

A linear regulator is similar to a resistor divider where the regulator drops the input voltage down to a usable "charging" voltage (see Fig. 1a). The

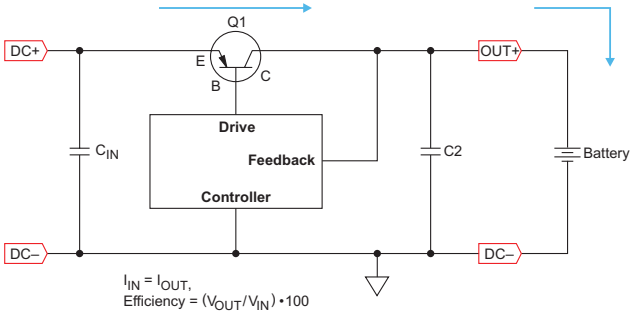


Fig. 1a. Linear regulator.

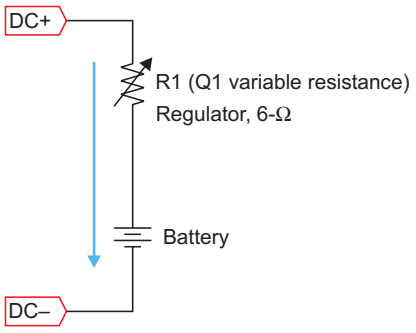


Fig. 1b. Equivalent DC circuit.

current is the same through both resistors (see Fig. 1b, where the top resistor represents the regulator and the bottom resistor represents the load). From the following equation one can see that, if 10 V is applied to a series 6-Ω regulator and a 4-Ω system load resistor, the system voltage will be 4 V and the current will be 1 A.

$I = V_{SYS}/R = 10\ V/(6\ \Omega + 4\ \Omega) = 1\ A$

$V_{SYS} = V_{IN} \cdot R2/(R1 + R2)$
$= 10\ V \cdot 4\ \Omega/(6\ \Omega + 4\ \Omega) = 4\ V$

$P = IV$

$P_{R1} = 1\ A \cdot 6\ V = 6\ W$

$P_{R2} = 1\ A \cdot 4\ V = 4\ W$

R1 (Q1, the linear pass element) will dissipate 6 W and R2 (R_{System} or battery) will use 4 W. One can see that, for a linear charger with a 10-V input and 4-V output, only 40% of the energy will be delivered to the system or battery. The linear design does not require an inductor or diode and is generally less expensive than a switcher for low-power, low-dissipation designs. As power demand

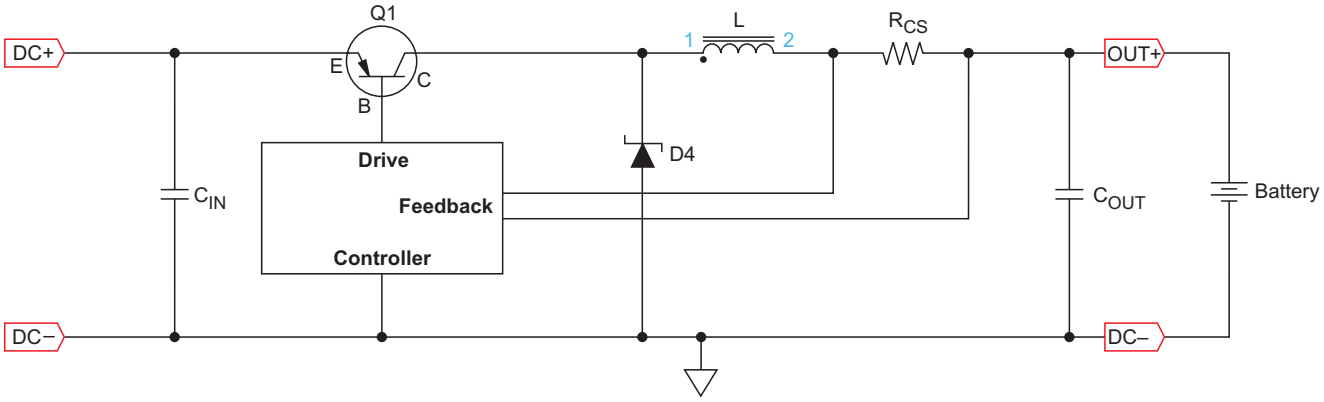


Fig. 2a. Buck power stage.

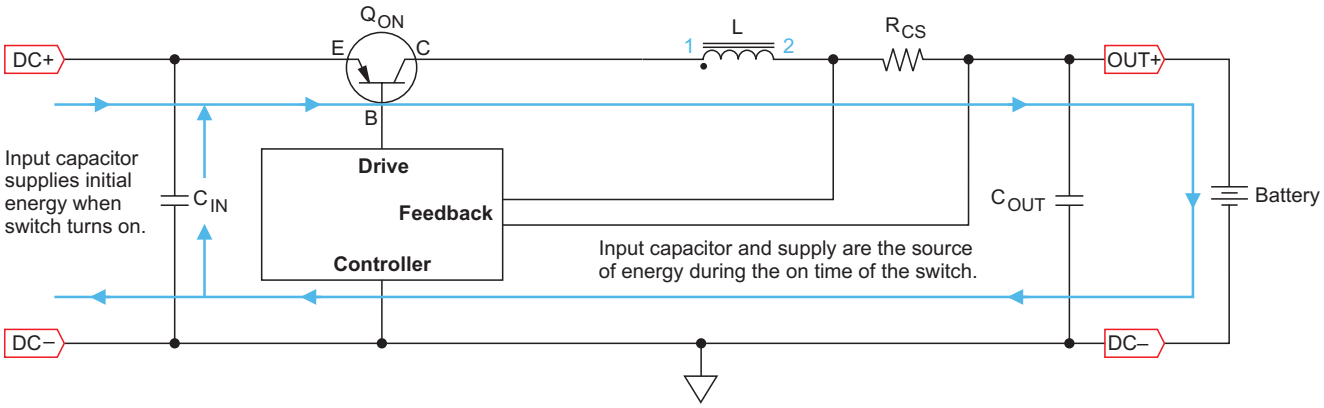


Fig. 2b. Current flow when switch is on.

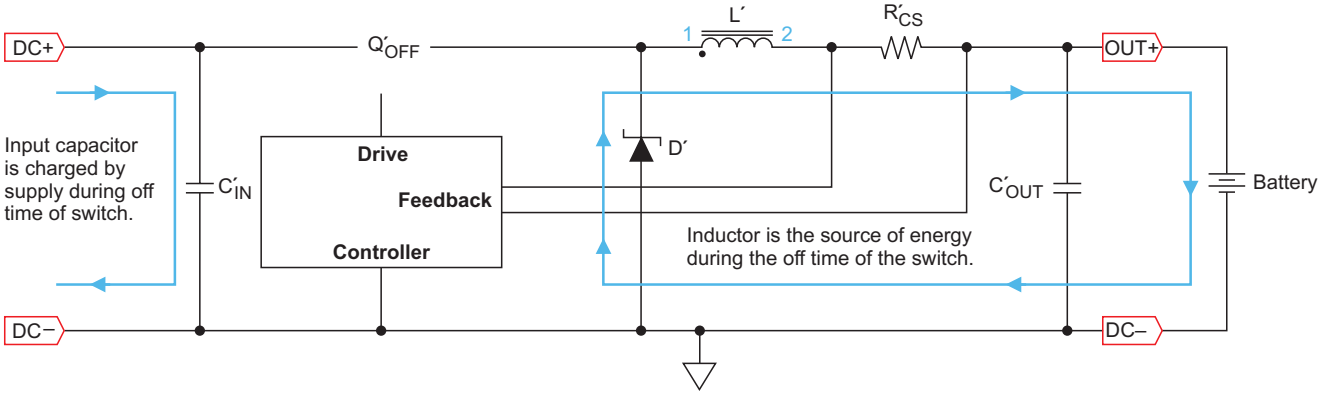


Fig. 2c. Current flow when switch is off.

increases or as linear efficiencies decrease, the cost or the ability to manage excessive power dissipation will make the linear topology a less desirable choice.

Switching regulators can boost or buck the input voltage. The buck switcher design converts (bucks) the input voltage down to a lower desired output voltage. The buck switcher (see Fig. 2a) is connected between the input supply voltage and the output load (battery or system load). Q1, the power switch, is turned on and off at a high frequency (> 50 kHz) by the controller for a controlled on time (t_{ON}). This results in a square wave with amplitudes between V_{IN} and ground, with a duty cycle proportional to V_{OUT}/V_{IN} (see Fig. 3). This square wave is applied to a low-pass LC filter that averages (filters) the signal, producing a DC output waveform. The controller monitors the feedback from the output and makes the necessary adjustments to the duty cycle to maintain the desired regulation. This power conversion method is more efficient than the linear because it stores excess energy in the inductor during the on time of the switch and delivers it to the load during the off time of the switch.

A. The Power Stage

In Fig. 2a, the power stage that converts the power from the input to the output consists of C3 (the input capacitor), Q1 (the power switch), D4 (the free-wheeling diode), L2 (the output filter inductor), R20 (the current sense resistor), C12 (the output capacitor), and the load (battery or system). The reference designators are the same ones used in the power stage of the bq2954 IC EVM schematic in Reference [1].

There are two stages to the power conversion, one with the switch on and one with the switch off (see Figs. 2b and 2c).* The control loop operates

*Note that, when the switching regulator switch is on, it provides a low resistive path and, when off, it has a very high resistance. In either state, the transistor is dissipating very little power (P = IV; i.e., low voltage times load current or input voltage times approximately zero current). For a bipolar switch, the power dissipation is approximately:

$$P = I_C \cdot V_{EC} + I_B \cdot V_{EB} \cdot \delta$$

where δ is the duty cycle. A MOSFET has three main types of power dissipation: The dissipation to drive the capacitances of the FET (switch FET on and off), the dissipation during the transition times from off to on and on to off (linear region of the FET), and the dissipation due to the switch current during its on time.

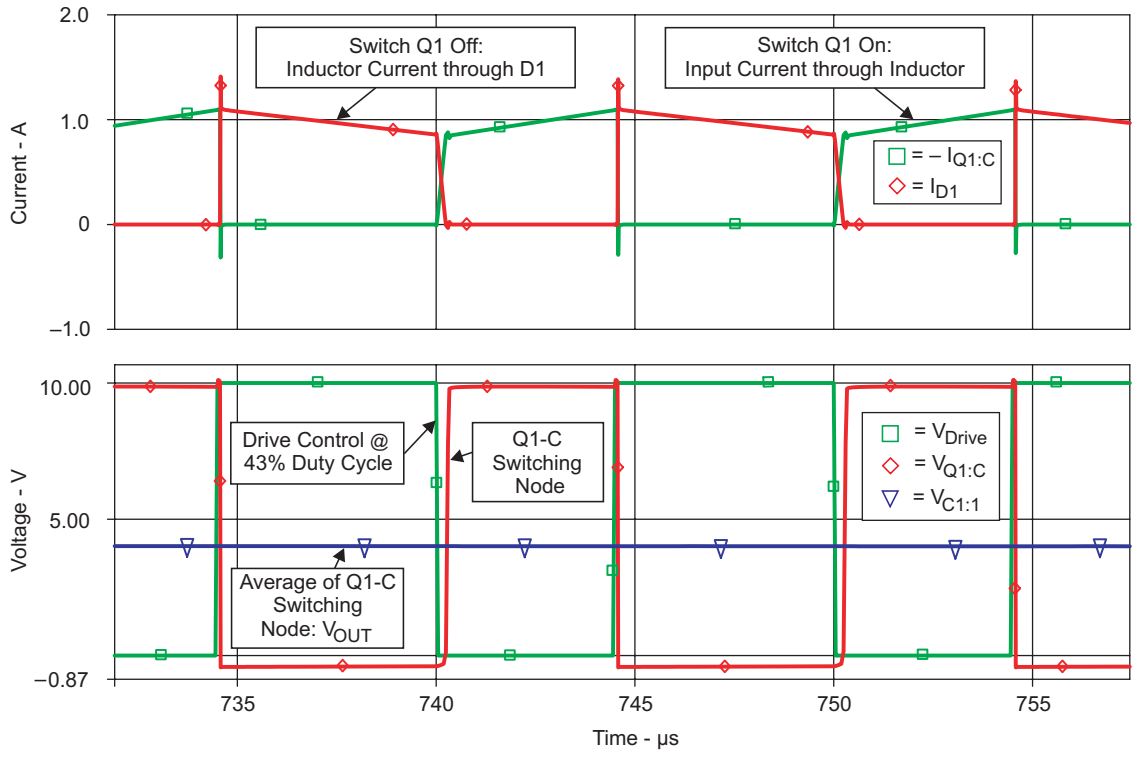


Fig. 3. Buck switcher waveforms.

on a fixed pulse-width modulation (PWM) that turns on the switch at a set time each cycle. If the switching frequency (f) was set to 100 kHz, the switch would turn on every 10 µs (1/f). The control loop, in steady-state operation, would turn off the switch after the current or voltage conditions were met. (The switch is usually on between 1 and 9 µs, depending on the input and output conditions.) For Li-ion battery chargers, there are usually two control loops, one for maximum constant current regulation and one for voltage regulation. Both loops control switch Q1 via an "or" operation. The current loop is in control until the cell voltage reaches 4.2 V, and then the voltage loop takes over as the current tapers off. When the switch is on, the current flows from the input capacitor through the switch, inductor, and sense resistor to the output capacitor/battery/system; then it returns through the ground plane to the input capacitor. The source is charging the battery and at the same time charging the output inductor. During the switch on time, the inductor's current ramps up at the rate of:

$$di/dt = V_{Inductor}/L$$
$$= (V_{IN} - V_{SW} - V_{SNS} - V_{OUT})/L$$

When the control loop turns the switch off, the input current through the switch goes to zero (the source replenishes the input capacitor's energy during the off time). The output inductor's current cannot change instantly; so after the switch is turned off, it has to become the source by flipping polarity. Now the current flows from the inductor through the output capacitor/battery/system, through the return ground plane, through D4, and back to the inductor. While it is the source of the current, the inductor's current ramps down at a rate of:

$$di/dt = (V_{Inductor} + V_{Diode})/L$$

The cycle repeats with the switch turning back on. The power stage components should be placed in sequence in the layout as the current flows from input to output. The routing should be heavy etch or mini-complex planes that connect the components, with the return path being routed on an adjacent layer underneath the path on the top layer. For this topology, a ground plane can be used as a good return path. The intent is to have all currents return to their source along the same path they initially followed, which will minimize the path length and keep them clear of sensitive components. It will also minimize the noise by reducing the inductive loop (antenna).

B. The Drive for the Switch Q1

The switch Q1 dissipates large amounts of energy in its active region during its transition between the off and on states. The faster this transition occurs, the lower the transition power loss. Linear regulators continually operate in their linear state and usually have poor efficiencies unless the overhead voltage is minimized. A low-impedance drive circuit, shown in Fig. 4, is required for turning off the bipolar switch to decrease switching losses. The bipolar switch, when fully on, is in saturation and requires a high-current drive to remove charge stored in the base quickly for a fast turn-off transition. A high signal (~4.7 V) from the MOD pin turns on Q4 and provides a constant current programmed by R16 [(4.7 V – 0.7 V)/220 = 18 mA]. This provides an 18-mA drive to turn on Q1 via D3. To provide fast turn-on of Q1, D3 shunts L1 initially until L1 ramps up to 18 mA, and then D3 turns off. When the MOD pin goes low, Q4 turns off; and the inductor flips polarity and becomes the source to drive its current into the base of Q2. This will turn on Q2 and drive the base of Q1 to its emitter's voltage, which will turn off Q1. R1 insures that any Q4 leakage will not pull on Q1. A similar

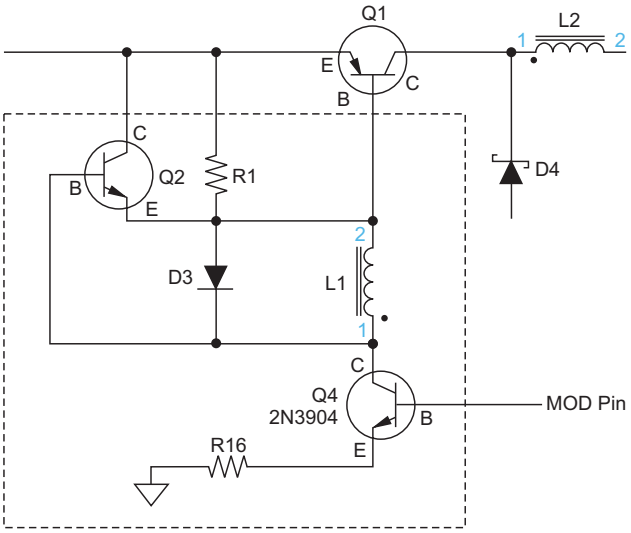


Fig. 4. Driver for the power-stage bipolar switch.

(capacitive) drive circuit is used to turn on and off a P-channel FET. The larger the C_{ISS} of the FET, the better the drive (the lower the impedance) has to be to switch the FET quickly on and off. A 75 ± 50-ns transition time is a good target for which to aim for a 100- to 200-kHz switching frequency. If the FET's input capacitance is small (as in a low-power application), a pull-up resistor may be good enough for turn-off.

C. Current Mirror

The current mirror is a method of converting a low-side to a high-side current-sensing design. The main advantage is that the battery current returns at the same potential as the system return, effectively removing the sense resistor from the battery discharge path and thus improving overall system efficiency. The current mirror monitors the voltage across the high-side current sense resistor and translates this information to the ground side as a reference (see Fig. 5). Current mirrors made from discrete components often cost less than ones produced on one silicon die but can't match the accuracy of the integrated circuit with its matched transistors and uniform die temperature.

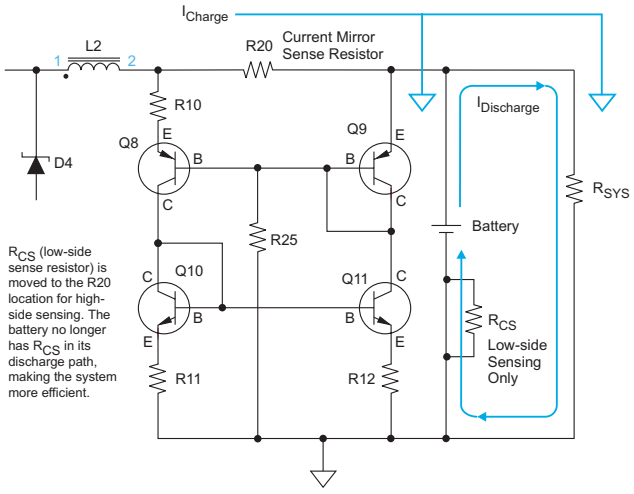


Fig. 5. Current mirror.

Notice the symmetry of the circuit: On the left are R10, Q8, Q10, and R11, which all have the same "collector" current running through them. On the right-hand side are R20, Q9, Q11, and R12, which also all have the same collector current running through them (R20 also has the output current). If these currents are the same magnitude, they will have the same V_{BE} drops, which are the key to the accuracy of the circuit. Note that R10 and Q8 are in series and also in parallel with R20 and Q9. R10 and R20 connect at the same node, and Q8-B connects to Q9-B. Since the V_{BE}'s are matched, the drops across R10 and R20 have to be the same. The current through R10 and R11 is the same; and if the values are the same, then the voltage drop across R11 is equal to the voltage drop across R10. Thus the voltage drop across R20, the sense resistor, is the same as the drop across R11. Note that if R11 and R12 remain the same value, the current through each leg will be the same with the same V_{BE} drops. The designer could scale R10 to change the gain of the current mirror. If the resistance was reduced by half, it would have twice the collector current and twice the sense voltage; and the controller would cut the current in half to get back to the desired regulation. Thus, reducing the value of R10 by half would cut the programmed current in half:

$$I_{OUT} = (V_{SNS}/R20) \bullet R10/R11$$

D. Switcher Design Considerations

The input should be of low impedance so that it can provide the necessary current when the switch turns on. The primary current jumps up to the inductor's current level when the switch is turned on. Therefore, since the source leads are inductive, a good input capacitor with low equivalent series resistance (ESR) (such as from the Panasonic Al Elect. FK series) is needed to supply the desired pulsed (switched) current. If the output impedance of the input filter matches the switcher's impedance, the system will oscillate. The resonance frequency of a capacitor and an inductor occurs when their impedances match each other. If the converter's input voltage drops, the input current increases to deliver the same amount of power. This negative change in voltage divided by the increase in current makes the switcher appear as if it is dropping in impedance like a negative-impedance device. For the system to remain stable, the impedance the switcher sees at the input capacitor has to be lower than the lowest impedance the switcher achieves.

The drive circuit should be designed with enough current to drive the bipolar switch into

saturation for worst-case conditions (h_{fe} gain when V_{EC} is at its minimum and at a minimum temperature, $I_{Drive} \geq I_C/h_{fe}$).

The output inductor should be able to deliver the peak programmed current without saturating. The inductor's ripple current should be no more than 60% of the programmed current:

$$di = V_{IND} \bullet dt/L \text{ or}$$

$$L = [V_{OUT(min)} + V_{Diode}] \bullet [1 - V_{OUT(min)}/V_{IN(max)}] \bullet T/(0.6 \bullet I_{PROG})$$

$$T = 1/f = 10\ \mu s \text{ for } f = 100\ kHz$$

The larger the ripple current, the larger the difference is between average current and peak current. If the current feedback signal is not filtered, the current will be regulated off of the peak. This often is the reason that the actual average charge current is less than the programmed current. The larger the ratio between input and output voltage, the larger the ripple current will be. As the battery increases in voltage, the ripple current decreases. If the control loop regulates off the peak current, the average current will rise as the ripple current is reduced.

The output capacitor's capacitance is small compared to the battery capacitance. The amount of ripple current through the capacitor is determined by the ratio of impedances between the capacitor and battery. The output capacitor should be placed across the battery terminals in a low-side sense configuration. This allows all of the ripple current through the output inductor to be regulated via the sense resistor. Changing the path of the AC current component does not change the average charge into the battery. The output capacitance is chosen mainly for desired operation in case the battery is absent. For a PWM converter, the output capacitance and its load produce a pole in the loop response, which affects the crossover frequency and loop stability. If the capacitance is too small, the pole will be at too high a frequency, the phase margin will be too low, and there will be stability problems. A hysteretic converter's switching is controlled by a hysteresis window and not by a fixed switching frequency and controlled duty cycle. The output low-pass filter, input/output voltages, and sense filters are the main factors that set the switching frequency.

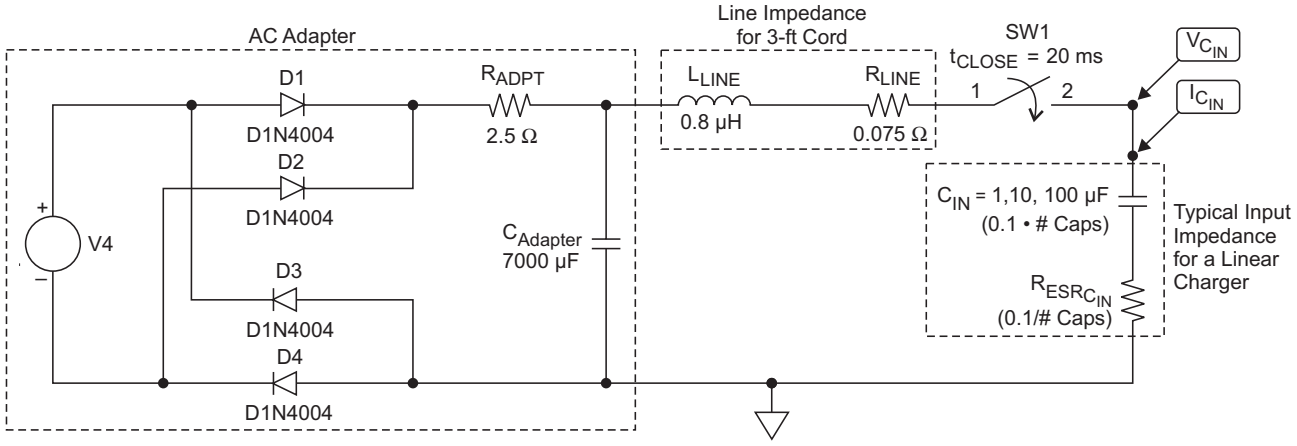
III. Effects of Connecting/ Disconnecting Sources and Loads for a Battery Charger

There are four components of a battery charger configuration: the power source, the charger/ battery management circuit, the battery pack, and the system load. The method by which these circuit blocks are connected/disconnected, their sequencing, and their state of charge can greatly affect the response. Some of the responses could result in damage to the circuitry if not accounted for during the design phase. Four design configurations will be reviewed along with their potential problems and solutions. Many of the issues presented may not result in problems due to the damping effects of circuit parasitics (mostly contact, line, and component resistances) and contact bounce, but the designer should be aware of the possible failure mechanisms.

The ideal battery charger configuration is a stand-alone unit that has the source always connected to the charger. The discharged battery is installed in the charger, and then the wall adapter is plugged into the outlet. This method minimizes any potential problems but also limits the number of applications and the flexibility of the charger.

Problem 1

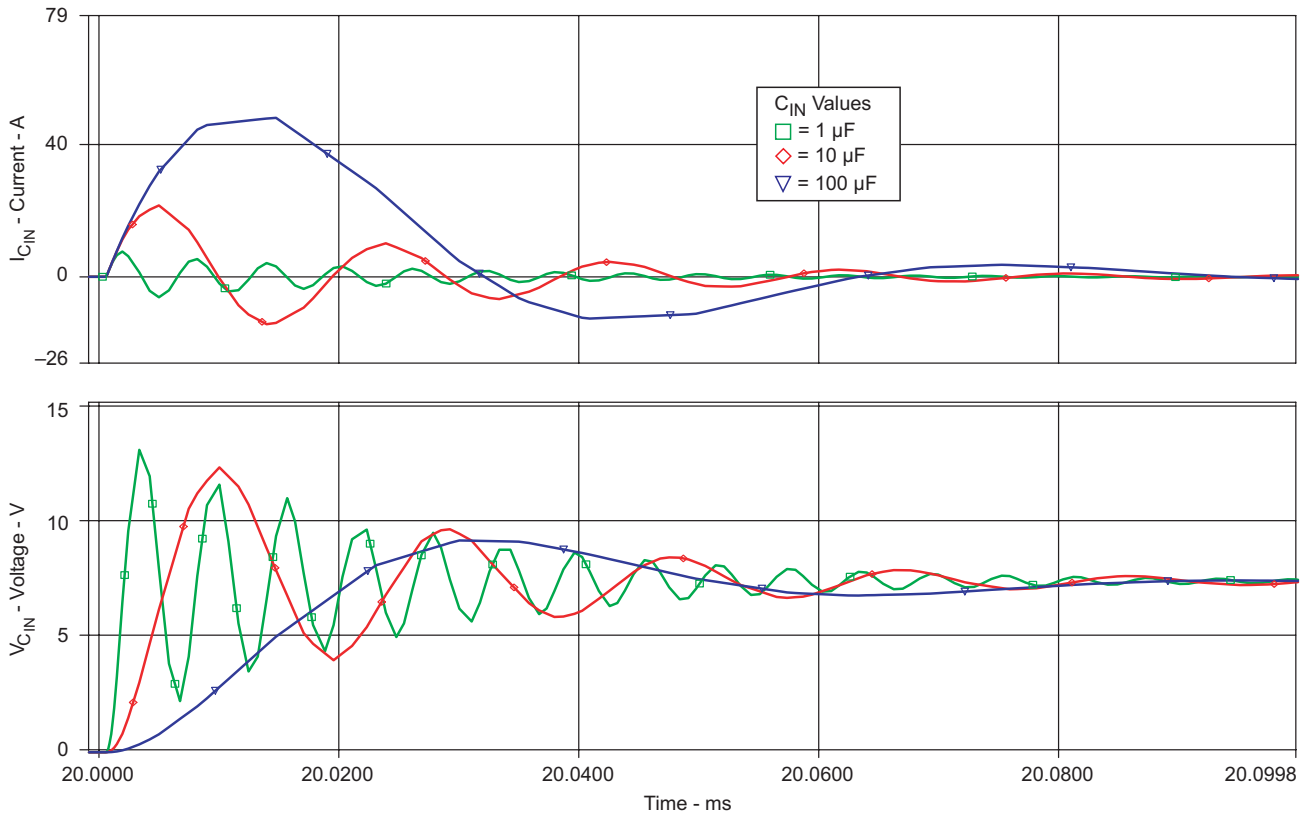
The first potential problem arises when the output of a charged wall adapter (plugged into an outlet) is connected to the input of the charger. The large capacitor in the output of the adapter is charged and is the source for quickly charging the input capacitance to the charger via the adapter's line inductance. This was modeled and simulated as shown in Fig. 6 and is similar to a step response on an LC filter. Typical adapter values were used for a 5-V (~7-V with no load at the output of the adapter), 1-A, 7000-µF output capacitance wall adapter with 36 inches of 21-AWG wire. The simulation was run with five different battery charger input capacitance values ranging from 0.1 to 1000 µF. In the top plot of Fig. 6b, the current peaks in the line inductance when the charger's input voltage reaches the adapter's output voltage (V_L = 0 V). The inductor then flips polarity, becoming the source, and delivers its energy into the charger's input capacitor, resulting in a voltage



Adapter (120 VAC to 5 VDC unregulated) is plugged into wall source and then hot plugged into charger's input capacitance.

Note that a DC source is used to represent the voltage at the peak of an AC waveform.
The adapter's output capacitor will be charged to this peak value prior to hot plugging into the charger circuit.
C1 will stay charged to its full value during this time of interest (80 µs).

a. Schematic.



b. Plot of current and voltage waveforms for C_{IN} = 1, 10 and 100 µF.

Fig. 6. Hot plugging an adapter into a charger circuit as a function of charger capacitance.

of ~2 • V_{OUT}. This would have the potential to damage any parts that are not rated for this 2× voltage. There are several solutions to this problem:

- Reduce line inductance by reducing the adapter's cable length.
- Increase damping resistance.
- Increase the input capacitance to the charger.
- Clamp the input of the charger with a zener diode.
- Increase the voltage rating on input components to ≥ 2× the hot-plug voltage.
- Avoid hot plugging the adapter into the charger.

The simulation shows that adding input capacitance to the charger can reduce the peak voltage. For a series RLC circuit, critical damping occurs at $R = 2\sqrt{L/C}$. Adding capacitance reduces the impedance of the LC circuit, increasing the damping ability of the 75-mΩ line resistance. As capacitance is added, the peak current rises. If the current gets too large the contacts may arc, causing damage due to the poor connection during the plugging action.

In this situation, it is better to increase the damping resistance along with moderate increases in charger capacitance. It is equally effective to increase the damping resistance without increasing the input capacitance. Note that for a switching charger, the input capacitance has to be a low impedance to avoid matching the switcher impedance and becoming unstable; so any resistive damping should be in series with the inductor (see Fig. 7). One can see from Fig. 7b that as the damping resistance is increased to critical damping, the ringing and overshoot are filtered. The one side effect is that 250 mW of line resistance now dissipates power and takes away from the drive. A parallel damping RC could be added in parallel with the charger capacitance, but it would have to be three to four times the capacitance of C_{IN} and have a resistance close to the resonance impedance of the LC circuit to be filtered. This would be the most costly solution. A zener in parallel with C_{IN} would cost slightly more than the R_{LINE} resistor but would avoid the IR drop. The zener's knee is selected at 1.5 • $V_{IN(nom)}$ for an unregulated supply. The peak voltage will be just below the knee, and any inductive voltage spike will be clamped. Since the inductive spikes are not repetitive, a low-power zener may be used.

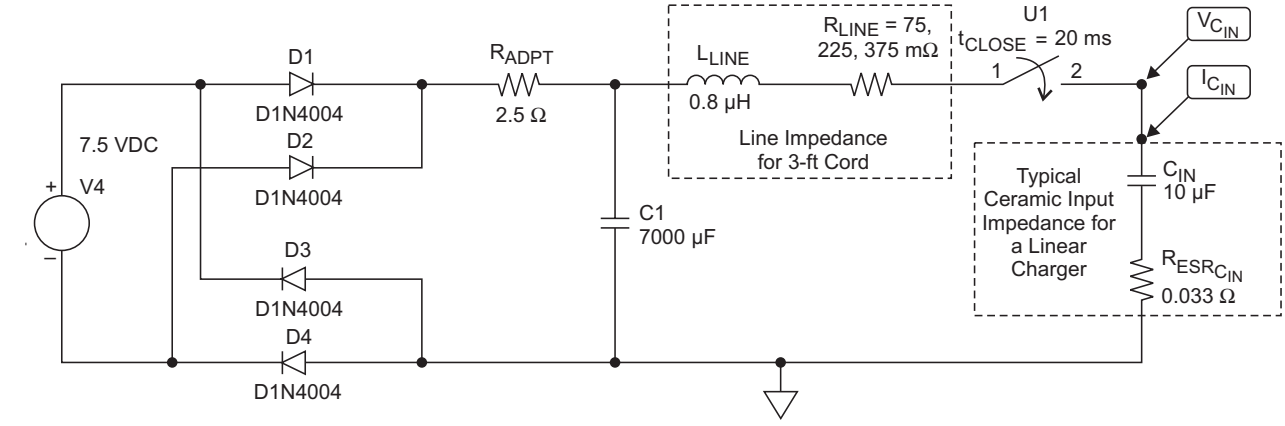
Problem 2

The second potential problem can occur when the adapter is unplugged from the charger while the charger is delivering the programmed fast-charge current (1 A in the simulation) near the regulation voltage of the battery (see Fig. 8). The charged inductance of the adapter's line cord flips polarity to continue to drive the line current. The switch is modeled to open the connection (go from a short to an open) in 1 µs, which leaves little time to discharge the inductor's energy. The waveforms in the top plot of Fig. 8b are the current in the load, the C_{IN} capacitor, and the line inductance. The waveform in the bottom plot is the voltage at the adapter's connector.

In reality a connector can't be unplugged very fast (maybe in 10 ms); and the contact resistance during this time slowly increases, allowing the inductor's current to decrease while keeping the inductor's voltage low. A mechanical switch may be able to open fast enough to cause an inductive voltage spike. One potential effect is arcing, which may degrade the contacts. A more likely failure is damage to a FET switch – which, if turned off quickly, would see a large inductive voltage spike. There are four basic solutions to this type of problem:

- Slow down the FET switch time by adding gate resistance.
- Put an RC series "snubber" across the switch.
- Clamp the inductive voltage spike with a zener upstream of the switch.
- Don't unplug the adapter from the charger during charging.

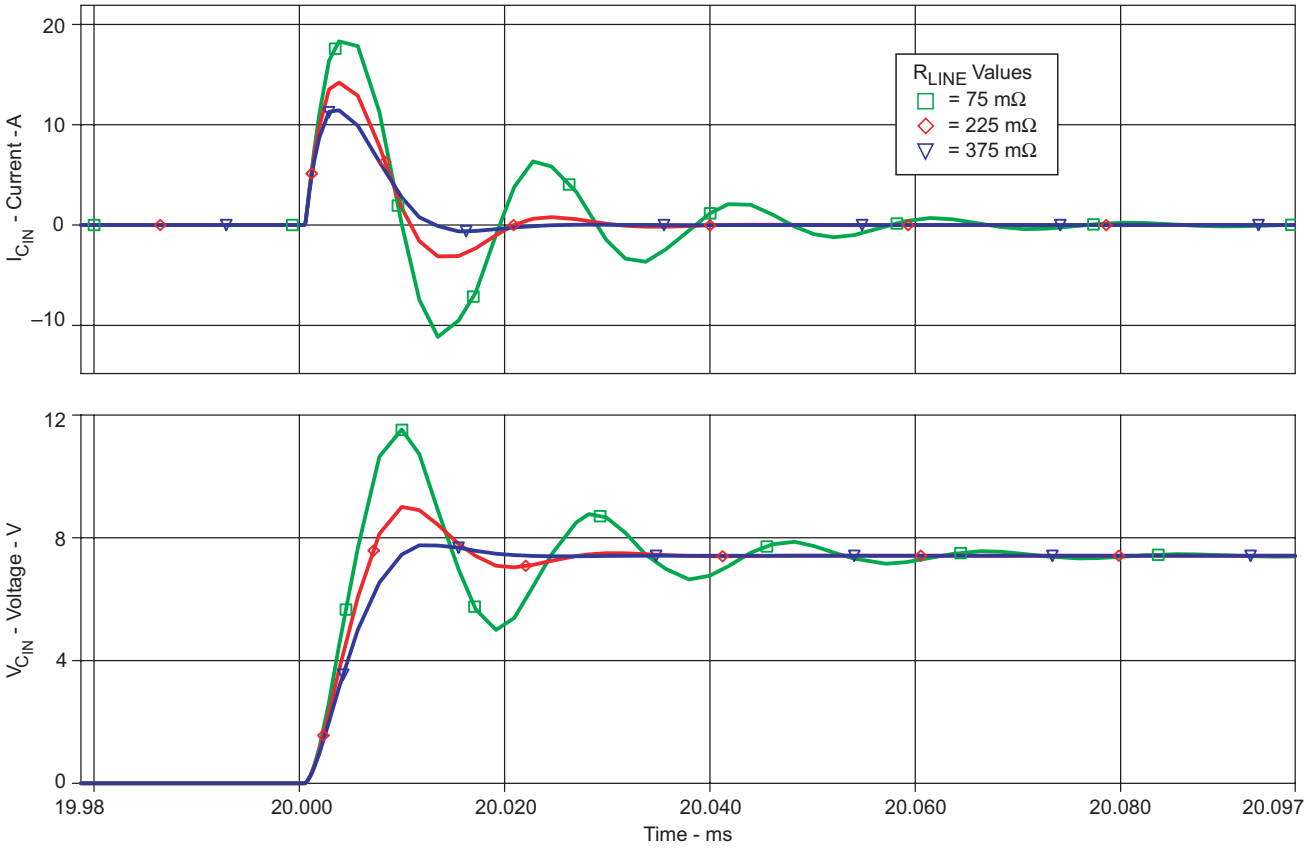
The typical application is unplugging a connector, which probably won't be a problem due to the relative slow speed of breaking the contact. Breaking the contact between the adapter and charger with a mechanical or semiconductor switch is rarely implemented, but this discussion is presented here to help the designer reach a complete understanding.



Adapter (120 VAC to 5 VDC unregulated) is plugged into wall source and then hot plugged into charger's input capacitance.

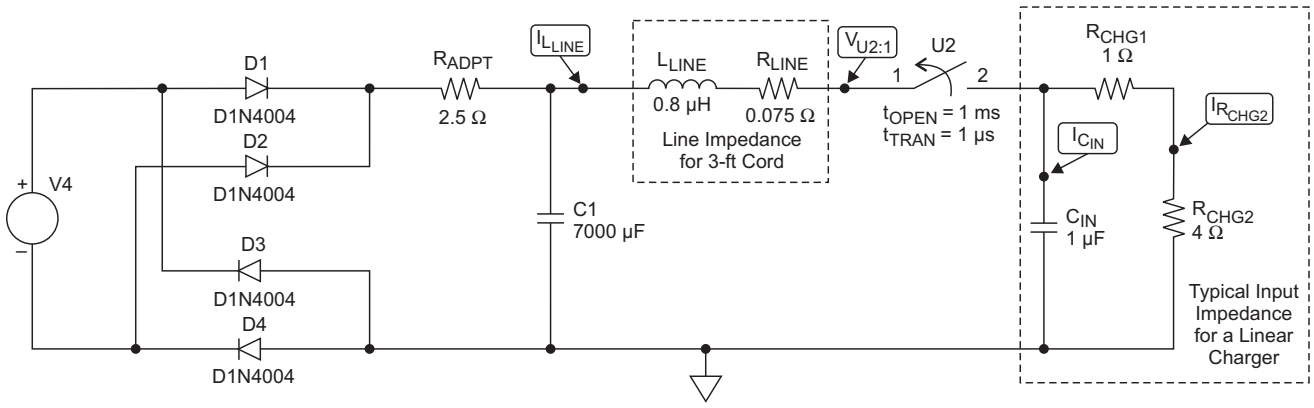
Note that a DC source is used to represent the voltage at the peak of an AC waveform.
The adapter's output capacitor will be charged to this peak value prior to hot plugging into the charger circuit.
C1 will stay charged to its full value during this time of interest (80 µs).

a. Schematic.



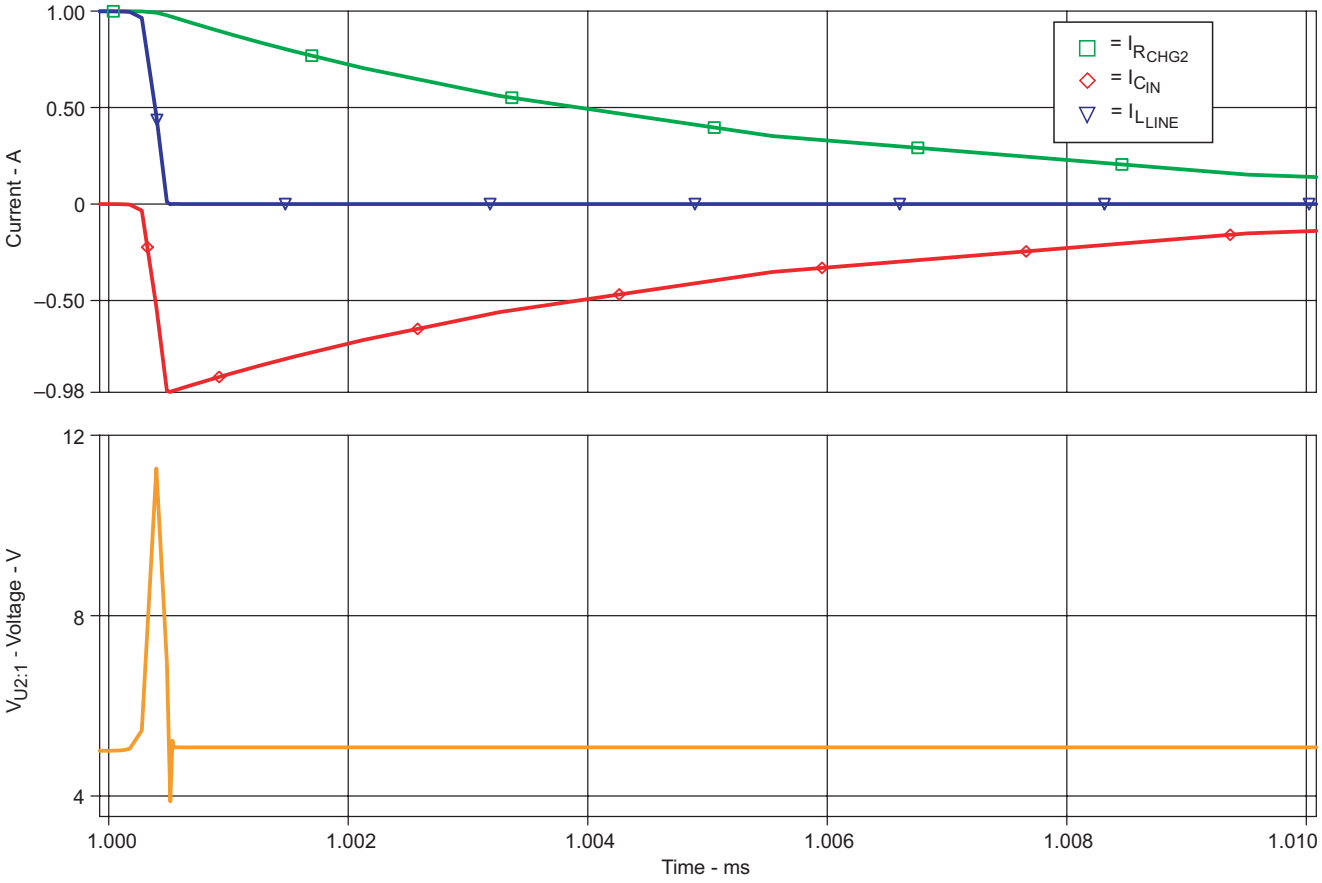
b. Plot of current and voltage waveforms for R_{LINE} = 75, 225, and 375 mΩ.

Fig. 7. Hot plugging an adapter into a charger circuit as a function of damping resistance.



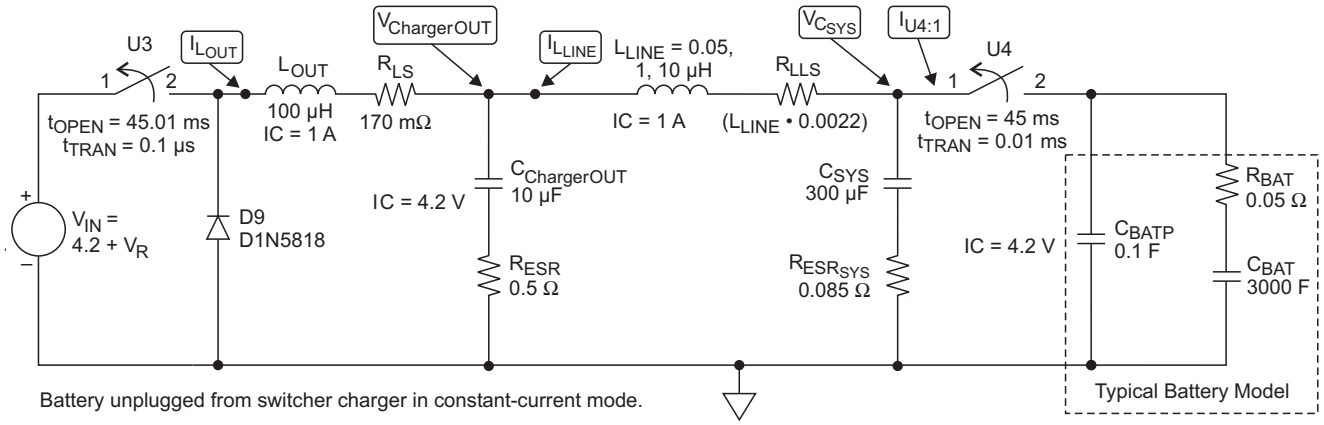
Adapter (120 VAC to 5 VDC, 1 ADC, unregulated) is charging battery pack, and then adapter is unplugged from the charger.

a. Schematic.



b. Plot of current and voltage waveforms for L_{LINE} = 0.8 µH.

Fig. 8. Effects of unplugging an adapter from a charging circuit.

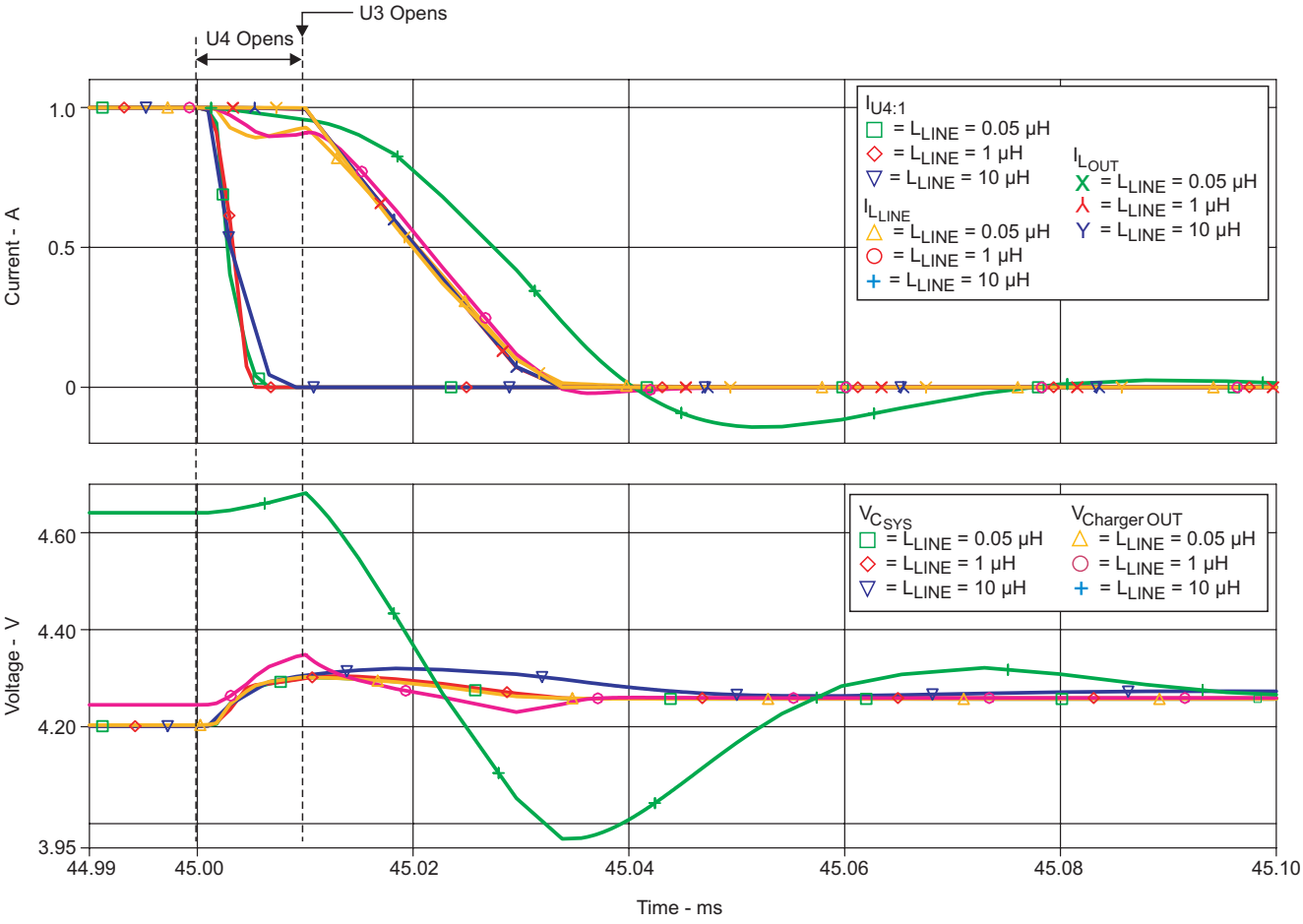


The line inductance is equivalent to 2.5" (0.05 µH), 50" (1 µH), or 500" (10 µH) of line cable. If the line conductors form a large loop, the inductance may be in the microhenry range with a much shorter length (<100").

V_R = Voltage drop from V_{IN} to V_{BAT}.

IC = Initial condition.

a. Schematic.



b. Plots of current (top) and voltage (bottom).

Fig. 9. Battery removal during fast charge for a switcher charger, with the system in low-power mode.

Plugging a battery or system load into the charger seldom causes issues due to the fast current loop limiting the current to the programmed level. There may be some system issues with detecting a system load (at 0 V) and supplying a regulation voltage, but this is not within the scope of this topic.

Problem 3

The third potential problem can occur when a charger's load (battery, system, or both) is unplugged while charge current is being supplied.

Unplugging the system load while a battery is connected does not present a hazard, since the battery can momentarily absorb any inductive kick from the line inductance until the controller makes necessary adjustments. If the output is in regulation, the additional pulse in the current could cause a slight voltage overshoot across the battery's impedance, causing the controller to turn off the pass element and then terminate. Discharging the battery to the refresh voltage will start a charge cycle.

Unplugging a charging battery while the system is at heavy load will limit the overshoot due to the damping effect of the system load (capacitive and resistive).

The most likely worst-case condition results from removing a load when there is little or no system load and the battery is removed during a fast charge near voltage regulation, or when the pack protector opens. A model of a switching charger is shown in Fig. 9, and a model of a linear charger is shown in Fig. 10. For both simulations, the battery switch was opened over a period of 10 µs, from 45 to 45.01 ms.

The switcher has a large output inductor that is driven by a voltage source equivalent to the output regulation voltage (4.2 V) plus the line drops. This explains the higher charger output voltages as R_{LLS} is increased. This source is disconnected (the high-side switch is opened) immediately after the battery is fully disconnected. Note that as soon as switch U3 is opened, the output and line inductor currents, L_{OUT} and L_{LINE}, start to decay along with all of the charger and system voltages. The free-wheeling diode provides a low-impedance return path for the discharging inductor. Typically the high-side switch will open as soon as the regulation voltage is exceeded (within a few microseconds) and before the battery is fully disconnected. Therefore there should be much less overshoot than that shown in the figures.

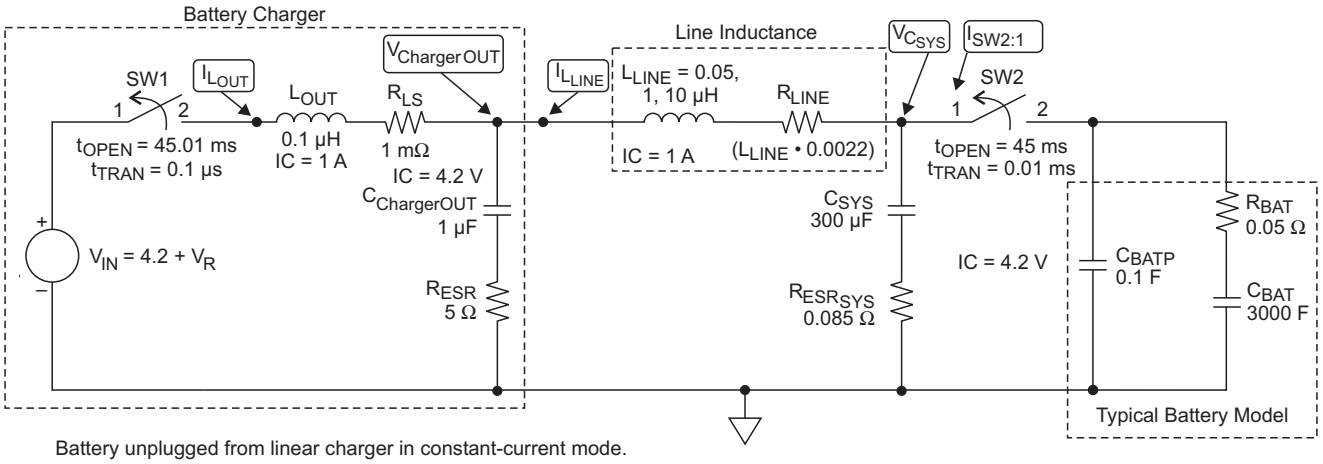
The battery removal for the linear charger simulation has results similar to those of the switcher. The inductor currents, along with the charger and system voltages, start to decay once the pass element is disconnected. The notable difference is that the linear design does not have a free-wheeling diode and therefore results in a discharge of the charger capacitance while the line inductance is discharging.

In all cases, it has been shown that as long as the control loop for the PWM or pass element is sufficiently fast (< 10 µs), the overshoot is negligible.

Problem 4

The fourth and last problem to consider is when the system is powered from the input. If the system is operating under heavy load and is disconnected, the line inductance between the input and the systems will flip its polarity and become the source. The voltage across the inductance will be used to continue to drive this current. There is typically an input charger capacitance and a system capacitance. During the discharge of the line inductance, the current will flow from the charger capacitance to the system capacitance. The smaller-value capacitor will change voltage the fastest. Typically, the input charger capacitance is much smaller and thus will discharge quickly. A large charge in the inductor can drive the charger capacitor negative, causing potential damage to the charger circuit. A Schottky diode, with cathode to the input and anode to ground, will protect the charging circuit. If the system capacitance is small or is disconnected with the load, the system voltage can spike high along with the charger capacitance voltage going negative. Adding a zener clamp can be effective in controlling this voltage. As always, reducing the line inductance or avoiding disconnection of the load is the best approach.

Overall, most of the issues that result in component damage or the necessity for resets are due to voltage spikes from hot plugging/unplugging components. The two most problematic cases are hot plugging a charged adapter into a charger and removing the adapter when directly powering a



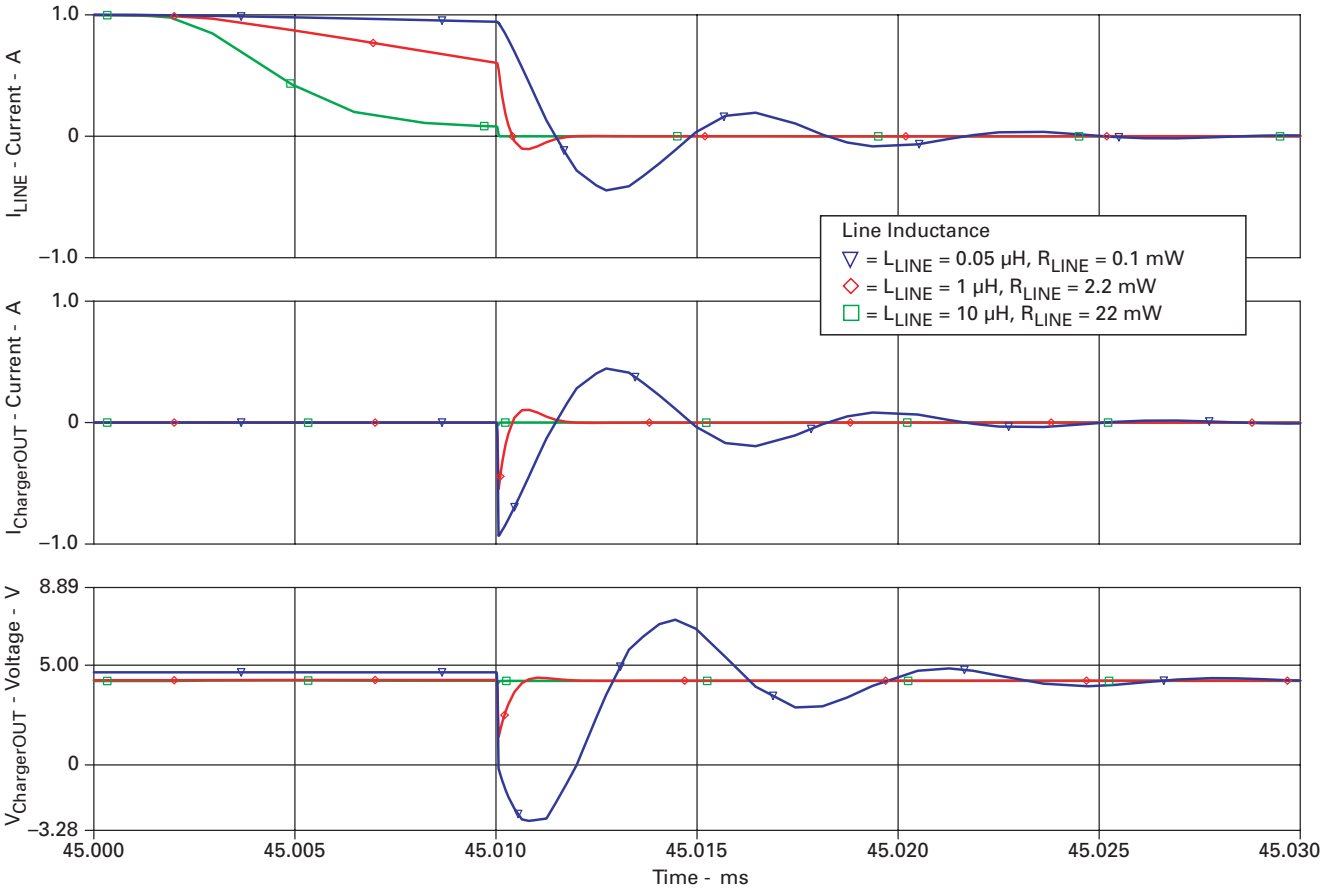
Battery unplugged from linear charger in constant-current mode.

The line inductance is equivalent to 2.5" (0.05 µH), 50" (1 µH), or 500" (10 µH) of line cable. If the line conductors form a large loop, the inductance may be in the microhenry range with a much shorter length (<100").

V_R = Voltage drop from V_{IN} to V_{BAT}.

IC = Initial condition.

a. Schematic.



b. Plots of current and voltage.

Fig. 10. Battery removal during fast charge for a linear charger, with the system in low-power mode.

heavy system load. This is because charged inductors can't change current instantly and will go to whatever voltage is needed to keep the current flowing. These inductive voltage transients often find the breakdown voltage of the lowest-rated component. The best solution is to reduce the line inductance by minimizing the length of the cables. This alone should eliminate the problems. If there is a need for long cables, the design should account for the potential problems presented. The typical solutions to consider are damping by series resistance or RC snubbing; clamping voltages with zeners; or increasing component ratings. Twisted pairs have the lowest inductance per length. To calculate wire inductance (signal and return) for twisted or parallel pairs, use 10 to 20 nH per inch of cable as an estimate. For a series RLC circuit, critical damping takes place when alpha and omega are equal and $R = 2\sqrt{L/C}$. For a parallel RLC circuit, $R = 0.5\sqrt{L/C}$.

Hopefully this discussion will help the designer consider, during the design phase, the potential field application problems that can arise from voltage/current transient failures.

IV. Effects of Charging a Battery with a System Load

In portable power, integration is paramount; and the trend is to use the battery charger also as a power source for the system. This seems like a logical progression, but several new issues arise that the charger controller has to handle. These problems are mainly associated with the system load profile. Understanding the system load profile is the key to finding system design solutions. The main problems occur during startup and termination.

In portable power the trend is to use high-energy, high-density batteries that give the longest run time for the smallest package size. The 4.2-VDC Li-ion battery has become increasingly popular among manufacturers; it fits well with the typical load/charge usage patterns of the consumer, since it is not susceptible to memory effects. For this reason, this section of the paper deals mainly with 4.2-V Li-ion batteries, with a few comments about the other chemistries along the way.

In the past, there were no start-up issues for stand-alone chargers. If a discharged battery was installed, the charger would start with a precharge current if the battery voltage was below ~3 V; with a constant current charge if between 3 and 4.2 V; and with voltage regulation if at 4.2 VDC. When the charger current dropped to ~C/10, the charge cycle would terminate. If the protector was open and the output was 0 V, a precharge current would attempt to close the protector. With the integration of a system load in parallel with the battery came start-up and termination issues.

The start-up issues occur when the stand-alone charger is used as a building block in the system design. If the charger powers up into precharge mode ($V_{BAT} < 3$ V), the power delivered will be

$$P = IV = (C/10) \cdot V = (I_{CHG}/10) \cdot V_{BAT}$$

and the system's average load (in watts) most likely will be greater than the power delivered. The system will have to go into a low-power mode so the precharge current can do its job and bring the battery into fast charge. If the charger enters fast-charge, constant-current mode, the system load (in watts) will still have to be considerably less than the charger output (in watts) for the battery to charge in a timely manner. The maximum available power deliverable by the charger occurs during voltage regulation:

$$P = IV = I_{CHG} \cdot 4.2 \text{ VDC}$$

The lower the output voltage, the less power a constant-current charge delivers:

$$P = I_{Fixed} \cdot V$$

Many constant-power loads (such as switching converters) require more current as the voltage drops. Therefore, the best way to avoid depleting the battery during charge is to keep the average system load (in watts) lower than the lowest charger output (in watts) in fast-charge mode:

$$P = I_{CHG} \cdot V_{BAT} = I_{CHG} \cdot 3 \text{ V}$$

Considering these issues during the design phase will insure a more robust product. Once fast charge enters voltage regulation, the concerns focus on proper termination.

Termination issues arise when the charger controller is designed with the assumption that all output current will go to the battery. With a system load connected across the battery, the charger can't determine the destination of the current. Battery manufacturers recommend terminating charge when the battery is full. Charging can be resumed after the battery is partially discharged. Leaving the pack connected to a voltage source (LDO) is not recommended. Termination is typically based on $I_{CHG}/10$, which is not likely to occur if there is a system load in addition to the battery charge current. If the termination is delayed, the safety timer may expire, terminate charging, and enter fault mode. Disabling the safety timer solves this problem but creates others. The purpose of the safety timer is to protect against a bad cell that is not taking a charge. The root problem of proper termination is that the charger can't accurately determine the actual minimum current of the battery. For these reasons, it is critical that the designer fully understand the system load profile and how it relates to the charger functions.

There are four controller thresholds that should be analyzed when the dynamic load profile is considered: precharge/fast-charge, taper, termination, and refresh. Transients near these thresholds may cause a change in charging states. Deglitch filters often take care of many transients, but some load profiles require additional application circuits for the product to operate as desired. Setting the duration of the safety timer requires understanding of the average system load current. A discussion of the external solutions for the different thresholds follows.

A. Precharge Threshold

Problem

Entering precharge from fast charge due to a pulsed load will reduce the charge current to a level that may not charge the battery or supply sufficient power to the system.

Solution

1. Identify the amplitude of the load pulse and the circuit and battery impedances to determine at what threshold the system needs to enter a lower-power mode to avoid dropping out of fast charge. Add more low-impedance filtering on the output if necessary. If there is a deglitch (filter) time before a mode change and the average power load is less than the output of the charger, there should not be an issue unless the load step is longer than the deglitch time.

2. Add an RC filter to the battery feedback voltage to filter the transient. This is equivalent to a deglitch circuit for load transients.

3. Have a microprocessor monitor the battery voltage and control the system load to avoid getting near this threshold. Keep in mind the diminishing returns: As the pack voltage drops, the power delivered by the charger drops, while the system load typically remains at constant power. A safe design will have an average system load (in watts) that is less than the minimum charger power output in fast-charge mode. In precharge mode, the system should be in sleep mode.

B. Taper Threshold

Problem

At the taper threshold the battery is considered full, but often a timer is set to give a little more charging time before termination. If there is a dynamic load or a slow-stepping system load, the threshold is exceeded and the timer is reset, avoiding normal termination.

Solution

1. For a transient load where the average current is below the taper threshold, the feedback sense current can be filtered to remove any transients. Average-current-mode chargers that use a current mirror to program the output current with an external high-value resistor are excellent candidates for filtering. Applying a small capacitor across the programming resistor to average the waveform prevents transients from affecting the taper timer.

2. For stepping loads with long durations (in seconds) that are not practical to filter, a circuit to detect a preset valley can be implemented to terminate the charge as shown in Fig. 11. This circuit was designed to interface with a charger that terminates instantly if the charger's current drops near zero. Switch Q4, controlled by a status output pin, disables the circuit during a no-charge condition to prevent battery discharge. Q22's emitter is preset just below the normal current

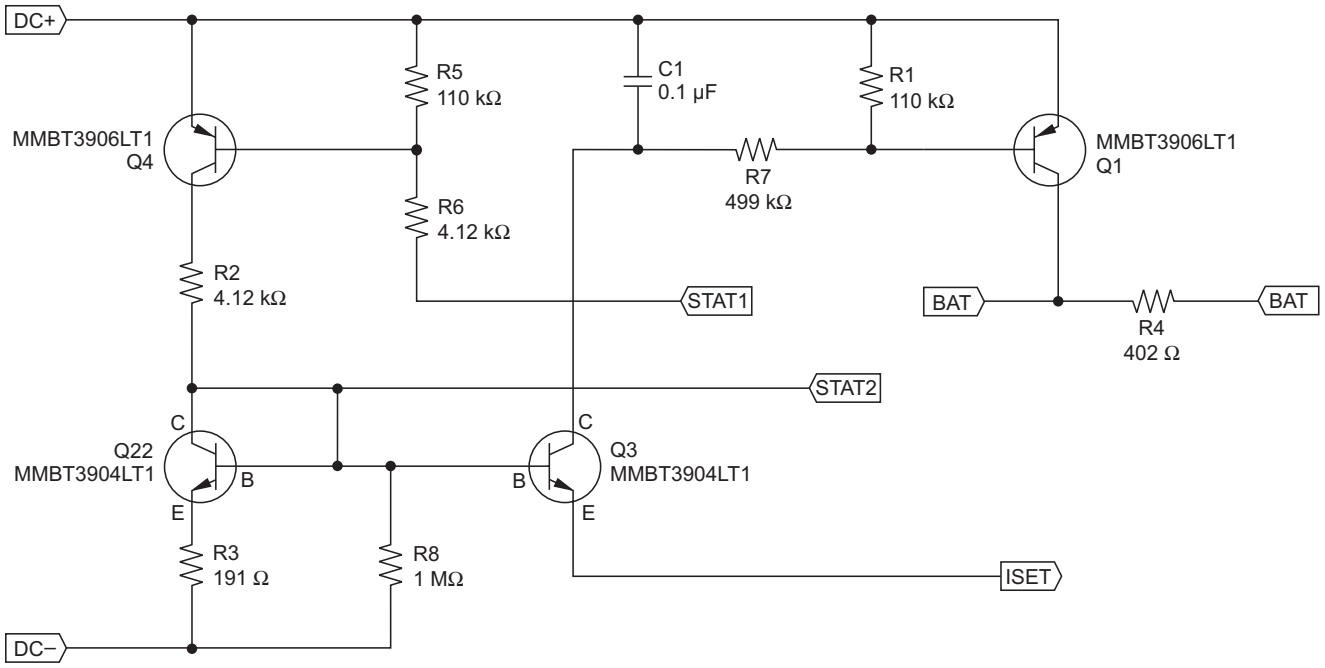


Fig. 11. Termination circuit triggered by minimum sense current.

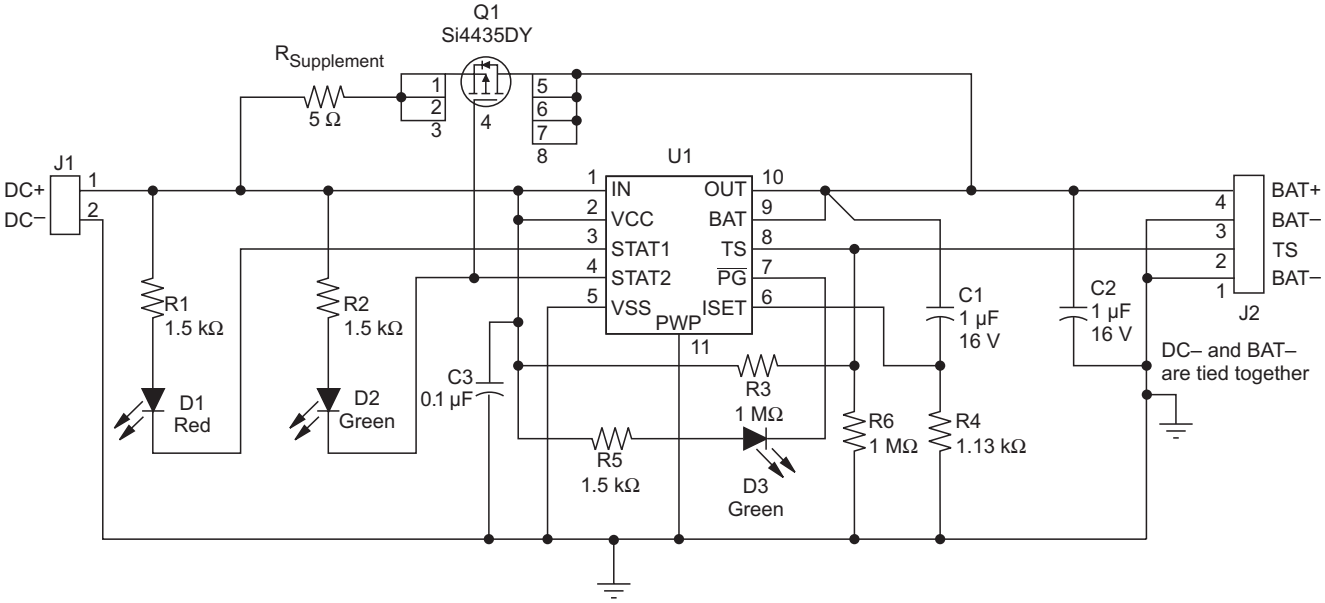


Fig. 12. Supplemental 160-mA charging current from input through Q1 to output offsets system minimum load. If system load current is 150 mA, all of the charger current will go into the battery and will terminate properly.

taper-threshold voltage by dividers R2 and R3. If Q3's emitter's voltage, which is tied to the sense current signal, drops below the voltage on Q22-E, Q3 turns on and pulls on Q1. This applies a current to the battery feedback signal at the IC's error amp and produces a small voltage on top of the battery pack voltage, thereby making the controller "believe" that the battery is slightly above voltage regulation. The charge current is reduced, which further reduces the sense voltage. This positive feedback drives the charge current to zero, and the controller terminates due to zero current. The battery then has to be discharged down to the refresh threshold for the charge to continue.

3. Another possibility for a fixed minimum system load is to supplement this current from the input source through a resistor and P-channel FET to the system (see $R_{Supplement}$ and Q1 in Fig. 12). The charger will no longer be delivering this current, and the battery can terminate normally. The gate of the FET is tied to the status pin that goes high when charging is terminating. This disconnects the supplemental current, which prevents overcharging of the battery.

C. Termination Threshold

There are several notable problems in dealing with termination.

If a system load is removed quickly during voltage regulation, it is possible for the battery to overshoot voltage momentarily due to the energy stored in the line inductance, which would drive the pass FET off and terminate the charge. This may result in termination with a battery at less than full capacity. The solution is to reduce the line inductance, reduce the amplitude or speed of the transient, or filter the battery sense feedback signal.

There are other conceptual problems with termination. Often designers use the C/10, C/5, or C/15 termination threshold as a figure of merit. One problem is that this is relevant only at a 1C programmed charge rate. In reality, if a fast charge is set to C/2, the termination threshold is actually at $I_{PGM}/10 = (C/2)/10 = C/20$. Thus the "C/10" termination threshold actually results in a termination of 1/20 the C-rate of the battery.

There are other problems associated with full capacity. The accuracy of termination affects capacity. The desire to have low power dissipation at fast charge necessitates having a small-current sense resistor. At termination the charge currents are very small. A small current multiplied by a small resistance is a small control signal that is very susceptible to noise. This problem is compounded if the battery is charging at less than 1C, since the termination then would be < C/10. To overcome these accuracy issues, a taper threshold (the point at which the battery is deemed full) can be created to set a 30-min timer for termination. The charge current tapers at an exponential rate, so accurately detecting the taper threshold makes little difference at the end of 30 min.

Other methods of current sensing and regulation use matched transistors that have the same biasing and are scaled to different current levels. For example, the current sense matched transistor in TI/Benchmarq products is typically 1/320 of the larger charge-pass transistor and delivers 1/320 of the current to the charge current program pin. The current is regulated by connecting a large resistance (0.7 to 8 kΩ) to this current source and driving the pass FET (on/off) to regulate the resistor voltage to 2.5 V. This allows one to program the output current by changing the program resistance:

$$R = 2.5\ VDC \bullet 320/I_{PGM}$$

Chargers with nickel chemistries shouldn't have any transient load in parallel with the battery, since any increase in load would produce an IR drop. This drop would be detected as a peak voltage detect (PVD), which terminates charge. The solution for dynamic loads is to monitor the temperature change in the battery pack via a thermistor. When the rate of change of ~1ºC/min is reached, termination occurs. This method of termination is not affected by load transients.

D. Refresh Threshold

Problem

If the battery is full, the charge has terminated, a system load is applied, and the battery is removed, the charger often will not start charging without going through a battery-detect cycle or a deglitch filter. This may cause the system to crash before the charger supplies sufficient power.

Solution

Add enough system capacitance to hold up the output for the deglitch and/or battery-detect routine time. An alternative is to detect the battery removal and toggle the charge enable pin to restart a charge. This still will require significant holdup capacitance.

One can see that there are many issues with adding a system load in parallel with the battery; and most of these issues have work-around solutions involving additional circuitry, provided the load profile is understood. Many manufacturers cannot predict all the load scenarios that may happen in the field. The next section presents one optimal solution that eliminates many of the problems with connecting the system across a battery while it is charging.

V. The Proper Way to Power a System Load from a Battery Charger Circuit

The recommended solution is to power the system directly from the input source, when it is available, and at the same time to charge the battery from the input via the charger. This allows the charger to be dedicated exclusively to the battery without any external disturbances. The overall efficiency is also greater, since the power to the system is not regulated down to a lower voltage by a linear regulator. This recommended solution does have some issues that are discussed next.

The transition timing of the FETs is the primary issue to consider when power to the system is switched from an input source to the battery pack. There are two types of switching transitions: "make-before-break" and "break-before-make." The former will connect the secondary source before disconnecting the primary source to make sure the system never loses power. The problem with this type of power transfer is that, if the sources are at different potentials, the sources may interact and cause damage or potentially high shoot-through currents.

Break-before-make switching will disconnect the primary source before connecting the secondary source, which solves the interaction between the supplies but momentarily causes the system to lose power. This method requires enough system capacitance to hold up the voltage for a specified amount of time.

Fig. 13 shows an example of how to implement switching between the source and the battery. When the input voltage is greater than the battery voltage, the power good ($\overline{PG}$) signal pulls low, turns on Q1/Q4, and turns off Q3 and Q2. If the input source drops below the battery voltage, the $\overline{PG}$ signal goes high, which turns off Q1/Q4 and turns on Q3 and Q2. The threshold of Q1 and Q3 overlaps such that when their gates are at 2.5 V, they are both nearly off (> 1 kΩ from source to drain). The partial overlap of the FET's turn-on thresholds emulates a break-before-make circuit.

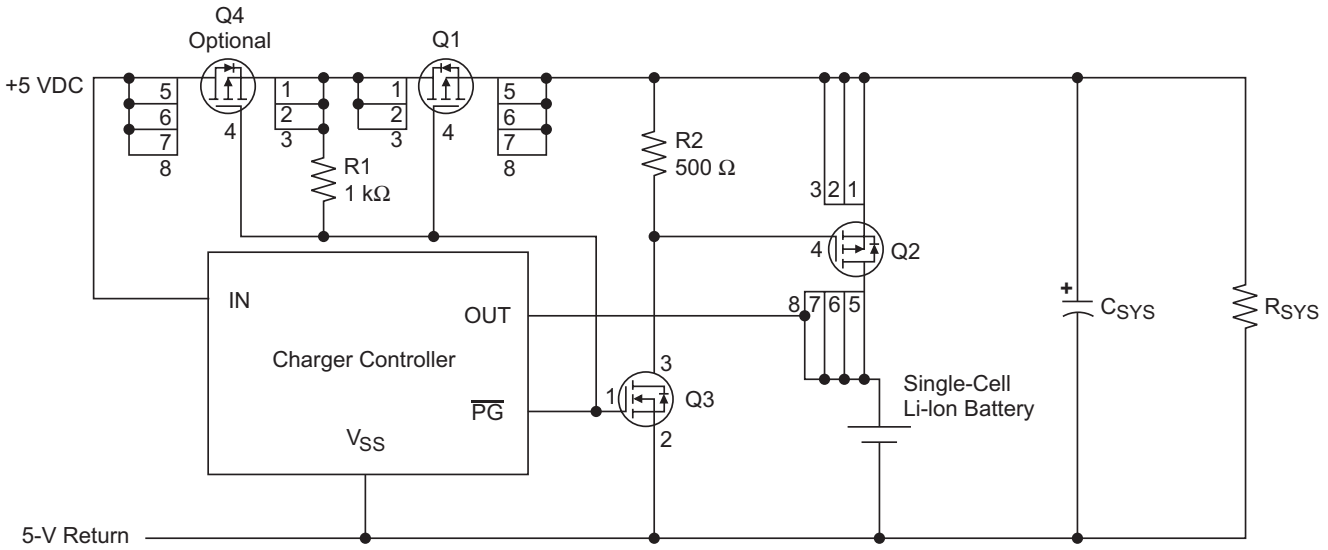


Fig. 13. Stand-alone battery charger controls power to system and battery.

The system capacitance should be large enough to hold up the system voltage for this 10- to 50-µs time period. Q2 has its body diode such that the battery can supply the current to the system if the system voltage falls a diode drop below the battery voltage. Q4 is optional and is needed only if there is something hanging on the input that will load the battery via the body diode of Q1. The charger controller selected for the design should have a $\overline{PG}$ pin to control the switching. (A status pin that shows sleep mode could be used as well.)

Placing the system load in parallel with the battery complicates the task of a smart charger. It is impossible for the charger to determine where the current is going or the condition of the battery. Designing a charger for a known DC system load across the battery requires some additional design, but designing for transient loads immensely complicates the task. The long-term solution for putting the system load in parallel with the battery is to emulate the circuit design in Fig. 13. This design powers the system from the input and switches the battery to the system only when input power is lost. This approach can be extended for multiple Li-ion cells with a little more attention to both timing and cross-conduction issues. Keeping the system current separate from the battery current during charging will also simplify the task of managing the battery pack.

VI. Summary/Conclusion

This paper has attempted to cover many issues that typically arise during the design and testing phase of a battery charger. Circuit design, thermal and layout issues, and other design concerns were discussed for power conversions. Product testing and return current issues dealing with connecting and disconnecting charging components during charging were presented. The paper concluded with issues surrounding charging a battery with a system load across the battery. Even though many types of work-around solutions were examined, the best is to power the system from the input, let the charger be only a battery charger, and connect the battery to the system only when input power is lost.

VII. Reference

[1] *DV2954S1H Li-Ion Charger Development System*, User Manual, TI Literature No. SLUU053

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