Noise Management in Portable RF Systems

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ABSTRACT

The evolution of battery-powered, handheld RF equipment has demanded ever-increasing battery life, which translates into higher efficiency requirements in the power supply. In some designs these efficiency improvements have been achieved by migrating from linear to switching supplies. Highly efficient state-of-the-art modulation schemes place stringent requirements on distortion and adjacent channel interference, which mandates that careful attention be paid to all noise sources, particularly those that are conducted throughout the power-supply system. This topic discusses noise generation and suppression in switched-mode and linear regulators as well as techniques to manage noise in portable battery-powered RF systems.

I. INTRODUCTION

A representative block diagram of a portable, battery-powered RF system is shown in Fig. 1. A number of potential noise sources are present: switched-mode power supplies; an AC power source; baseband and RF oscillators, amplifiers, and modulators; linear regulators; and interference from external sources. There are three ways that noise couples into other circuitry: electromagnetic coupling through the air and circuit-board dielectric, conduction through circuit-board traces and components, and conduction through the ground plane. If these noise sources sufficiently couple into the signal chain, they can cause unwanted interference, possibly enough to fail FCC regulations.

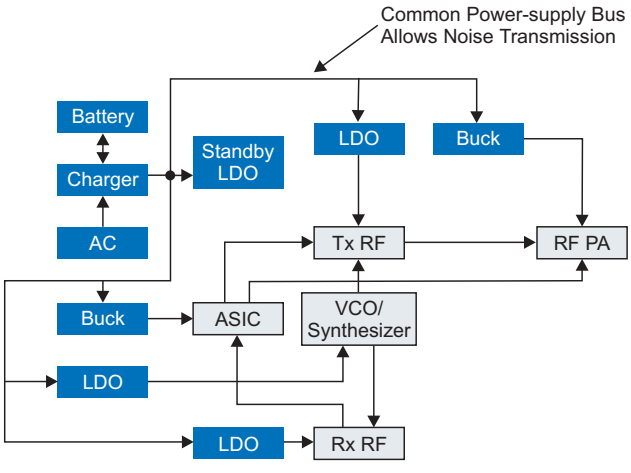

Fig. 1. Typical battery-powered RF system block diagram.

II. SOURCE IMPEDANCE

The source impedance of a freshly charged battery is typically very low. Some other power sources such as a partially discharged battery, a wall adapter, or a battery charger can result in higher source impedances. Long circuit-board traces, vias, and interconnecting wires also increase source impedance. The resistive part of source impedance causes ripple at its output due to the effective degradation of load regulation of the supply. The inductive part of source impedance causes voltage spikes on the power-supply line when load transients occur. This inductance can cause high voltage spikes at the input to power-supply integrated circuits (ICs), possibly exceeding safe operating levels. Due to these effects, source impedance can be a source of unwanted supply noise to the entire system. Voltage ripple (V_{RIPPLE}) due to a series trace resistance (R_{TRACE}) and a switched-supply current ripple (I_{RIPPLE}) is easily calculated as:

$$V_{RIPPLE} = R_{TRACE} \bullet I_{RIPPLE} \quad (1)$$

The input current (I_{RIPPLE}) waveform to a buck converter looks like a square wave from zero current to I_{LOAD} plus half of the small-inductor current ripple (I_L):

$$I_{RIPPLE} = I_{LOAD} + (1/2)I_L \approx I_{LOAD} \quad (2)$$

A series R_{TRACE} of 100 mΩ and an I_{LOAD} of 500 mA results in a 50-mV peak-to-peak ripple. Switching noise on the input power supply can be

greatly reduced by placing bypass capacitors at the input of switching regulators.

III. Buck and Boost Converter Topology Review

Switched-mode regulators are very efficient at converting one DC voltage to another because they use "lossless" components to achieve voltage conversion. These regulators also have several sources of noise that can be radiated and conducted throughout other circuitry. The buck regulator shown in Fig. 2 has several such sources: a ripple current in the inductor L, a current waveform at the input to the switch, equivalent series inductance (ESL) and equivalent series resistance (ESR) of C_{IN} and C_{OUT}, and the switching waveforms driving the gate of the switch. An understanding of these noise sources and design techniques to mitigate them are essential to good power-supply design for noise-sensitive applications.

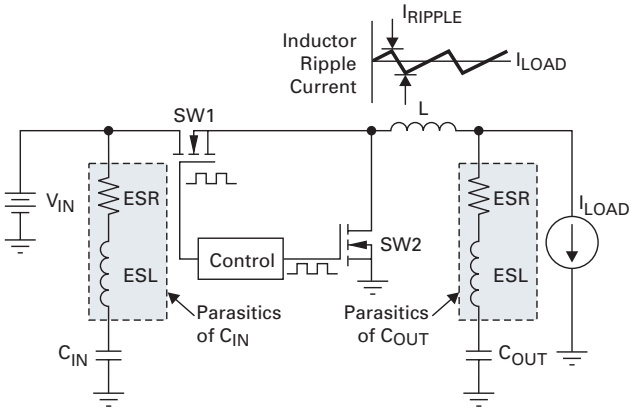

Fig. 2. Buck converter schematic.

A. Charge/Discharge of Switch Gates

Voltage and current waveforms that are present when the gates of the switches are being charged and discharged can be a significant source of noise. Peak-to-peak amplitudes can be multiple volts with sharp rising and falling edges and with ringing present after each switch transition. The current and voltage waveforms depend primarily on gate drive capability, gate parasitic capacitance and resistance, and control-loop methodology and compensation. If external switches are employed, lower C_{GS} and higher R_G reduce noise at the expense of $R_{DS(ON)}$ and efficiency.

B. Ringing at the Switch Node

For both integrated and external switches, ringing can be seen at the node common to the switches and inductor due to the tank circuit formed by the inductor and stray capacitances on this node. A snubber circuit (shown in Fig. 3) can be used to absorb this energy and reduces ringing at the expense of efficiency.

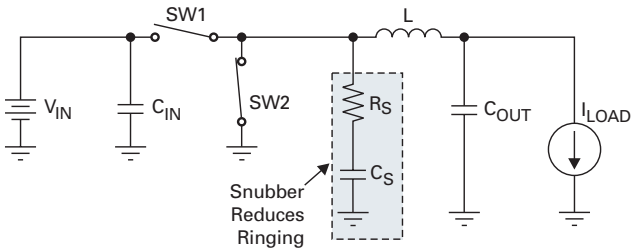

Fig. 3. Snubber used to reduce ringing at the switch node.

C. Switched Inductor Current

The AC current waveform in the inductor causes a changing electromagnetic field in its vicinity. This field can be coupled to nearby traces, components, and the ground plane, causing small voltage perturbations that appear as noise at the switching frequency and its harmonics. The amplitude of coupled voltage in a buck converter is dependent on inductor construction, peak-to-peak inductor current ripple, frequency components of the inductor current slope, and physical layout design. Shielded inductors are manufactured for switching converters to contain the inductor fields, possibly at the expense of efficiency, cost, and component size. Attention should be paid to these fields during board-layout design to prevent the fields from coupling to critical nearby lines. If layout constraints require that traces be run very near traces or inductors with these switching currents, it is generally preferred to make these DC traces so that bypass capacitors can be added to the coupled lines to reduce noise voltage. In addition, surrounding the inductor and switch nodes with ground planes is good practice.

D. Output Capacitor Selection and Load Transients

Load transients can cause output voltage ripple that can be a source of noise to loads that share a common supply bus. If the output of each converter

is treated as a source with some impedance connected to a supply bus, placing bypass capacitors near each load can greatly reduce this noise on the supply bus. Fig. 4 shows the behavior of a typical buck converter during a load transient. The top part of the figure shows the load-current transient and the resultant inductor-current waveform. The bottom waveform is the output voltage response.

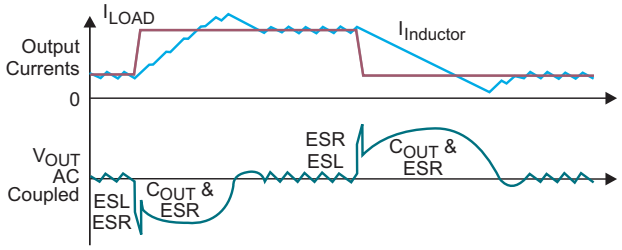

Fig. 4. Load-transient response in a typical buck converter.[1]

The initial undershoot spike is dependent on the load-transient magnitude, slew rate, and the ESL and ESR of the output capacitor. This undershoot can be minimized by use of large-value, low-ESL and low-ESR output capacitors.

The undershoot after the initial spike results from the time it takes for the inductor average current to catch up to the new load current. The amount and duration of this undershoot depend on the inductor value being used and on the IC switching frequency and feedback control loop characteristics. The current increase per switching cycle is inversely proportional to the inductor value, so small inductors improve load-transient response.

When this undershoot has been overcome, the inductor current may have overshot the average load current, resulting in a slight output-voltage overshoot. A negative-going load transient has very similar characteristics. While the undershoot in the positive transient is dependent on both the input and output voltage, the negative transient overshoot is dependent only on output voltage. A bulk-storage tantalum capacitor is needed when load transient di/dt can be large compared to the slope of inductor current [(V_{IN}/V_{OUT})/L].

The filter formed by the inductor and output capacitor of a buck converter filters noise conducted from the input supply rail or resulting from switching waveforms in the regulator. A high-quality ceramic capacitor can be effective in bypassing both switching and broadband noise, while a bulk tantalum capacitor helps with the relatively slower load transients.

E. Frequency-Synchronized and Phase-Offset Supplies

When multiple switching supplies are used in a system, they can be synchronized to a common clock frequency to avoid filtering multiple clock frequencies. Clocks can be phase-offset so that only one switcher draws current from the supply at a time. This reduces the peak load currents and therefore the voltage ripple on the common supply; it also reduces the capacitance needed on the supply source for a given ripple.

F. Power-Savings Modes

Many modern switching regulators offer power-savings modes, typically pulse-skipping or frequency-reduction modes for when light load currents are present. In pulse-skipping mode, the inductor current is allowed to decay and remain at zero until the output voltage falls below tolerance. Then a number of switching cycles are performed to bring the output voltage to its upper tolerance. This cycle repeats and results in the waveforms shown in Fig. 5. One benefit of this power-savings approach is that switching noise frequency is constant; although a new, lower switching frequency is introduced due to pulse skipping.

In frequency-reduction mode, the switching frequency is reduced significantly to improve efficiency. This has the disadvantage of creating a wide spectrum of noise that is more difficult to filter.

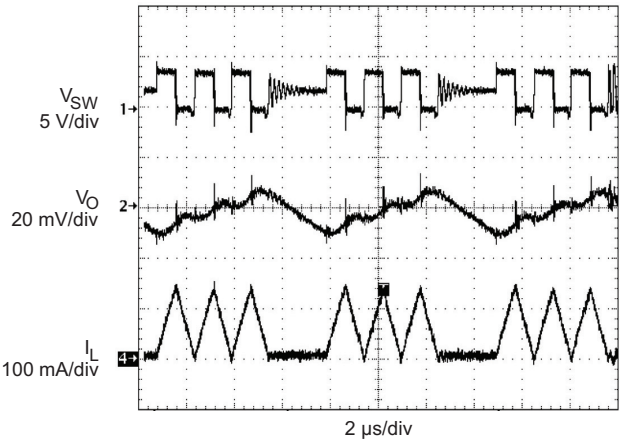

Fig. 5. Ringing at switch node in buck converter without a snubber.[2]

G. *Layout Considerations*

The schematic of a buck converter is shown in Fig. 6. Connections that are sensitive to layout are highlighted with bold lines. The following guidelines apply to the layout of this circuit and are illustrated by the layout shown in Fig. 7:

- **C_{IN}** – A low-ESR and low-ESL capacitor of high value is desired for C_{IN}. Effective ESR and ESL include traces and vias connecting the capacitor to the supply line and to ground, which includes the ground return current path. C_{IN} should be located physically close to the IC to provide the lowest source impedance possible.
- **L1** – Long traces connecting to L1 increase the amount of radiated energy. These traces should be kept as short as is practical.
- **C_{OUT}** – As with C_{IN}, trace and via impedances to the source and ground add to the ESR and ESL of this capacitor. Low ESR and ESL minimize output voltage ripple from charge being injected and removed from this capacitor. Higher values for C_{OUT} also improve output voltage ripple by minimizing changes in output voltage that are due to increasing or decreasing stored charge in the capacitor.

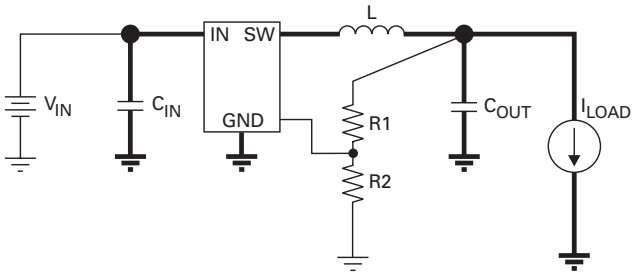

Fig. 6. Buck converter schematic. Bold lines show critical layout areas.

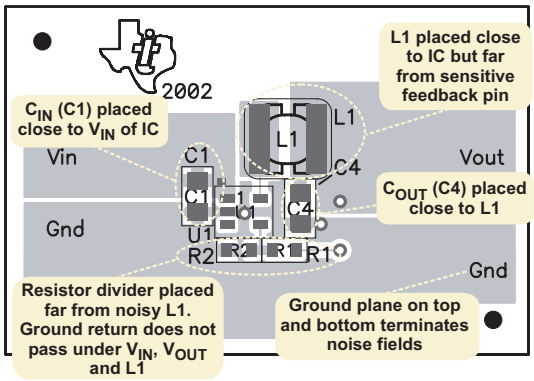

Fig. 7. Compact buck converter layout optimized for performance and noise.[3]

- **Tap point** – The tap for the feedback pin should be taken close to the load rather than closer to the inductor L1. This improves load regulation by taking into account trace resistance between L1 and the load. The tap point is also isolated from switching noise by physical location and the ground plane.
- **IC ground connection** – The ground connection for the IC should have a very low impedance. This is accomplished by having a short return path to the input supply of the device.
- **Tight layout** – In general, tighter layouts that reduce any line lengths that carry AC voltage or current waveforms will reduce radiated noise.

IV. Low-Dropout (LDO) Linear Regulator Overview

LDO linear voltage regulators, while generally being less efficient than switching supplies, have significant advantages in noise suppression and generation. A typical block diagram of an LDO is shown in Fig. 8. The bandgap provides a voltage reference that is stable with supply, temperature, and process variations. This voltage is compared with a sample of the output voltage, and the error amplifier modulates the series resistance of the pass transistor to maintain a constant output voltage under all conditions. A noise-reduction (NR) or bypass pin is typically included on low-noise LDOs to suppress noise generated by the on-chip bandgap. Due to the improved noise suppression properties of LDOs, power-supply designers often use them to filter noise from switching supplies or other noisy

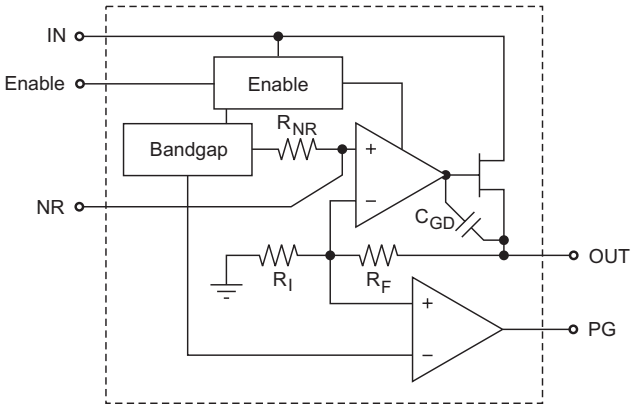

Fig. 8. Simplified LDO block diagram.

supply sources. LDOs also may be preferred for applications that need fast load-transient response.

A. Noise Generation by LDO Regulators

The dominant noise source in LDOs results from shot noise in the bandgap and is related to $V_T \bullet \ln(N)$, where V_T is the thermal voltage and N is the ratio of the area of two transistors used in a bandgap. This is a broadband white-noise source roughly proportional to $1/\sqrt{I_C}$, so LDO designers can reduce the amount of noise by increasing the current consumed by the bandgap. Bandgap noise also can be reduced if an NR (bypass) pin is present on the LDO as shown in Fig. 8. An external capacitor connected to this pin creates a pole in the broadband noise spectrum of the reference. The time constant of this pole is determined by $Z_{NR} \bullet C_{NR}$, where Z_{NR} is R_{NR} plus the output impedance of the bandgap; and C_{NR} is the bypass capacitor value.

Power-supply designers should pay careful attention to the effects of C_{NR} on start-up time. Low-current bandgaps are often used in LDOs designed for battery-powered equipment, so it may take several milliseconds to charge an external capacitor, significantly slowing start-up time. Some LDO regulators mitigate this effect by using a quick-start circuit to increase the current drive of the bandgap output. The output capacitor is also an important factor in bypassing output noise. Fig. 9 shows the effects of C_{OUT} and C_{NR} on output noise.

The following relationship shows the impact of output voltage on output noise:

$$V_{N(OUT)} \cong V_{N(BG)} \bullet (V_{OUT}/V_{BG}) \qquad (3)$$

where $V_{N(OUT)}$ is the output noise voltage, $V_{N(BG)}$ is the bandgap noise voltage, V_{OUT} is the regulator output voltage, and V_{BG} is the bandgap voltage. It is easily seen that, when output noise specifications on LDO data sheets are compared, they should be scaled to a common output voltage for proper comparison.

Designers must be careful when comparing output noise on LDO data sheets. Few data sheets present noise characterization under identical conditions. The conditions for output voltage, output current, output capacitance, C_{NR}, input voltage, and frequency range must all be the same in order to compare the noise of one LDO to another. To emphasize the importance of frequency range, for pure white noise the amount of noise between 10 Hz and 50 kHz is the same as between 50.01 kHz to 100 kHz.

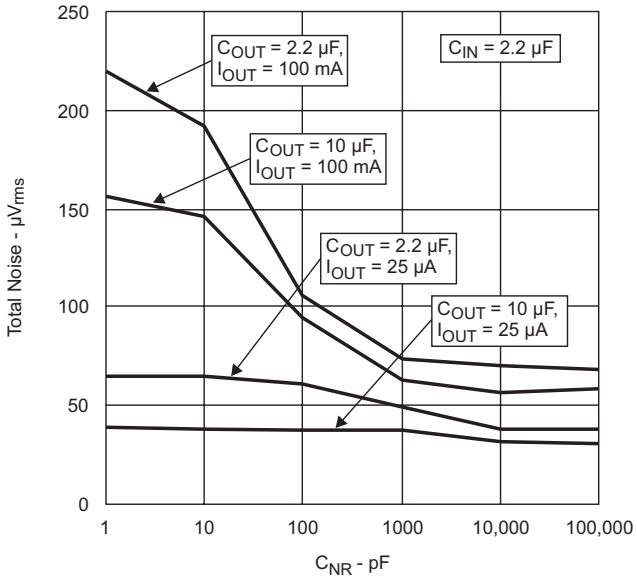

Fig. 9. Output noise as a function of C_{NR}.[4]

It is also important to study the noise spectral curves to determine if noise in critical bands is within acceptable limits. For example, noise within the bandwidth of a PLL is rejected by the effective PLL gain. Noise outside this band will show up at the output.

Designing low-noise power supplies with LDO regulators is not difficult as long as careful attention is paid to characterization conditions, the noise spectrum as it pertains to a specific design, and the choice of C_{OUT} and C_{NR}.

B. LDO Power-Supply Rejection

A relatively high power-supply rejection ratio (PSRR) is often the most important attribute of LDO regulators. PSRR at low frequencies is determined almost solely by the error amplifier loop gain. This is also demonstrated as better DC accuracy over input-voltage and load-current variations. Rejection of typical switching-supply frequencies (50 to 100 kHz) up to 50 dB can be achieved with an LDO if good design practices are followed. This higher-frequency PSRR can be

thought of as a function of the low-pass filter action of Z_{OUT} (output impedance) and Z_{IO} (input to output impedance) as shown in Fig. 10.

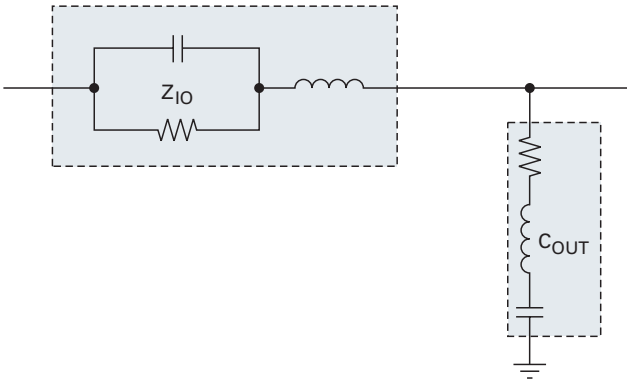

Fig. 10. Schematic of low-pass filter composed of Z_{OUT} and Z_{IO}.

To increase PSRR, Z_{OUT} can be reduced and Z_{IO} can be increased. Z_{OUT} is determined by:

$$Z_{OUT} = Z_{C_{OUT}} // Z_{O(LDO)} \quad (4)$$

where $Z_{O(LDO)}$ is the output impedance of the LDO and C_{OUT} is the output capacitor or combination of capacitors. $Z_{O(LDO)}$ and Z_{IO} are determined by the internal IC design if the pass transistor is integrated, and they are affected by the external pass transistor of LDO controllers. The following effects can be seen in LDOs whether the pass transistor is integrated or external:

- **Effective resistance of the pass element** – At light load currents the pass transistor resistance is relatively high, increasing Z_{IO} and improving PSRR. At high load currents the resistance is lower, decreasing PSRR.
- **Configuration of the pass element** – The common source topology of P-type pass transistors causes an out-of-phase relationship between the control node and the regulator output. In this case, parasitic capacitance from the regulator input to the control node can work in favor of PSRR due to the canceling effect of the control-to-output phase relationship if the transistor gain is > 1.0. In an N-type configuration, the common-collector topology gives a gain of about 1 from the control node to the output, so noise coupled from the regulator input to the control node passes directly to the regulator output.
- **Parasitic C_{GD} of the pass element** – In both P- and N-type topologies, the voltage gain from gate to source is unity, so the parasitic capacitance from gate to drain passes ripple voltage from the input to the output.
- **Parasitic C_{DS} of the pass element** – In both P- and N-type topologies, C_{DS} can be an important part of the Z_{IO} impedance. This parasitic capacitance passes ripple voltage from the input to the output.
- **PSRR as a function of $V_{IN} - V_{OUT}$** – Since $V_{DS} = V_{IN} - V_{OUT}$, the pass element has higher gain at higher $V_{IN} - V_{OUT}$, giving better supply rejection as shown in Fig. 11. If the LDO is to be used in or near dropout (usually at low battery voltages), this effect should be considered.

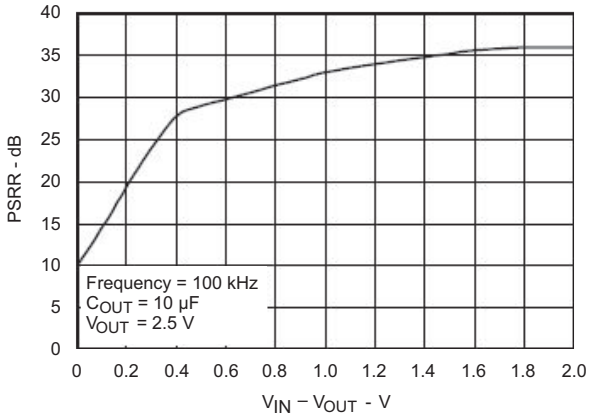

Fig. 11. PSRR vs. $V_{IN} - V_{OUT}$.[5]

Output capacitor selection is also critical to high-frequency power-supply rejection. Low-ESR, low-ESL capacitors give optimal results. Higher-value capacitors also improve PSRR if ESR and ESL are not significantly compromised. High-frequency rejection can be significantly affected by the resonant frequency of C_{OUT}. In Fig. 12 the peaks in rejection at 500 kHz are caused by the 10-µF output capacitor. Changing the output capacitor value can move these peaks up and down in frequency; but variations due to layout, capacitance, and ESL should be taken into account.

Using data sheets to compare the PSRR of two LDOs is often not possible since there is no standard for measurement conditions. PSRR can be significantly affected by $V_{IN} - V_{OUT}$, I_{OUT}, C_{OUT},

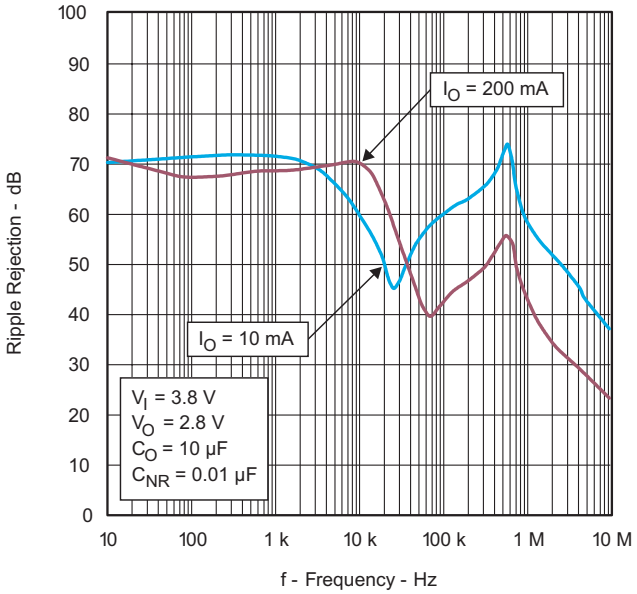

Fig. 12. Ripple rejection vs. frequency, showing peaks due to C_{OUT} resonance.[4]

C_{NR}, and I_{OUT}, so care must be made when specifications from different data sheets are compared.

C. LDO Load-Transient Response

Load-transient response of LDOs is typically very good compared to switching regulators. This improved transient response results in lower output-voltage ripple propagating through the output bus. In pulsed applications or applications requiring fast start-up times, LDOs can provide an excellent solution.

When load current changes rapidly, the pass transistor must change its resistance quickly to prevent the output voltage from changing. The transistor resistance is changed by the error amplifier that drives its gate. The speed at which this occurs is dependent on several factors in the IC design:

- **Control-loop bandwidth** – The regulator can respond only as quickly as the control loop can respond. The higher the loop bandwidth, the faster the regulator will respond to load changes.
- **Dynamic range** – At very low current levels, some control loops are at the low end of their dynamic range and have lower loop gain. This results in degraded transient response on positive-going transients starting from low current. Higher output-voltage undershoot may occur from transients starting near zero output current than from those with, say, a few milliamps of output current.
- **Open-loop output impedance** – Newer N-type LDOs have inherently lower open-loop output impedance, improving load transient response. The load-transient response of an N-type LDO with various C_{OUT} values is shown in Fig. 13. The difference between no capacitor and a typical-value output capacitor is relatively small.
- **Error-amplifier output capability** – The speed at which the error amplifier can charge or discharge the pass transistor gate is determined by its frequency response and its output-drive capability. Increased drive capability usually requires increased supply current, another important specification in many applications.

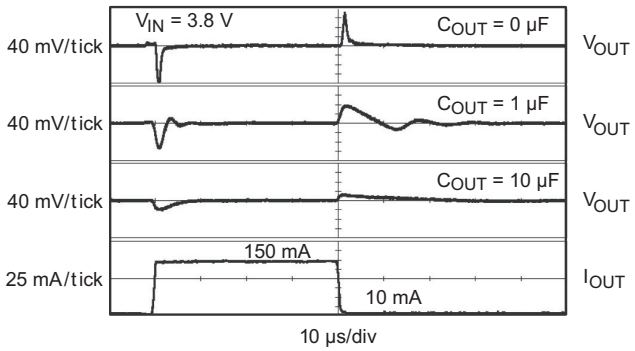

Fig. 13. Transient response of an N-type LDO vs. C_{OUT}.[5]

Load-transient response also can be heavily dependent on $V_{IN} - V_{OUT}$ and the absolute value of the pre- and post-transient load currents. As $V_{IN} - V_{OUT}$ approaches dropout, error-amplifier dynamic range and drive capability are usually compromised, limiting how quickly the regulator can respond to load changes. This can result in over- and undershoot of the output voltage. A good example of this can be seen during certain sequential decreases, then increases, in load current as shown in Fig. 14. A negative-going load transient near zero current that is faster than the loop response will cause an overshoot of the output voltage due to the extra charge dumped into the output cap before the control loop catches up. This extra charge, referred to as a "hiccup," bleeds off at a rate typically determined by the

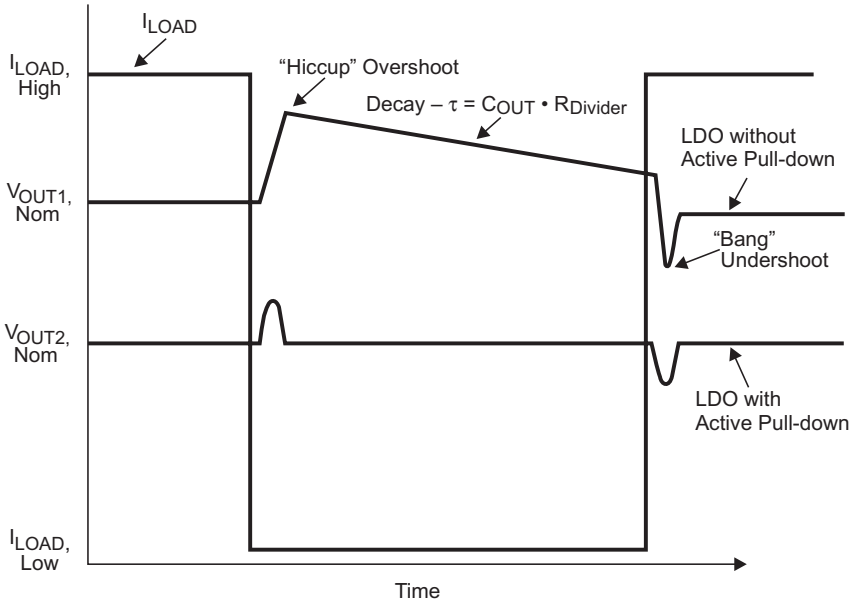

Fig. 14. Transient effects of active output pull-down.

resistor divider that sets the output voltage. If a fast, positive load-current transient (called a "bang") occurs before the control loop catches up, a severe undershoot can result. This hiccup-bang behavior is not a problem for most applications, but designers should be aware that it may occur. Some LDOs have active pull-down devices on the output that turn on when output overvoltage is detected. While this is desirable in some applications, it can be a problem if another supply is to be connected in parallel with the LDO.

Input and output capacitors can affect load-transient response. Low-ESR, high-value capacitors near the input of an LDO can minimize output-voltage droops due to source impedance. Low-ESR, high-value output capacitors also improve transient response by reducing over- and under-shoot during fast positive and negative transients.

Ringing can occur under certain conditions at the unity-gain bandwidth of LDOs. This is caused by low phase margin at this frequency. Increased phase margin reduces ringing at the expense of slower transient response and degraded PSRR.

When the transient response of different LDOs is compared, test conditions must be similar. $V_{IN} - V_{OUT}$, load-transient slope, minimum I_{OUT}, and C_{OUT} all have significant effects on transient response.

V. Conclusion

Noise management in battery-powered portable RF systems demands careful trade-offs between noise and efficiency. Noise sources in switching and linear regulators have been discussed along with design principles to mitigate them. The use of linear regulators to suppress noise has also been discussed. The design techniques presented in this paper provide practical methods for addressing the noise management challenges faced by RF system designers.

VI. References

[1] Brian Lynch and Kurt Hesse, *Under the Hood of Low-Voltage DC/DC Converters*, TI Literature No. SLUP206

[2] *High-Efficiency, SOT23 Step-Down, DC-DC Converter*, TI Literature No. SLVS417B

[3] *TPS62203EVM-211, TPS62200EVM-211*, User's Guide, TI Literature No. SLVU069

[4] *200-mA Low-Noise, High-PSRR Negative Output Low-Dropout Linear Regulators*, TI Literature No. SLVS346

[5] *Cap-Free, NMOS, 150mA Low-Dropout Regulator with Reverse Current Protection*, TI Literature No. SBVS034

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