Section 4

Selecting the Right High-Speed Amplifier

Driving High Speed ADC's and Transmission Lines

Topics Covered

- Pipeline ADC converter input interface options
- Preserving full converter performance in real world applications
- Interface Consideration: RC vs. RLC filter
- Driving Analog and Digital Signals over Transmission Lines

Key Assumptions for this Presentation

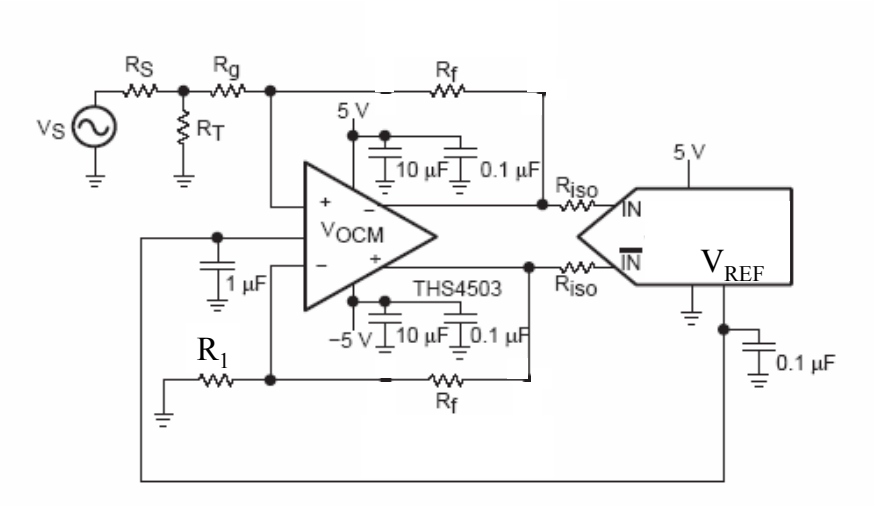
1. Only Looking at Frequency Domain Issues - focus specs are SNR and SFDR for the Converter - and then the Converter + Amplifier + Filter combination
2. Considering only Baseband Application here - 1st Nyquist zone running at Maximum Specified ADC Clock Frequency with a Maximum Analog Frequency below $\frac{f_{CLOCK}}{2}$.
3. Differential Input Signal is only condition analyzed to give best even order harmonic suppression - single ended interface possible, but brings in the 2nd order harmonics as the limiting factor
4. Target Specifications for both the converter and the system are known.

ADC Interfacing Outline

- Some Differential Driver Circuits
  - DC Coupled*
  - Diff. AC Coupled In, DC Coupled Out
  - SE AC Coupled In, DC Coupled Out
  - AC Coupled In and Out
- Combining Amplifier and Converter Performance
- Filter Structure
- Other Amplifier Considerations

(*) For applications where DC-coupling is required, consider using Fully Differential Amplifiers. For all other applications, you can use either regular operation amplifiers, single or dual, or fully differential amplifiers.

ADC Drivers: DC Coupled



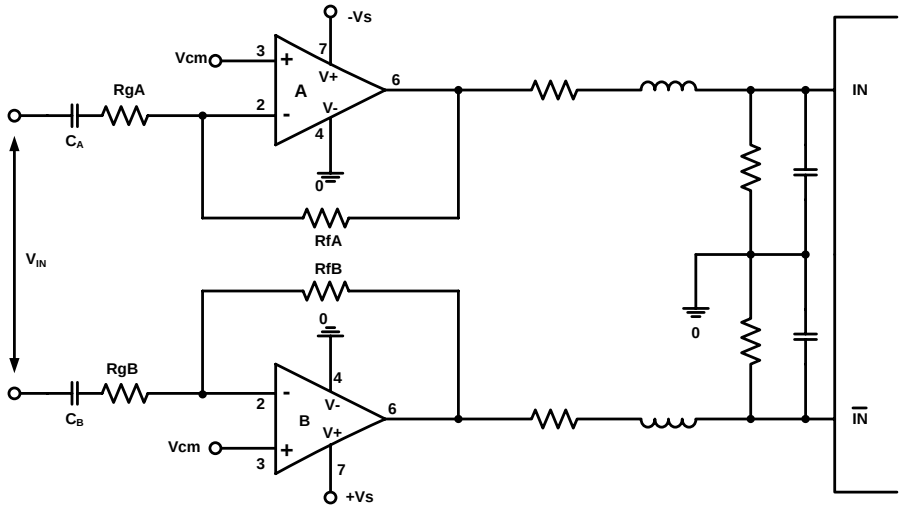
For applications requiring to operate from DC to a maximum operating frequency and transform a single-ended signal to differential, the best choice available to use is differential amplifiers in the configuration shown above.

The differential amplifier above is providing both DC bias and DC coupled differential signal to the converter. R_1 is set to be equal to R_g plus the parallel combination of R_S and R_T.

The Common-mode voltage is tapped from the ADC and adequately bypassed.

The interface between the amplifier and the converter is an RC-filter using the parasitic C of the converter.

ADC Drivers: Diff* AC In, DC Out



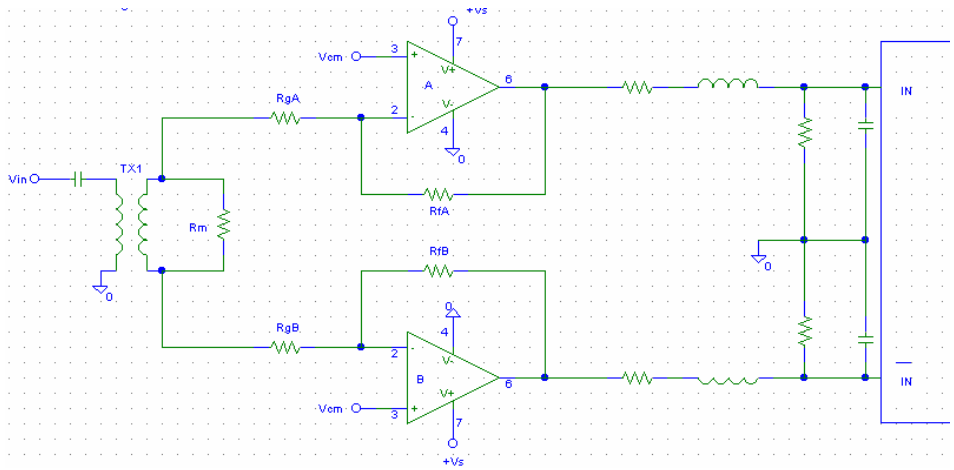
This circuit uses a dual amplifier or two single amplifiers to create a differential signal. It is assumed that the signal is fed differentially and is AC-coupled. The inverting configuration is shown due to the slew rate advantage that can be gained by operating inverting amplifiers. A common-mode voltage if needed can be added through the non-inverting input.

It is shown here that the amplifiers are using single supplies.

A proposed RLC filter is shown here. More details on this RLC filter to follow.

Note: * Diff = Differential

ADC Drivers: SE* AC In, DC Out

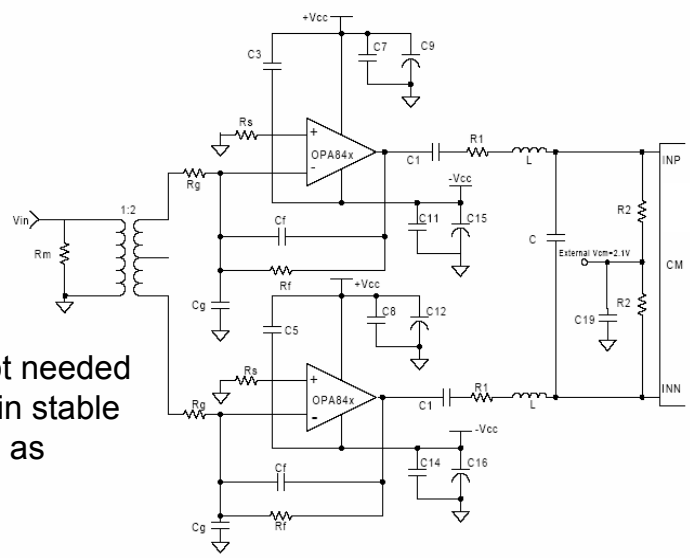


This circuit uses the same scheme as in the preceding circuit shown with the single-ended to differential conversion realized by a transformer.

Using a 1:1.4 or 1:2 transformer can be advantageous as it can reduce the input referred noise as well as provide some amplification.

Note: * SE = Single-Ended

ADC Drivers: AC In, AC Out



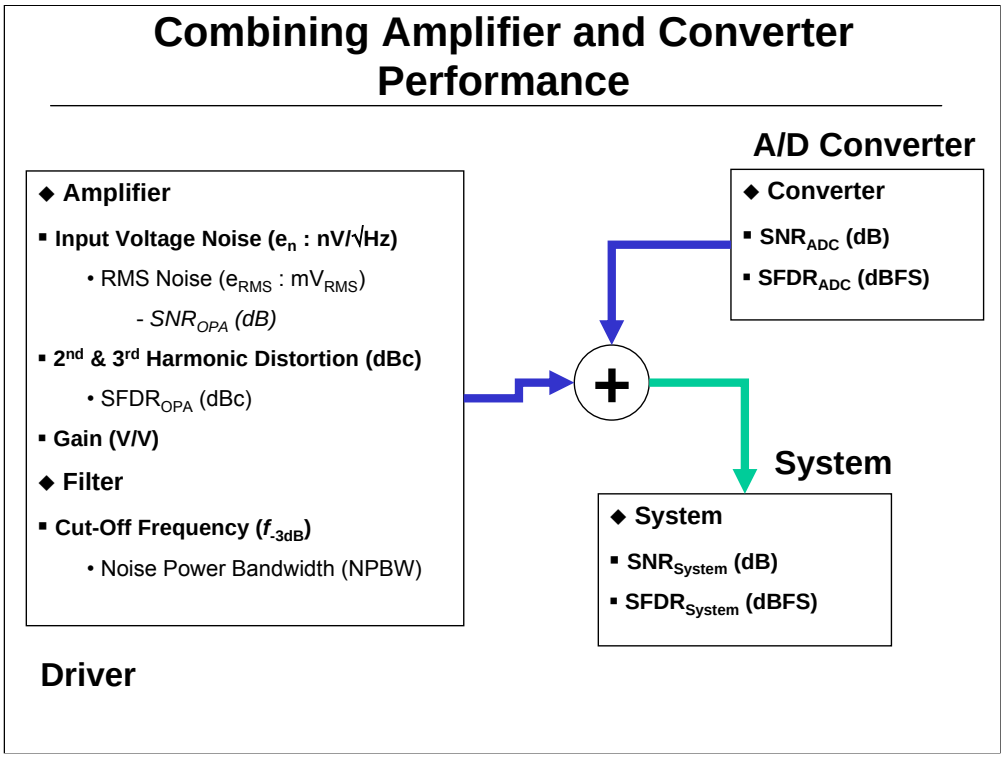
C_f & C_g are not needed for a Unity Gain stable Amplifier such as OPA842

This circuit is based on the previous circuit but this time AC coupling the output of the amplifier with the input of the ADC therefore eliminating all offset contribution of the amplifier to the common-mode of the converter.

The common-mode voltage of the converter is provided through the R_2 resistors.

The external common-mode voltage will need to be larger than the one specified by the converter as the input impedance of the converter reduces as the clock frequency increases.

The filter realized is a first order high-pass filter and a second order low-pass filter realizing a bandpass. As long as the high-pass pole is far from the low-pass pole, both filters can be considered and designed independently.



As shown above, amplifiers and converters are defined in different terms.

For the amplifier noise is usually referred as spot noise in both current and voltage terms. To simplify this discussion, only the input voltage noise is going to be used here, disregarding both current noise and thermal noise. Combining the input voltage with the amplifier gain and the filter cut-off frequency, it is possible to derive a signal to noise ratio (SNR_{OPA}) for the amplifier.

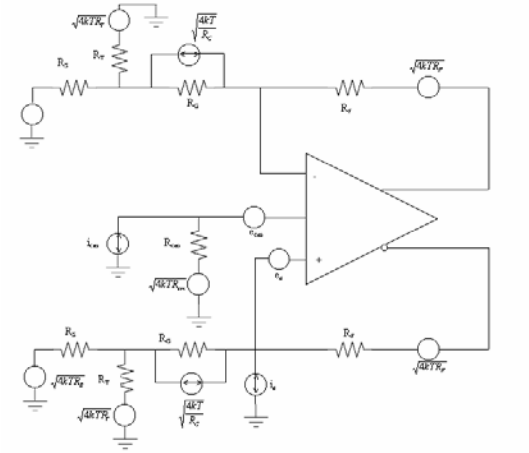
In the same manner, using the 2nd and 3rd harmonic distortion, the dominant distortion terms for an amplifier, it is possible to derive an Spurious Free Dynamic Range ($SFDR_{OPA}$) for the amplifier.

Given these SNR_{OPA} and $SFDR_{OPA}$ numbers, it is possible to combine them with those of the converter and see a predicted combined performance or system performance.

An example will be developed towards the end of this presentation to show how to apply this method on selecting an appropriate amplifier given targeted system and converter performance.

Differential Noise: Diff Amp

$$e_o^2 = (e_n NG)^2 + 2 \times (i_n R_F)^2 + 2 \times 4kTR_F NG$$



$$NG = 1 + \frac{R_F}{R_G + R_S \parallel R_T}$$

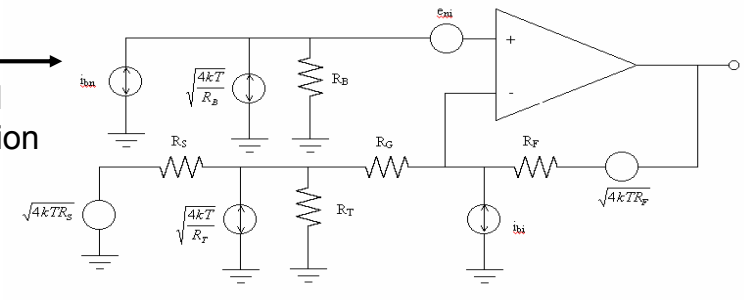
The output noise can be calculated using the above equation for the Fully Differential Amplifier.

The fully differential noise is equivalent to the noise calculation for a single ended amplifier with the 2nd and 3rd term doubled.

The input voltage noise times the noise gain is the dominant term.

Diff. Noise: Diff. Configuration

½ of a differential configuration



$$e_{odiff}^2 = 2 \times [(e_{ni}^2 + (i_{bn} R_B)^2 + 4kTR_B) NG^2 + (i_{bi} R_F)^2 + 4kTR_F NG]$$

For Inverting Operation

$$NG = 1 + \frac{R_F}{R_G + R_S \parallel R_T}$$

- Inverting and non-inverting amplifier in differential configuration have the same noise formula. What varies is the noise gain definition

For the inverting configuration the noise gain is given by $1+R_f/(R_g+R_s||R_t)$. A simple method to translate single-ended noise into differential noise is to multiply the single-ended result by sqrt(2). As the method to calculate noise is explained more thoroughly in the amplifier section.

Calculating RMS Noise (e_{RMS})

$$e_{RMS} = e_O \cdot \sqrt{f_{NPBW}}$$

- Minimize e_{RMS} by:
  - Minimizing e_O
  - Reduce f_{NPBW}

Combining the output noise result from the previous slide allows us to calculate the RMS output noise of the amplifier. The RMS output noise of the amplifier is dependent on two parameters:

•The output spot noise of the amplifier

•The noise power bandwidth

In order to reduce the RMS noise seen by the converter and increase the SNR of the Amplifier/Filter combination, you can either:

•Choose a low noise amplifier to minimize noise contribution

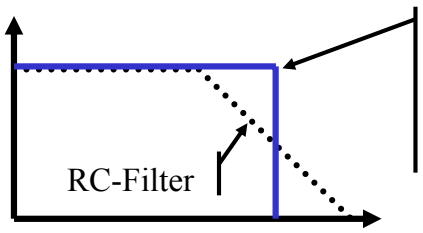
•Reduce the Noise Power Bandwidth (NPBW) seen by the converter. The NPBW should be limited by a post-amplifier filter and not by limiting the bandwidth of the amplifier as limiting the bandwidth of the amplifier will result in increase distortion and/or increasing high frequency noise gain.

Thus the importance of using as sharp a filter as you can. But how can you calculate the noise power bandwidth?

Calculating NPBW for RC Filter 1st Order Filter

$$f_{NPBW} = \frac{\pi}{2} \cdot f_C$$

- f_{NPBW} is the noise bandwidth for the equivalent Noise Power "Brickwall" Filter for an RC filter of cut-off frequency of $f_C = F_{-3dB}$



Equivalent Noise Power "Brickwall" Filter

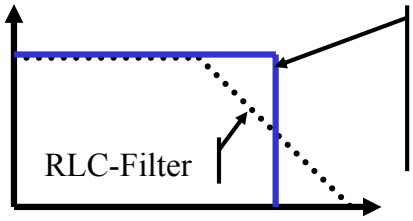
Calculating the NPBW for the RC-Filter corresponds to finding the equivalent Noise Power Brickwall Filter.

For an RC-Filter of cut-off frequency f_C, the equivalent "Brickwall" filter has a bandwidth f_{NPBW} given by the equation above.

Calculating NPBW for RLC Filter 2nd Order Filter

$$f_{NPBW} = Q \cdot \frac{\pi}{2} \cdot f_O$$

- f_{NPBW} is the noise bandwidth for the equivalent Noise Power "Brickwall" Filter for an RLC filter of characteristic frequency of f_O



Equivalent Noise Power "Brickwall" Filter

The same method can be applied to the RLC-filter with the resulting equation above, where Q is the Quality factor of the RLC-filter.

Calculating e_{O_RMS}

$$SNR_{OPA} = 20 \cdot \log\left(\frac{V_{Signal\_RMS}}{e_{O\_RMS}}\right)$$

- SNR can be calculated with the above definition given the RMS signal amplitude and the RMS output noise.

But

- One difference in calculating the SNR for the converter and the amplifier.
  - The SNR is calculated at the input of the converter for the converter, thus using the full input range of the converter as defined in the datasheet.
  - For the Amplifier, the SNR needs to be calculated at the output of the Amplifier/Filter, thus using the full input range of the converter to set the RMS signal.

Finally we can calculate the SNR_{OPA} for the amplifier using the above SNR definition.

One difference in calculating the SNR for the converter and the amplifier.

The SNR is calculated at the input of the converter for the converter, thus using the full input range of the converter as defined in the datasheet.

For the Amplifier, the SNR needs to be calculated at the output of the Amplifier/Filter, thus using the full input range of the converter to set the RMS signal.

All we have left to do now is to combine SNR_{OPA} with SNR_{ADC}

Preserving full converter performance in real world applications

SNR_{ADC}, SNR_{System} & SNR_{OPA}

$$SNR_{System} = -20 \cdot \log \sqrt{\left(10^{\frac{-SNR_{ADC}}{20}}\right)^2 + \left(10^{\frac{-SNR_{Op-Amp}}{20}}\right)^2}$$

- SNR_{System} is the RMS addition of SNR_{ADC} and SNR_{OPA}
- As an example, for a 70dB SNR_{ADC} for the converter, the combined SNR becomes →

SNR_{OPA}	SNR_{System}
65 dB	63.8 dB
70 dB	67 dB
75 dB	68.8 dB
80 dB	69.6 dB
85 dB	69.86 dB
90 dB	69.95 dB

The SNR for the system is the RMS addition of SNR for the converter and the op-amp/filter combination. This implies that in order not to add to much noise in the amplifier stage, both filter and converter ought to have a very low noise. For example, with a 70dB SNR converter, in order to target a system SNR of 69.9dB, the SNR for the amplifier should be better than 85dB.

In amplifier terms, the SNR is the integrated output noise through a defined bandwidth. The bandwidth is limited by either:

•Post amplifier filter

•Amplifier small-signal bandwidth

$SFDR_{ADC}$, $SFDR_{System}$ & $SFDR_{OPA}$

$$SFDR_{System} = -20 \cdot \log\left(10^{\frac{-SFDR_{ADC}}{20}} + 10^{\frac{-SFDR_{Amp}}{20}}\right)$$

- A/D Converter and Amplifier Distortion add linearly.
- As an example, for a 70dBc $SFDR_{ADC}$ for the converter, the combined SFDR becomes →

$SFDR_{OPA}$	$SFDR_{System}$
65 dB	61.1 dB
70 dB	64 dB
75 dB	66.2 dB
80 dB	67.6 dB
85 dB	68.5 dB
90 dB	69.17 dB

The $SFDR_{OPA}$ for an amplifier is given by the worst of the 2nd and 3rd harmonic distortion. Also the unit used for the amplifier is dBc or dB below carrier. For the converter, the $SFDR_{ADC}$ is expressed in dBFS or dB below Full-Scale, as what matters here is the maximum amplitude of the input signal. The method of matching these units is to extract the SFDR from the op-amp datasheet at the maximum input signal of the converter. For example, a 2Vpp full scale input for the converter ends up being 1Vpp for each output as the signal is differential.

Given that, the above equation shows that no matter how good the harmonic distortion of an given amplifier is, it will add in phase with the distortion generated by the converter, reducing the overall system performance.

For example, a 70dBc converter SFDR is going to be reduce the system SFDR by 9dB if the amplifier distortion is 5dB worse than that of the converter (or 65dB). To get only a 1.5dB drop from a 70dBc converter spec., a 15dB margin between the converter and amplifier distortion is required.

At low frequency, it is possible to find an amplifier for all converters. As frequency increases, this becomes harder if not impossible. Also, the amplifier should be operating at some gain in order to reduce the distortion requirement for the previous stages.

We can now have a closer look at different filter solutions.

SFDR and Filter Order

- Things to consider
  - Flatness
    Vs. Cut-Off Frequency (f_{-3dB})

Flatness @ 10MHz	Butterworth RLC Filter	RC Filter
0.1dB	30.5 MHz	65.5 MHz
0.2dB	25.6 MHz	46.1 MHz
0.5dB	20.3 MHz	28.6 MHz

  - 3rd Harmonic attenuation
    - Getting the cut-off frequency as close as possible to the signal fundamental without attenuating it will improve greatly the attenuation of the 3rd harmonic. This is further emphasized by the slope of the filter. A 2nd order filter will provide better attenuation than a first order filter.

Given a fundamental at 10MHz, the 2nd harmonic will be at 20MHz and the 3rd harmonic will be placed at 30MHz. For the following discussion, it will be assumed that the 2nd harmonic is cancelled due to the differential configuration. This leaves the 3rd harmonic as dominant distortion.

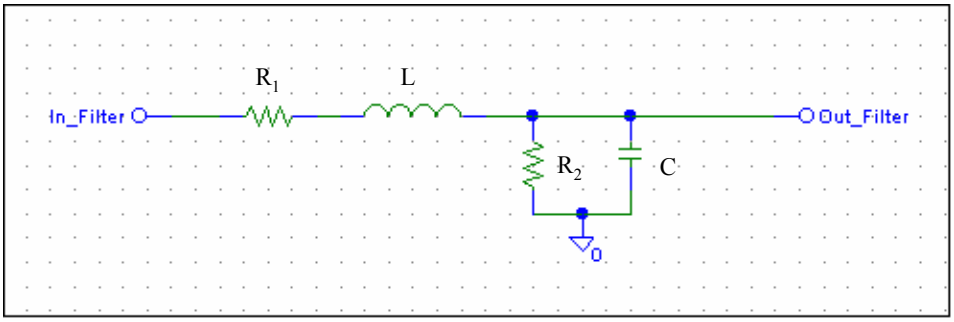
We are trying here to optimally place the RC-filter or RLC-filter Cut-Off Frequency so that it does not attenuate the fundamental frequency (0.2dB flatness is tolerated for the fundamental at 10MHz) but maximize the 3rd harmonic attenuation. The best that can be obtained for the RC filter given the flatness requirement is a cut-off frequency of 46.1MHz. This proves not to be helping at all on 3rd harmonic distortion. The same cut-off frequency placement for a Butterworth RLC-Filter (0.2dB flatness is tolerated for the fundamental at 10MHz) gives 25.6MHz.

The RLC filter proves to be overall better than the RC-filter as far as we are concerned with ADC interfaces due to:

•Lower Cut-Off Frequency (and thus lower NPBW) reducing noise requirement for the driver

•Attenuation on 3rd harmonic provided earlier than RC-Filter helping to lower driver requirement on distortion

RLC Filter Structure



◆Structure for the single-ended RLC filter. This can be converted to a differential filter easily.

◆A full discussion for the selection of filter elements is given in application note SBAA108 “RLC Filter Design for ADC Interface Applications”

As RC-filters are well known, let’s have a more detailed look at the RLC-filter. The structure shown here is composed of two resistors providing a DC attenuation, one inductor and one capacitor.

Adding a second resistor to ground (R_2) provides more flexibility in the design.

RLC Filter Design

The transfer function can be expressed as:

$$\frac{V_O}{V_I} = \frac{\frac{1}{L \cdot C}}{s^2 + s \cdot \left[\frac{1}{\alpha R_T C} + \frac{R_T \cdot (1-\alpha)}{L} \right] + \frac{1}{\alpha LC}}$$

With:

$$\alpha = \frac{R_2}{R_1 + R_2} \qquad \textit{DC Attenuation}$$

$$R_T = R_1 + R_2 \qquad \textit{Total DC impedance}$$

- Simply selecting R_T and α allows a simple solution for L and C to get a desired ω_o and Q for the filter.
- The addition of R_2 creates two possible solutions for L that provides much needed design flexibility in the filter.

RLC Filter Design

$$L = \frac{R_T}{2\omega_0 Q}\left[1 + \sqrt{1-(1-\alpha)(2Q)^2}\right]$$

or

$$L = \frac{R_T}{2\omega_0 Q}\left[1 - \sqrt{1-(1-\alpha)(2Q)^2}\right]$$

$$C = \frac{1}{\alpha L \omega_0^2}$$

The two solutions for L derives from a quadratic equation and thus are distinguished only by the sign before the square root. In turns, those two L solutions provides two C solutions.

Given a 10% maximum DC attenuation or α ~ 0.9.

The two solutions comes out as:

- High Inductance, Low Capacitance
- Low Inductance, High Capacitance

RLC Filter Characteristics

- The benefits/inconvenience for each solutions are:
  - Large L, Small C solution
    - Harder to get High Frequency Inductors
    - May have better SFDR performance.
    - Can implement this filter option just using the converters input parasitic C
    - Can be a higher input impedance to the amplifier.
  - Small L, Large C solution
    - Lower valued inductors available to higher frequencies.
    - Can present low input impedance degrading amplifier distortion - need to scale R_1 up to set a floor to impedance for this design.

RLC Filter Advantages

- Add poles for improved 3rd harmonic suppression and better noise power bandwidth control (over RC filter).
- DC-bias current if V_{IN} sitting at V_{CM} to get Class A current - this can be used to improved 3rd order distortion in the driving amplifier.
- Capacitor on converter's input as often suggested by the converter data sheets.
- The inductor isolates the capacitor from amplifier. This allows R_1 to be selected as needed for the filter independent of stability concerns for the amplifier.
- Higher input impedance filter limits loading over frequency for the amplifier possibly improving distortion.

RLC Attenuation Considerations

- The divider realized with R_1 and R_2 has several effects:
  - It increases the peak-to-peak output voltage at the amplifier.
  - It can be used to set the class-A current of the amplifier if needed.
  - It sets the Q of the filter.
  - It sets the filter input impedance.
  - If used in DC coupled out of the amplifiers, it will result in a smaller common-mode voltage. Check that the converter will not lose performance by operating at lower common-mode voltage.
  - If used in AC coupled out of the amplifiers, as R_2 is used to provide the common-mode voltage, R_2 and the input impedance of the converter will create a divider network for the common-mode signal.

The divider realized with R_1 and R_2 has several effects:

• It increases the peak-to-peak output voltage required of the amplifier.

• It can be used to set the class-A current of the amplifier if needed.

• It sets the Q of the filter.

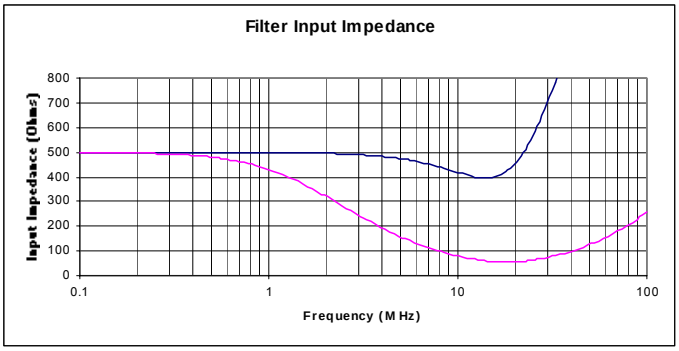
• It sets the filter input impedance.

• If used in DC coupled out of the amplifiers, it will result in a smaller common-mode voltage. Check that the converter will not lose performance by operating at lower common-mode voltage.

• If used in AC coupled out of the amplifier configuration,as R_2 is used to provide the common-mode voltage, R_2 and the input impedance of the converter will create a divider network for the common-mode signal.

All of the above affect in turn the SFDR performance.

RLC Filter - Input Impedances



- The lower curve in the above plot results if the circuit simple uses the same resistor values and we substitute the “low L, high C” values into the solution
- Bench testing with the converters and this filter showed very poor SFDR at 10MHz - this was due to the <100ohm load this filter presents to the amplifier .
- Added constraint on this “low L, high C” solution is to set R1≥200ohm to set a floor to the input impedance.

Each solution has its own sets of difficulties, the Large-L Low-C solution provides much larger input impedance, therefore reducing the amplifier loading and thus improving the amplifier’s distortion. However, it has a couples of limitation:

• Finding good high frequency Large inductor is difficult

• The minimum capacitor is limited by the input capacitance of the converter.

The Low-L Large-C solution presents a very small impedance in the band of interest. This large load at higher frequency does affect the amplifier.

A solution to this dilemma is to increase R_1 to set a floor to the load impedance presented by the filter to the amplifier.

RLC Filter Summary Advantages

- For a given f_{max} desired at the converter input, and using the approach of setting

  $f_{-3dB} = 1.8 * f_{max}$

  we get :

  1. 1.5dB improvement in SNR over the simple RC filter
  2. Drops the minimum SFDR frequency to $0.6 * F_{max}$ (If we are 3rd Harmonic Limited)

  This can be used to extend the useable frequency range for a given amplifier solution.

Other Amplifier SFDR Sensitivities

- Gain
  - A given amplifier generates less harmonics at low gain (for example gain of 1) than it does at higher gain.
  - Some gain is recommended in the ADC driver in order to reduce the distortion requirement from previous stages.
- Supply Voltage
  - For a given amplifier, the larger the supply voltage, the smaller the distortion.

Other Amplifier SFDR Sensitivities

- Single or dual amplifiers as driver
  - Two single amplifiers in differential configuration usually give better distortion than a dual amplifier in differential configuration. This is partially due to the internal layout to accommodate the dual standard pinout.
- Noise is usually independent of the supply voltage
  - Voltage and current noise for an amplifier are mostly independent from the supply voltage.

Setting Amplifier + Filter SNR and SFDR Targets

- For a given ADC, how do we estimate what amplifier + filter solutions will provide a viable interface. Key points to consider -
  1. Going from the passive interface used for data sheet characterization, to an amplifier with filter, there will be a degradation in SNR and SFDR for the combination vs. just the numbers shown in the converter data sheet.
  2. The only reasonable question is how much of a degradation is allowable.
  3. SNR will add for the converter + (amplifier + filter) as an RMS sum
  4. The 3rd harmonic powers present at the output of the filter will add linearly to the 3rd harmonic generated by the converter due to the fundamental power present at the converter input.

Application with ADS826

Burr-Brown Products
from Texas Instruments

ADS823
ADS826

SBAS070B – OCTOBER 1995 – REVISED AUGUST 2002

10-Bit, 60MHz Sampling ANALOG-TO-DIGITAL CONVERTER

FEATURES

- HIGH SNR: 60dB
- HIGH SFDR: 74dBFS
- LOW POWER: 265mW
- INTERNAL/EXTERNAL REFERENCE OPTION
- SINGLE-ENDED OR DIFFERENTIAL ANALOG INPUT
- PROGRAMMABLE INPUT RANGE
- LOW DNL: 0.25LSB
- SINGLE +5V SUPPLY OPERATION
- +3V/+5V LOGIC I/O COMPATIBLE (ADS826)
- POWER DOWN: 20mW
- SSOP-28 PACKAGE

APPLICATIONS

- MEDICAL IMAGING
- COMMUNICATIONS
- CCD IMAGING
- VIDEO DIGITIZING
- TEST EQUIPMENT

The example converter will to be the ADS826 10-Bit 60Msps Analog to Digital Converter.

ADS826 Datasheet Parameters

- Typical Characteristics Curves
  - Spectral performance at sampling rate = 60Msps

	f_{IN} (MHz)	SNR	SFDR	Units
Differential Input 2Vpp	10	59	73	**dB, dBFS**
	20	60.4	72	**dB, dBFS**
Undersampling ($f_{sampling}$ = 56MHz)	41	59.8	78	**dB, dBFS**

$SNR_{ADS823/6typ}$ = 60/59dB

$SFDR_{ADS823/6typ}$ = 74/73dBFS

The maximum input signal frequency is 10MHz. The ADS826 datasheet gives us some SNR and SFDR specifications for the converter: 59dB SNR and 73dB SFDR for full scale input signal.

The worst case SNR for the ADS826 is 56dB.

The full scale input signal is $2V_{pp}$.

Application with ADS826

							Required Amplifier		
							SNR		Typical
Part #	Max Clock	Input Test	Single Enc	Differential	Typ SNR	WC SNR	to meet	Combined	Combined
	MSPS	Condition	Spec. Vp	Spec Vpp	at Fs/2	at Fs/2	WC SNR	SNR if WC	SNR Degra
					(dB)	(dB)	(dB)	(dB)	(dB)
ADS826	60	Single Ended 2Vpp 10MHz	2	2	59	56	65.14	58.50	0.50

- 0.5dB degradation for Worst Case (WC) targeted
- SNR_{OPA} needs to be at least 65.1dB
- SNR_{System} within 1dB of SNR_{ADC_Typ}

Targeting a 0.5dB System SNR degradation from the converter worst case specifications allows to determine the operational amplifier SNR.

For worst case converter SNR_{ADC} of 56dB, the amplifier SNR_{OPA} need to be at least 65.1dB. This gives us for a typical combined SNR_{System} of 58.50dB or a typical system performance 1dB below the typical converter SNR.

Application with ADS826

	RC-Filter	RLC-Filter
f_c (MHz)	f_{NPBW} (MHz)	f_{NPBW} (MHz)
18	28.3	20.0

- Considering the maximum signal frequency of 10MHz, the cut-off frequency for the RLC-filter is chosen to be 18MHz as seen previously in order to maximize SFDR and minimize SNR_{OPA}.

Considering the maximum signal frequency of 10MHz, the cut-off frequency for the RLC-filter is going to be 18MHz as seen previously in order to maximize SFDR and minimize SNR_{OPA}.

Notice the large reduction for going from an RC-Filter to an RLC-Filter.

Application with ADS826

		Target Minimum	
		SNR_{OPA} (dB)	**65.1**
		e_{RMS} (μ V_{RMS})	555.9
Differential Amplifier	RC-Filter	e_O ($nV/\sqrt{Hz}$)	104.5
	RLC-Filter	e_O ($nV/\sqrt{Hz}$)	124.3
Differential Circuit	RC-Filter	e_O ($nV/\sqrt{Hz}$)	73.9
(Each Amplifier)	RLC-Filter	e_O ($nV/\sqrt{Hz}$)	87.91

- The maximum allowable output noise at the output of the amplifier. It is considered here that the noise from the filter is negligible.
- Here the larger the number the better, as it will be easier to find an operational amplifier or a differential amplifier with a larger noise.

The maximum allowable output noise at the output of the amplifier. It is considered here that the noise from the filter is negligible.

Here the larger the number the better, as it will be easier to find an operational amplifier or a differential amplifier with a larger noise and higher input stage gain will be possible.

Here the configuration you have chosen, either differential amplifier or differential circuit is entering into consideration. The allowable output noise for each amplifier in a differential circuit is lower individually than for a differential amplifier, however the maximum noise at the output of the differential circuit is the same as in the circuit using the differential amplifier.

Using all the previous equations, you can go from the amplifier SNR_{OPA} to the RMS noise and then finally to the output spot noise for the desired configuration, or from 65.1dB amplifier SNR_{OPA} to 88nV/√Hz output spot noise for each amplifier for a differential configuration using 2 operational amplifiers.

Application with ADS826

Differential Circuit	RC-Filter	e_O (nV/ √ Hz)	**73.9**
(Each Amplifier)	RLC-Filter	e_O (nV/ √ Hz)	**87.9**
Gain of 2 Input	RC-Filter	e_n (nV/ √ Hz)	37.0
Gain of 2 Input	RLC-Filter	e_n (nV/ √ Hz)	44.0

- Using a first order approximation and considering that the dominant noise source of the amplifier is the voltage noise, the input referred voltage noise can be determined for easy comparison.
- Let suppose that the signal chain going to the ADC is single-ended, and that we want to drive the converter differentially. The circuit is then going to be AC-coupled and does require Single-ended to differential conversion via a transformer. As the total distortion is not to restrictive for preceding stages, a gain of 2 will be used.

Using a first order approximation and considering that the dominant noise source of the amplifier is the voltage noise, the input referred voltage noise can be determined for easy comparison. The targets above are easily met by many amplifiers. This implies that higher gains configuration can be used easily.

We now have to make more choices as far as the final configuration is concerned.

Let suppose that the signal chain going to the ADC is single-ended, and that we want to drive the converter differentially. The circuit is then going to be AC-coupled and does require Single-ended to differential conversion via a transformer. As the total distortion is not to restrictive for preceding stages, a gain of 2 will be used. For each amplifier, the allowed maximum input voltage noise at gain of 2 can be calculated to be 44nV/√Hz.

Application with ADS826

$SFDR_{ADC}$	**73dB**	
$SFDR_{OPA}$	$SFDR_{System}$	Degradation
70	65.4	-7.6
75	67.9	-5.1
80	69.8	-3.2
85	71.1	-1.9
90	71.9	-1.1

- For a system target of 72dBFS and a converter $SFDR_{ADC}$ at 10MHz of 73dBFS, the operational amplifier is required to be better than 90dBc. This would result in slightly more than 1dB decrease in SFDR.
- Target $SFDR_{System}$ = 70dBFS

For a system target of 72dBFS and a converter $SFDR_{ADC}$ at 10MHz of 73dBFS, the operational amplifier is required to be better than 90dBc. This would result in slightly more than 1dB decrease in SFDR.

An overall target $SFDR_{System}$ is chosen to be 70dBFS. This will reduce the driver constraints down to 80dBc at 10MHz.

Amplifier Choice with ADS826

	e_n (nV/√Hz)	$SFDR_{OPA}$ (HD3 @ 6MHz)	I_Q (mA)	V_S (V)	P_D (mW)	Cost ($/1ku)	
OPA690	5.6	76	4.9	+5	49	$ 3.20	2 needed
OPA691	1.7	74	4.5	+5	45	$ 3.10	2 needed
OPA2690	5.6	76	9.8	+5	49	$ 2.45	
OPA2691	1.7	74	9	+5	45	$ 2.45	
OPA2684	3.7	70	2.88	+5	14.4	$ 2.10	
OPA842	2.6	98	20.2	±5	404	$ 3.10	2 needed
THS4150	7.6	72	15.8	±5	158	$ 4.70	SE to Diff
THS4501	7	78	20	+5	100	$ 3.65	SE to Diff

- More requirements:
  - Driver needs to use the same supply as the converter (single supply +5V)
  - Power consumption needs to be considered. There is no need to burn ½W in the driver to meet 58dB SNR and 70dBFS SFDR for the system.
  - One package instead of two to have a more compact layout.
  - Cost (the costs shown above are for 2 devices where needed)

In this case, most amplifier satisfying a input voltage noise of less than 44nV/rtHz will meet the noise criteria if an RLC filter is used. If the RC-Filter is used the input voltage noise goes down to 37nV/rtHz.

The table above is showing a selection of amplifier and the input voltage noise associated. Since the requirement for SNR and SFDR are not to restrictive, more requirements need to be expressed, these are:

• Driver needs to use the same supply as the converter (single supply +5V)

• Power consumption needs to be considered. There is no need to burn ½W in the driver to meet 58dB SNR and 70dBFS SFDR for the system.

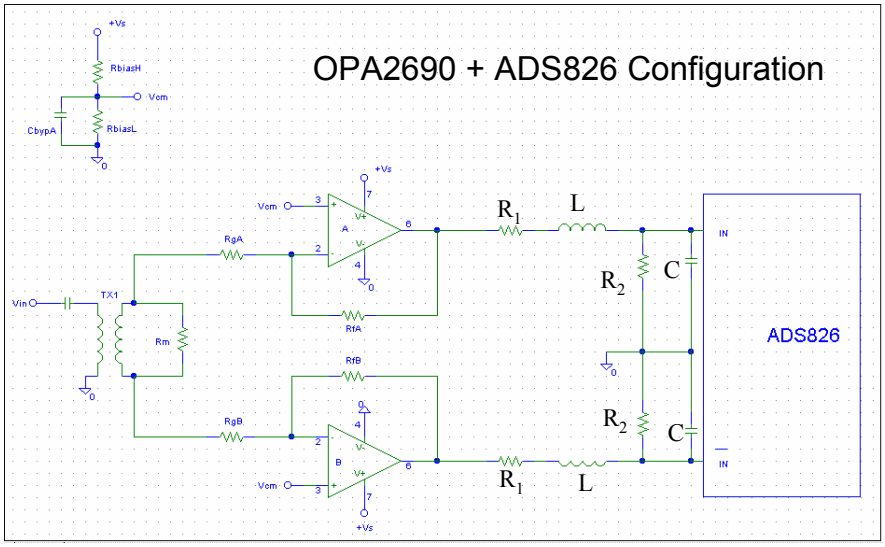
• One package instead of two to have a more compact layout.

• Cost

Since we want AC-coupled on the input, the choice is not limited to differential amplifiers, but extend to single and dual operational amplifiers.

As the circuit is differential, 2nd harmonic distortions is considered small enough not to be an issue, only 3rd harmonic distortion are considered initially at the worst frequency. Here it is 6MHz as the filter is placed at 18MHz.

Example Design Using OPA2690



The OPA2690 is set at a gain of -2 in an inverting configuration. The filter chosen is an RLC-Filter set at 18MHz. The common-Mode voltage required by the converter is generated by a resistor divider on the non-inverting input of the OPA2690. The Single-Ended to Differential conversion is done with a transformer.

Test values are:

Rf = 1 kohm

Rg = 500 ohm

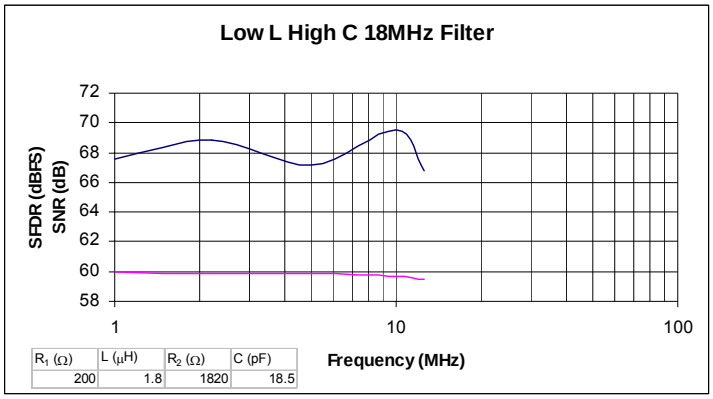
R_1 = 200 ohm

L = 1.8µH

R_2 = 1820 ohm

C = 18.5pF

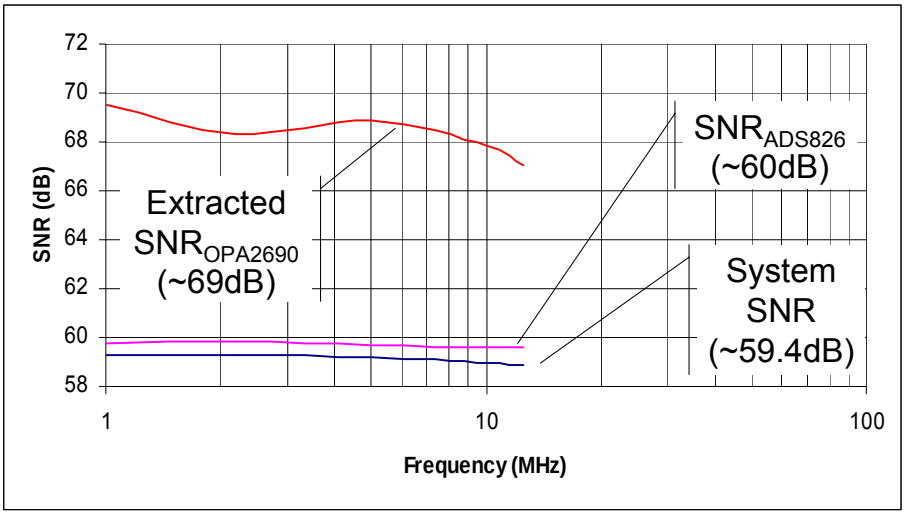
OPA2690 Driving ADS826 Results



- Very good SNR retention - apparently have an SNR out of filter well below the converter.
- Minimum SFDR at 6Mhz as predicted. Combined performance consistent with the Op Amp data.

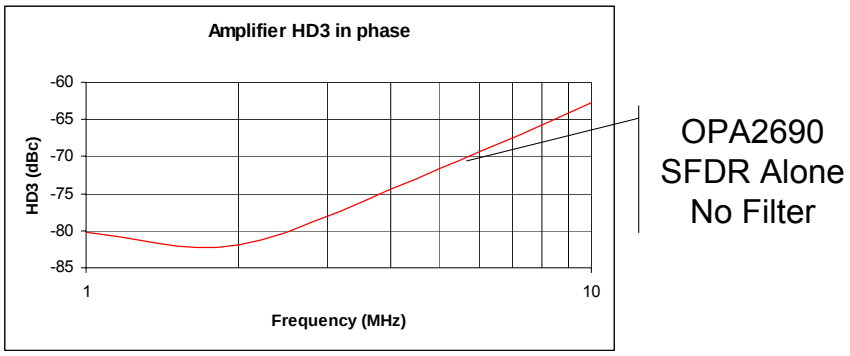
Please note that other solutions can improve SFDR further. This particular solution is low power.

System Degradation Due to Op-Amp



Extracting the SNR_{OPA} for the amplifier over frequency.

System Degradation Due to Op-Amp



Op amp distortion consistent with combined results. The -78dB at 3Mhz should give a combined number of 69.5 from calculation and we get about 68.

The 6MHz number of -69 is reduced to -72 by the filter to give 66.5dB combined - we get 67. From 6 to 10Mhz, the OPA2690 increases 6dB while the filter roll-off increases 9dB - giving the improved system SFDR >6MHz

Op amp distortion consistent with combined results. The -78dB at 3Mhz should give a combined number of 69.5 from calculation and we get about 68.

The 6MHz number of -69 is reduced to -72 by the filter, at 18 MHz, to give 66.5dB combined - we get 67. From 6 to 10Mhz, the OPA2690 distortion increases 6dB while the filter roll-off increases 9dB - giving the improved system
SFDR >6MHz

Driving Analog and Digital Signals Over Transmission Lines

Driving Transmission Lines

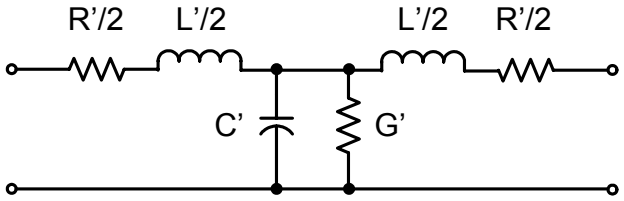
- Any interconnection can be considered a transmission line which has a characteristic impedance even if this impedance is not controlled!!!
  - Long PCB Traces
  - Telephone / Modem / xDSL systems
  - Video systems
  - Audio systems
  - RF systems
  - Test and measurement systems
  - Distribution networks

Most electrical circuits require some means to connect to other circuits. Any interconnection to another circuit is a transmission line. A transmission line is any pair of conductors which are used to move electromagnetic energy from one place to another.

AC power lines are transmission lines. Twisted pair wires are transmission lines. We see transmission lines in audio, video, RF, etc, etc, etc.

Common to all of these systems is the fact that there is some sort of characteristic impedance involved. This impedance is best kept well controlled and can cause major headaches if not controlled - especially in high speed systems.

Transmission Line Model



L' = Characteristic Inductance per Unit Length (nH/cm)

C' = Characteristic Capacitance per Unit Length (pF/cm)

R' = Characteristic Resistance per Unit Length (Ω/cm)

G' = Characteristic Conductance per Unit Length (S/cm)

Characteristic Impedance $Z_0 = \sqrt{\frac{j\omega L' + R'}{j\omega C' + G'}}$

The equivalent circuit of a transmission line consists of an inductance L' - representing the inductance of the transmission line -, a resistor R' - representing the ohmic resistance of the line, a capacitance C' - representing the capacitance of the line - and the conductance G' representing the losses in the capacitance of the line. All these values are length dependent and are therefore specified in unit/length, e.g.: nH/cm, pF/cm, Ω/cm, and S/cm. By setting up a set of differential equations, one can calculate the impedance of a transmission line:

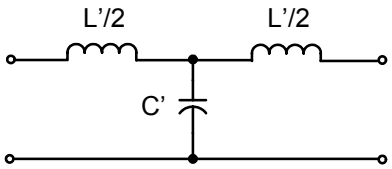
In practice this equation is difficult to handle. First the line impedance results in a complex number which makes the required calculations time consuming. Second the line impedance is frequency dependent. This fact becomes uncomfortable especially in digital circuits, where one has to consider many frequencies simultaneously.

Summary: Inherent inductances and capacitances dominate the behavior of transmission lines as soon as their physical dimensions cannot be neglected in comparison to the wavelength.

The characteristic impedance describes the ratio of voltage to current for a traveling wave.

Loss-Free Transmission Line

At high frequencies the transmission line losses on printed circuit boards in most systems can be neglected.



With R' << jωL' and G' << jωC':

Line impedance $Z_0 = \sqrt{\frac{L'}{C'}}$

Propagation time $\tau = \sqrt{L' \times C'}$

Cut-off-frequency $f_0 = \frac{1}{2\pi\sqrt{L' \times C'}}$

Loss due to R':

$$Attenuation\ at\ x\ inches = e^{-\left[\frac{R \cdot x}{2\sqrt{L/C}}\right]}$$

$$Loss\ per\ inch\ (dB) = 4.34\left[\frac{R}{\sqrt{L/C}}\right]$$

Where: L = Transmission Line Inductance (H/in.)
C = Transmission Line Capacitance (F/in.)
R = Transmission Line Resistance (W/in.)
x = Transmission Line Length (in.)

In digital circuits low frequencies are not generally of concern. At higher frequencies (above some 10 MHz) the impedance of the inductance jωL' becomes large compared to the resistance R' of the wire. The admittance jωC' is also much greater than the corresponding conductance G'. Under this assumption R' and G' can be neglected. The impedance of the transmission line can now be calculated by the simple formula

The impedance is now a real number which can be handled like an ohmic resistor. A further advantage is Z_o is now independent of the frequency.

An important parameter in data transmission circuits is the propagation time t_p of the signal on a transmission line. This time is also determined by the parameters of the line:

On typical cables used in transmission circuits (coaxial cable, twisted pair cable) the propagation time becomes t_p = 5 ns/m. This reflects a propagation speed v = 200 000 km/s (about 60 % of the speed of light).

Typical Line Impedances

	L'(nH/cm)	C'(pF/cm)	Z (Ω)	τ (ns/m)
Single Wire (far away from GND)	20	0.06	600	≈ 4
Space	μ_0	ε_0	370	3.3
Twisted pair cable	5 - 10	0.5 - 1	80 - 120	5
Flat cable	5 - 10	0.5 - 1	80 - 120	5
Wire on PC board	5 - 10	0.5 - 1.5	70 - 100	≈ 5
Coax cable	2.5	1.0	50	5
Bus line	5 - 10	10 - 30	20 - 40	10 - 20

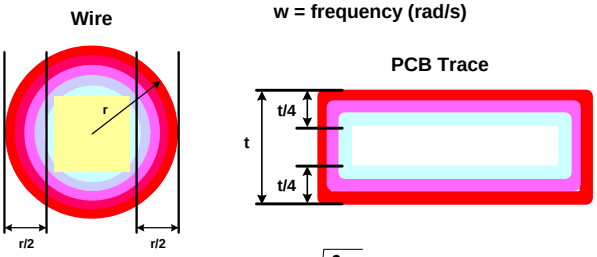
The table shows typical Inductive and Capacitive Layers (L', C') of various signal traces. The last two columns display the corresponding impedance and propagation delay time along the wire calculated from L' and C'.

Common signal traces show an impedance in the range of 20-Ω to 120-Ω and propagation delay times of 4ns/m to 20ns/m.

Skin Effect and Losses

Skin Effect accounts for high frequency current flow at the edge of a conductor – causing an increase in resistance.

Where: r = Volume Resistivity
m = magnetic permeability of the conductor
w = frequency (rad/s)



$$Skin\ Depth = \sqrt{\frac{2\rho}{\omega\mu}}$$

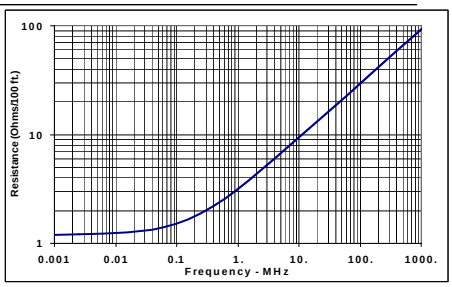
Critical Depth is when Skin Depth =
Radius / 2 (Round Conductor) –OR- Thickness / 2 (PCB Trace)

The characteristic impedance of a transmission line will remain fairly constant at high frequencies. But, one of the drawbacks of high frequencies is the skin effect. At low frequencies, the current flows throughout the wire evenly. But, at high frequencies, the current flows only near the surface of the wire. Because the current only flows through the outer edges of the wire, the AC resistance increases proportionally to the square root of the frequency.

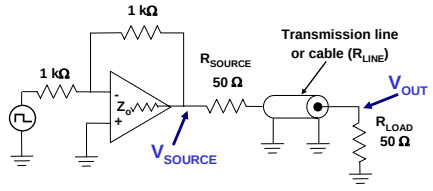
Skin Effect and Losses

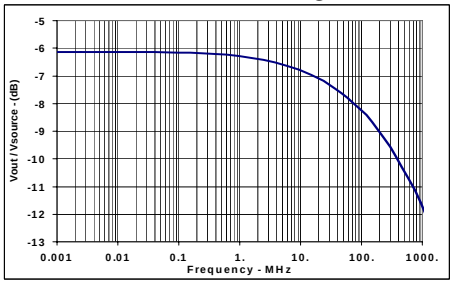
$$R_{LINE}(\Omega) = x \cdot \sqrt{R_{DC}^{\,2} + R_{SE}^{\,2}} = x \cdot \sqrt{R_{DC}^{\,2} + \left(\frac{2.61 \cdot 10^{-7} \sqrt{f \cdot p_r}}{Surface\ Area}\right)^2}$$

Where: R_{SE} = Resistance of Wire in Skin Effect Region (W/in.)
R_{DC} = Resistance of Wire at DC (W/in.)
x = length of conductor (inches)
f = frequency (Hz)
p_r = Relative Resistivity (Relative to Copper = 1)
Surface Area = p D for Round Conductor
= 2 x length + 2 x thickness for Trace



RG-58/U Coax Loss Effects @ 100ft.





$$\frac{V_{OUT}}{V_{SOURCE}} = \frac{R_{LOAD}}{R_{LOAD} + R_{SOURCE}}$$

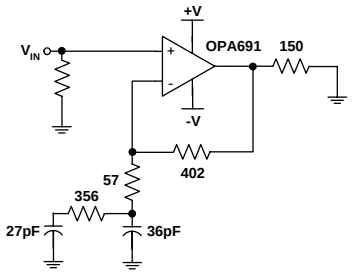
For comparison's sake, the frequency at which the skin effect starts to be noticeable is 21kHZ for RG-58/U, 65kHz for AWG24 wire, and 14 MHz for 0.010 inch PCB trace width with 1 ounce copper weight. Although skin effect increases the AC resistance of a transmission line, the characteristic impedance will still remain constant at high frequencies. This is due to the effects of the inductance and capacitance of a transmission line out-weighing the effects of the AC resistance.

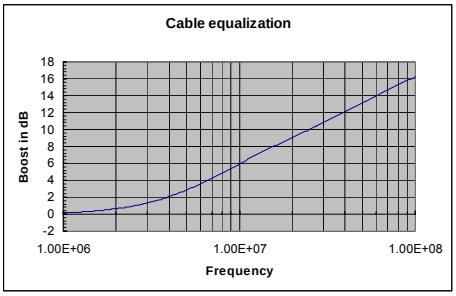
Skin Effect is important because it reduces the signal amplitude at the load end of the line. This reduction is a function of the square-root of the frequency and thus cannot be compensated very easily.

The best way to reduce skin effect is to simply shorten the length of wire used. If you cut the length of a wire by one-half, the frequency response goes up by a factor of four. You typically see the skin effect on sharp rising pulses over a long transmission line. The edge rate will have a tendency to slow down, especially near the corners of the pulse.

Equalizing Signals to Account for Skin Effect

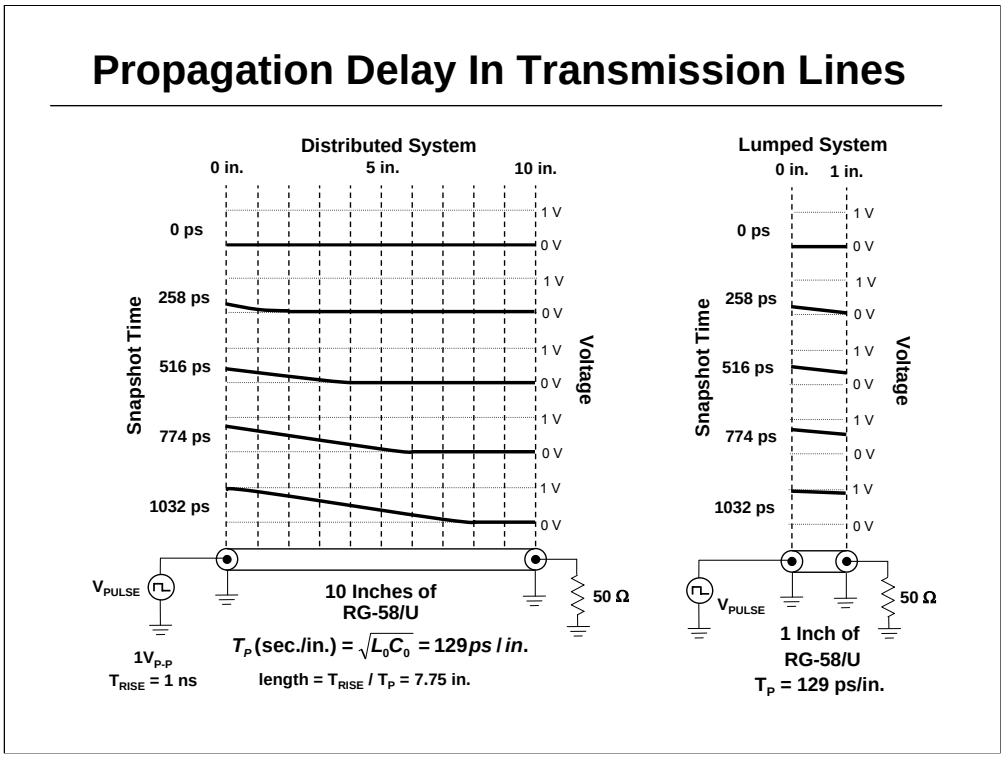
- Matching the Roll-Off Reduces the Resistive Loss and Attenuation for Long Lengths of Cables
- Equalized for FIXED Cable Lengths:
  - Too much Gain at High Frequencies for Shorter Cables
  - Not Enough Gain at High Frequency for Longer Cables





On the transmit and/or receive side of the cable, adding high-frequency gain can help compensate for skin effect losses. But due to the loss being a function of the square-root of the frequency, a simple R-C network will not suffice. Instead adding multiple R-C zeroes spread throughout the frequency spectrum are the only way to account for such a loss.

One must pay attention to the applied voltage and the frequency dependent gain or else the amplifier can go into clipping. The problem with this is it only works for a specific cable length. If the cable length becomes shorter, then there will be too much high-frequency gain. If the cable becomes longer, then there will not be enough high frequency gain.



The propagation delay (Tp) for RG-58/U is about 129 ps./in., FR4 PCB inner trace is about 180 ps./in., and air has a delay of 85 ps./in. This is an important aspect when it comes to pulse/digital signals. The effective length of a pulse edge in a transmission line as it propagates through the line is:

$$E_{LENGTH} = \frac{T_R}{T_P}$$

Where : E_{LENGTH} = effective length of rising edge (in.)

T_R = rise time of pulse (ps)

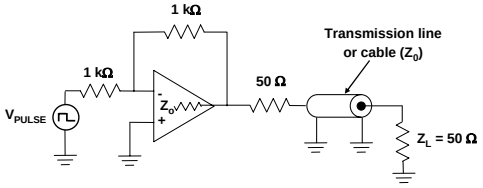
T_P = Propagation Delay (ps/in)

The importance of this arises depending on how far the receiving circuit is from the source signal. If the receiving circuit is less than one-fourth (some engineers use one-sixth) the effective length of the rising edge (l), then the system is termed a lumped system. Due to the short distances within a lumped system, the voltage at every point within the transmission line is fairly uniform. Reflections occur within the rising and falling edges and the system is typically well behaved.

If the transmission line is greater than one-fourth the effective length, the transmission line will have different voltages at different point throughout it's length. This is defined as a distributed system. When this happens, reflections will occur outside the rising and falling edges if the line is not terminated properly due to the voltage distribution within the line itself. If you do not terminate a distributed system, there will be an amplitude doubling at the receiving end of the line. Due to the reflected wave, there will then be a negative reflection at the source driver. This keeps re-occurring until a steady state value is reached, much in the same way a high Q circuit "rings".

VSWR: Voltage Standing Wave Ratio
(Reflection Coefficient)

- Who cares? Mainly applications when driving transmission lines, cables, PCB traces, twisted pair, etc.



Amount of the signal reflected:

Where : V_R = Percentage of incoming voltage signal reflected
Γ_L = Reflection coefficient
Z_L= Load Impedance
Z_0 = Line Impedance

$$V_R = 100 \bullet \Gamma_L = \frac{Z_L - Z_0}{Z_L + Z_0}$$

VSWR is the ratio of the maximum voltages along the line to the minimum voltage along the line:

$$VSWR = \frac{V_{MAX}}{V_{MIN}} = \frac{1+|\Gamma_L|}{1-|\Gamma_L|}$$

The amount of the signal reflected is given by:

$$V_R = 100 * \Gamma_L = \frac{Z_L - Z_0}{Z_L + Z_0}$$

Where : V_R = Percentage of incoming voltage signal reflected

Γ_L = Reflection coefficient

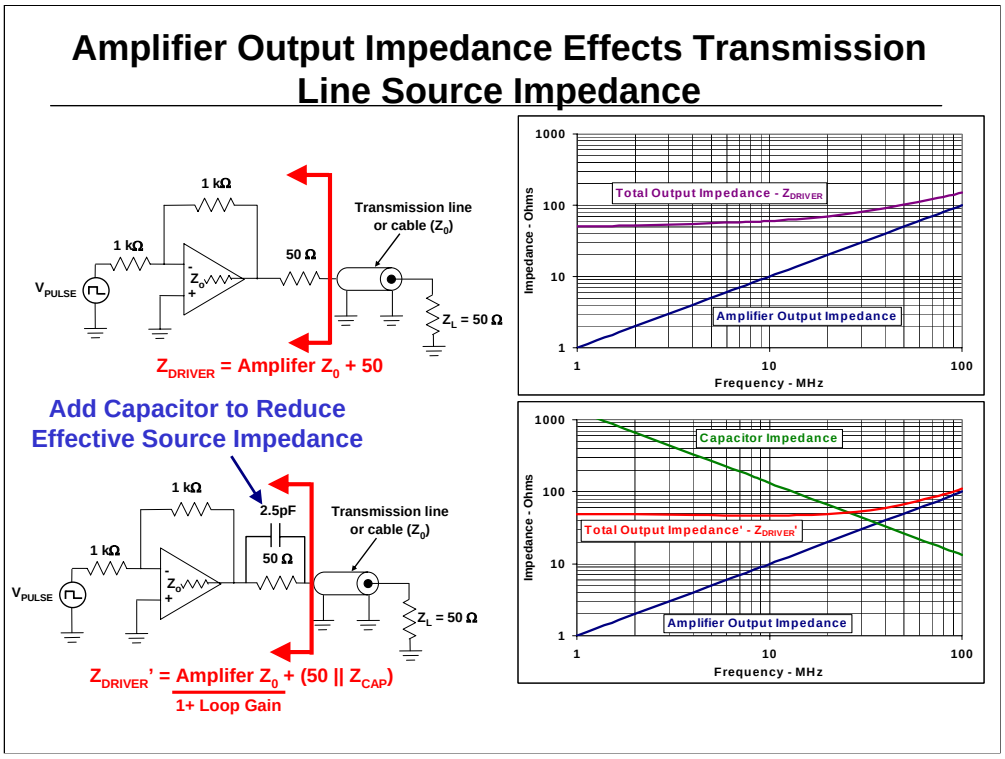
Z_L= Load Impedance

Z_0 = Line Impedance

The terms within the equation may be swapped, depending on where the wave is traveling from. The form shown above shows a wave traveling from a line driver to a load termination. To see what the reflected wave from the load to the line driver will do, just redefine Z_L as the impedance at the line driver end of the transmission line. The reflection coefficient is also used when defining the voltage standing wave ratio (VSWR). The VSWR is the ratio of the maximum voltages along the line to the minimum voltage along the line. The formula is:

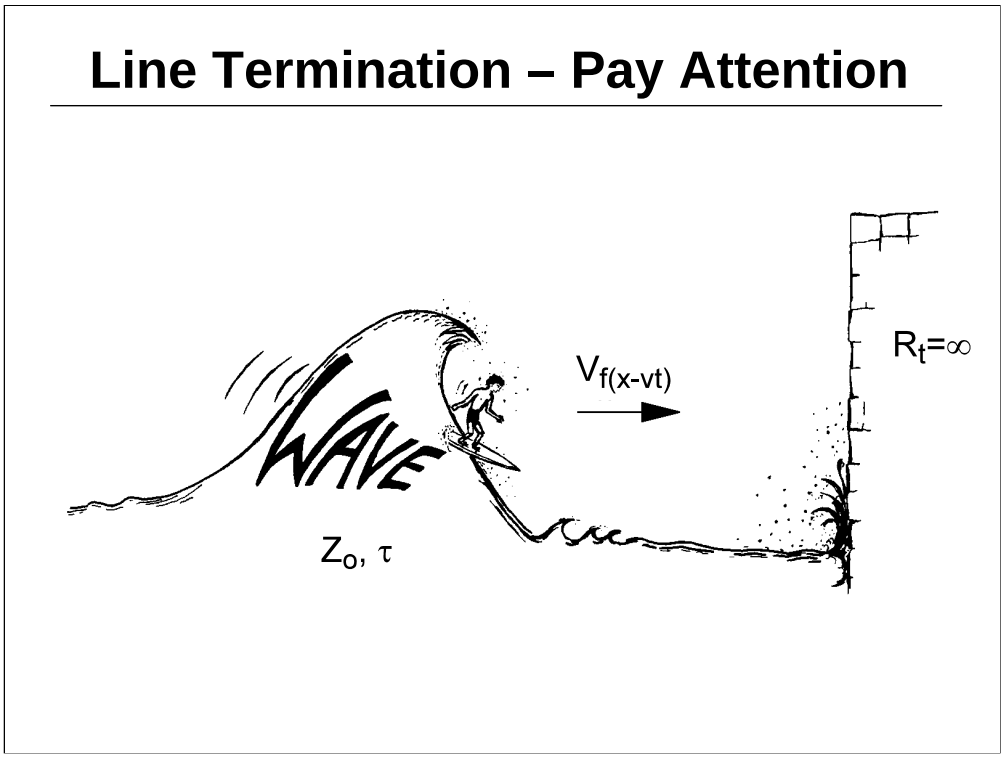
$$VSWR = \frac{V_{MAX}}{V_{MIN}} = \frac{1+|\Gamma_L|}{1-|\Gamma_L|}$$

A VSWR of 1, the optimal case, shows that the line is perfectly matched and all of the power is delivered to the load without any reflections. Remember that any driver has an output impedance that varies over frequency that may cause aberrations in the signals.



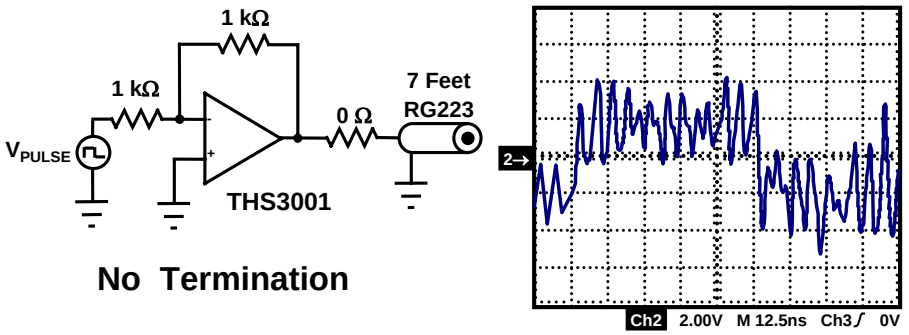
Every Amplifier has an output impedance. The internal impedance is reduced by the amplifier's excess loop gain and is ideally 0-ohms at DC. But as the frequency increases, the loop gain decreases and the output impedance starts to increase at approximately the same rate. At very high frequencies, the amplifier's output impedance may become a problem.

One way to minimize this issue is to simply add a capacitor in parallel with the series source resistance as shown. This effectively reduces the source impedance at a rate similar to the amplifier's own output impedance rate. Eventually the amplifier's source impedance becomes too high and there is no more matching. But the amplifier is most likely beyond it's useable range at this point anyways.



In ANY signal transmission system the designer has to take care of line reflections caused by improperly terminated lines. These line reflections may lead to an additional signal distortion which cause incorrect amplitudes at the line end (receiver input). This may result in a system that simply does NOT function properly. This is true for both digital and analog systems.

Distributed System with No Termination



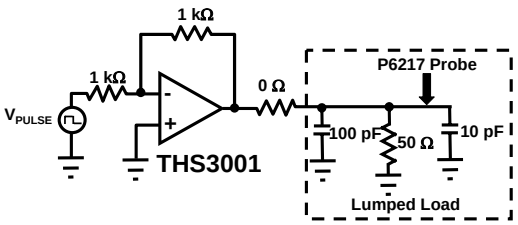
No Termination

Output Very Unstable

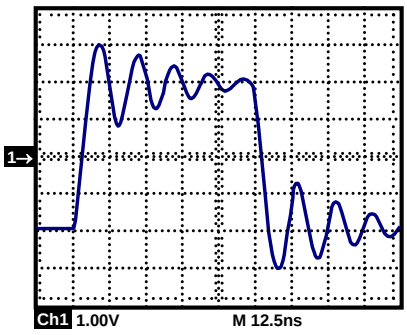
To stress the importance of transmission line terminations, let's look at a few cases of termination using a THS3001 current feedback amplifier with extremely high slew rate capabilities. The reactive impedance of the non-terminated cable in a distributed system causes an unstable system. This is due primarily to the distributed capacitance of the cable which in this case is about 30pF/foot. Thus, the amplifier "sees" about 210pF directly on it's output, resulting in a unstable and useless system.

Lumped System Without Source Termination

- Without source termination, the destabilizing effects of the lumped capacitance can be seen.



No Source Termination



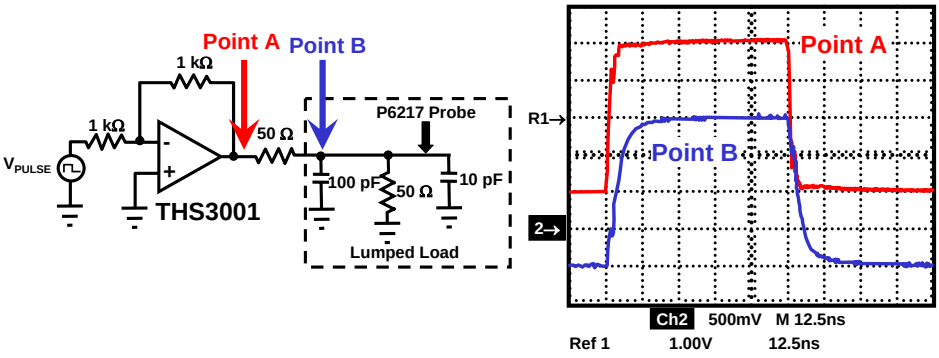
Output Rings

The circuit above shows a lumped capacitance at the output of a THS3001 high speed amplifier. A lumped capacitance is one way of showing the effects of an unterminated transmission line. Remember that a system will behave as a lumped system if the wavelength of the signal is much greater than the length of the cable.

The measurement was done with a Tektronix P6217 4GHz FET probe and a TDS794D 2GHz oscilloscope. The results of this test are obvious. The line driver is very unstable and the system has a relatively high Q. The reason for this oscillation is that the line driver sees the lumped capacitance directly on it's output. Combined with the line driver's output impedance, this causes some phase shift to occur. This phase shift causes the phase margin of the line driver to decrease yielding an unstable amplifier. This is definitely not what the receiving circuitry at the end of a line wants to see.

Lumped System with Double Termination

- Doubly Terminating lines removes the effects of lumped capacitance on the driver



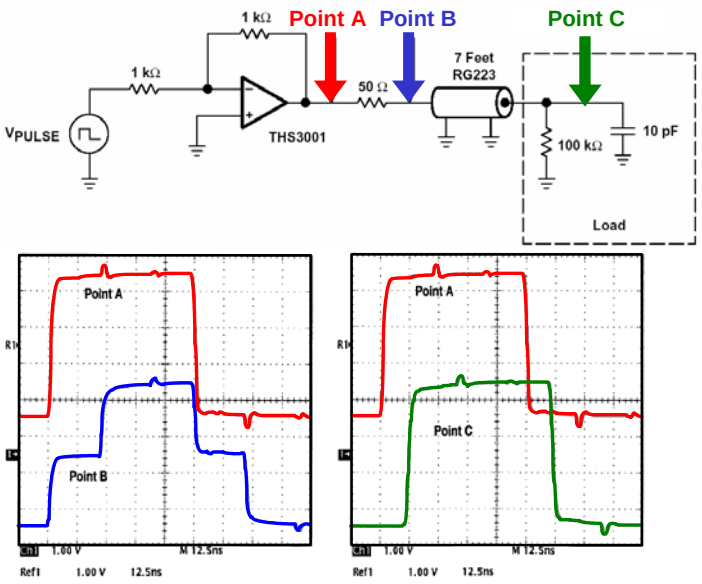
Double Termination

By isolating the capacitance in the lumped system with 50O resistor, the system becomes stable. But, there are two main drawbacks of doing this. The first drawback is the voltage division caused by the source resistor and the load resistor causes the output waveform amplitude to be reduced by a factor of two.

The second drawback is the source resistance and the load capacitance causes a R-C time constant to occur. The edges of the load side waveform is slowed down due to the limited current being supplied through the source resistor. There may be some techniques to reduce this issue, but are beyond the scope of this presentation.

The line driver should be considered carefully when you do this. This is because a standard voltage feedback amplifier's bandwidth will be cut in half. But, a current feedback amplifier, such as the THS3001 shown, will not have a large reduction in bandwidth due to the internal architecture of the amplifier. This can be a big advantage when setting up a transmission line system.

Distributed System with Source Termination



The next circuit is an improvement over no termination. By placing a source resistance between the line driver and the transmission line we have created a source terminated system. The effect of the source resistance is two-fold. The first is that the source resistance helps to isolate reactive impedances in the transmission line from the driver's output. Thus keeping the line driver's phase margin in tact.

The second thing the source resistance does is to absorb the reflections coming back from the load. The load is high impedance and using the reflection coefficient (Γ_L) formula previously, we can see that a voltage reflection coming back from the load will be about +1. Without the source resistance, this reflected wave would run directly into the line driver. This would have created a highly unstable system resulting in oscillations.

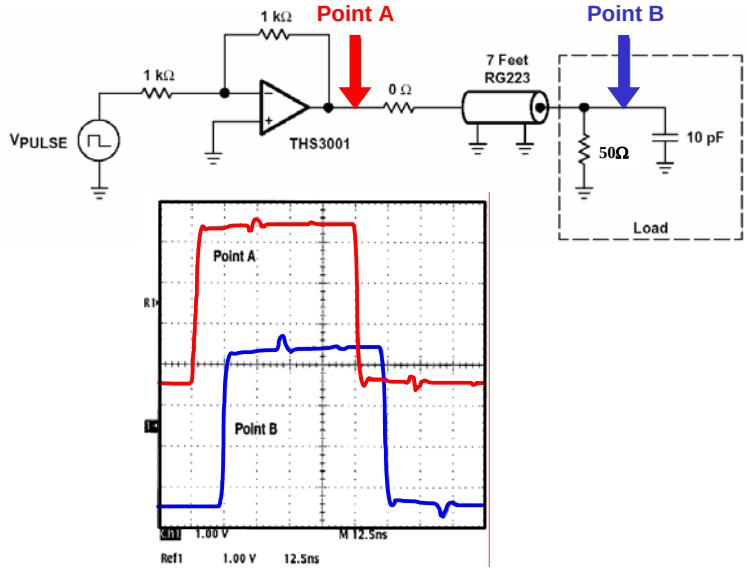
The first graph usually brings the question of why does it look like a staircase response? Initially the pulse does not know what the terminating load is due to the propagation delay of the transmission line (T_P). The only thing the wave will see is the characteristic impedance (Z_0) of the transmission line. This initially follows the classic voltage divider equation where the source resistance is equal to the line impedance. Thus, the voltage after the source resistor is one-half the line driver output voltage (see Point B on the plot).

The pulse will then travel down the 7 feet of RG-223 coaxial cable to the load. At which time, approximately 11 ns later (129 ps/in × 84 in.), the load causes an equal reflection to be sent back to the line driver. This is again due to the reflection coefficient (Γ_L) discussed previously. Because this reflection is equal to the initial pulse amplitude, the voltage at the load end will be doubled (see Point C in the plot) and remain at this amplitude unless other reflections occur.

The wave pulse will then reflect back to the line driver side of the transmission line. Another 11 ns later, the reflected wave hits the source resistor. This equal and in phase wave pulse doubles the amplitude (see Point B Plot). In systems like this, it is not uncommon for another reflection to occur back to the load-end of the line. The reason for another reflection to occur is that there is always some output impedance on the line driver. This reflection can be seen by the small ”blip” occurring every 22 ns (2 * 129ps/in. * 84in.) on all of the waveform plots. This is the round trip time for the wave to go from the one end of the transmission line, hit the end of the line, and then reflect back to the beginning. The steady state value on the line should be equal to approximately the output voltage of the line driver due to the high impedance at the load.

This is an improvement over no termination, but the power transfer efficiency is almost non-existent. Not to mention the fact that reflections do occur within this system.

Distributed System with End Termination

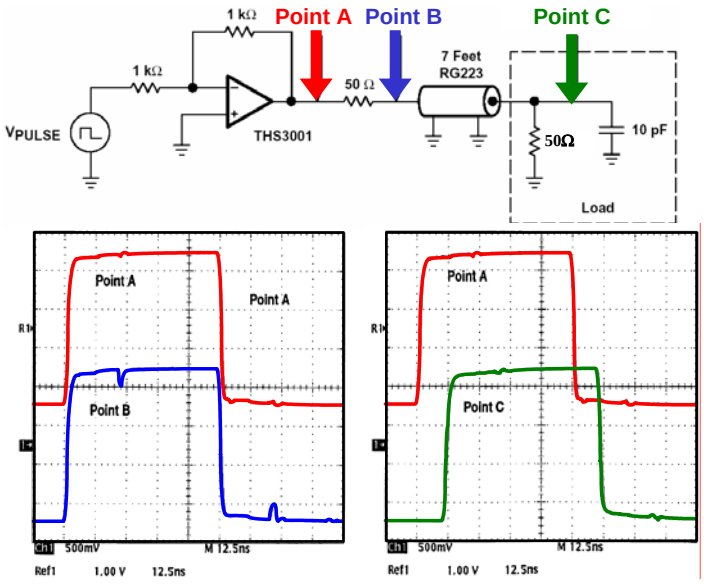


The next configuration in line terminations is the load terminated line. This can be seen in the circuit shown where the load resistance is equal to the characteristic line impedance. Just like the source termination case, the initial load seen by the line driver will be the characteristic impedance of the transmission line (Z_0). After propagating down the transmission line for about 11 ns, the wave pulse will hit the load resistance.

If the load resistance was strictly equal to the line impedance (50 Ω), there will not be any wave reflections traveling back to the driver. The problem occurs when there is also capacitance at the load end. Even if the load end does not have a physical capacitor, there is usually some form of stray capacitance. Because of this capacitance, some portion of the wave pulse will be reflected back to the line driver. This can be seen initially on the point A plot. This ”blip” occurs about 22 ns after the initial pulse occurs. This is the same type of reflection ”blip” seen in the source terminated system.

If this reflection is too severe, caused by a high capacitance at the load or a non-matched load resistor, the line driver may go into an oscillation because there is not a source termination resistor to absorb this reflected energy. This ”blip” also occurs on the load side after it propagates back from the line driver. If you look very carefully, this blip occurs every 22 ns on both the line driver output and the load termination side. Although it’s amplitude will be reduced as it propagates throughout the transmission line. Again, this is explained by the reflection coefficient (Γ_L). Eventually though, this ”blip” will settle down to the final value if the waveform remained at a constant voltage.

Distributed System with Double Termination



This brings us to probably the most common and desirable form of termination, the double terminated line. The circuit above shows that a source and a load resistance equal to the characteristic line impedance is placed into the circuit. The effect that this has is that all reflections should be absorbed by both terminators.

Even with some capacitance at the load end, the reflected wave is absorbed by the source resistor. The effect of this is that the line driver will remain very stable due to the purely resistive load presented to the output of the line driver maintaining it's phase margin for stability. By examining the point C plot, you can see that the "blip" caused by the 10 pf capacitor is almost eliminated at the load end. The output of the line driver is reproduced almost exactly at the load end, just as one would want the source signal to get passed onto the next system. The power transfer is also extremely good with this configuration. The VSWR with this setup, minus the 10 pf capacitor, will be a perfect 1.

As with the Lumped System previously described, one drawback to this approach is that the voltage at the load end is one-half the output of the line driver. Also there may be a slight reduction in rise time due to the RC load effects.

Driving Transmission Lines Summary

TERMINATION	ADVANTAGES	DISADVANTAGES
NONE	- Compact - Minimize Parts - Output Voltage is Retained	- Reflections Occur - Capacitive Loading - Very Unstable
SOURCE	- Isolates Line Driver From the Load - Absorbs Load Reflections - Output Voltage Is Retained	- Load Must Be High Impedance - Stray Capacitance Is Likely - "Blips" Are Highly Probable
LOAD	- Load Absorbs Reflections - Stray Capacitance Is Minimized (Due to Low Impedance) - Output Voltage Is Retained	- Low Impedance Load Presented To Driver - Driver Impedance Is Critical To Reflections
DOUBLE	- All Reflections Are Absorbed - Load Voltage Characteristics Look Identical To Source - Line Driver "Sees" Resistive Load (i.e. Very Stable)	- Voltage at Load End Is Reduced By Two - May Reduce Line Driver Bandwidth To Compensate - Requires 2 Resistors