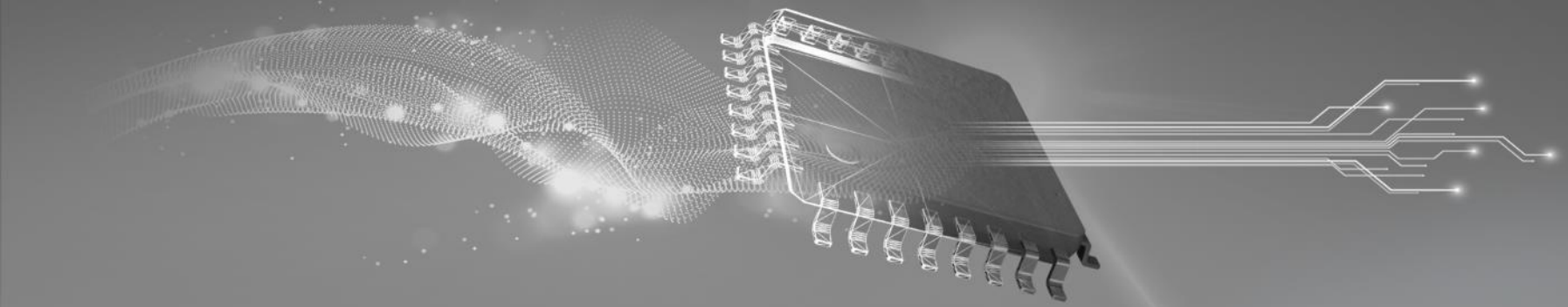
TI TECH DAYS



Design Challenges for Automotive USB Type C® in CarPlay Application

Michael Tan

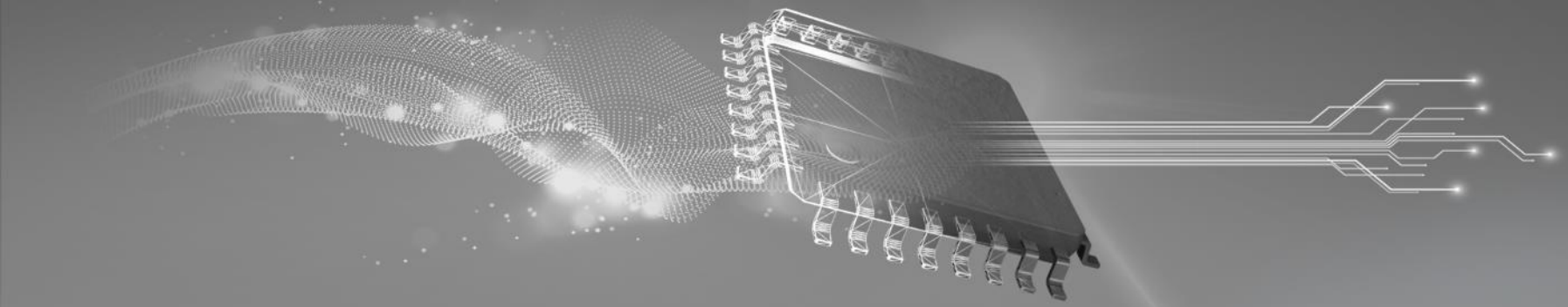
TI-APP-PSIL

Texas Instruments

Agenda

- **What is CarPlay/MFi and what is USB's role in the application?**
- **How to pass MFi VBUS requirement with TPS2583x/4x**
  - TPS2583X/4x introduction
  - MFi VBUS spec and test set up
  - Cable compensation introduction
  - Cable compensation design to pass MFi
- **How to pass MFi OCP requirement with TPS2583x/4x**
  - MFi OCP spec and test set up
  - How to pass MFi OCP with TPS2583x/4x
- **How to improve eye diagram performance with TPS2583x/4x**
  - Eye diagram introduction and challenges in long cables
  - How to improve eye diagram performance with TPS2583x/4x
- **How to improve EMI with TPS2583x/4x**
- **Q&A**

TI TECH DAYS



What is CarPlay/MFi and what is USB’s role in the application?

On-the-Go (OTG)

- On-the-go:
  - Allows USB devices to act as host
  - In automotive: Interoperability between automotive infotainment systems (head unit) and USB devices (phone)
  - Phone becomes the host and control phone App on the Head Unit

- Major players:
  - Apple CarPlay, Google Android Auto,

What is Apple CarPlay?

* ***"Apple CarPlay*** *is a smarter, safer way to use your iPhone while you drive. With an all-new CarPlay Dashboard that helps you with tunes, turns, and Siri suggestions, a Calendar app that lets you view and manage your day, and maps for navigation."*

Apple Carplay will swap the host between the Head Unit and Apple phone, you can control the App on the actual Head Unit.

***Text source : https://www.apple.com/ios/carplay/**

Apple CarPlay handshake process

1. Phone connect to head unit and is recognized by head unit
2. If CarPlay feature enabled in phone, the head unit will send some packets indicating made for iPhone (MFi) information.
3. Head unit sends role switch request
4. If phone supports CarPlay, it will disconnect from the D+ and D-
5. Head unit turns on and pull up D+ (per OTG supplement)
6. Head unit waits for Apple device to enumerate, communication success

Apple MFi

Apple MFi ----Made For iPhone/iPod/iPad
It is a licensing program for developers of hardware and software peripherals that work with Apple's iPod, iPad and iPhone.

MFi has strict requirement for USB port voltage, current and bandwidth.

What is USB’s role in the Apple CarPlay/MFi?

1. USB port VBUS voltage range
2. USB Port bandwidth and signal integrity
3. USB Port Overcurrent and short circuit protection

What is USB's role in the Apple CarPlay/MFi?

- USB port VBUS voltage range

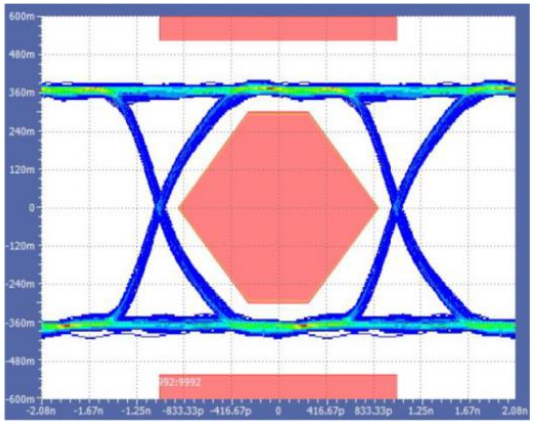
Power for non-lightning accessories			
Supply Rating	Min Output	Max Output	
1 A	4.90	5.25	V
2.1 A delivering up to 1 A	4.90	5.25	
2.1 A delivering up to 1 to 2.1 A	4.97	5.25	
2.4 A delivering 1 to 2.4 A	4.97	5.25	

*Data from MFi

USB port voltage range should always within apple MFi VBUS windows.

What is USB's role in the Apple CarPlay/MFi?

- USB Port bandwidth and signal integrity

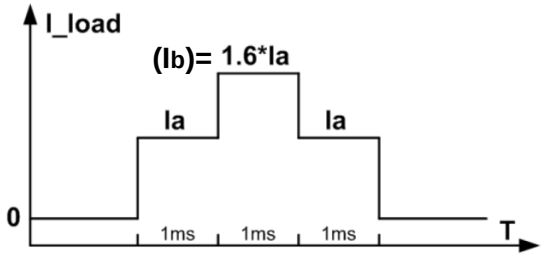


Lightning cables transfer data at USB 2.0 speeds.

USB 2.0 need to supports 480Mb/sec data rate transfer, Apple Carplay will require the good signal integrity quality for the USB Port.

What is USB's role in the Apple CarPlay/MFi?

- USB Port overcurrent and short circuit protection



Data from MFi

Threshold	Definition
I_a	Nominal accessory output current (i.e. 1000 mA, 2100 mA, 2400 mA, 3000 mA).
I_b	I_a + 60%.
I_c	Lowest device current draw that will cause accessory output voltage (measured at Lightning Device Power) to drop below 2 V.

Table 12-3 Overcurrent/Short Circuit Protection Behaviors

Region	Name	Accessory Behavior
A	Normal Operation	Accessory must not limit or shutdown output current.
B	Overcurrent Transient	Accessory must not shutdown output current. Accessory may limit output current to I_a or higher.
C	Overcurrent	Accessory must shutdown output current.
D	Potential Overcurrent	Accessory may shutdown output current.
E	Potential Short Circuit	If Lightning Device Power voltage drops below 2 V, the accessory may trigger short circuit protection. Accessories must not trigger short circuit protection on device current draw.

The USB port need to sustain 160%Ia for 1mS without VBUS drop to Zero.

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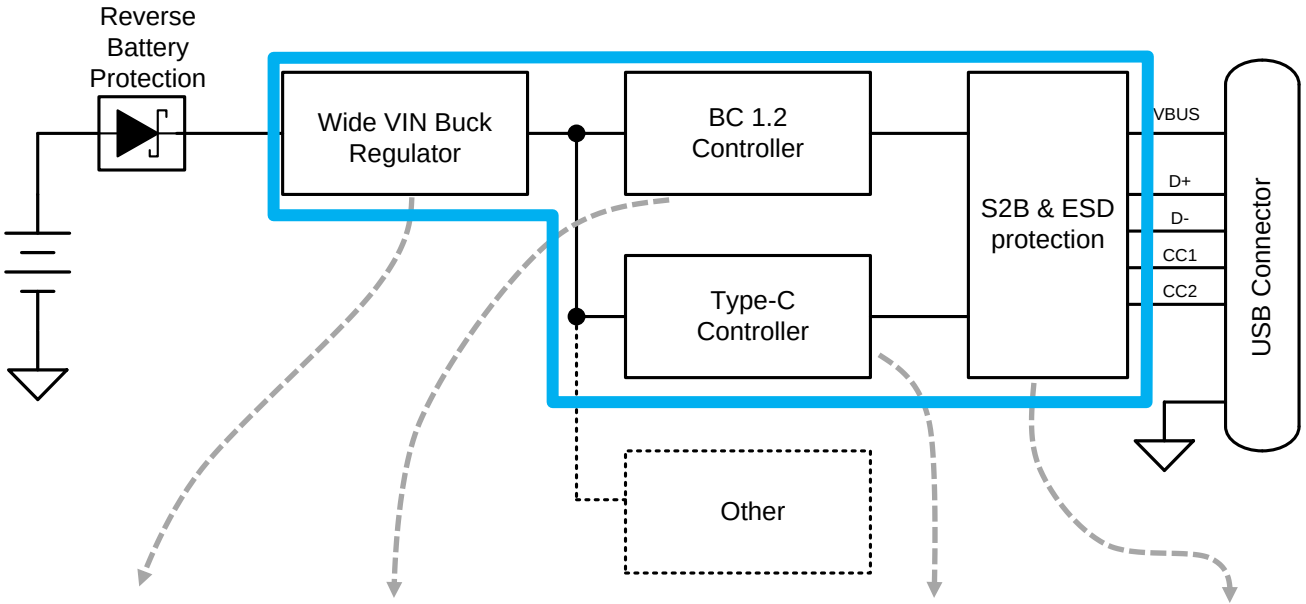
Automotive USB power



Buck (36V / 2.5A+)
LM14030-Q
LM53635-Q
LMS3635-Q
LMR33630-Q

BC 1.2
TPS2546-Q
TPS2549/900-Q

TPS2514A-Q

Type-C
TPS25810/A-Q
TUSB319-Q

ESD & S2B
TPDxS300-Q
TPDxEyyy-Q

USB All-in-One
TPS25830/1-Q

TPS25830/1: Single USB Port Controllers

Common Features:

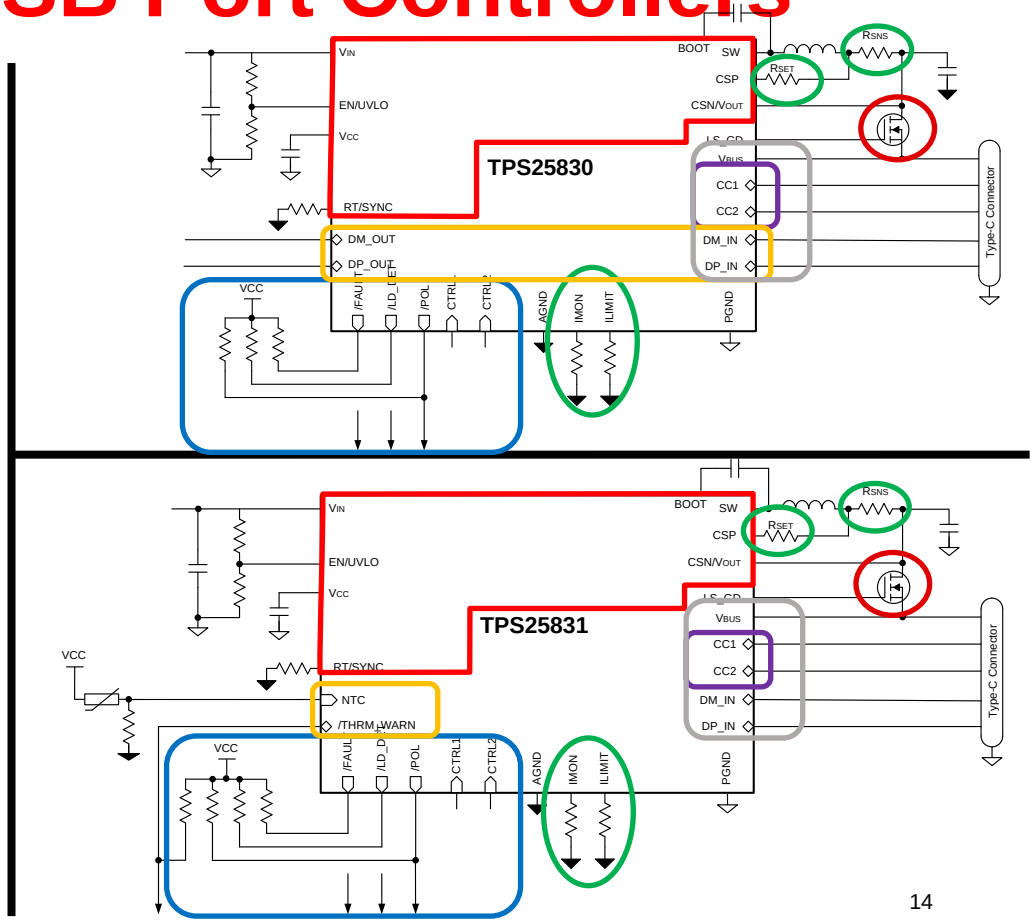
- 6-36V VIN, 3.5A Buck with Spread-Spectrum
- USB Type-C & BC1.2 port control with DCP, CDP, SDP
- ± 7% Acc. Current Sense / Current Limit
- Linear VBUS Droop Compensation
- External FET for current limited
- VCONN support: 5V @ 250mA
- Simple Control & Status flags
- Fault protection:
  - VBUS: short to VBAT (OV) or GND (OC)
  - CC: short to VBAT (OV) or GND (OC)
  - Dx: Short to VBAT (OV)
  - IC Over-temperature

TPS25830:

- >800MHz USB HS pass-through switch with IEC61000-4-2 ESD protection

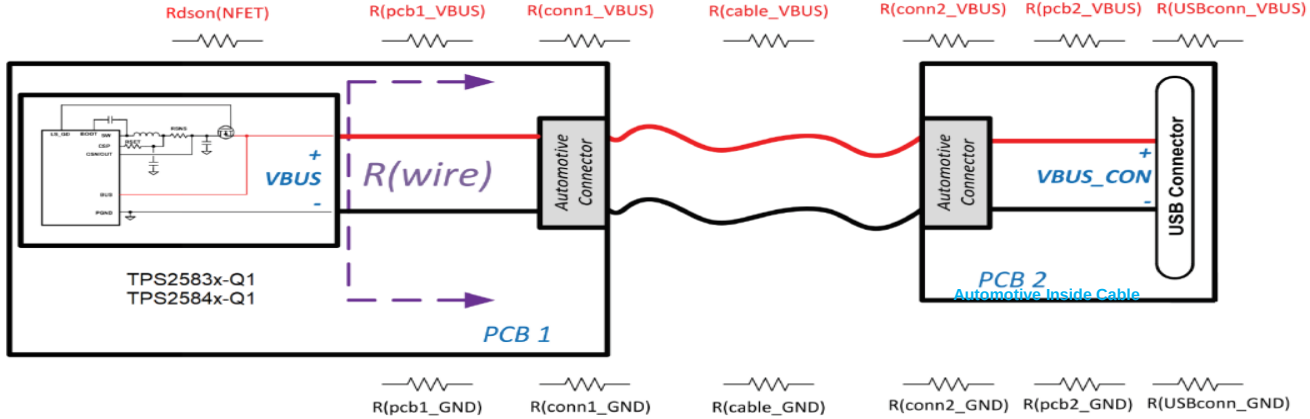
TPS25831:

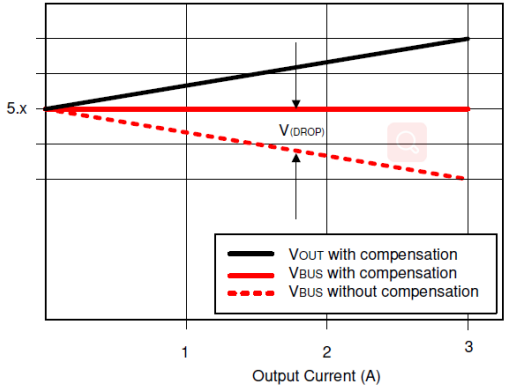
- Thermistor input and thermal warning flag for monitoring PCB temperature



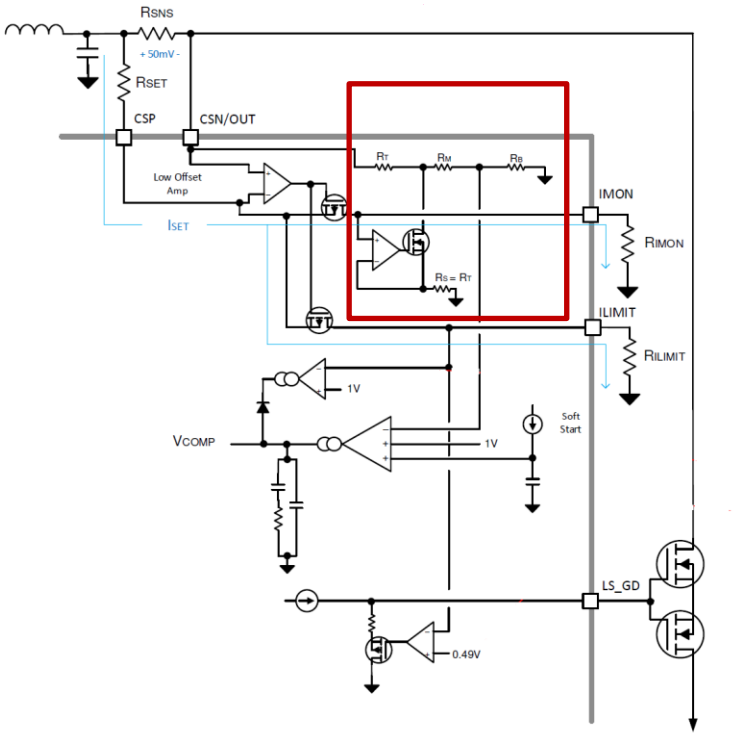
MFI output current and VBUS voltage range

SUPPLY RATING	MINIMUM OUTPUT	MAXIMUM OUTPUT
1 A	4.90 V	5.25 V
2.1 A delivering up to 1.0 A	4.90 V	5.25 V
2.1 A delivering 1.0 to 2.1 A	4.97 V	5.25 V
2.4 A delivering 1.0 to 2.4 A	4.97 V	5.25 V





TPS2583X/4X block diagram for cable compensation



The current that passes the RSET can be calculated by equation:

$I_{SET} = RSNS \times ILOAD / RSET$

The voltage on the IMON can be calculated by equation :

$V_{IMON} = (ISET / 2) \times RIMON = RSNS \times ILOAD \times RIMON / (2 \times RSET)$

Cable compensation voltage as equation:

$VCOMP = VIMON$

RIMON can be deduced by equation:

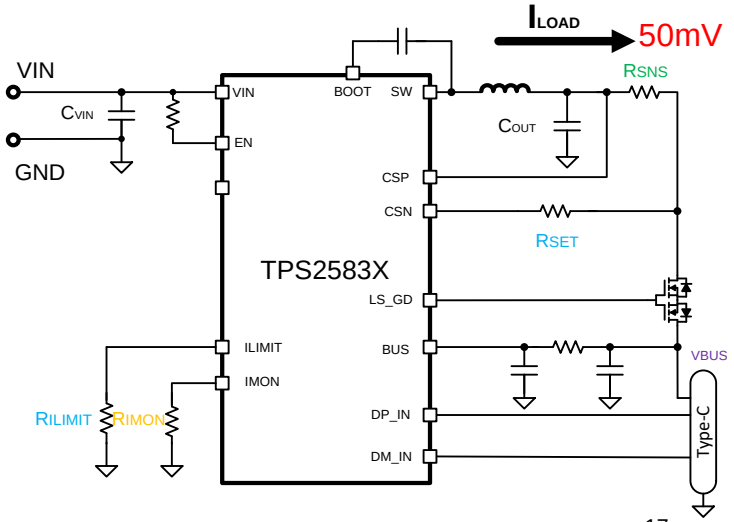
$R_{IMON} = VCOMP \times 2 \times R_{SET} / (ILOAD \times RSNS)$

VBUS accuracy estimation for MFi certification

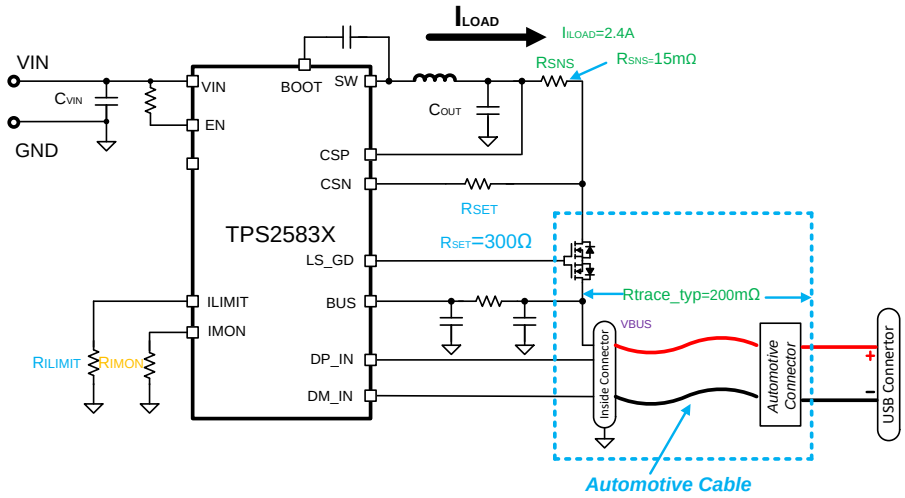
Cable compensation voltage						
PARAMETER	**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNIT**	**Compensation Accuracy**
V_{IMON}	(VCSP - VCSN) = 46 mV, RSET= 300 Ω, RILIMIT = 13 kΩ, RIMON = 13 kΩ	0.935	1	1.065	V	**±6.5%**
V_{IMON}	(VCSP - VCSN) = 26 mV, RSET = 300 Ω, RILIMIT = 13 kΩ, RIMON = 13 kΩ	0.435	0.5	0.565	V	**±13%**

TI Recommends: *Choosing the suitable R_{SNS}, which has an approximate 50 mV voltage drop under desired maximum output current.*

VBUS_typ = VOUT_typ + VCOMP_typ - VDROP_typ
VBUS_min = VOUT_min + VCOMP_min - VDROP_max
VBUS_max = VOUT_max + VCOMP_max - VDROP_min



VBUS cable compensation design example



1. *VDROP_typ = ILOAD_typ × Rtrace_typ = 2.4 A × 200 mΩ = 480 mV*

2. *ILOAD_min = ILOAD_max = ILOAD_typ = 2.4 A;VDROP_max = VDROP_min = VDROP_typ = 480 mV.*

3. *Choose **RSNS = 15 mΩ (choose reason)***

4. *Choose **RSET = 300 Ω***

5. *VCOMP = VDROP = 480 mV*

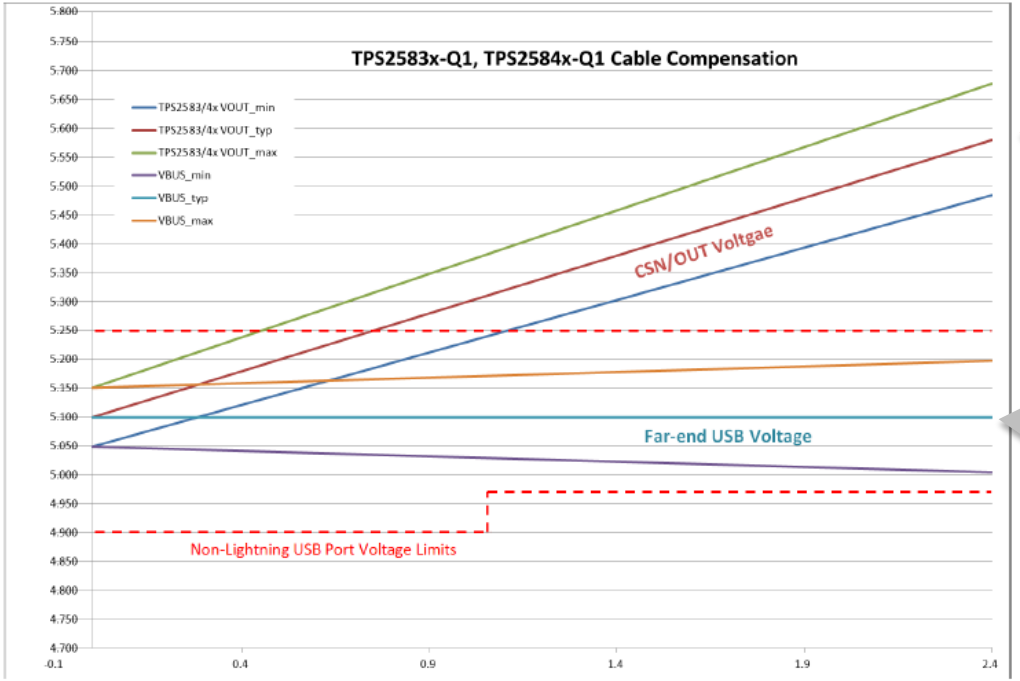
6. *RIMON = VCOMP × 2 × RSET / (RSNS × ILOAD) = 480 mV × 2 × 300 Ω / (15 mΩ × 2.4 A) = 8 KΩ*

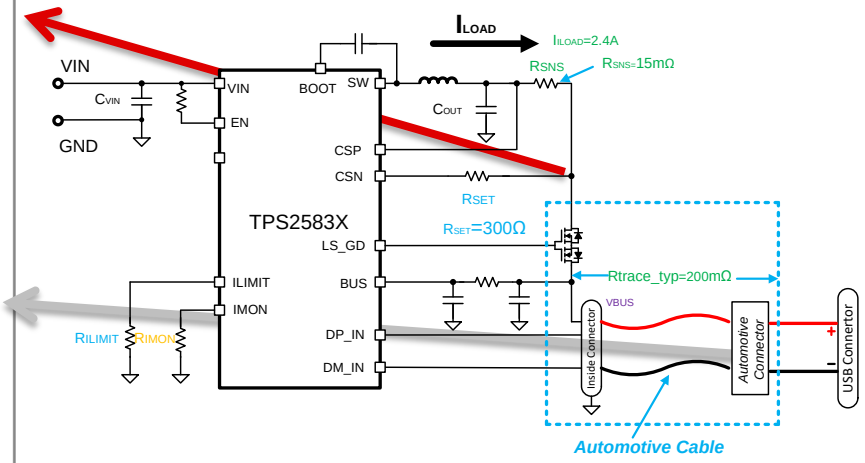
7. *Assume the resistor accuracy is ±1%, that is **RSNS**_min/max = 15 mΩ × (1 ± 1%), RIMON_min/max =8 KΩ × (1 ± 1%), and **RSET** = 300 Ω × (1 ± 1%).*

8. *VCOMP_min = 15 mΩ × 99% × 2.4A × 8 KΩ × 99% / (2 × 300 Ω × 101%) × 93.5% ≈ 435.5 mV. Choose VIMON_acc = ±6.5% according.*
VCOMP_max = 15 mΩ × 101% × 2.4 A × 8 KΩ × 101% / (2 × 300 Ω × 99%) × 106.5% ≈ 526.74 mV

9. *VBUS_min = 5.1V × 99% + 435.5 mV - 480 mV ≈ 5.005 V*
VBUS_max = 5.1 V × 101% + 526.74 mV - 480 mV ≈ 5.198 V

TPS2583x-Q1 far-end USB voltage





Application Note Link: http://www.ti.com/lit/an/slvaeb8/slvaeb8.pdf?&ts=1589098739222

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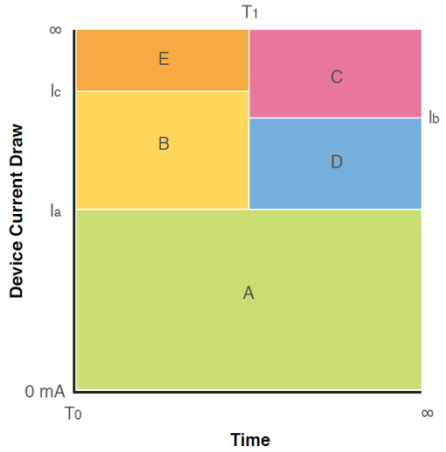
MFi OCP test standard



standard load waveform for OCP test

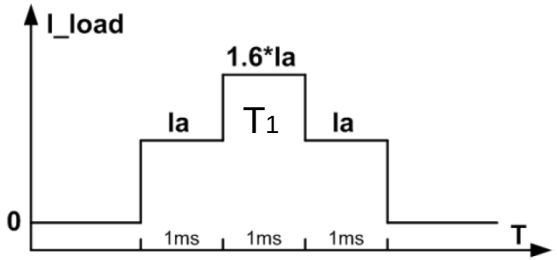


Table 12-2 Overcurrent/Short Circuit Protection Time Thresholds

Threshold	Definition
T_0	Start of any device current draw transient.
T_1	Accessory overcurrent/short circuit deglitch/debounce time, must ≥ T_0 + 1 ms.

Threshold	Definition
I_a	Nominal accessory output current (i.e. 1000 mA, 2100 mA, 2400 mA, 3000 mA).
I_b	I_a + 60%.
I_c	Lowest device current draw that will cause accessory output voltage (measured at Lightning Device Power) to drop below 2 V.

Table 12-3 Overcurrent/Short Circuit Protection Behaviors

Region	Name	Accessory Behavior
A	Normal Operation	Accessory must not limit or shutdown output current.
B	Overcurrent Transient	Accessory must not shutdown output current. Accessory may limit output current to I_a or higher.
C	Overcurrent	Accessory must shutdown output current.
D	Potential Overcurrent	Accessory may shutdown output current.
E	Potential Short Circuit	If Lightning Device Power voltage drops below 2 V, the accessory may trigger short circuit protection. Accessories must not trigger short circuit protection on device current draw.

Required equipment for MFi test

KEYSIGHT N6705C Mainframe

MFi lightning tester fixture

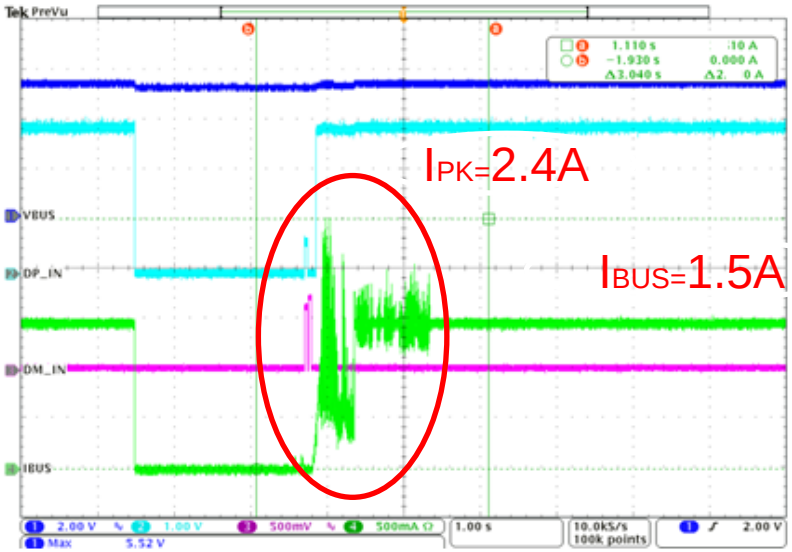
N6791A 100W Electronic Load

Performance Specifications		N6791A
Input Ratings:		
Current		0 - 20 A
Voltage		0 - 60 V
Maximum Power @ 40 °C		100 W
Specified Current @ Low Voltage Operation:		
1.6 V		20 A
1 V		12.5 A
0.5 V		6.25 A
0.1 V		1.25 A
Programming Accuracy:		
Current high range	20 A/40 A	0.04 % + 2.6 mA
Current low range	2 A/4 A	0.04 % + 0.46 mA
Voltage	60 V	0.03 % + 7.2 mV
Resistance high range	8 kΩ	± (0.1 % + 0.0014) S
Resistance medium range	100 Ω	± (0.1 % + 0.014) S
Resistance low range	3 Ω	± (0.1 % + 0.38) S
Power high range	100 W/200 W	0.06 % + 180 mW
Power low range	10 W/20 W	0.06 % + 30 mW
Measurement Accuracy:		
Current high range	20 A/40 A	0.04 % + 2.4 mA
Current low range	2 A/4 A	0.04 % + 0.40 mA
Voltage	60 V	0.03 % + 7.2 mV
Power high range	100 W/200 W	0.06 % + 160 mW
Power low range	10 W/20 W	0.06 % + 25 mW

Apple charging test

CURRENT LIMIT - BUCK REGULATOR PEAK CURRENT LIMIT						
$I_{L-SC-HS}$	High-side current limit		4.6	5.4	6.2	A
$I_{L-SC-LS}$	Low-side current limit		3.5	4	4.5	A
$I_{L-NEG-LS}$	Low-side negative current limit		–3.1	–2.1	–1.3	A

Apple SE charging waveform



Apple MFi OCP Transient Current

Ia(A)	Ib(A)=160%*Ia
1.5	2.4
2.1	3.36
2.4	3.84
3	4.8

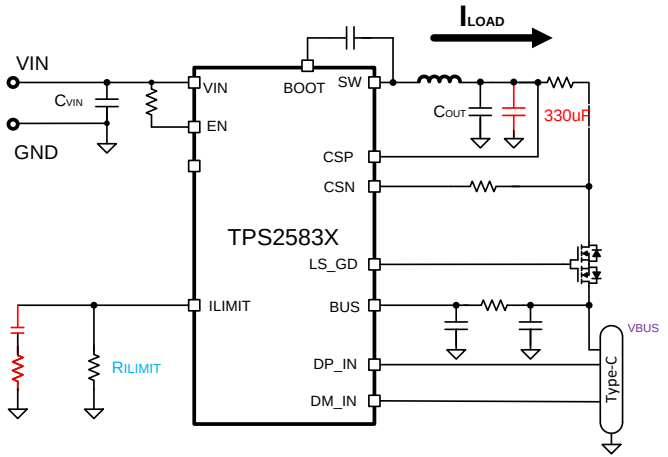
Current solution based on TPS2583x/4x-Q1

*Solution 1. Set current limit >1.6*Ia*

- 1.5A port, set current limit > 2.4A
- 2.1A port, set current limit > 3.36A
- 2.4A port, set current limit > 3.84A
- 3A port:set current limit >4.8A and add **330uf** cap on CSP(***High-side current limit=4.6A***)

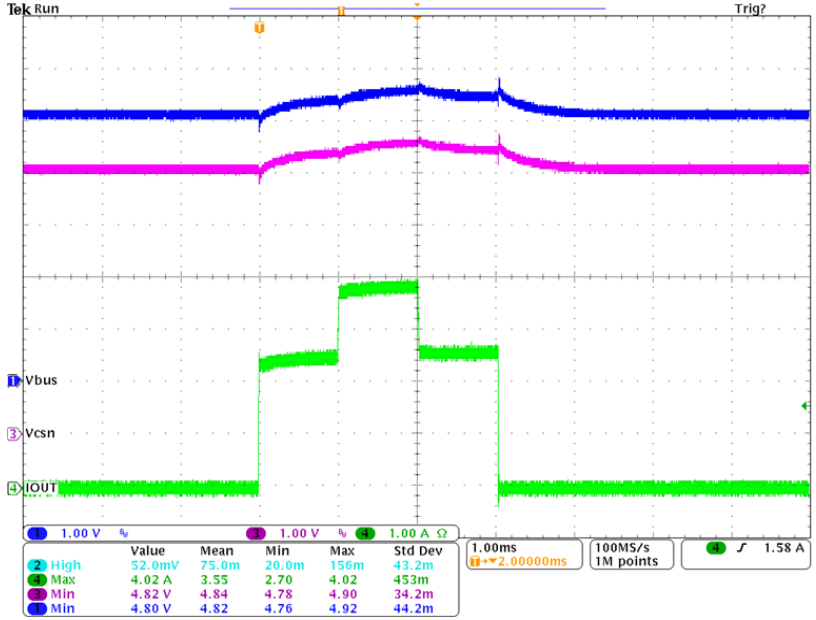
Solution 2. Parallel Cap+R with Rlimit to delay the response of current limit.

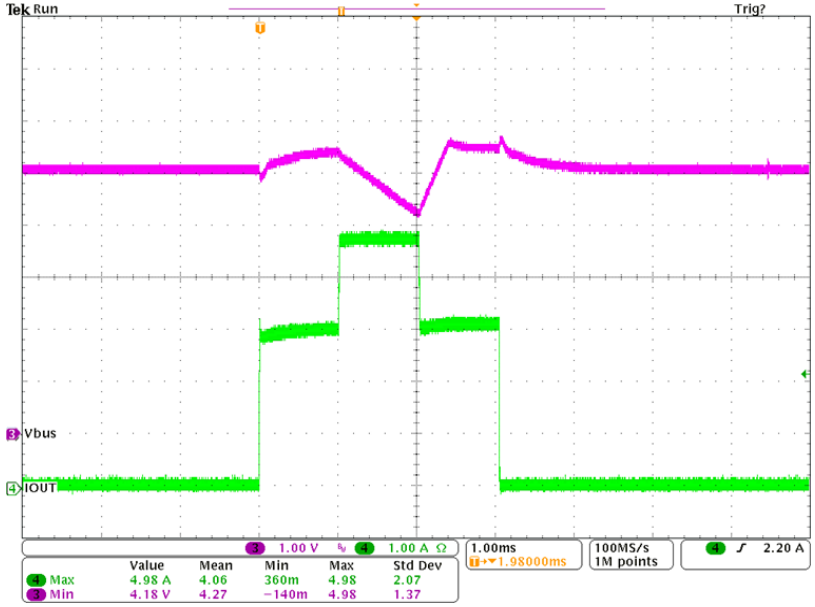
Solution and result	With ex FET Rlimit//RC	Without ex FET Rlimit//RC
1.5A port (1.8A current limit)	10.7kΩ//10.7k+82nF Vbus no drop	21.5kΩ//21.5KΩ+82nf Vcsn no drop
2.1A port(2.52A current limit)	7.68kΩ//7.68kΩ+82nf Vbus no drop	15.8kΩ//15.8kΩ+82nf Vcsn no drop
2.4A port(2.88A current limit)	Recommend using ***Solution*** 1	13.7kΩ//13.7kΩ+82nf Vcsn no drop
3A port(3.5A currnt limit)	Recommend using ***Solution*** 1	11.3kohm//11.3kΩ+82nf add 330uf on CSP Vcsn drop to 4.02V



Solution 3 . Next generation products

Solution 1: 2.4A and 3A MFI OCP test results (with external FET)

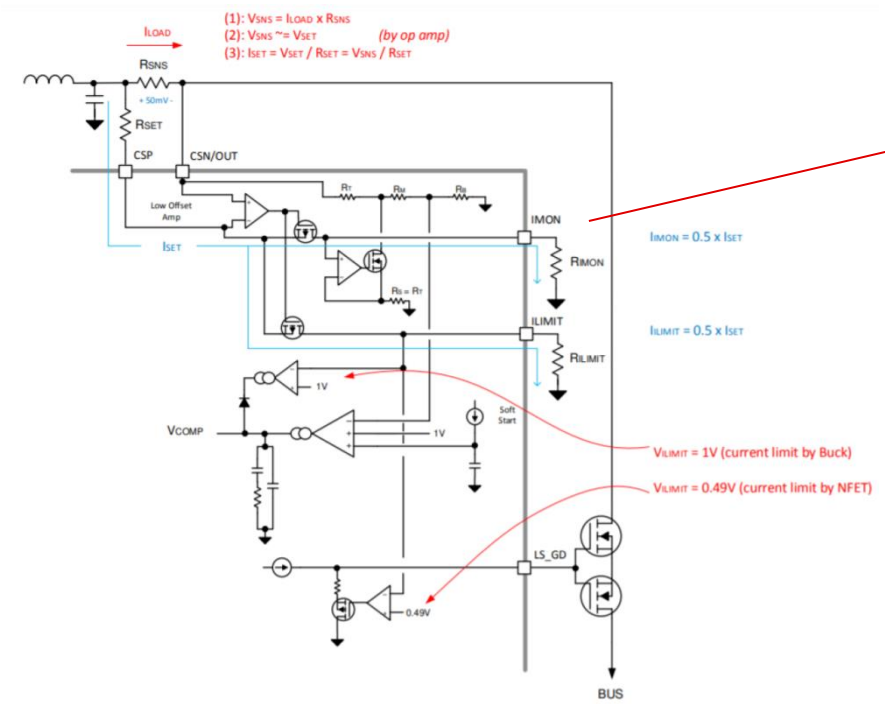


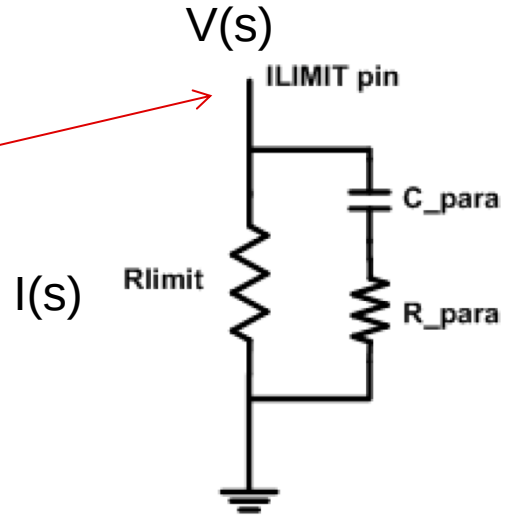


Set 3.96A Current Limit for 2.4A Port

Set 5A Current Limit, and Add 330 µf Cap on CSP for 3A Port

Solution 2: Paralleling RC with Rlimit to delay the current limit response



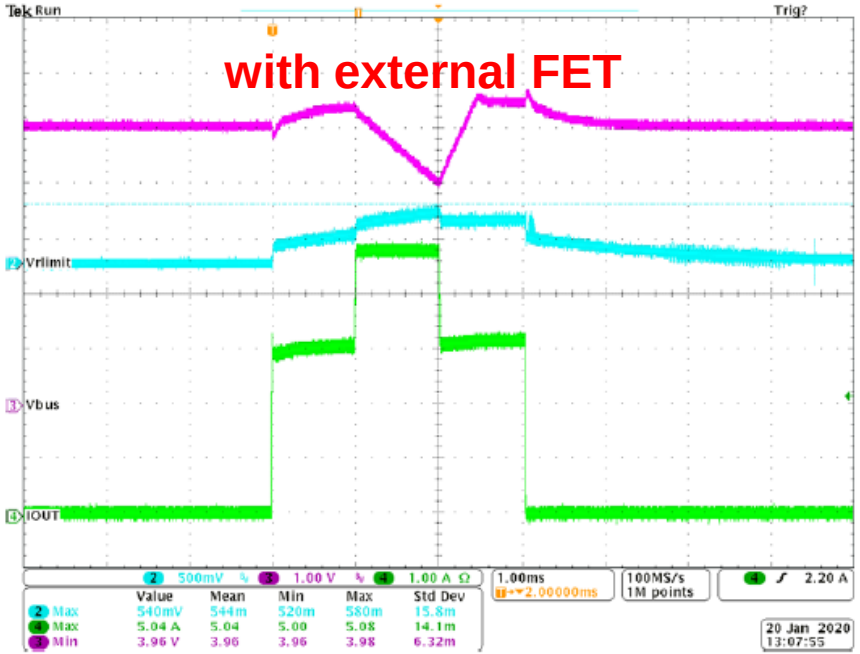


$$\frac{V(s)}{I(s)} = \frac{R_{limit} \times (1 + sC_{para}R_{para})}{1 + sC_{para}(R_{limit} + R_{para})}$$

Current limit function diagrams

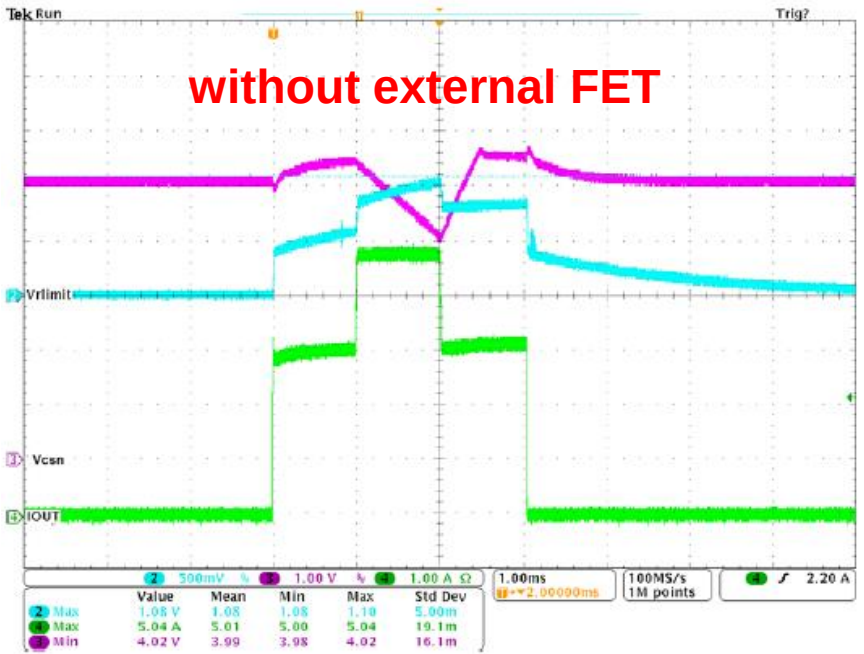
Solution 2 :Paralleling RC with Rlimit to Delay the current limit Response

5.49kΩ Parallel 3.5kΩ+220nF with RC Rlimit



Set 3.5A current limit for 3A port

11.3kΩ Parallel 11.3kΩ + 82 nF with RC Rlimit



Set 3.5A current limit for 3A port

TPS2583x/4x- MFi OCP summary of solution

Solution and result	with external FET-- Rlimit//(Rpara+Cpara)	without external FET-- Rlimit//(Rpara+Cpara)
1.5A port (1.8A current limit)	10.7kΩ//(10.7kΩ + 82nF) Result: Vbus no drop	21.5kΩ//(21.5KΩ + 82nF) Result : Vcsn no drop
2.1A port (2.52A current limit)	7.68kΩ//(7.68kΩ + 82nF) Result: Vbus no drop	15.8kΩ//(15.8kΩ + 82nF) Result: Vcsn no drop
2.4A port (2.88A current limit)	6.65kΩ//(6.65kΩ + 82nF) Result: Vbus no drop	13.7kΩ//(13.7kΩ + 82nF) Result: Vcsn no drop
3A port (3.5A current limit)	5.45kΩ//(3.5kΩ + 220nF) add 330 μf on CSP Result: Vbus drop to 3.96V	11.3kΩ//(11.3kΩ + 82nF) add 330 μf on CSP Result: Vcsn drop to 4.02 V

***Application Note Link*:** *http://www.ti.com/lit/an/slvaeq2/slvaeq2.pdf?&ts=1589098829411*

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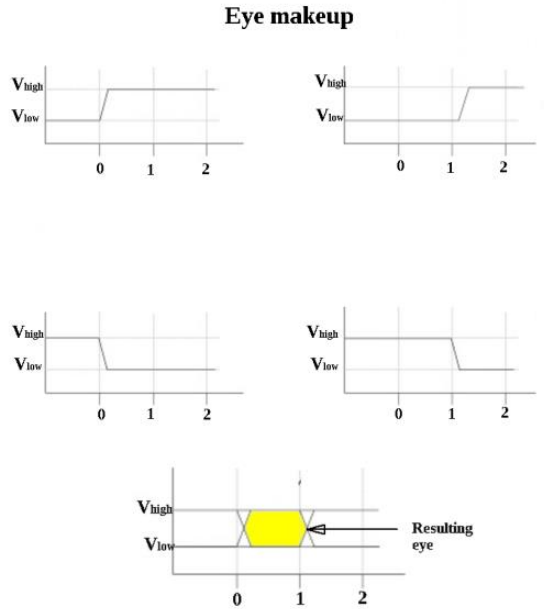
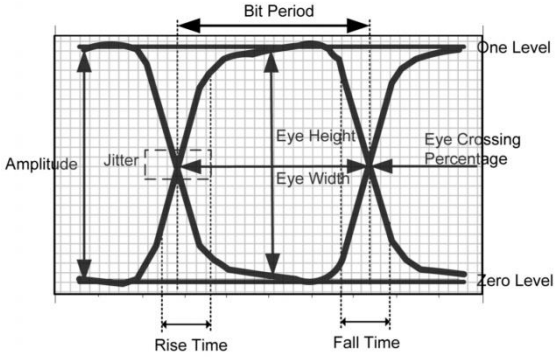
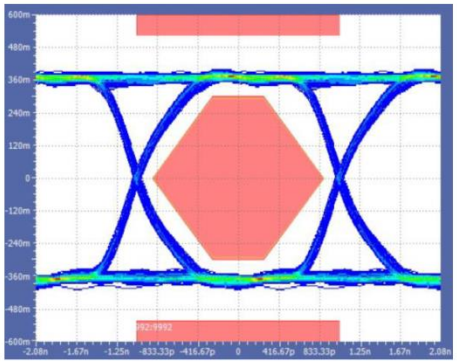
- **How to improve eye diagram performance with TPS2583x/4x**
  - Eye diagram introduction and challenges in long cables
  - How to improve eye diagram performance with TPS2583x/4x
- **How to improve EMI with TPS2583x/4x**
- **Q&A**

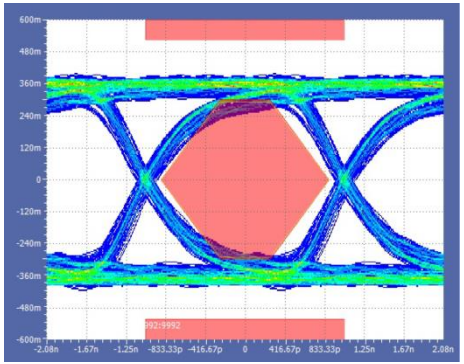
Eye diagram introduction

An eye diagram is evaluation method the signal quality in system data communication.



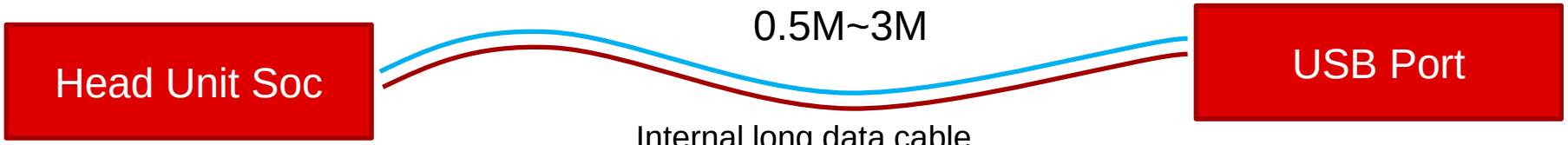


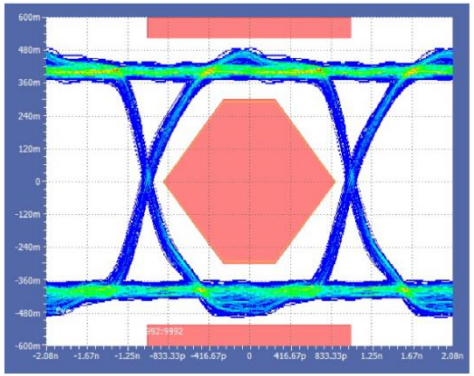




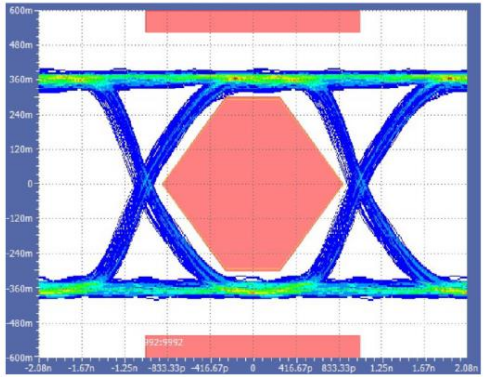
The bit sequences 011, 001, 100, and 110 are superimposed over one another to obtain the example eye diagram.

Challenge: Eye diagram in long cables

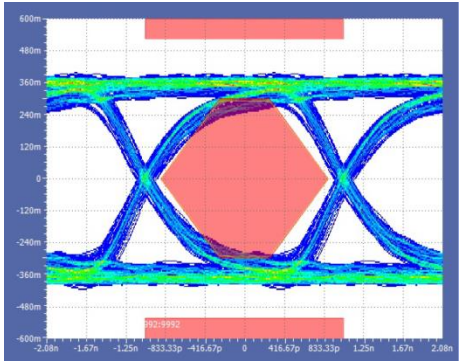




Source



1.8 Meter



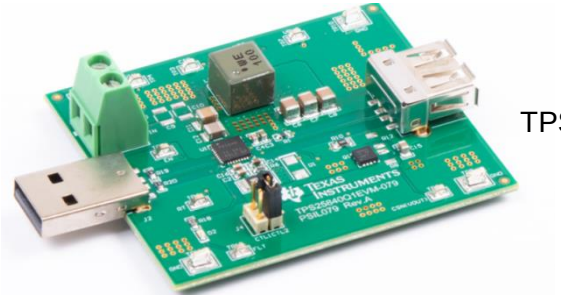
3 Meter

The long cable will create the equivalent capacitance and resistance which will make the system bandwidth become narrow. It is challenging to design good eye diagrams in long data cable applications.

How to improve eye diagram performance with TPS2583x/4x

1. TPS2583x/4x eye diagram performance
2. PCB layout
3. Using LC network
4. Using signal re-driver (TPS25840 + TUSB217)

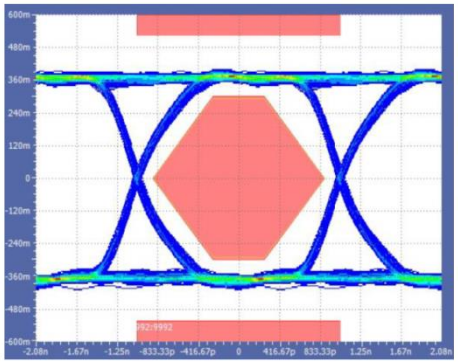
TPS2583x/4x eye diagram performance



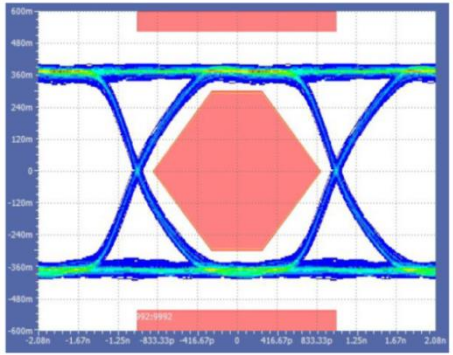
TPS25840Q1EVM-079

Bandwidth (–3 dB)=800Mhz

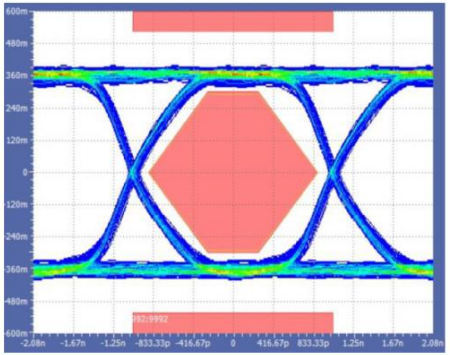
30cm Cable+ EVM TPS25840



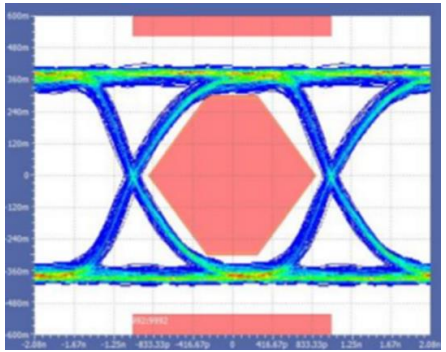
1m Cable+ EVM TPS25840



1.5m Cable+ EVM TPS25840



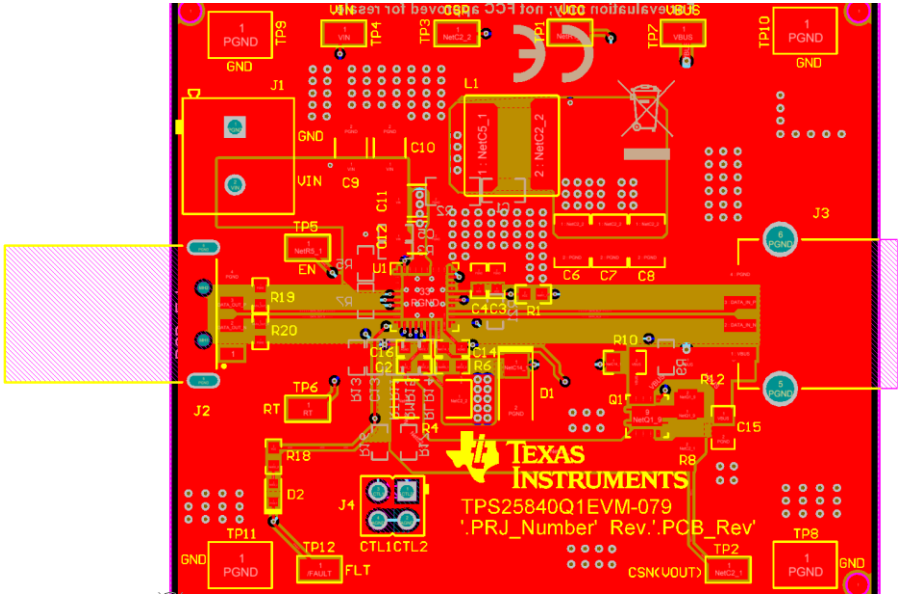
1.8m Cable +EVM TPS25840



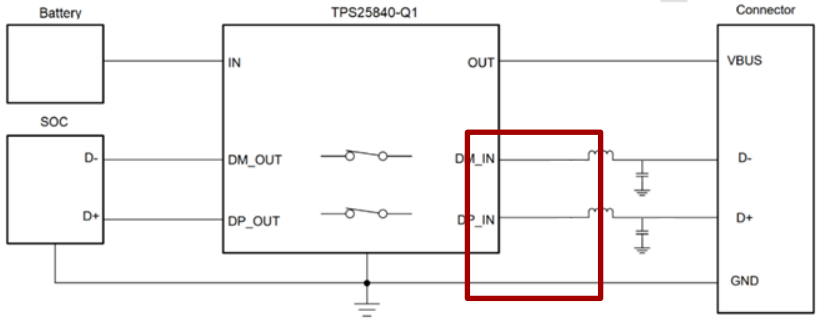
The TPS2583x have 800Mhz bandwidth help system pass 1.5Meter long cable eye diagram test.

PCB Layout

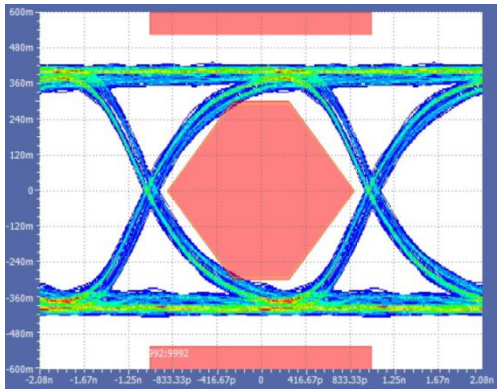
1. Both the DP and the DM signals should travel the same distance.
2. Control the DP and DM trace differential impendence to 90 ohm.
3. DP and DM signals should consistently be routed over a signal ground layer.
4. DP and DM keep away from noisy power signals and clock circuitry components.



How to improve eye diagram with TPS2583x/4x-Q1

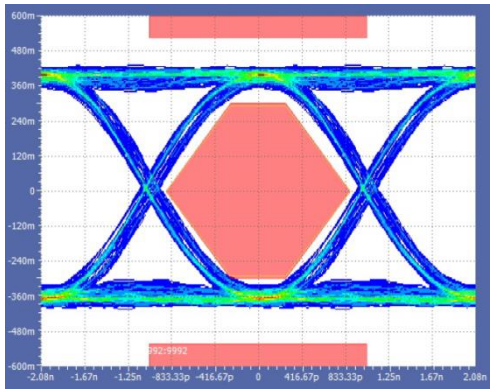


1.8m cable customer board



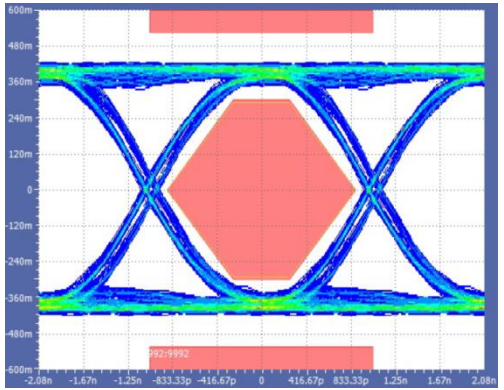
Fail

LC=16nH + 10pF



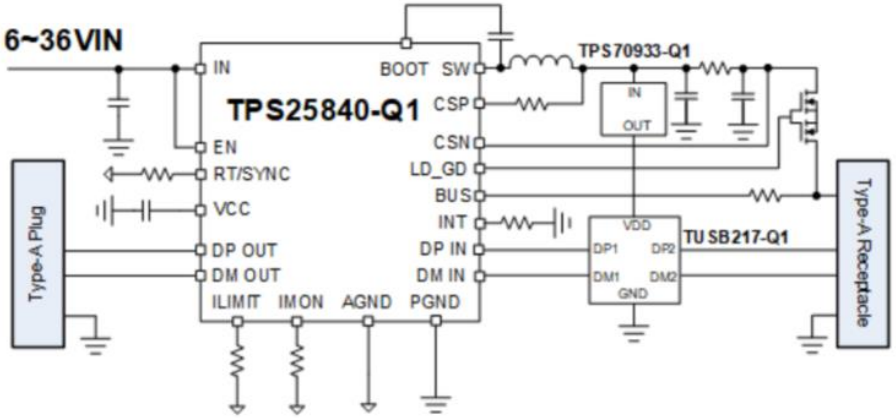
Fail

LC=16nH + 4.7pF



Pass

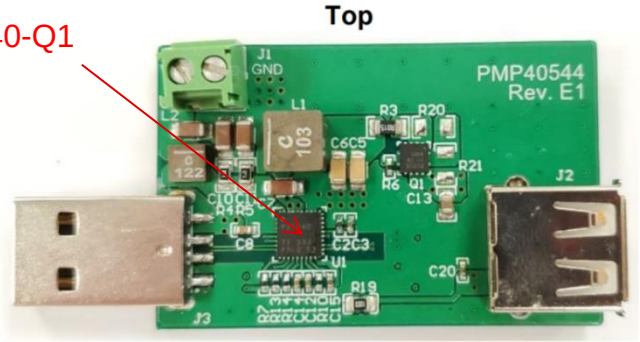
TPS25840 + TUSB217 eye diagram performance

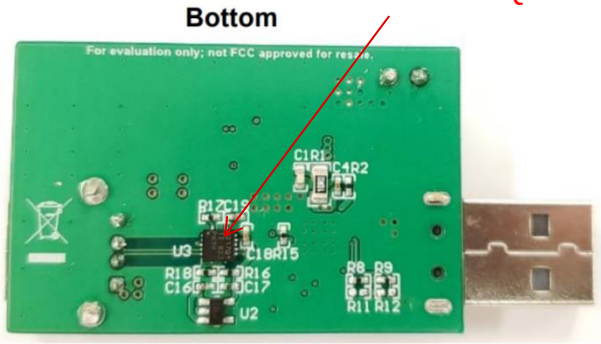


Reference Design: PMP40544

TPS25840-Q1

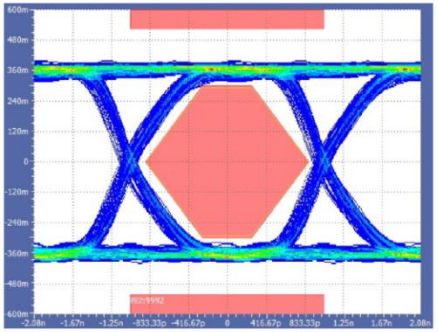
TUSB217-Q1



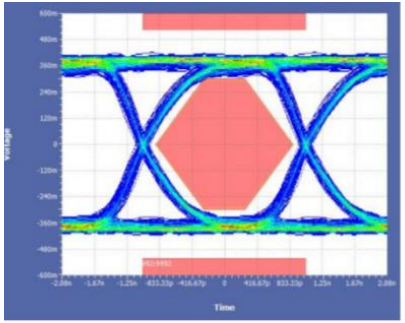


TPS25840 + TUSB217 eye diagram performance

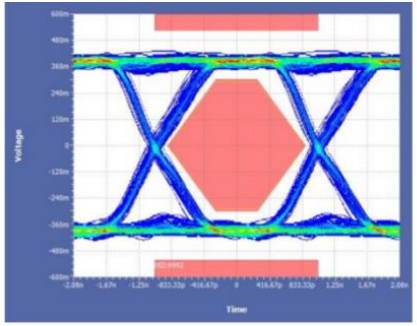
1.8M source



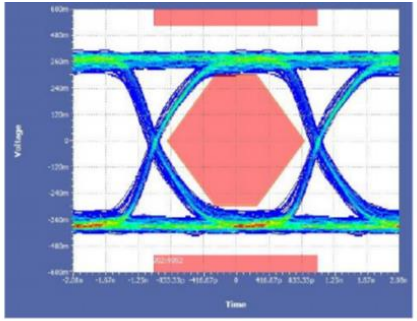
Add TPS25840



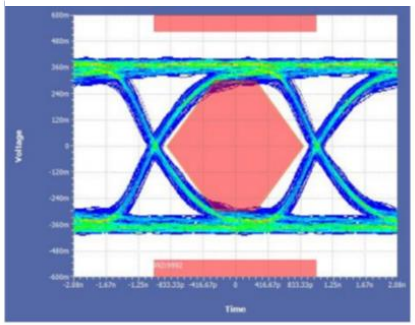
TPS25840+TUSB217



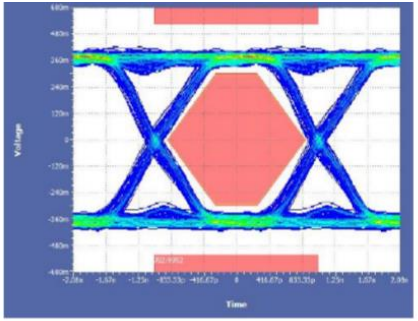
3M source



Add TPS25840



TPS25840+TUSB217



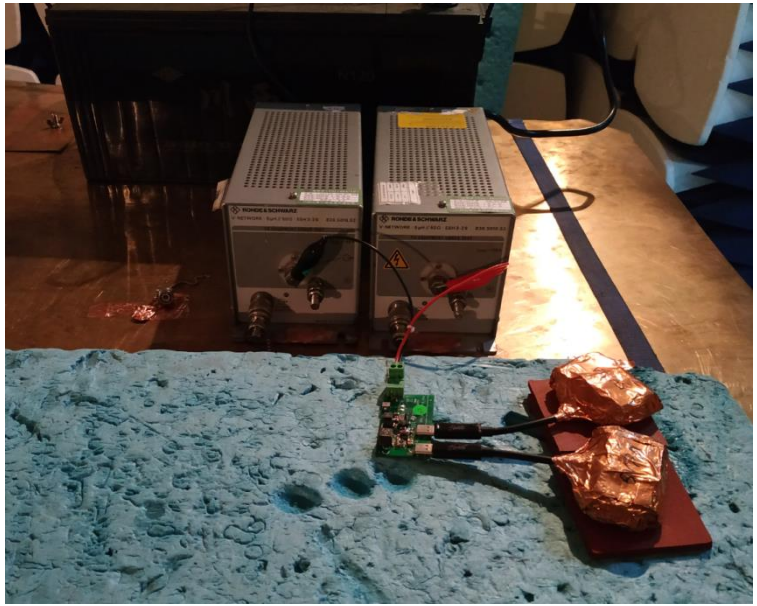
Agenda

- **What is CarPlay/MFi and what is USB's role in the application?**
- **How to pass MFi VBUS requirement with TPS2583x/4x**
  - TPS2583X/4x introduction
  - MFi VBUS spec and test set up
  - Cable compensation introduction
  - Cable compensation design to pass MFi
- **How to pass MFi OCP requirement with TPS2583x/4x**
  - MFi OCP spec and test set up
  - How to pass MFi OCP with TPS2583x/4x
- **How to improve eye diagram performance with TPS2583x/4x**
  - Eye diagram introduction and challenges in long cables
  - How to improve eye diagram performance with TPS2583x/4x
- **How to improve EMI with TPS2583x/4x**
- **Q&A**

TPS2583X/4X EMC test setup

CONDUCTED EMISSION STANDARD: CISPR25, CLASS 5

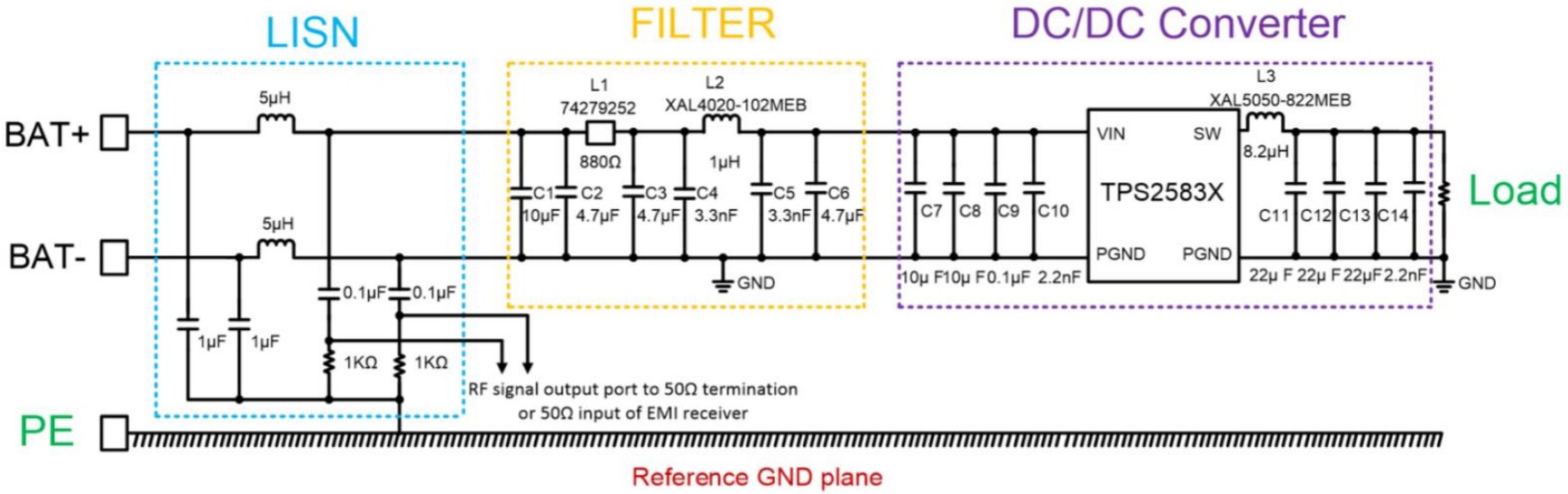
Test Site: Accurate technology Co., Ltd(ATC)



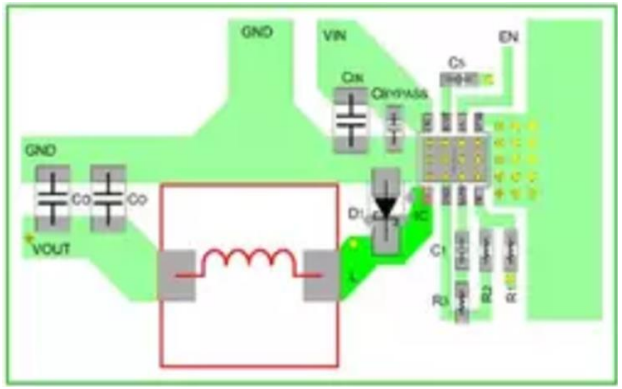
CE Setup

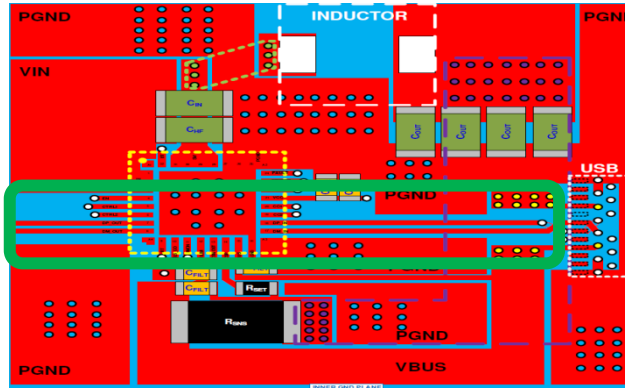
RE Setup

Recommended parameters for input filter



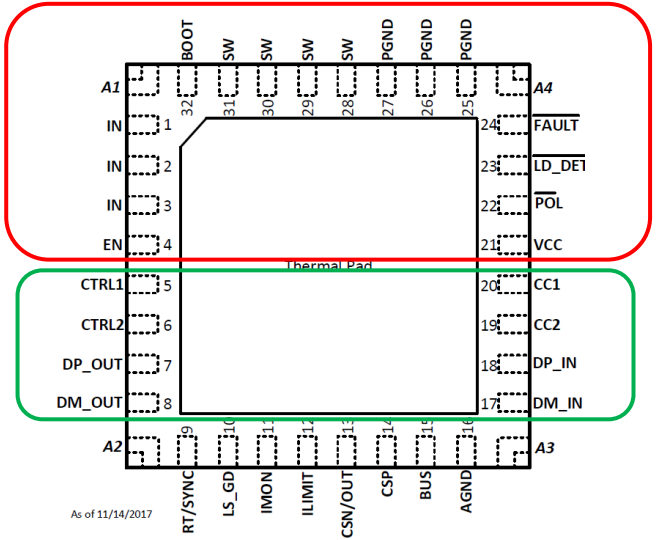
TPS2583X/4X pin layout





DC/DC

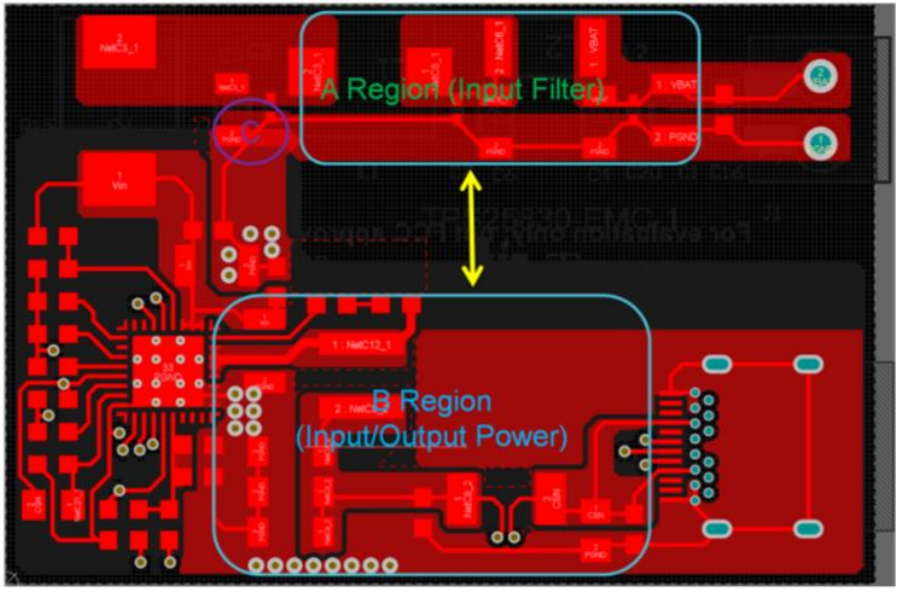
Type A/C protocol



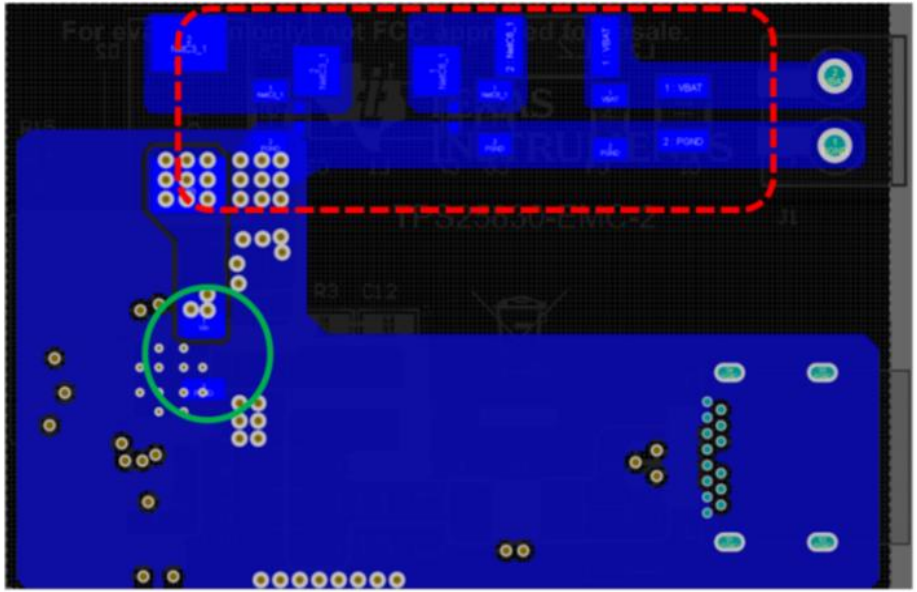
TPS25830-Q1 32-Pin (VQFN) 5×5mm

Input filter

Distance between input filter and DCDC controller should be more than 15 mm in order to prevent the switching noise bypassing the input filter.



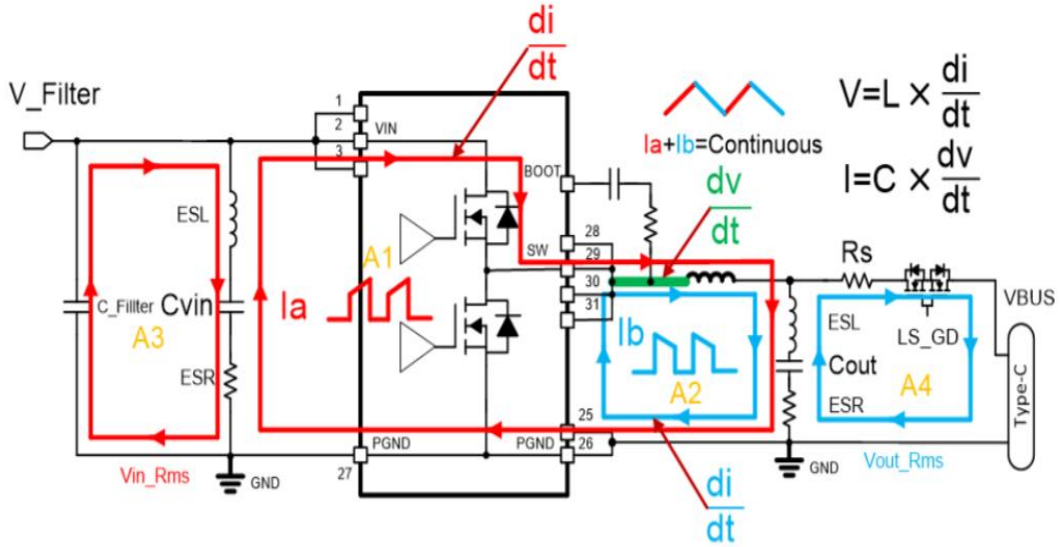
Top-layer of the PCB layout for input filter

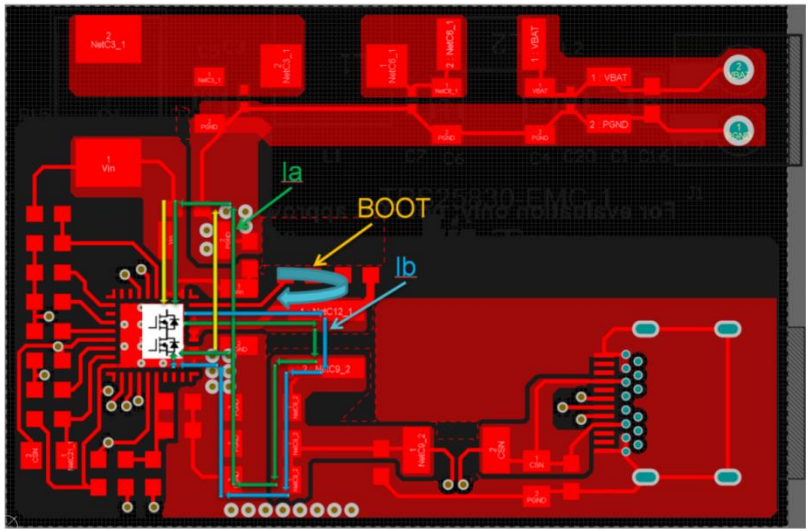


Bottom Layer of the PCB layout for input filter

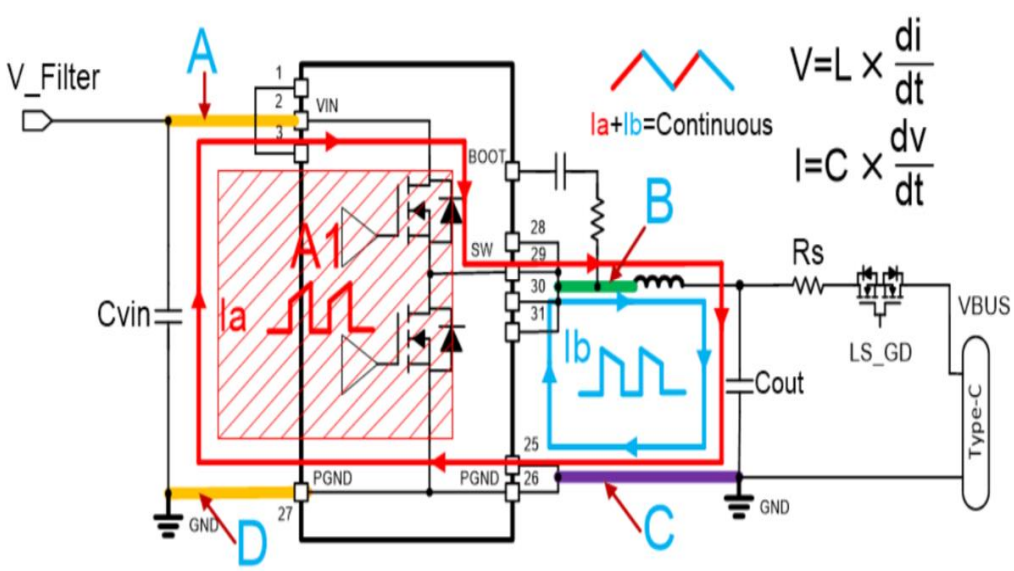
DC/DC power loop

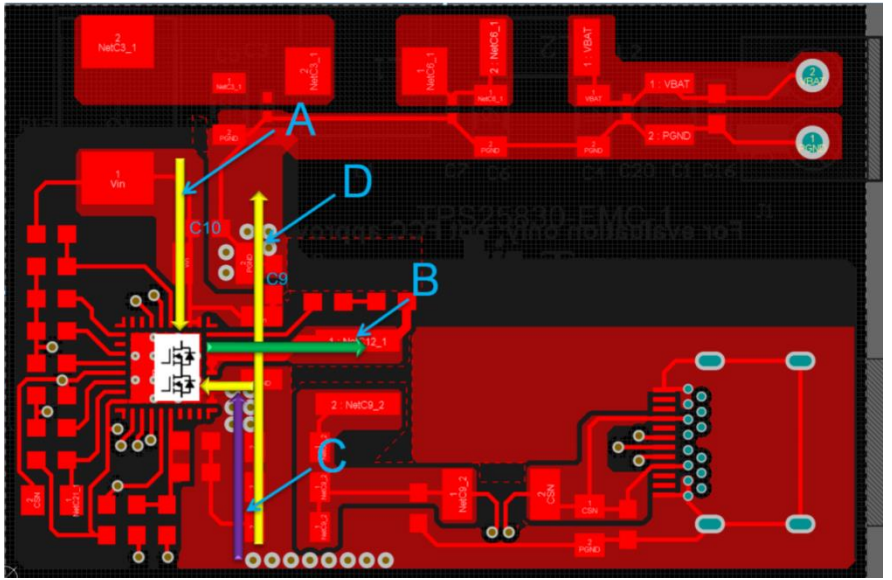
***Ia* and *Ib* have high di/dt . These two loops should be kept as small as possible**





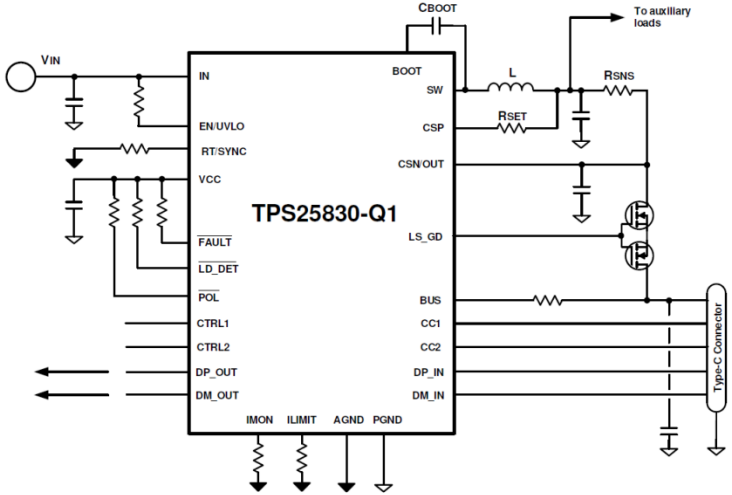
DC/DC power loop

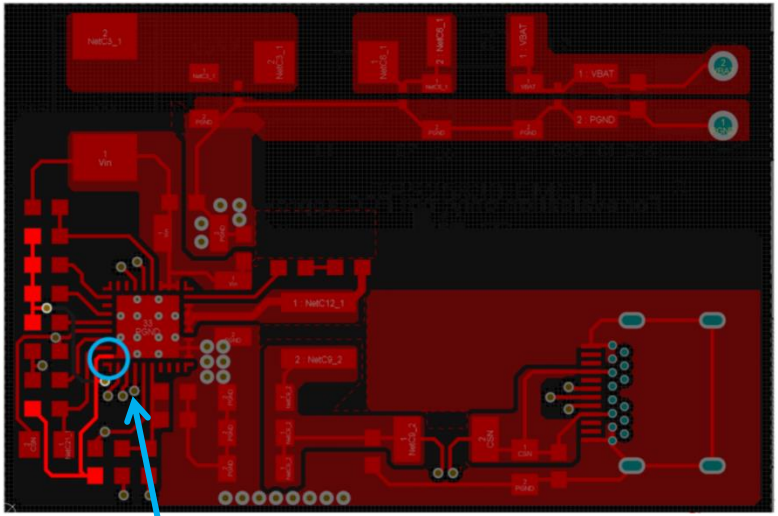




***line A**, **line B**, **line C**, and **line D** trace length should be as short as possible.*

PGND and AGND





The signal ground AGND and the power ground PGND need to be separated in the actual PCB layout to reduce the power ground PGND causing* oscillating *to interfere with the signal ground AGND.

PGND includes: *the ground of the input capacitor, output capacitor, VCC capacitor, input port, output port, and so forth.*

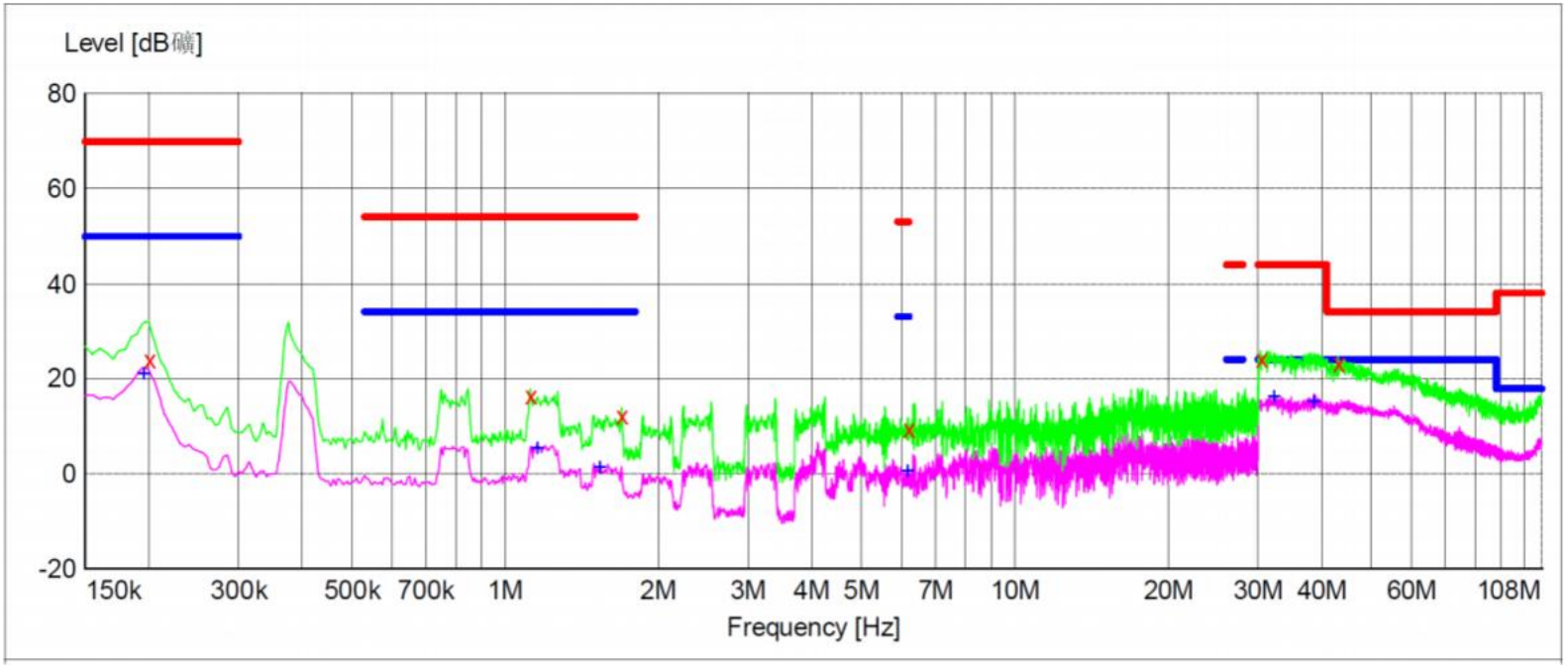
AGND includes: *the ground of RT, IMON, ILIMIT, CC1, CC2, FAULT, LD_DET, POL, CTRL1/2, DP, DM resistors, capacitors and ground lines.*

AGND and PGND connect point

TPS2583X EMI test result

CONDUCTED EMISSION STANDARD: CISPR25, CLASS 5

Test Condition: Vin=12v VBUS=5V/3A F=400KHz



Summary

1. The input and output capacitors should be as close as possible to the input and output pins of the device.

2. Do not put Via on SW lines and keep the SW area as small as possible.

3. The input and output power loop should be as small as possible.

4. The BOOT pin trace loop circuit should as small as possible.

5. Power ground PGND and signal ground AGND should be separated.

6. The input and output capacitors better selected different value and package ,such as 10 µF(1210) + 0.1 µF(0603) + 2.2 nF(0603).

Application Note Link: *http://www.ti.com/lit/an/slvaen5/slvaen5.pdf?&ts=1589098906250*

Thank you for listening!

Do you have any questions?

TEXAS INSTRUMENTS

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