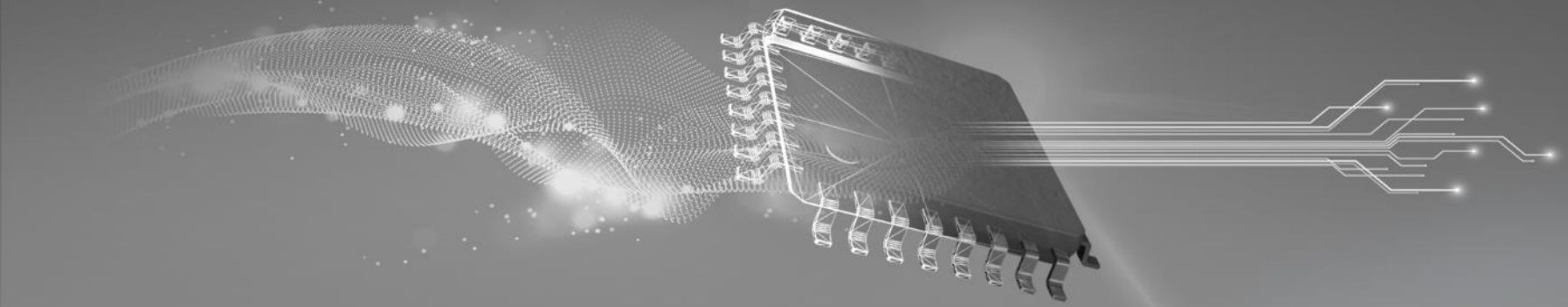
TI TECH DAYS



Achieving ultra-low output noise with DC/DC switching regulators

Jimmy Hua, Analog Applications Engineer

Jimmy Hua

Analog Power - Applications Engineer

Career

- Electrical Engineering degree from University of California, Davis
- Joined TI through Application Rotation Program (2016)
- Joined TI Power Modules group (2017)
- Controllers, Converters & Modules, High-Current (Aug. 2020)

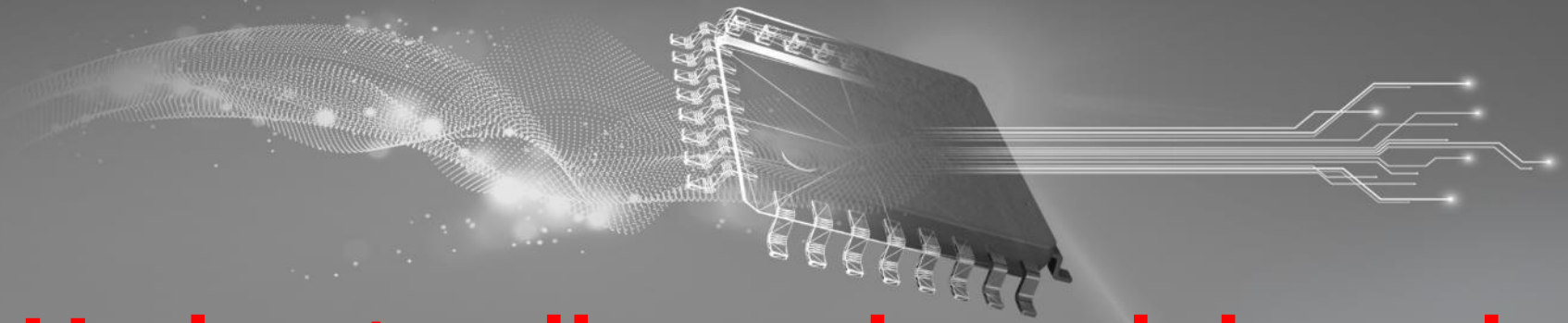
Role

- As an applications engineer in the power modules team I am responsible for customer and FAE support, writing datasheets and application notes, new product development, and creating training presentations and field collateral.

Detailed agenda

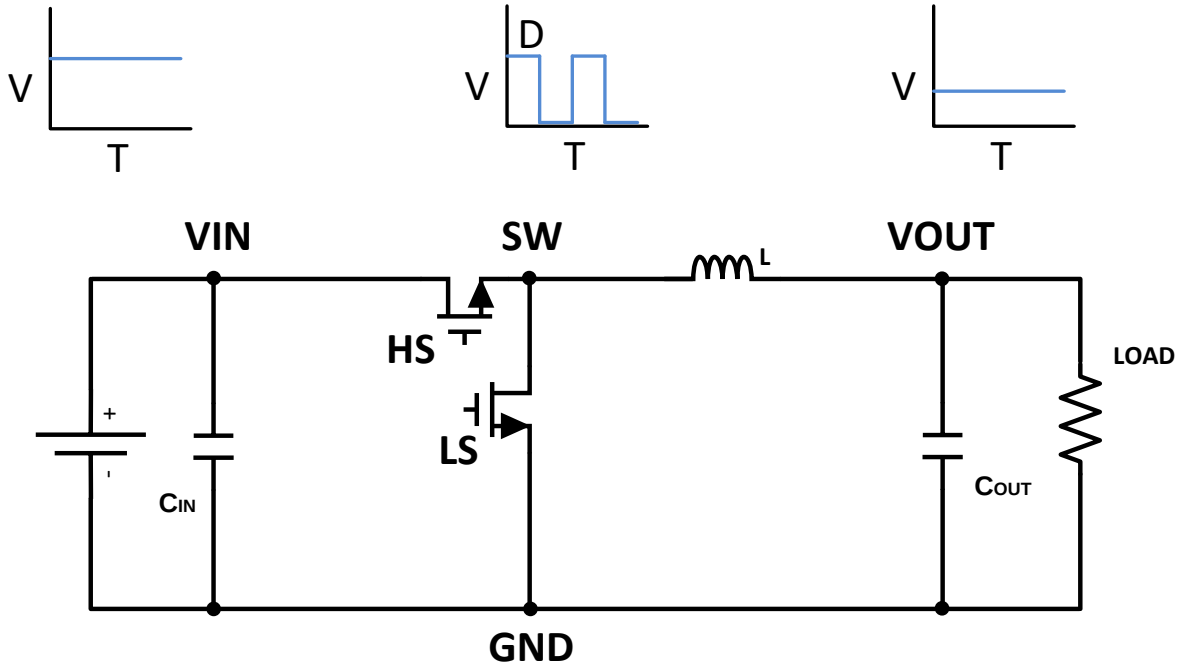
- Understanding noise origin and measurement
  - Noise origin, relevant parasitic elements, high frequency and low frequency components
  - Measurement techniques and examples
  - Noise reduction techniques
- Output noise filtering comparison
  - 2nd Stage LC filters
    - Passives parasitic elements and filter performance
    - Design example
  - LDOs
    - Filtering performance
    - Design example

TI TECH DAYS

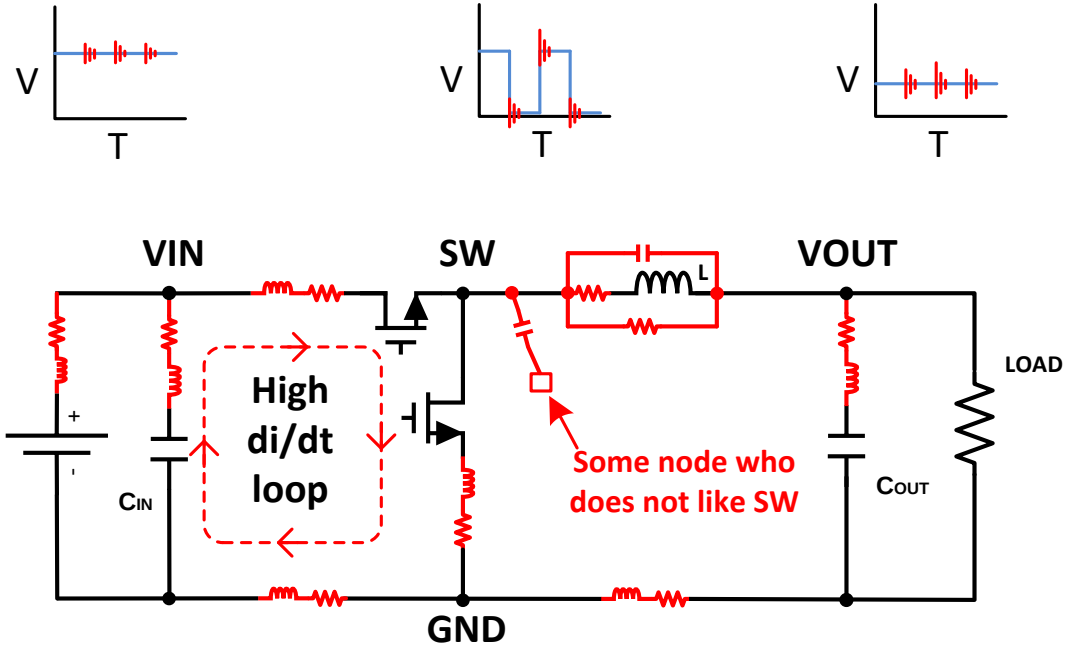


Understanding noise origin and measurement

The ideal buck regulator



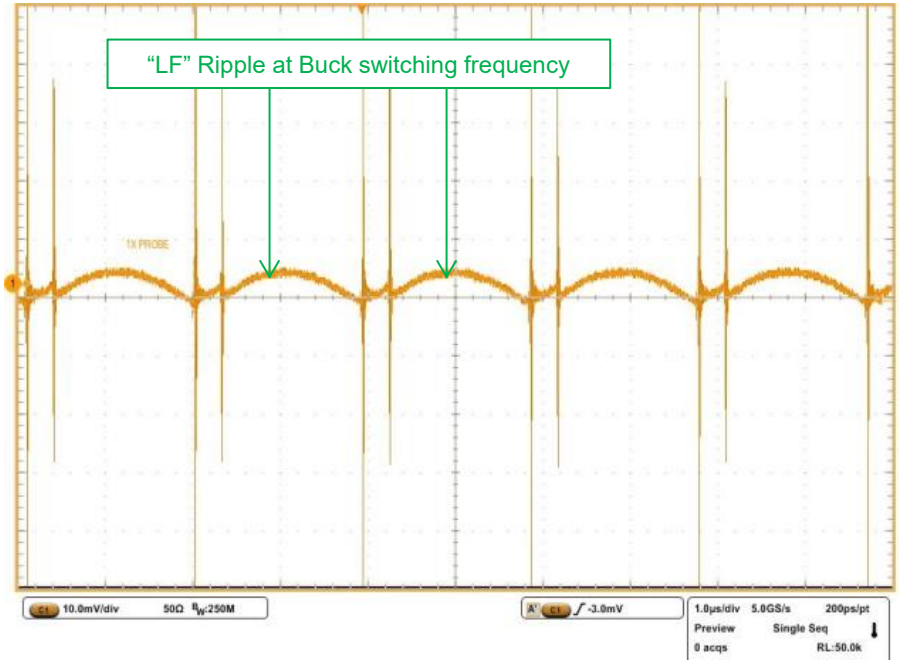
More real buck regulator

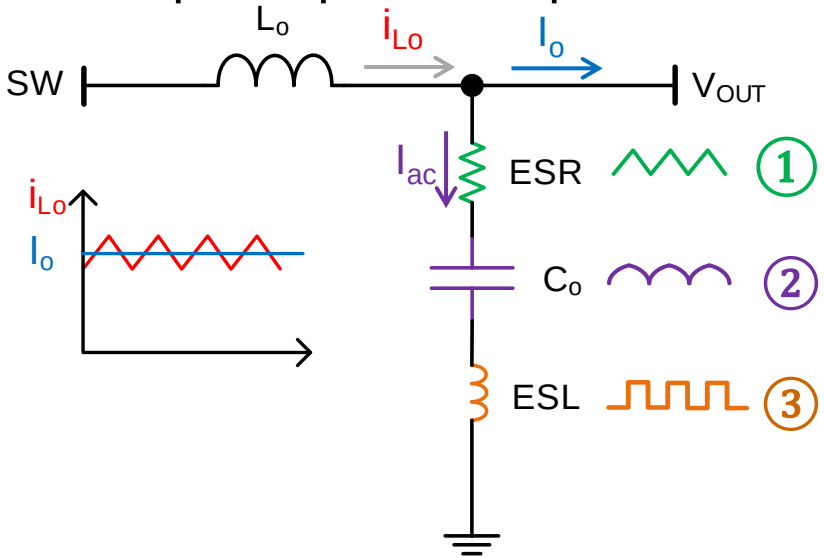


"Free" components in red

LF ripple origin

- Result of the inductor ripple current and output capacitor impedance

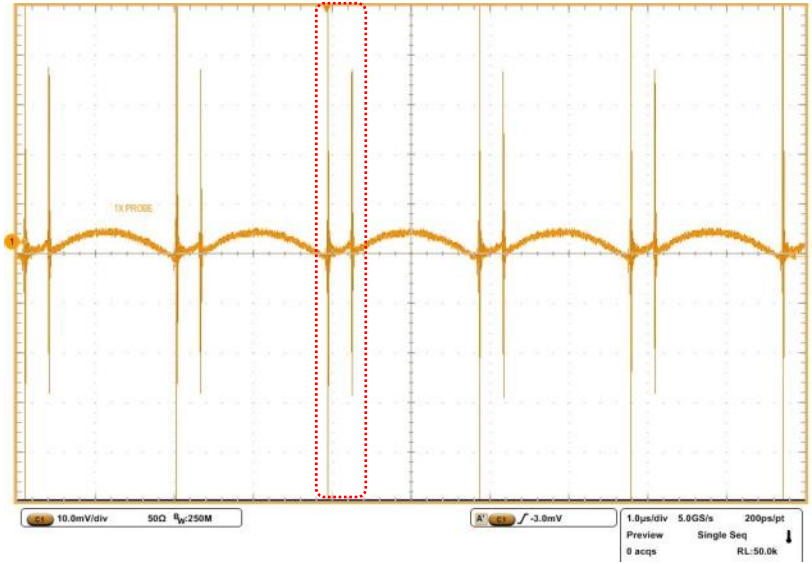


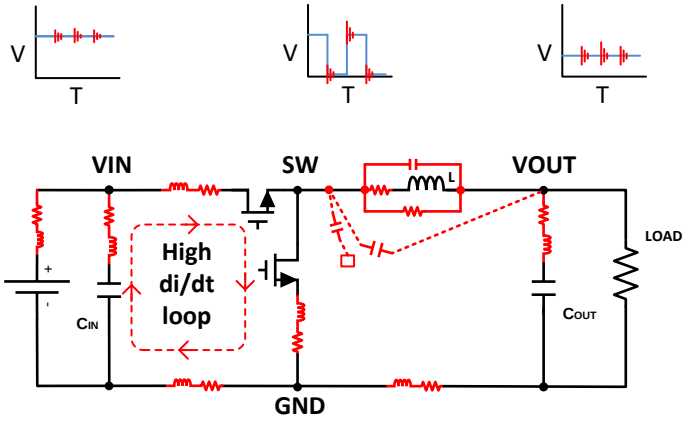


Total LF Ripple = ① + ② + ③

HF noise origin

- Who is generating the noise?
  - High di/dt current loop and any inductance in its path
  - Noise appears on the SW node as ringing at each edge



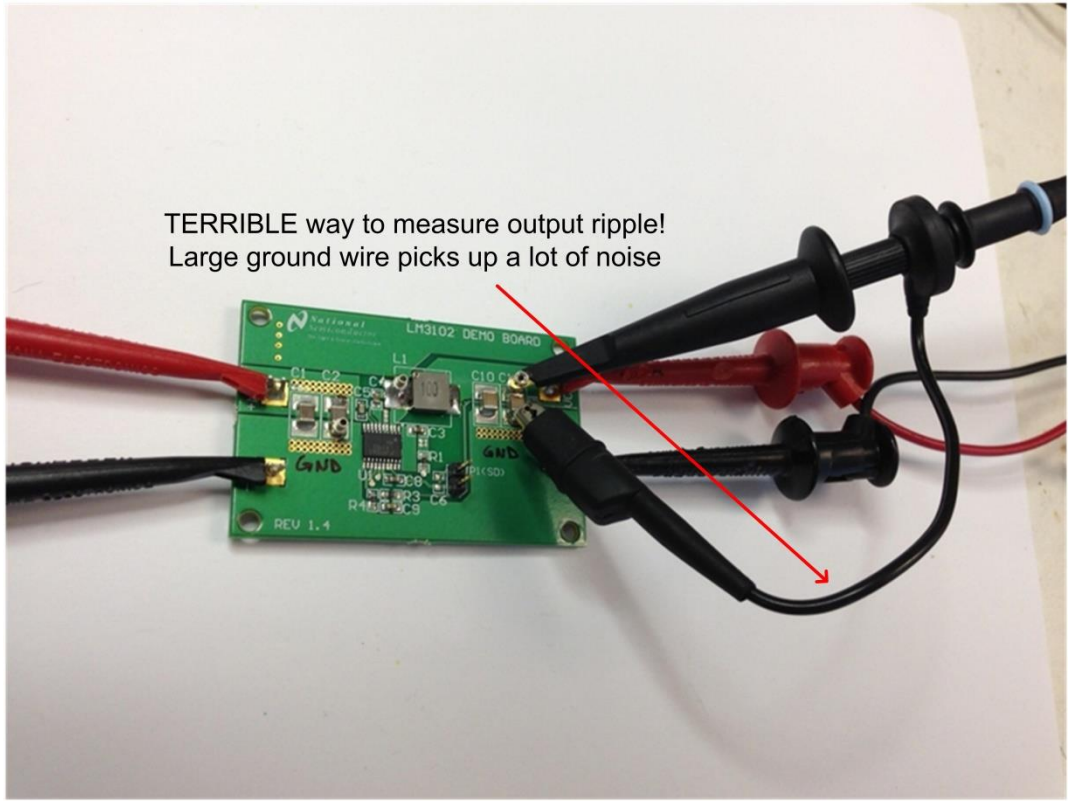


"Free" components in red

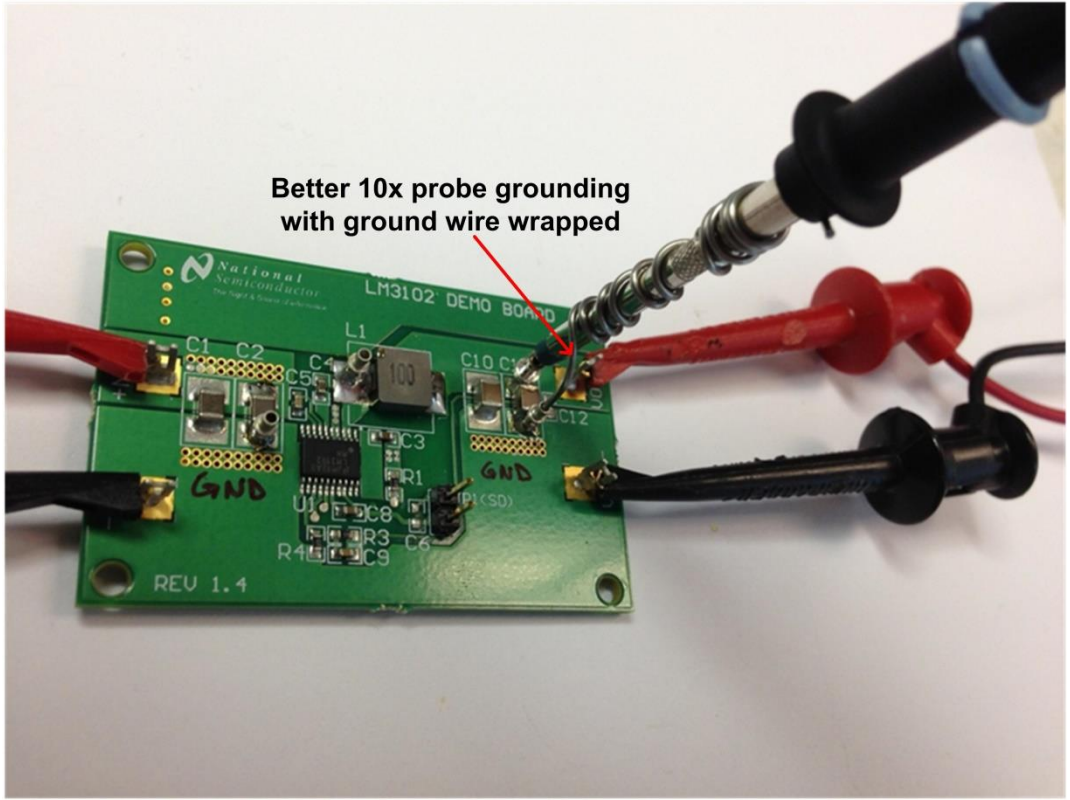
Measuring noise

- Before we explore ways/tools for reducing the output noise, let’s make sure we are measuring it properly.
- Improper measurement techniques can results in exaggerated output noise.
- Exaggerated output noise measurements can result in overly conservative “methods” for fixing it.
- It is important to know the “real” amount of noise before we start reducing it.

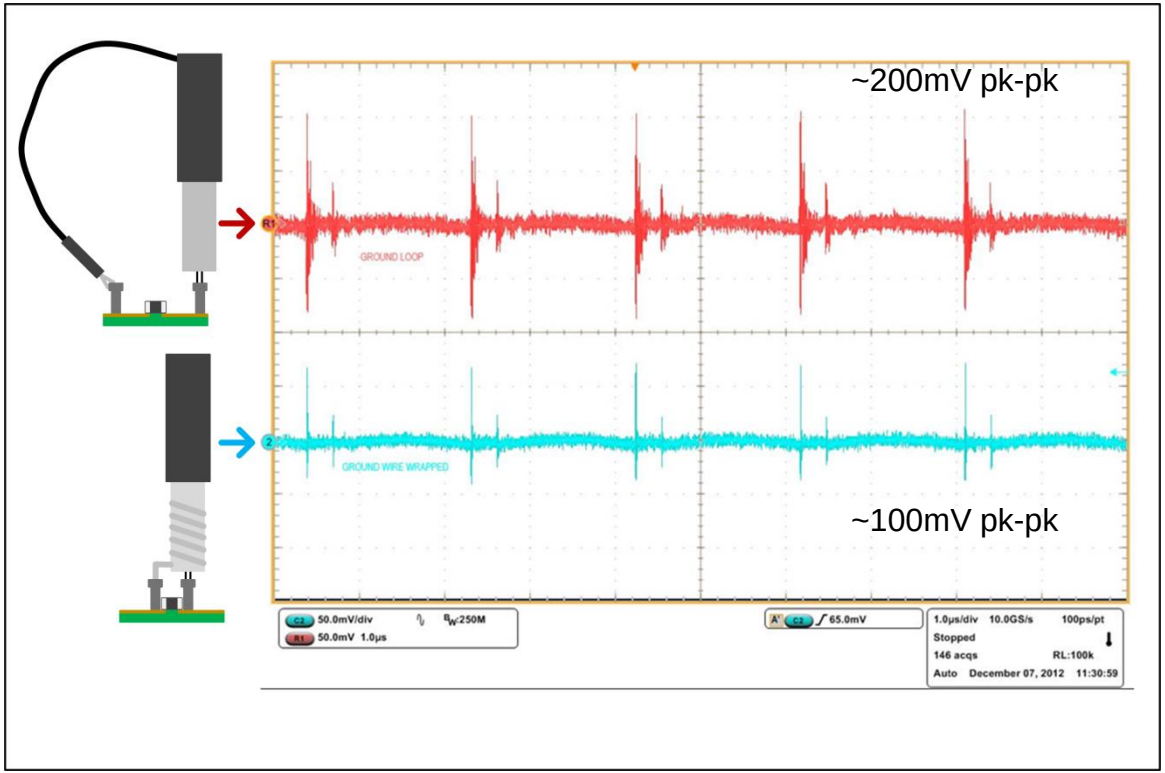
Bad measurement (example)



Improved measurement (example)



Measurement comparison

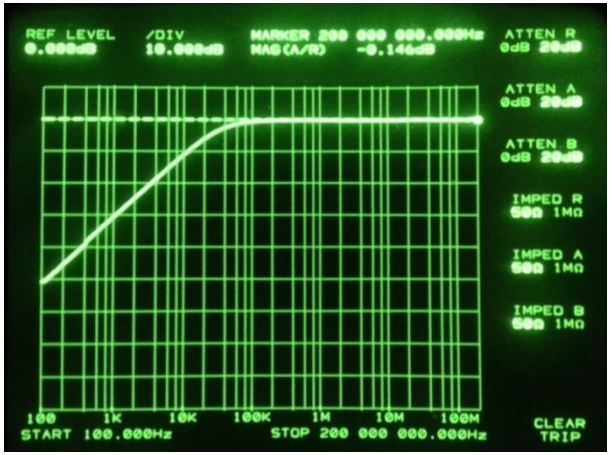


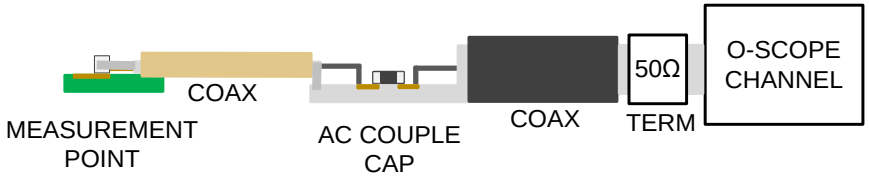
~2x difference in measured noise!

The circuit is exactly the same.
The difference is the measurement technique.

Making a 1x probe (example)

- Short coax cable soldered to the output
- 0.1µF coupling capacitor
- 50Ω termination





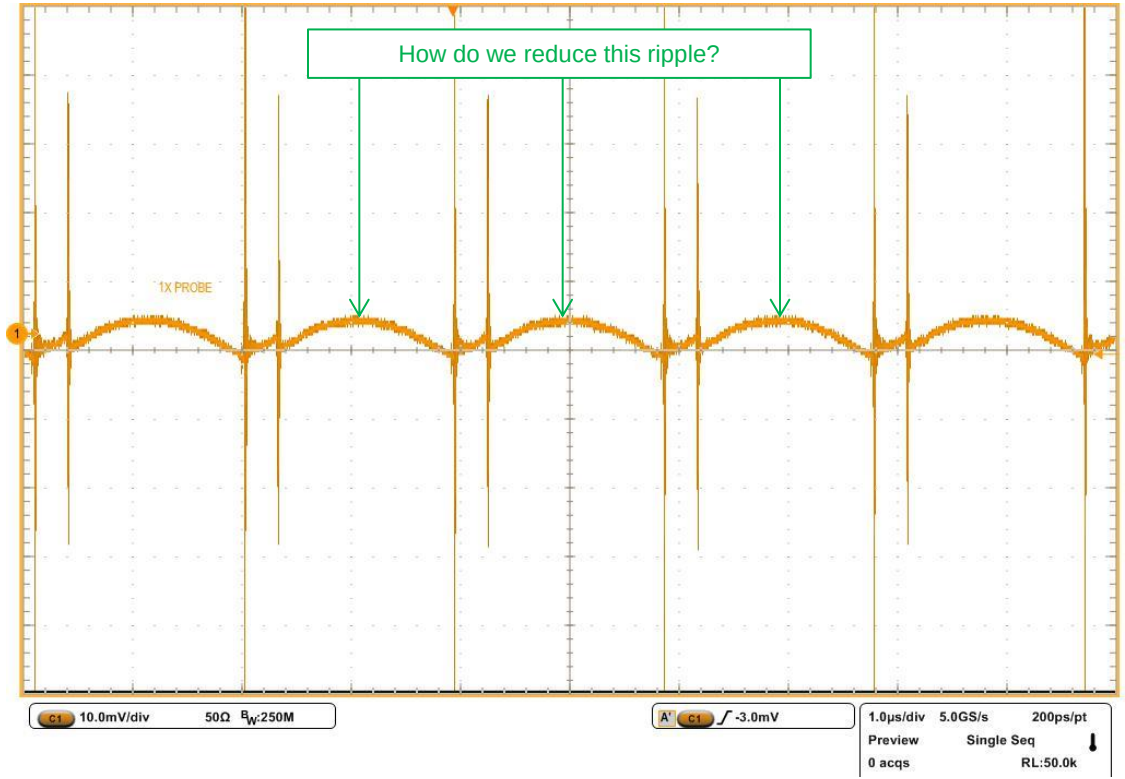
- Probe frequency response
- High pass filter with cutoff frequency at 31.8kHz. OK for most modern switchers with loaded output.
- Probe OK for 250MHz scope BW

Advantage of 1x probe

1x probe

10x probe

LF ripple reduction



LF ripple mitigation

- Inductor vs Switching Frequency
- Output capacitor

Inductor ripple current

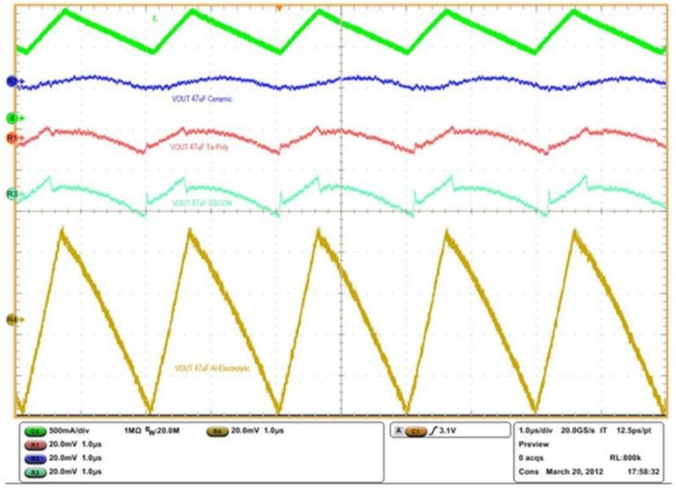
VOUT RIPPLE Ceramic cap (C dominated, low ESR low ESL)

VOUT RIPPLE Tantalum cap (medium ESR, some ESL)

VOUT RIPPLE OSCON cap (medium ESR, some more ESL)

VOUT RIPPLE Aluminum Electrolytic cap (ESR dominated)

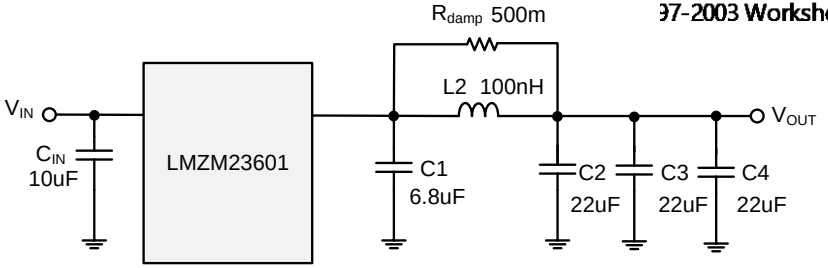
Each capacitor above is 47µF. The difference is the chemistry

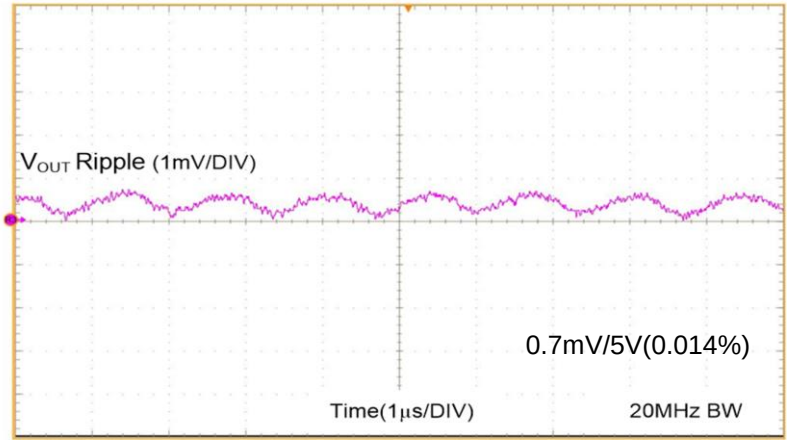


Filter Calculator with Equations

Microsoft Excel 97-2003 Worksheet

- Second stage filter





LF ripple mitigation and mixing capacitor types

Inductor ripple current

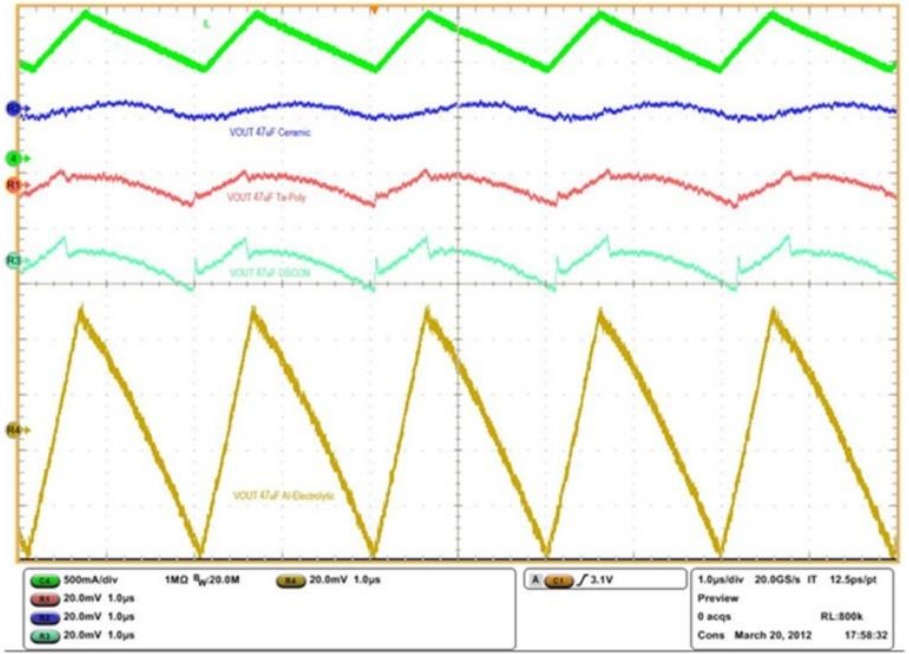
VOUT RIPPLE — Ceramic cap (C dominated, low ESR low ESL)

VOUT RIPPLE — Tantalum cap (medium ESR, some ESL)

VOUT RIPPLE — OSCON cap (medium ESR, some more ESL)

VOUT RIPPLE — Aluminum Electrolytic cap (ESR dominated)

Each capacitor above is 47µF.
The difference is the chemistry



Ceramic

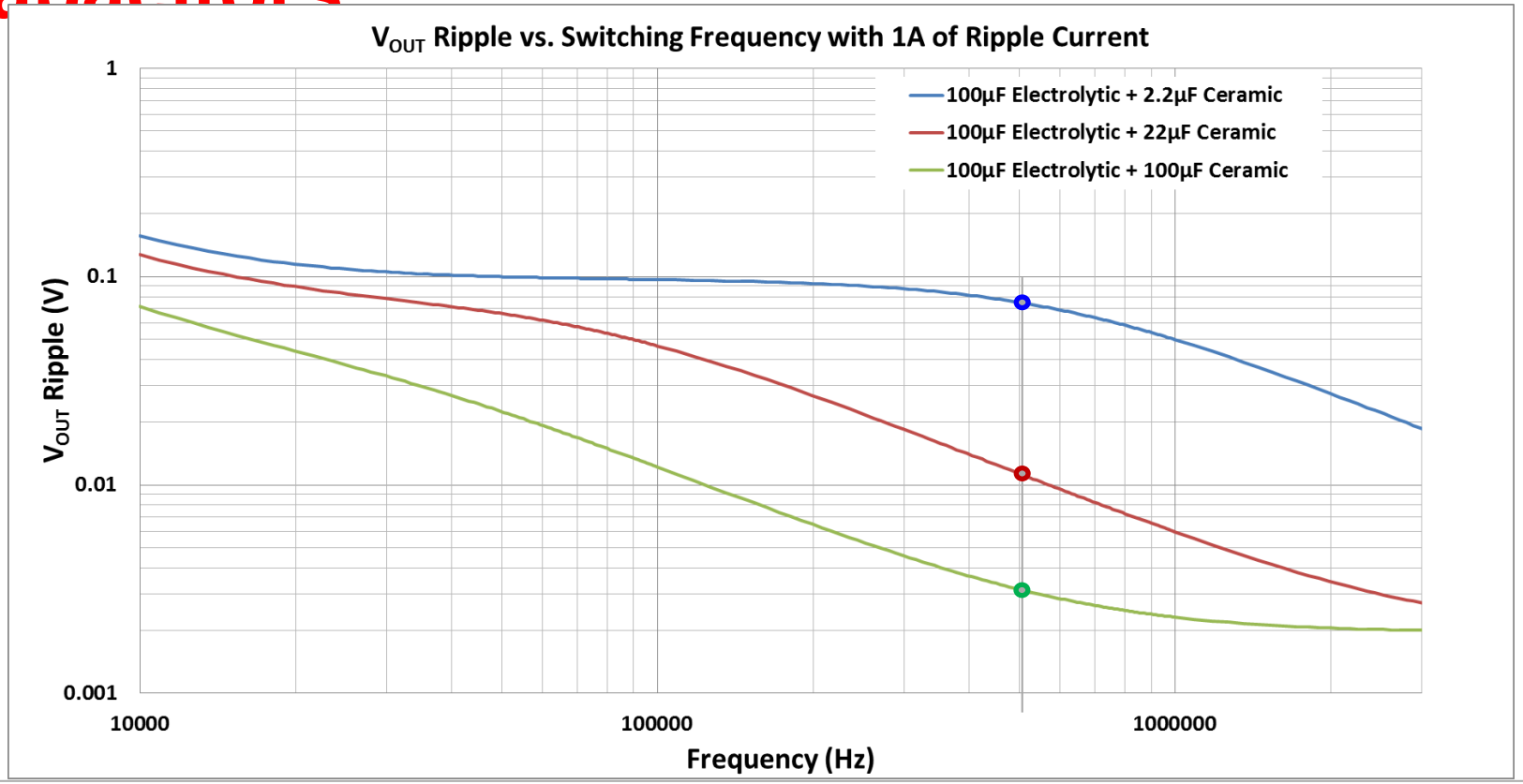
Tantalum

OSCON

Aluminum electrolytic

What if we parallel different types?

LF output voltage ripple with parallel capacitors

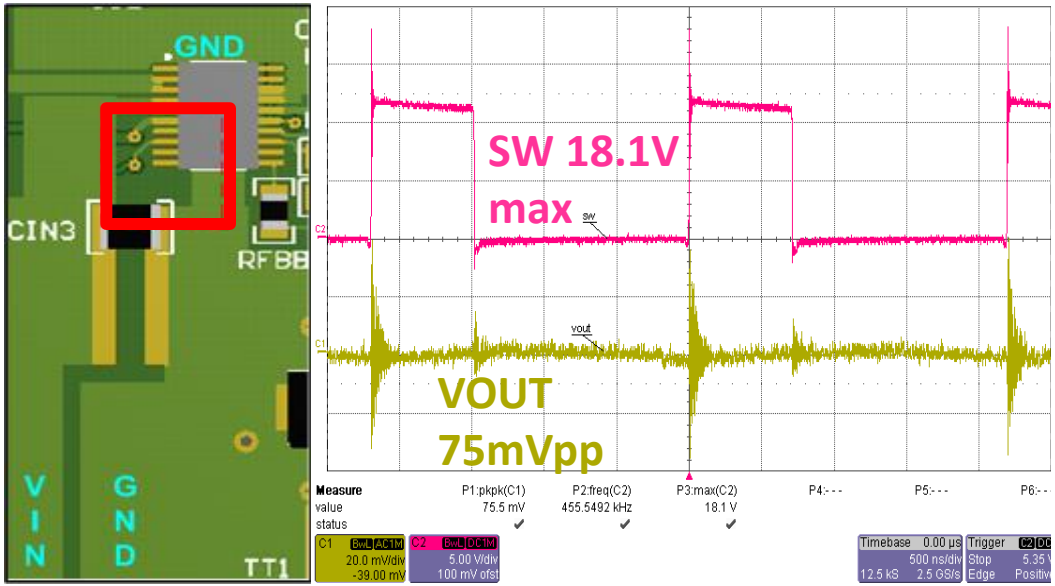


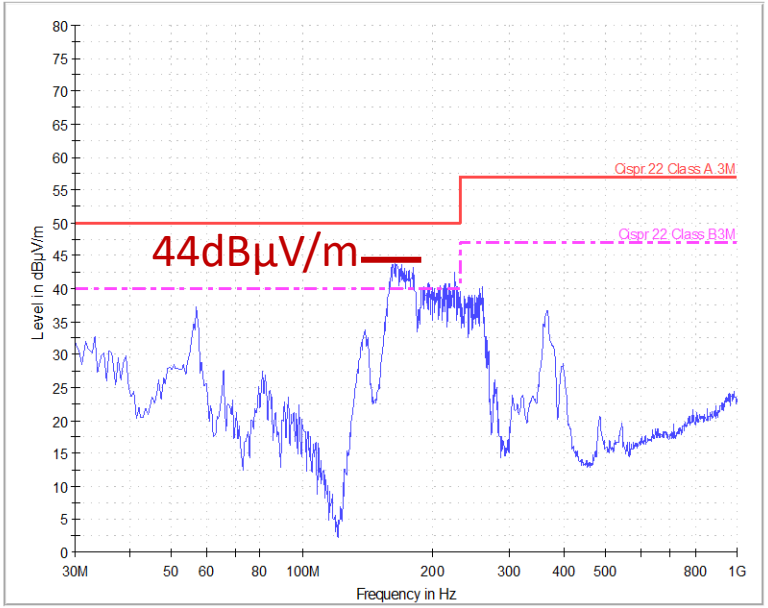
HF noise reduction – component placement

- First step is to optimize (minimize) the area of the high di/dt loop.
- For Buck, the high di/dt loop is formed by the input capacitor and the power MOSFETs (switches).
  - Input capacitor as close as possible to IC = Smaller loop area
  - Smaller loop area = Lower ringing on SW node
  - Lower ringing on SW node = Lower output noise
- So first step = optimize input capacitor placement for Buck

High di/dt capacitor placement - example

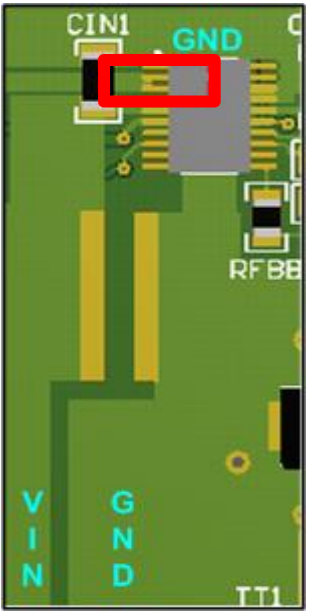
- Buck Regulator comparison with Cin location
- 12V input, 3.3V output, 2A Buck

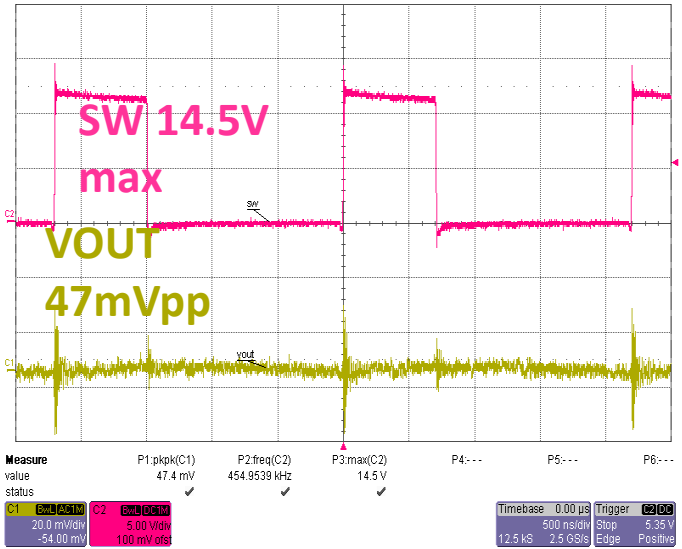


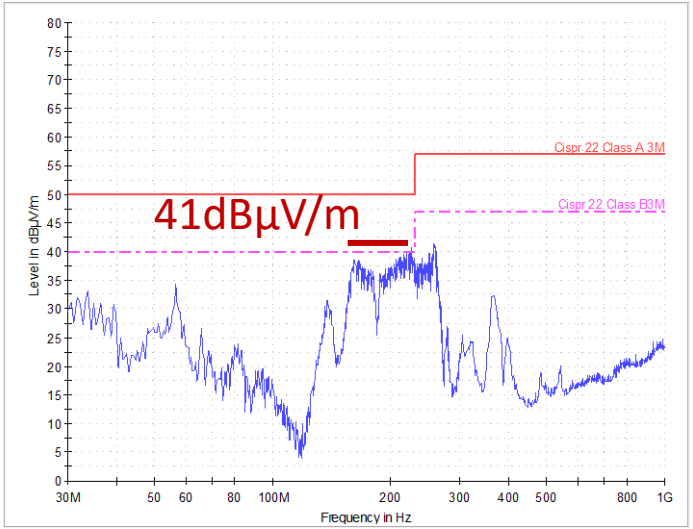


High di/dt capacitor placement - example

- Buck Regulator comparison with Cin location (2 times smaller loop area)
- 12V input, 3.3V output, 2A Buck



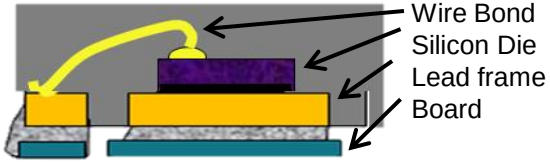




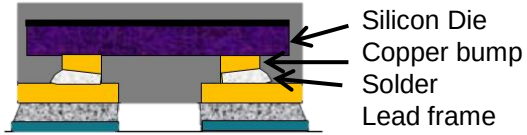
How IC package construction can help

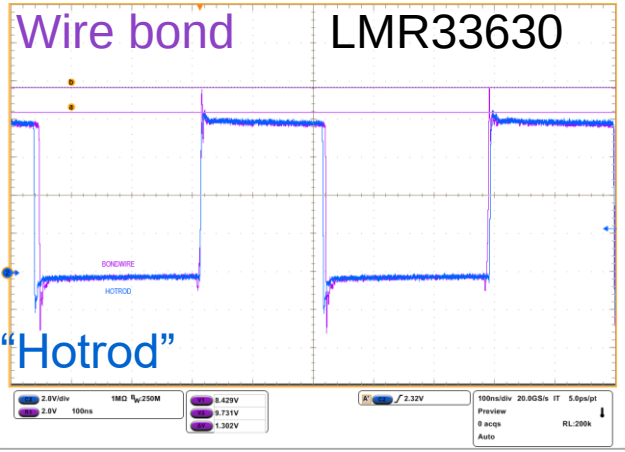
- Bond wire vs Copper pillar interconnects

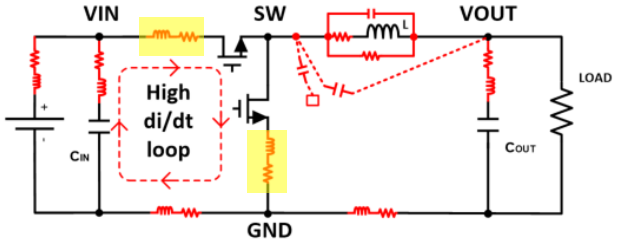
Standard wire bond QFN package



'Hotrod' flip chip on lead frame QFN

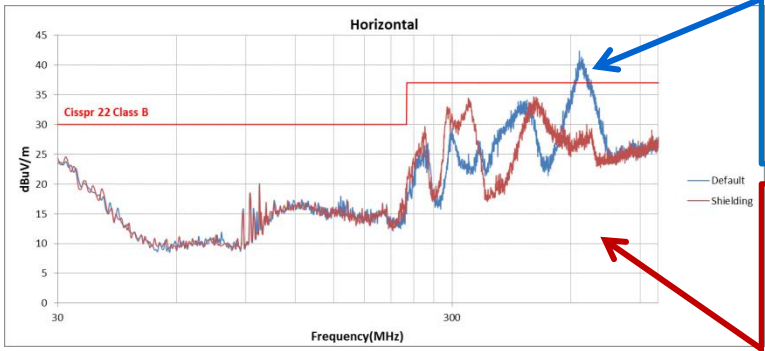


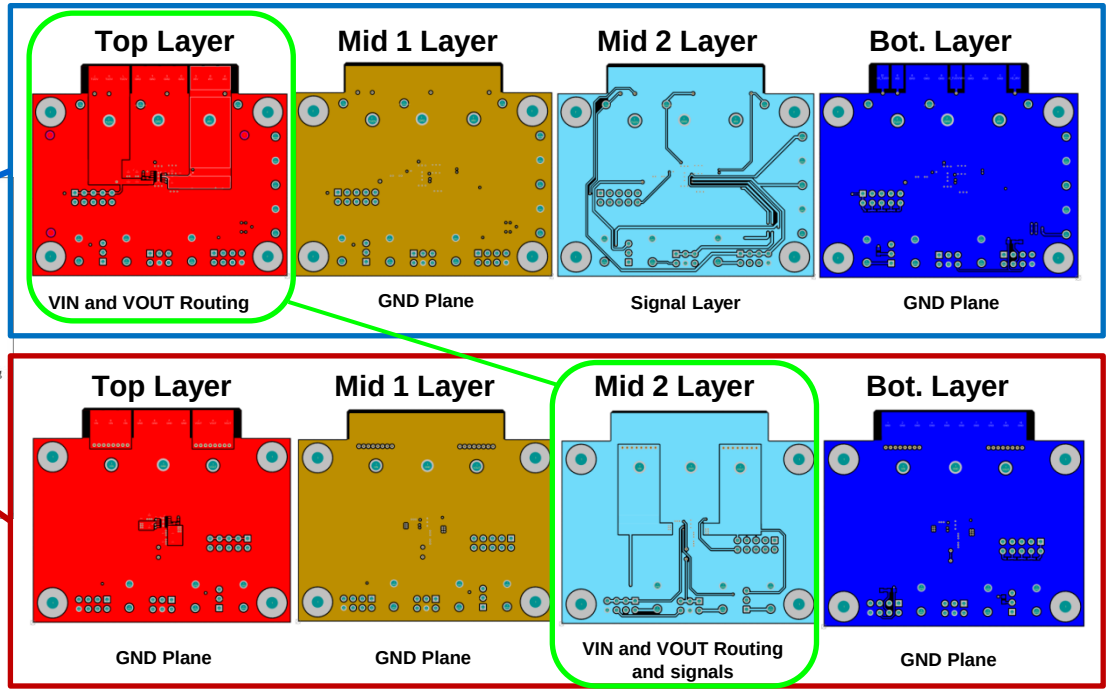




HF noise reduction – board layout tricks

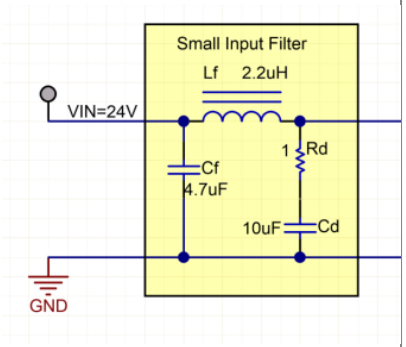
Shielding



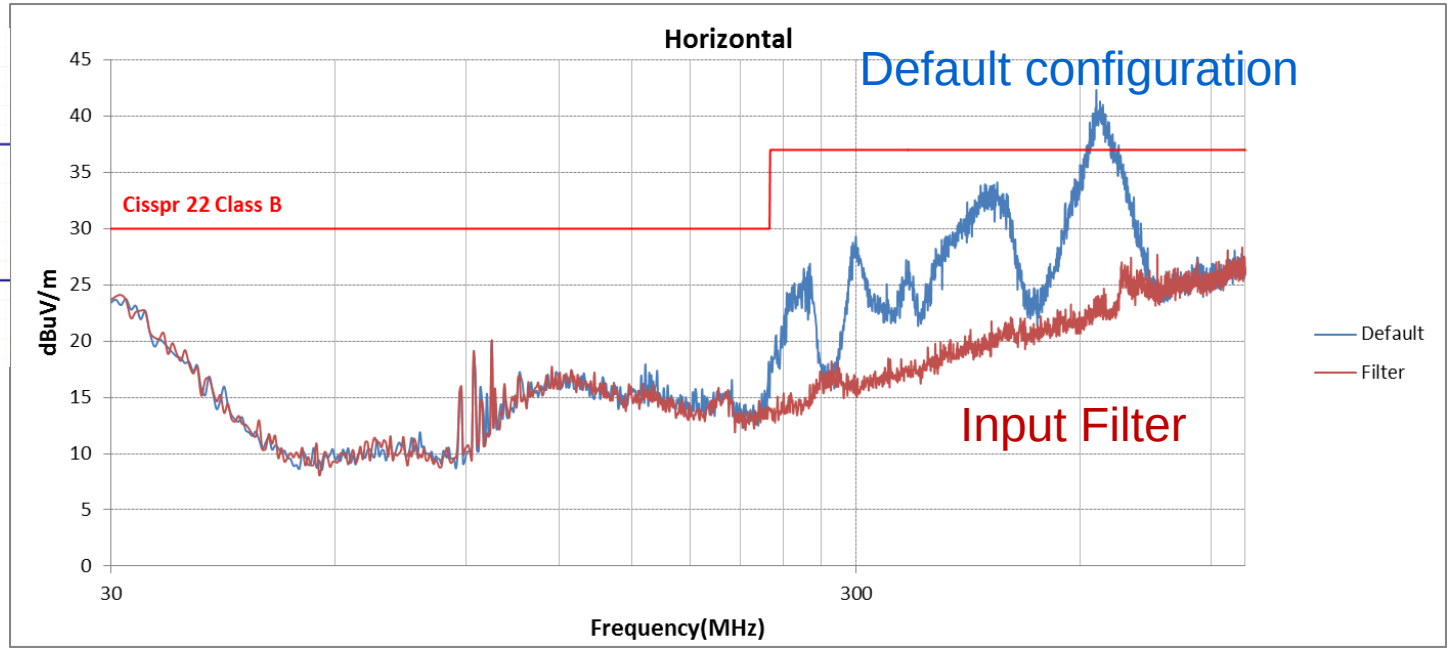


- Same BOM!
- Different stackup
  - Shielding the input (noisy) and output lines
  - Fail by ~5dB vs Pass by ~2dB

Conducted EMI filter and radiated EMI performance

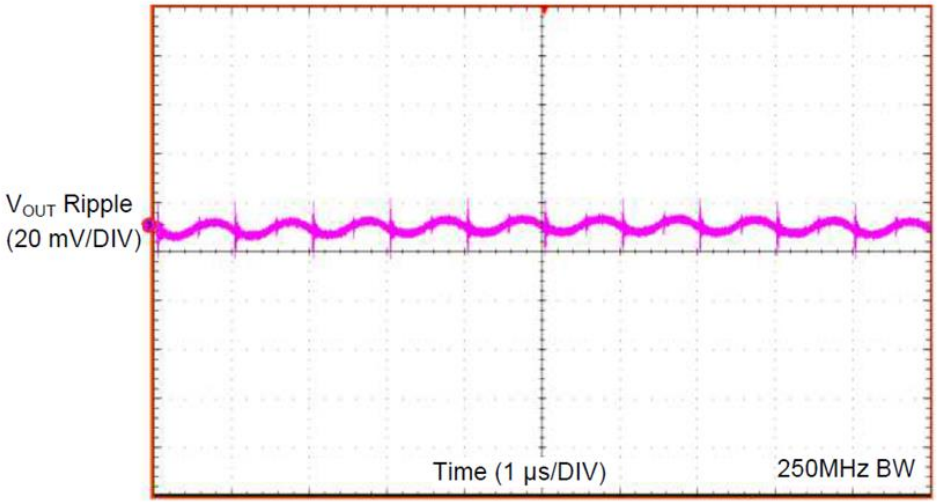


Calculator

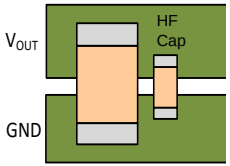


HF filtering

- After careful input capacitor placement and layout there will be some left over high frequency noise – we cannot completely eliminate parasitic L and C.

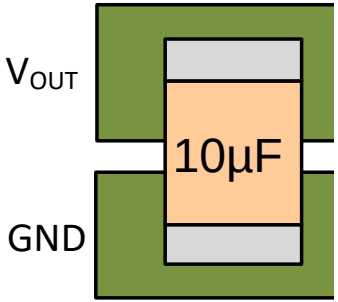


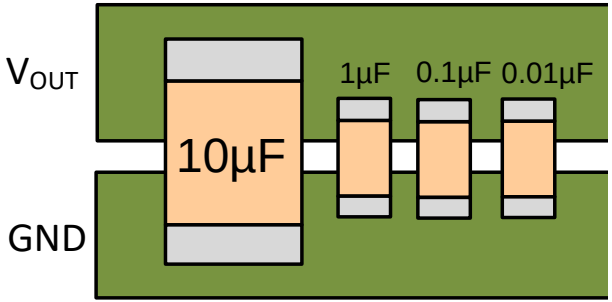
How can we reduce it?

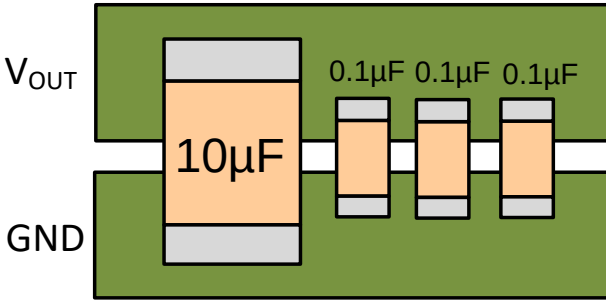


HF filtering – parasitic component and pitfalls

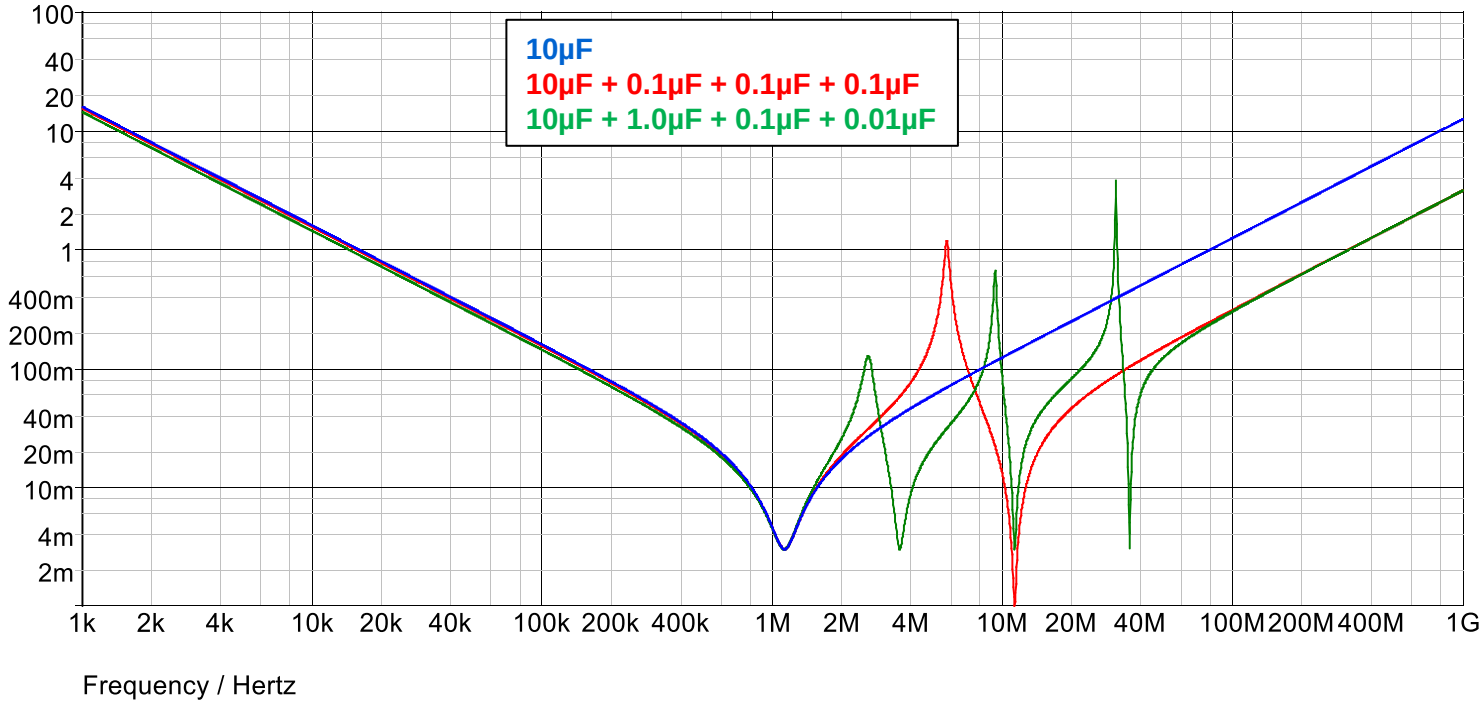
- Which one is better?



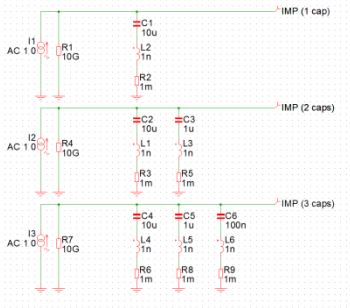




HF filtering – parasitic component and pitfalls

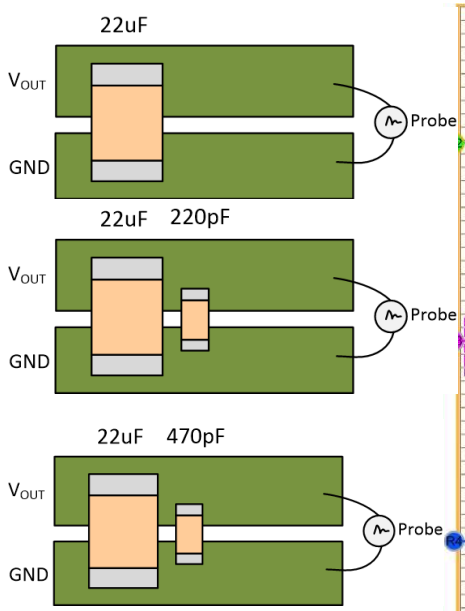


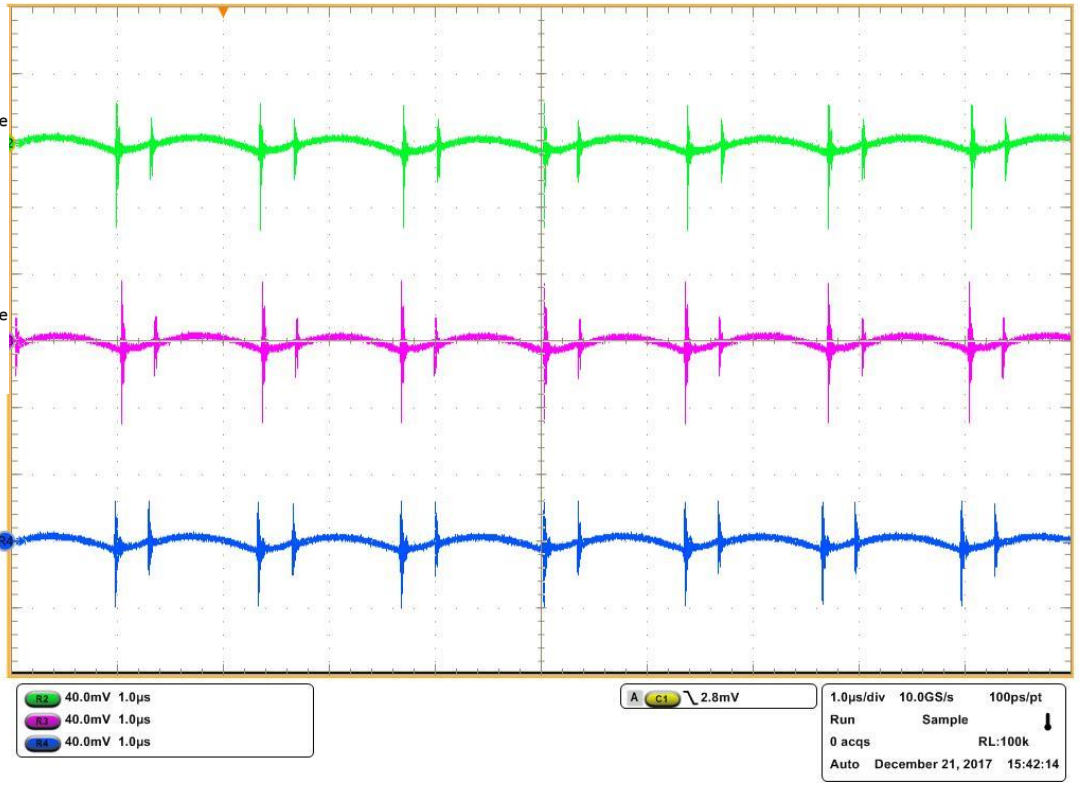
SIMetrix schematic example:



parallel_capacitor_impedance.sxsch

HF filtering with wrong capacitor (example)





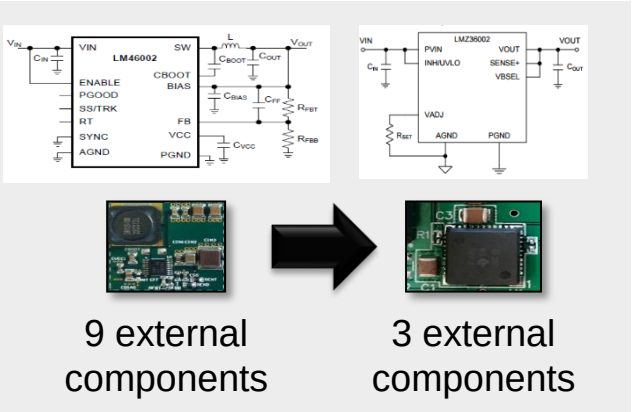
76.2mV

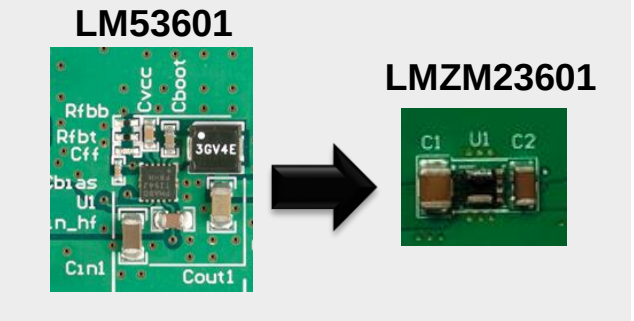
85.7mV

64.4mV

What are power modules?

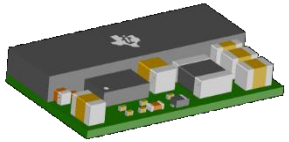
- DC/DC converter that integrates: controller, power MOSFETs and power inductor into single package
- Simplifies and reducing customer's BOM

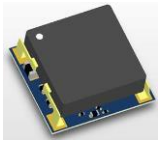




Power modules simplify design

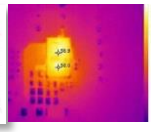
Small Solution Size

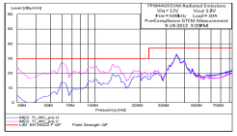


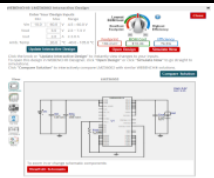


- ✓ Smaller solution size vs discrete
- ✓ Minimal external components
- ✓ Inductors over active components

Easy to Use

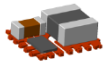


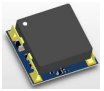




- ✓ Simple Design
- ✓ Best in Class Thermals
- ✓ Reliability Data
- ✓ Meet EN55022 Class B Emissions
- ✓ Design Tools

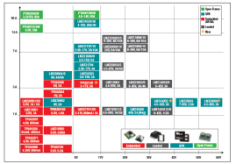
Range of Package Options





- ✓ Package option matched to IC and application
- ✓ Range of surface mount, leaded and through-hole options
- ✓ Pin-Pin Compatible Options

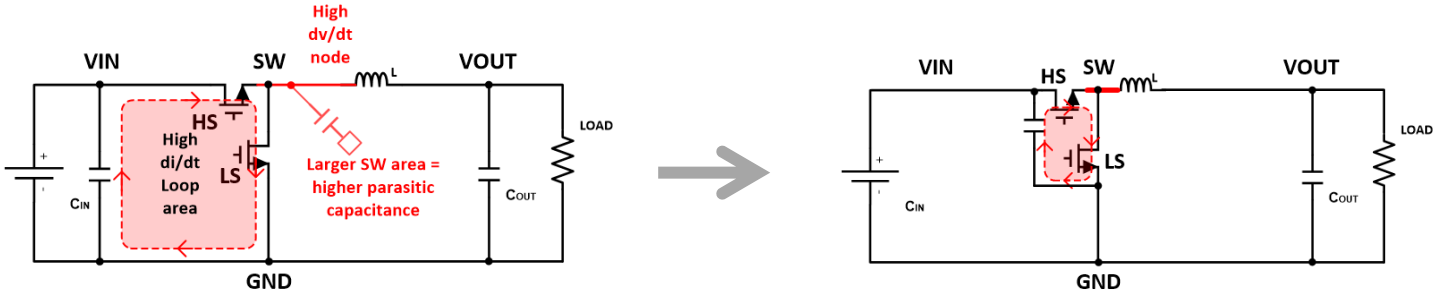
Broad Portfolio



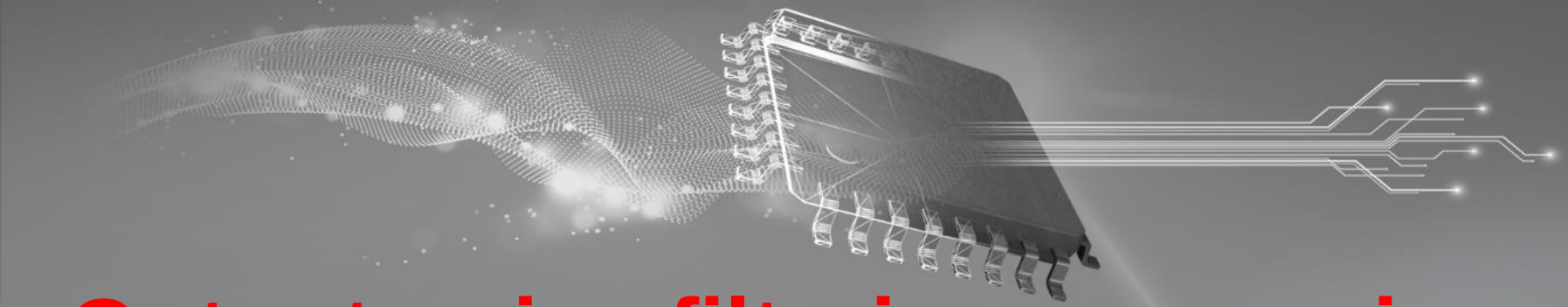
- ✓ Input Voltages from 2.2V up to 60V
- ✓ Output Currents up to 70A
- ✓ Stackable options for reduced noise and high Iout

HF noise reduction – DC/DC power modules save layout troubles

- Reducing the high di/dt loop area – integrated input capacitance.
- Reducing the high dv/dt node area – integrated L and smaller switch node.
- Discrete solution without optimized layout -> DC-DC Power Module



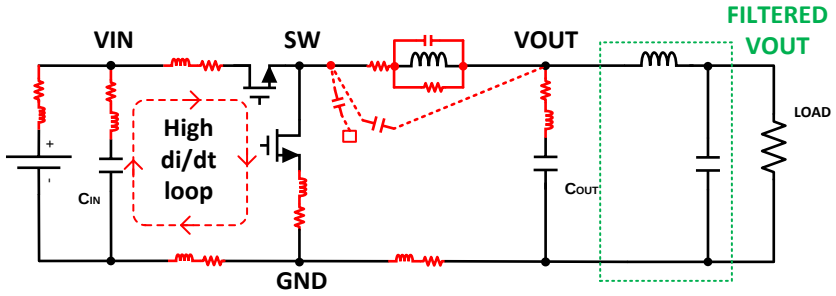
TI TECH DAYS

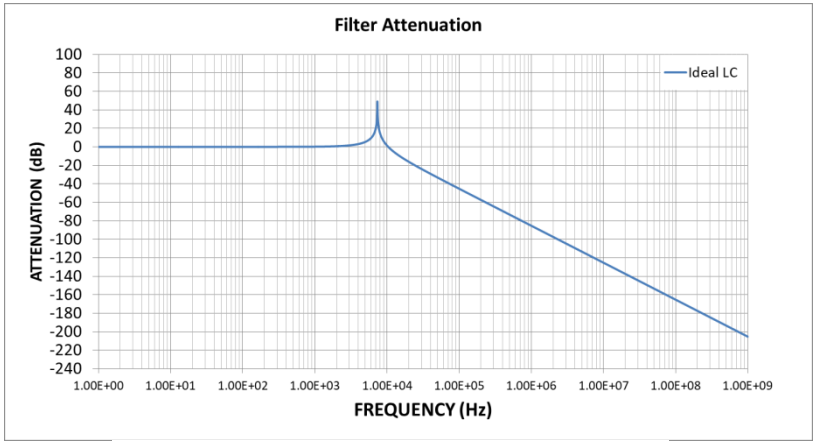


Output noise filtering comparison

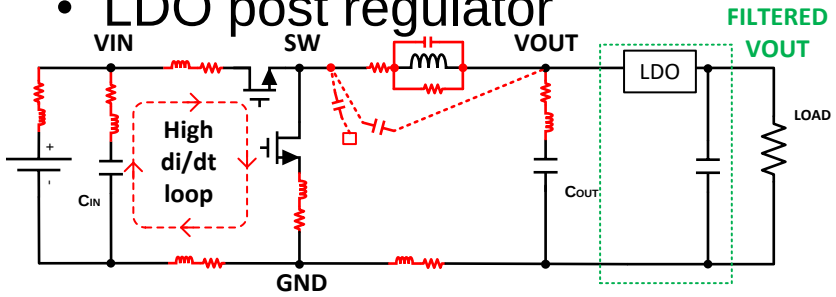
Filtering techniques comparison

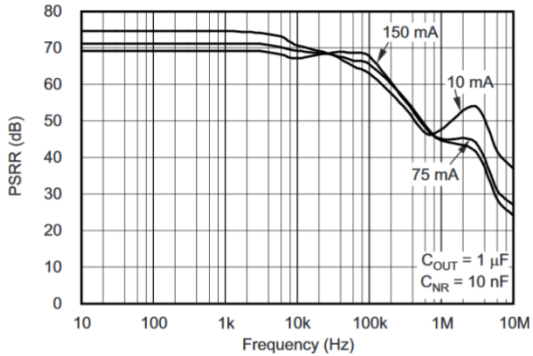
- 2nd stage filter (L-C)





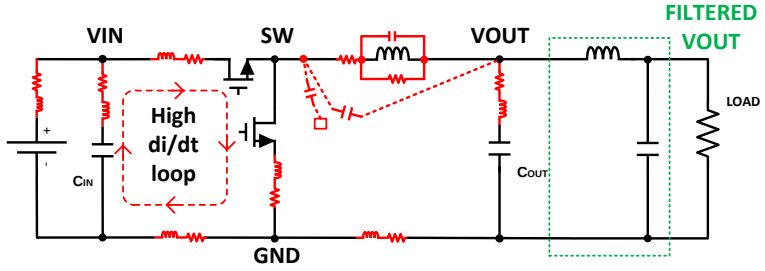
- LDO post regulator



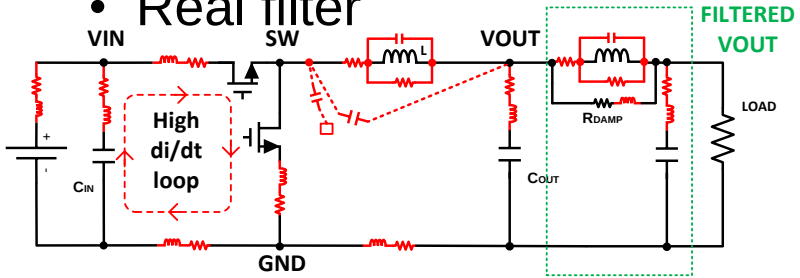


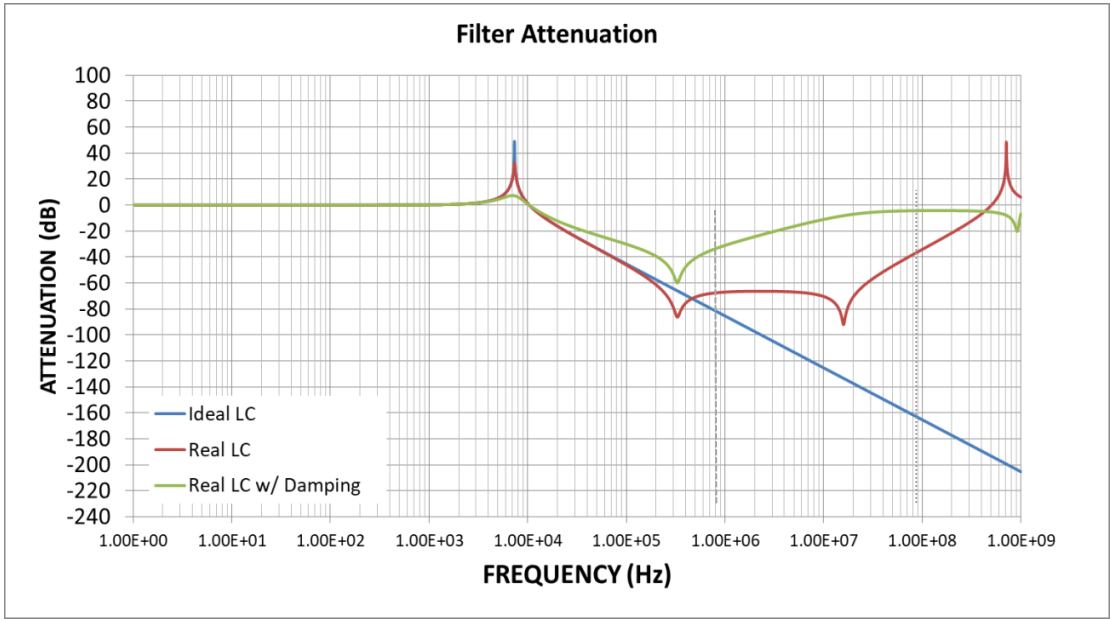
2nd stage filter tradeoffs

- Ideal filter

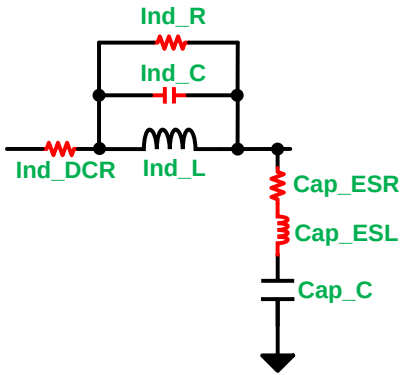


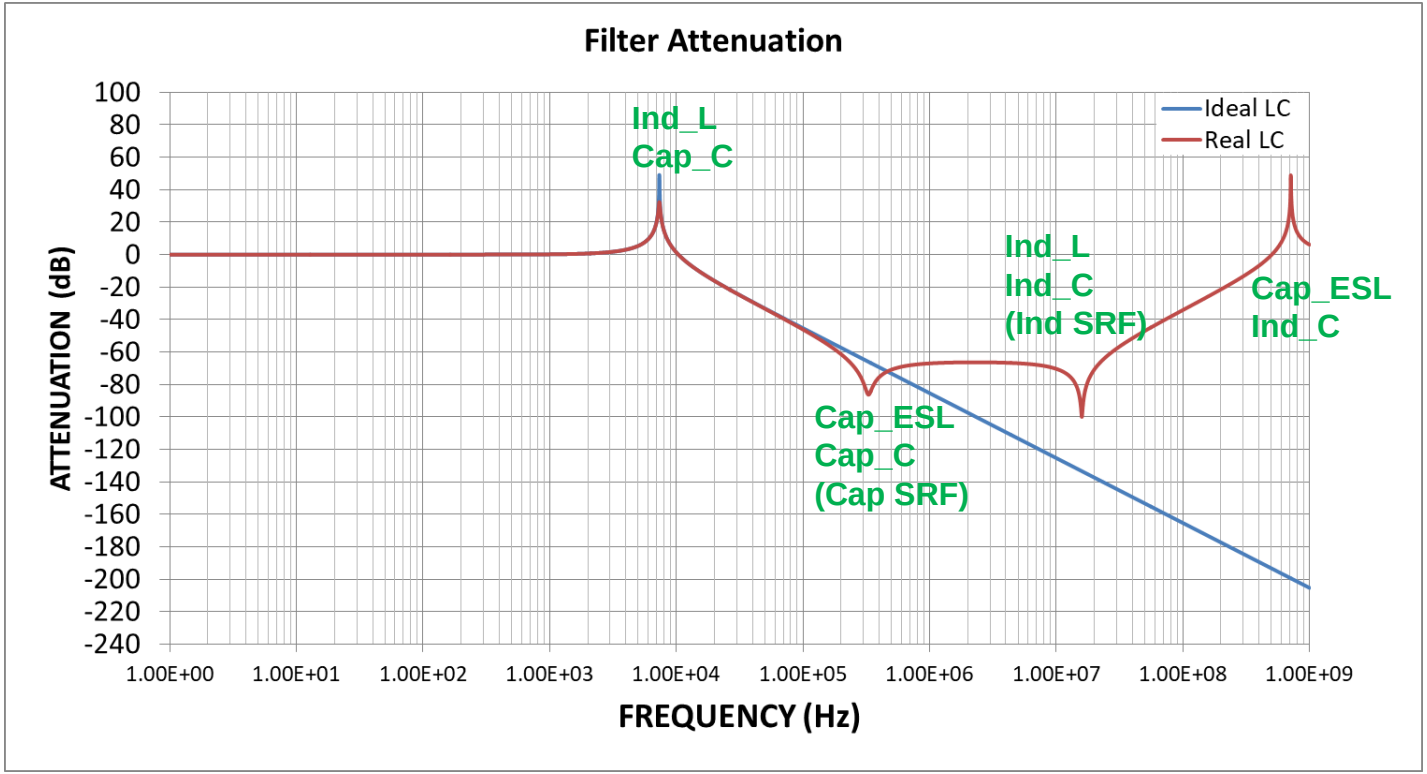
- Real filter





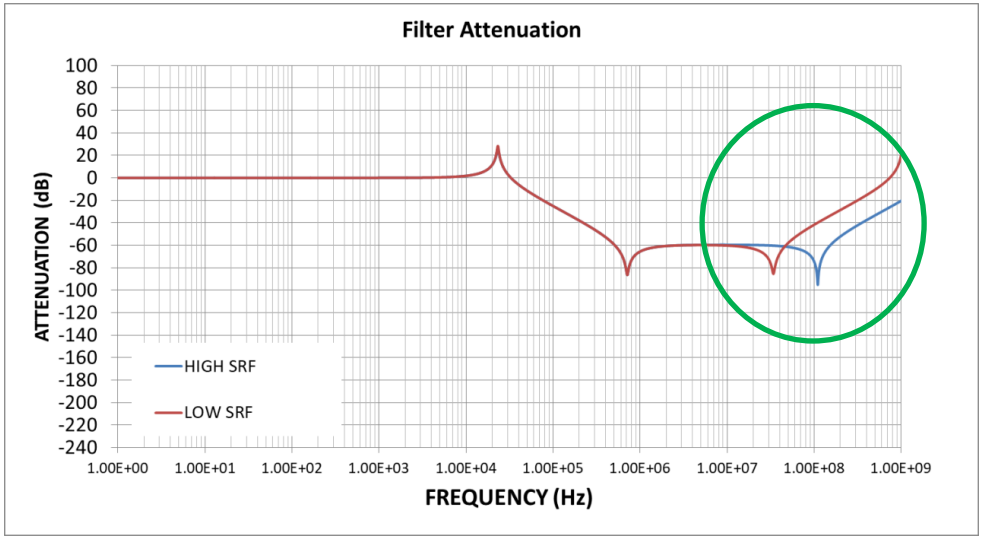
2nd stage filter parasitic elements





Inductor tradeoffs: high frequency filtering and SRF

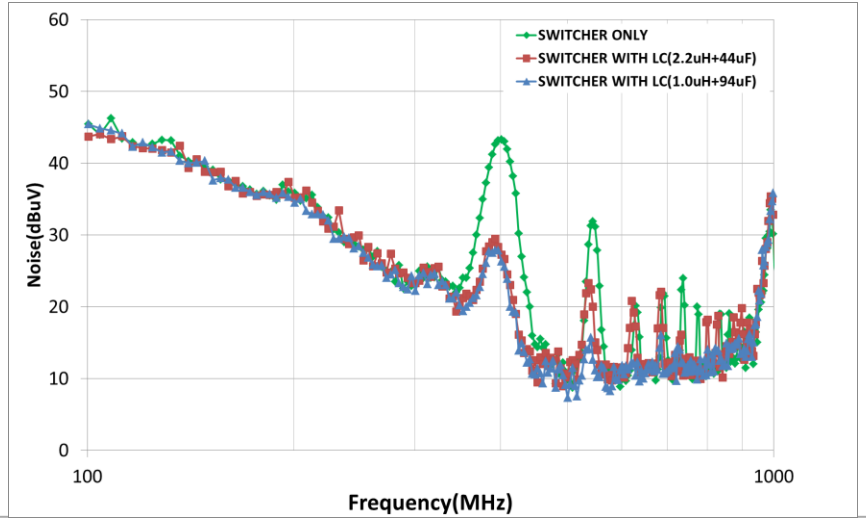
- High frequency filtering
  - The SRF of the inductor can affect the L-C filter performance at high frequency.
  - May be better to choose smaller L and larger C if HF attenuation is desired.



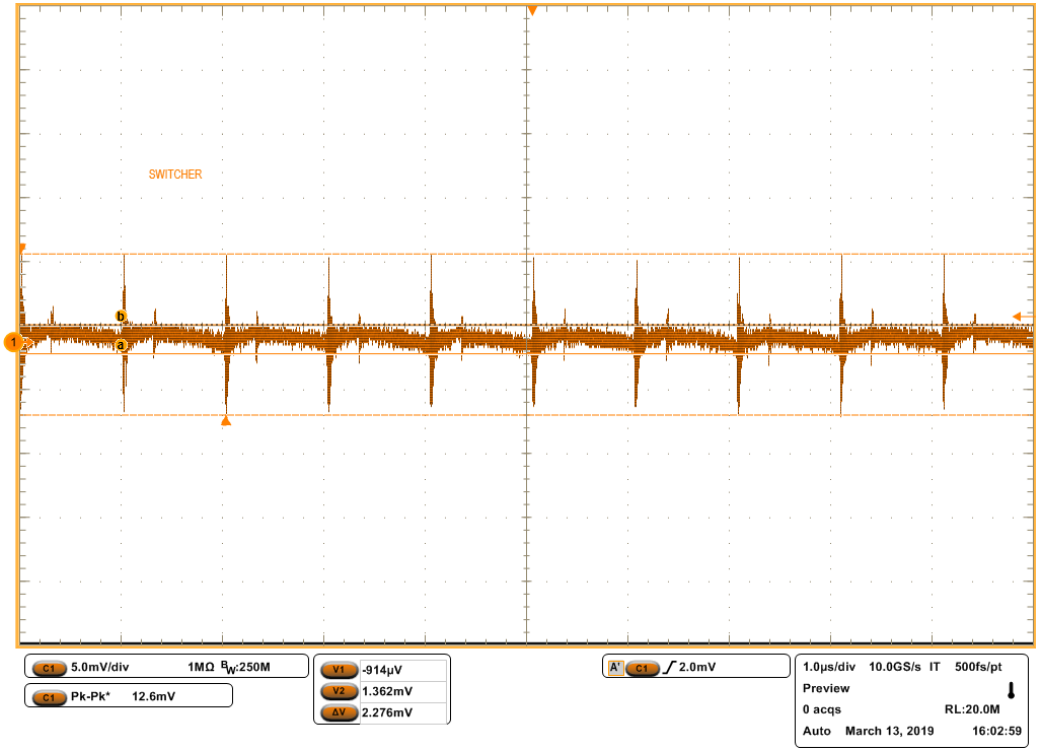
Part number[1] Click to get parts	Inductance[2] ±20% (µH)	DCR (mOhms)[3] typ	DCR (mOhms)[3] max	SRF typ[4] (MHz)
XFL4030-471ME_	0.47	3.6	4.4	110
XFL4030-102ME_	1.0	5.5	6.6	67
XFL4030-202ME_	2.0	9.5	11.5	46
XFL4030-302ME	3.0	17.0	20.5	39
XFL4030-472ME_	4.7	25.0	30.0	34

Inductor tradeoffs: high frequency filtering and SRF – example in frequency domain

- High frequency filtering
  - The SRF of the inductor can affect the L-C filter performance at high frequency.
  - May be better to choose smaller L and larger C if HF attenuation is desired.



Example with 2nd stage filter with LMZM23601EVM

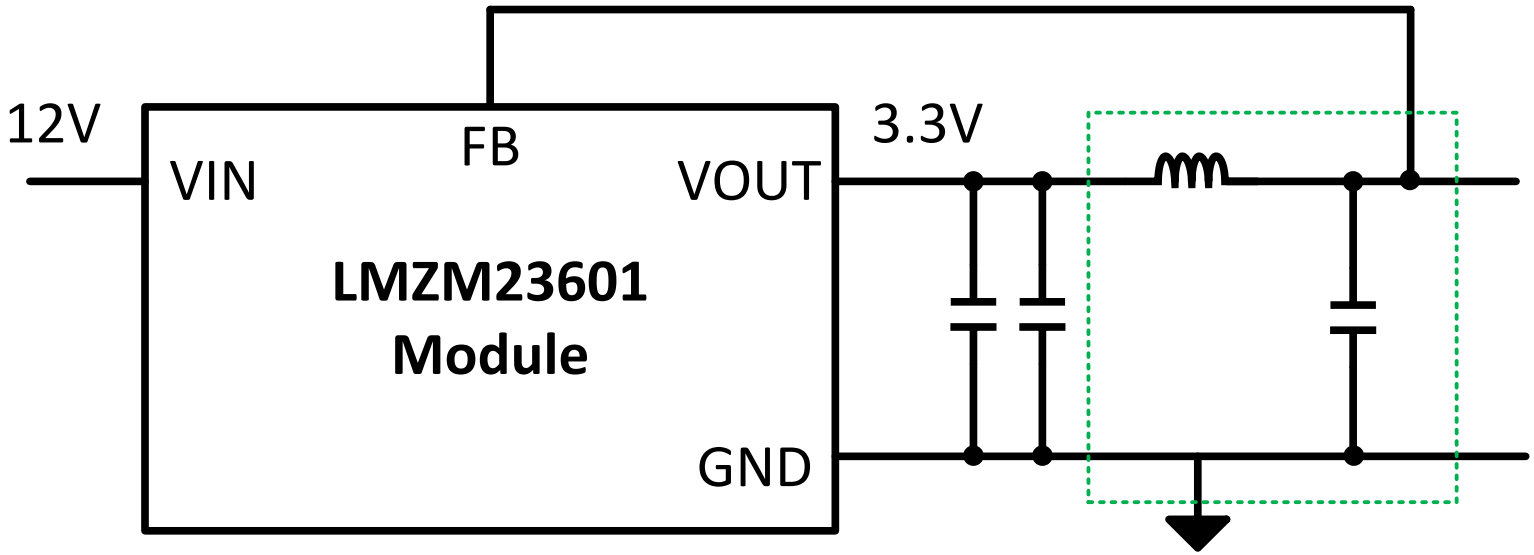


Conditions:

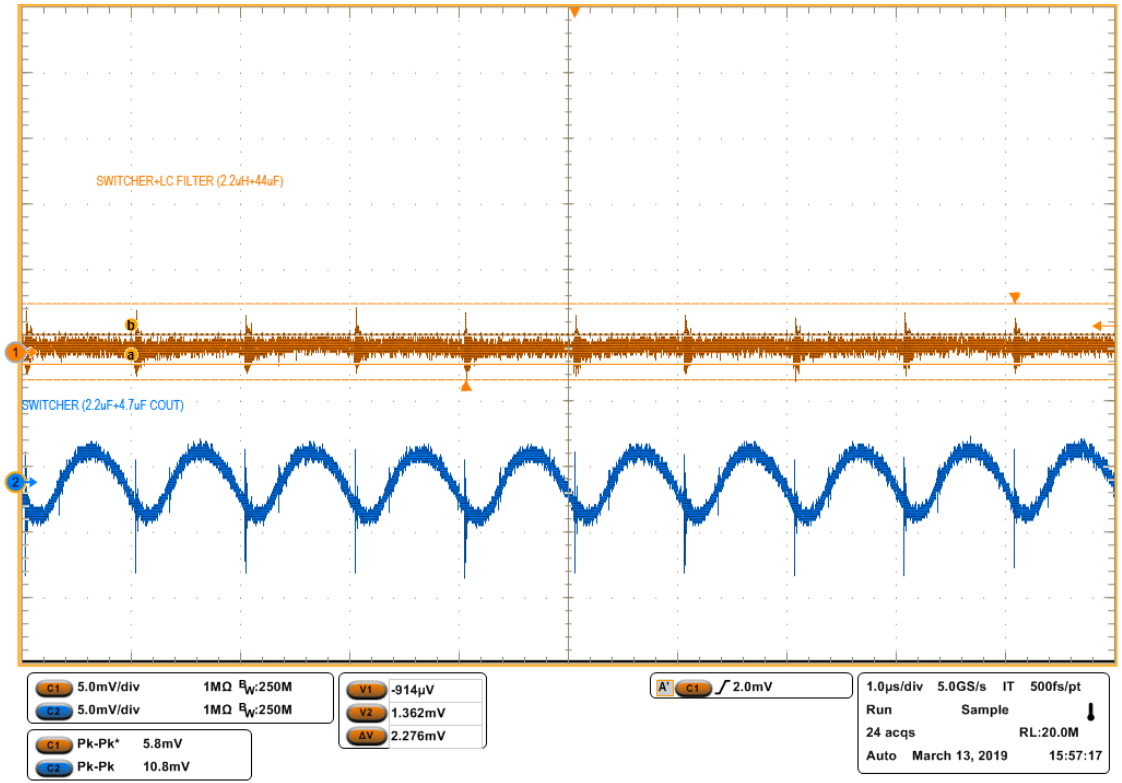
- Vin =12V
- Vout = 3.3V
- Iout = 500mA
- 1X Scope probe
- BW set to 250MHz

HF noise peak-to-peak = 12.6mV

2nd stage output filter schematic



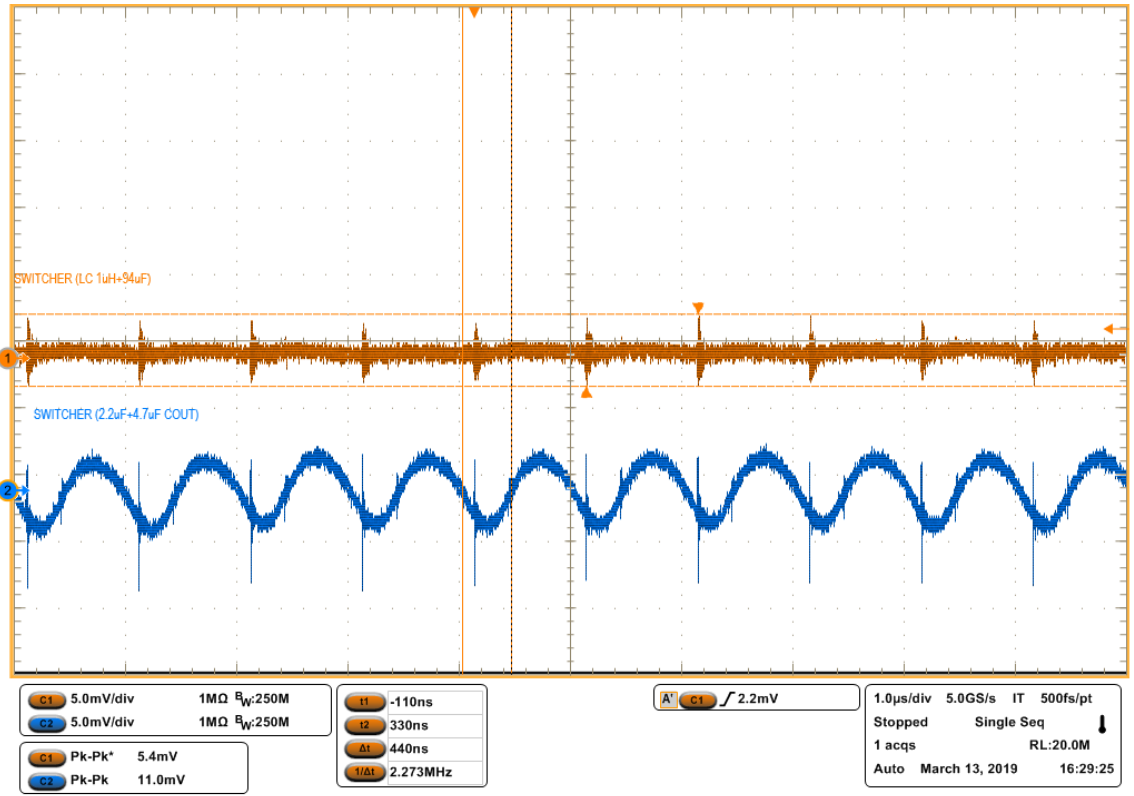
Initial filter design (2.2uH + 44uF)



HF noise = 5.8mV

Calculated HF attenuation = 6.7dB

Another filter design (1uH + 94uF)

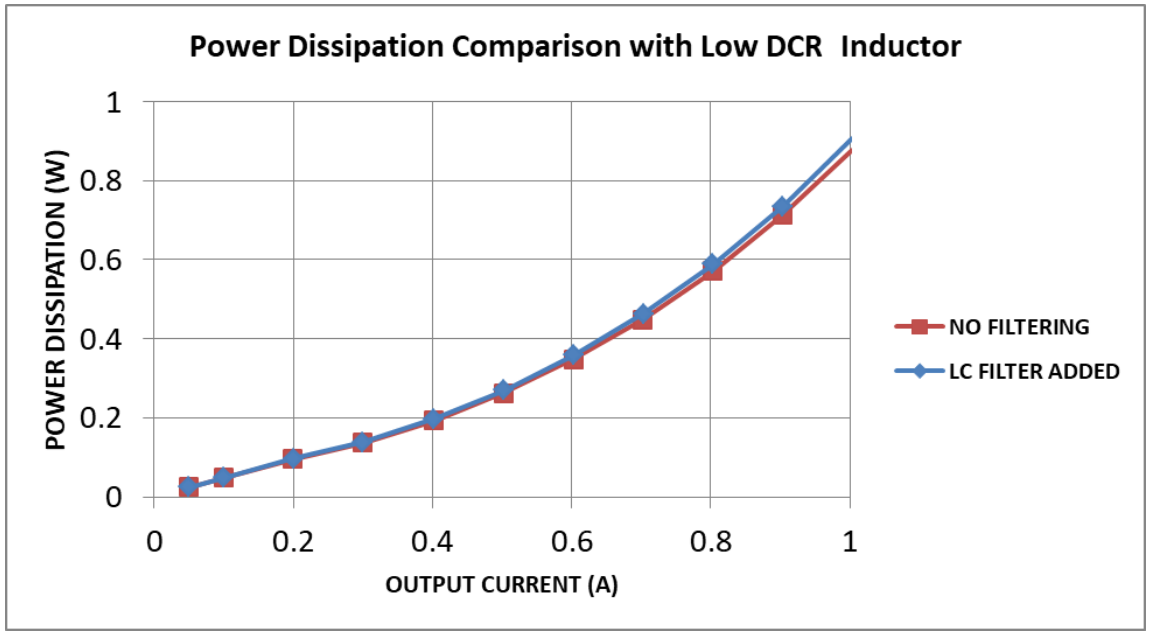


HF noise = 5.4mV

Calculated HF attenuation = 7.7dB

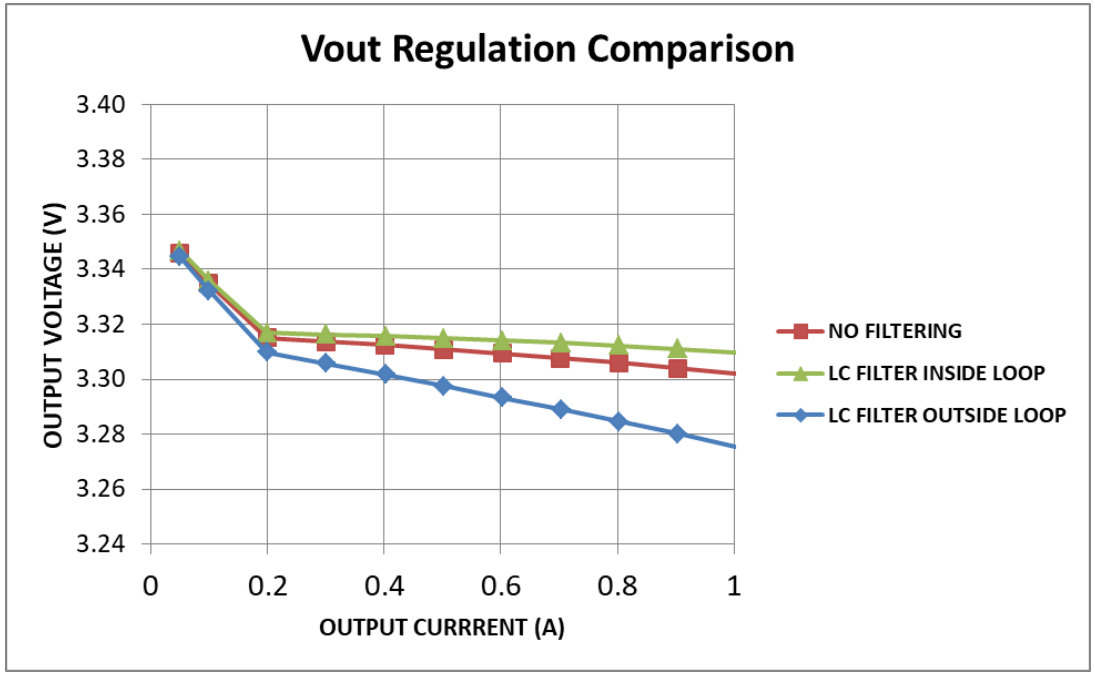
2nd stage filter tradeoffs (efficiency)

- Power dissipation penalty depends on the DCR of the inductor and the load current



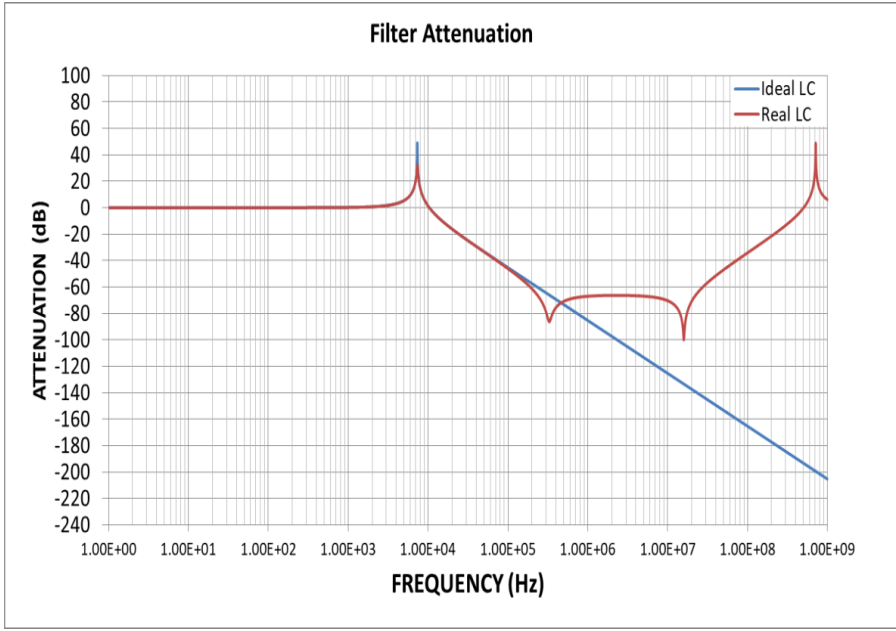
2nd stage filter tradeoffs (load regulation)

- Depends on whether the 2nd stage filter is inside the feedback loop



2nd stage filter tradeoffs (LF attenuation at light load)

- LC filter is chosen to attenuate ripple at the switching frequency.
- Many switchers employ power savings mode at light load.
- At low frequencies below the LC filter cutoff, the LF ripple may pass through at light loads
- If attenuation is needed at light load, the LC filter must be oversized to capture the light load frequency.

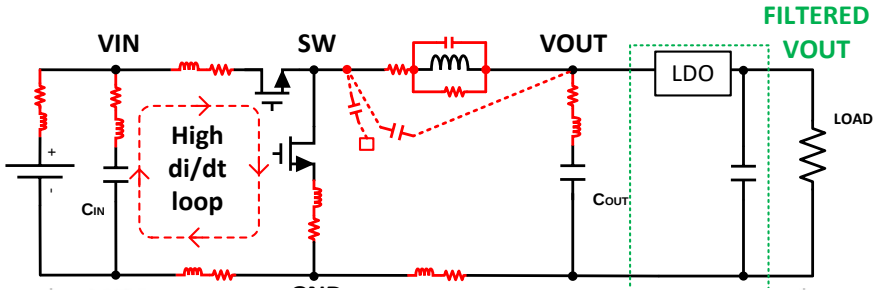


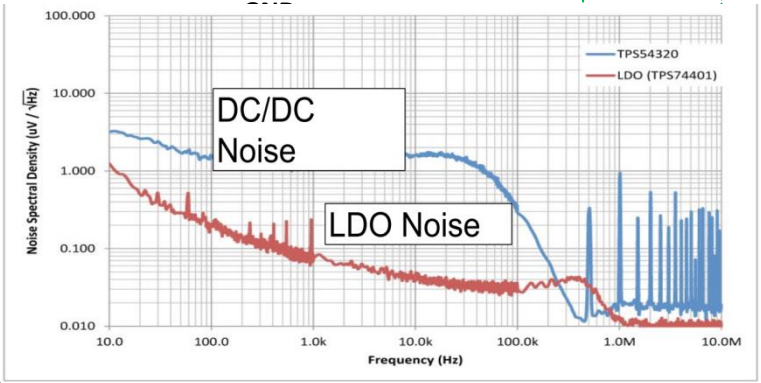
2nd stage LC filter key takeaways

- 2nd stage filter can help reduce both LF ripple and HF switching noise
- Using the power savings mode feature at light load and lower switching frequency may require LC filter readjustment
- HF switching noise reduction highly depends on the filter parasitics
  - Simulate and optimize filter design at HF ringing frequency
- If LC filter is inside the FB loop
  - Regulation penalty is avoided
  - May need damping to avoid regulator stability issues
  - Damping will affect the filter attenuation at HF so HF switching reduction may be affected

LDO as a filter

- Many low-noise applications utilize the PSRR (power supply rejection ratio) of the LDO to “clean the supply”.

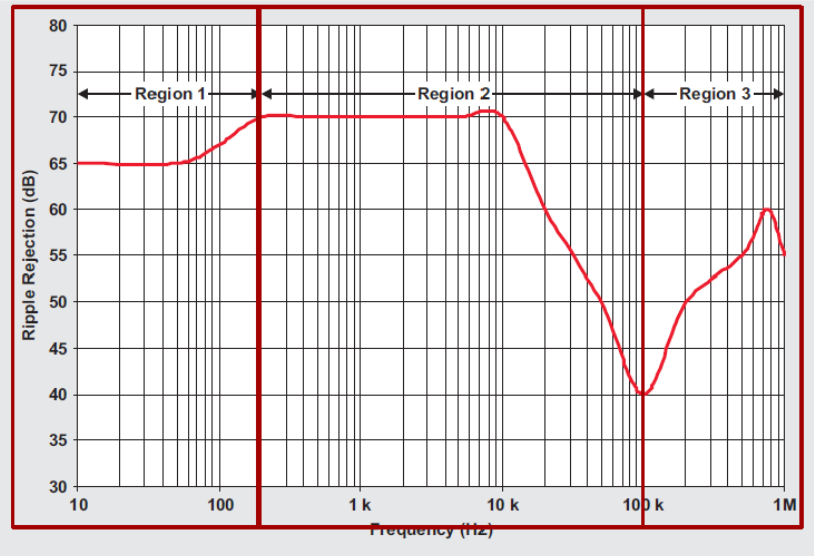




Source: You Think LDOs are Simple?
https://training.ti.com/sites/default/files/docs/you_think_ldos_are_easy-detroit_tech_day.pdf

PSRR curve details

- Region 1 depends on:
  - Internal reference and internal filtering
- Region 2 depends on:
  - Open-loop gain of the LDO error amp
- Region 3 depends on:
  - Parasitic capacitance across the pass device and the LDO output cap size



Source: You Think LDOs are Simple?
https://training.ti.com/sites/default/files/docs/you_think_ldos_are_easy-detroit_tech_day

LDO as a filter for LMZM23601

- **LMZM23601 is a 36V 1A power module**

TEXAS INSTRUMENTS

LMZM23601

SNVSAQ4A – DECEMBER 2017 – REVISED APRIL 2018

LMZM23601 36-V, 1-A Step-Down DC/DC Power Module in 3.8-mm × 3-mm Package

1 Features

- 4-V to 36-V Wide Operating Input Voltage
- 2.5-V to 15-V Adjustable, and 3.3-V or 5-V Fixed Output Voltage Options
- 1-A Output Current
- Only Input and Output Capacitors Needed for 5-V and 3.3-V Output Designs
- 27-mm^2 Solution Size With Single-Sided Layout
- 28-µA Supply Current at No Load
- 2-µA Shutdown Current
- Power-Good Flag
- External Frequency Synchronization
- MODE Selection Pin
  - Forced PWM Mode for Constant Frequency Operation
  - Auto PFM Mode for High Efficiency at Light Load
- Built-in Control Loop Compensation, Soft Start, Current Limit, and UVLO
- Miniature 3.8-mm × 3-mm × 1.6-mm Package

3 Description

The LMZM23601 integrated-inductor power module is specifically designed for space-constrained industrial applications. It is available in two fixed output voltage options of 5-V and 3.3-V, and an adjustable (ADJ) output voltage option supporting a 2.5-V to 15-V range. The LMZM23601 has an input voltage range of 4-V to 36-V and can deliver up to 1000-mA of output current. This power module is extremely easy to use, requiring only 2 external components for a 5-V or 3.3-V output design. All aspects of the LMZM23601 are optimized for performance driven and low EMI industrial applications with space-constrained needs. An open-drain, Power-Good output provides a true indication of the system status and negates the requirement for an additional supervisory component, saving cost and board space. Seamless transition between PWM and PFM modes along with a no-load supply current of only 28 µA ensures high efficiency and superior transient response for the entire load-current range. For easy output current scaling the LMZM23601 is pin-to-pin compatible with the 500-mA output current capable LMZM23600.

- **TPS7A4701 is a 36V 1A ultra low noise LDO**

TEXAS INSTRUMENTS

TPS7A4700, TPS7A4701

SBVS204F – JUNE 2012 – REVISED SEPTEMBER 2014

TPS7A470x 36-V, 1-A, 4-µV$_{RMS}$, RF LDO Voltage Regulator

1 Features

- Input Voltage Range: +3 V to +36 V
- Output Voltage Noise: 4 µV$_{RMS}$ (10 Hz, 100 kHz)
- Power-Supply Ripple Rejection:
  - 82 dB (100 Hz)
  - ≥ 55 dB (10 Hz, 10 MHz)
- Two Output Voltage Modes:
  - ANY-OUT™ Version (User-Programmable Output via PCB Layout):
    - No External Feedback Resistors or Feed-Forward Capacitors Required
    - Output Voltage Range: +1.4 V to +20.5 V
  - Adjustable Version (TPS7A4701 only):
    - Output Voltage Range: +1.4 V to +34 V
- Output Current: 1 A
- Dropout Voltage: 307 mV at 1 A
- CMOS Logic Level-Compatible Enable Pin
- Built-In Fixed Current Limit and Thermal Shutdown

3 Description

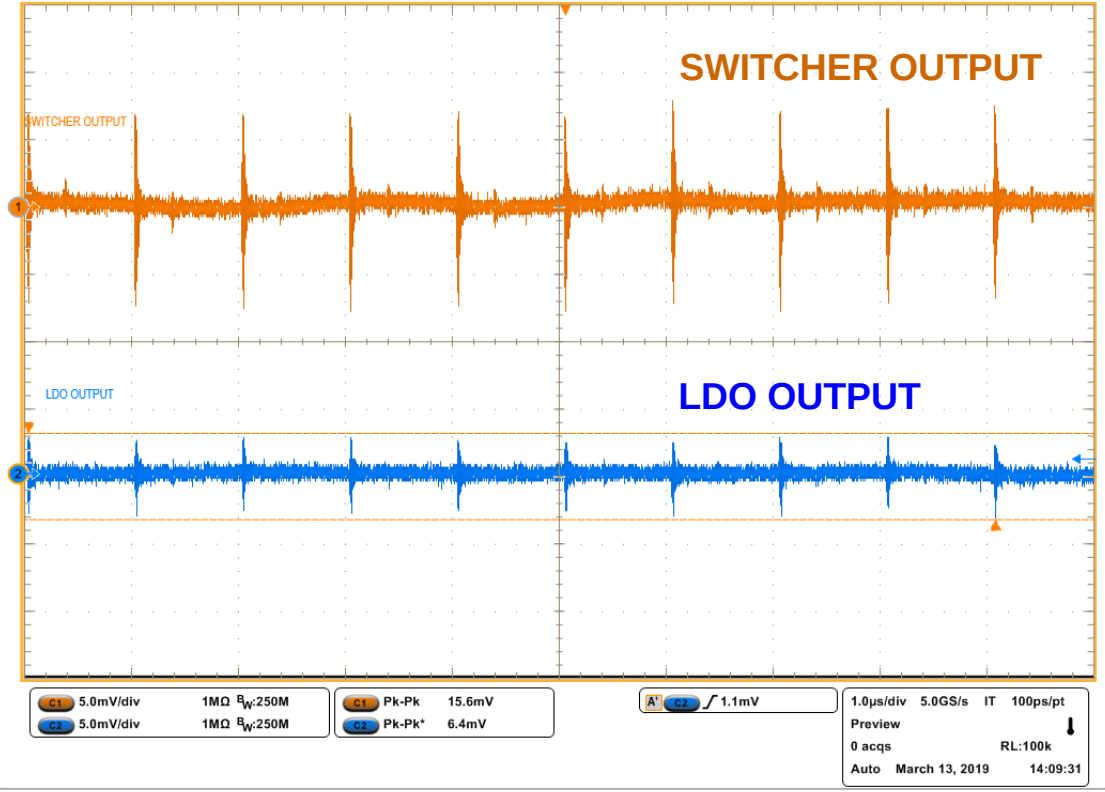
The TPS7A47 is a family of positive voltage (+36 V), ultralow-noise (4 µV$_{RMS}$) low-dropout linear regulators (LDO) capable of sourcing a 1-A load.

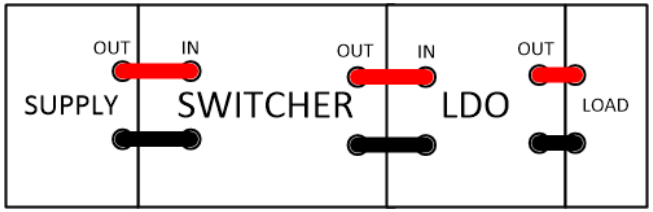
The TPS7A4700 output voltages are user-programmable (up to 20.5 V) using a printed circuit board (PCB) layout without the need of external resistors or feed-forward capacitors, thus reducing overall component count.

The TPS7A4701 output voltage can be configured with a user-programmable PCB layout (up to 20.5 V), or adjustable (up to 34 V) with external feedback resistors.

The TPS7A47 is designed with bipolar technology primarily for high-accuracy, high-precision instrumentation applications where clean voltage rails are critical to maximize system performance. This feature makes the device ideal for powering operational amplifiers, analog-to-digital converters (ADCs), digital-to-analog converters (DACs), and other high-performance analog circuitry in critical applications such as medical, radio frequency (RF), and test-and-measurement.

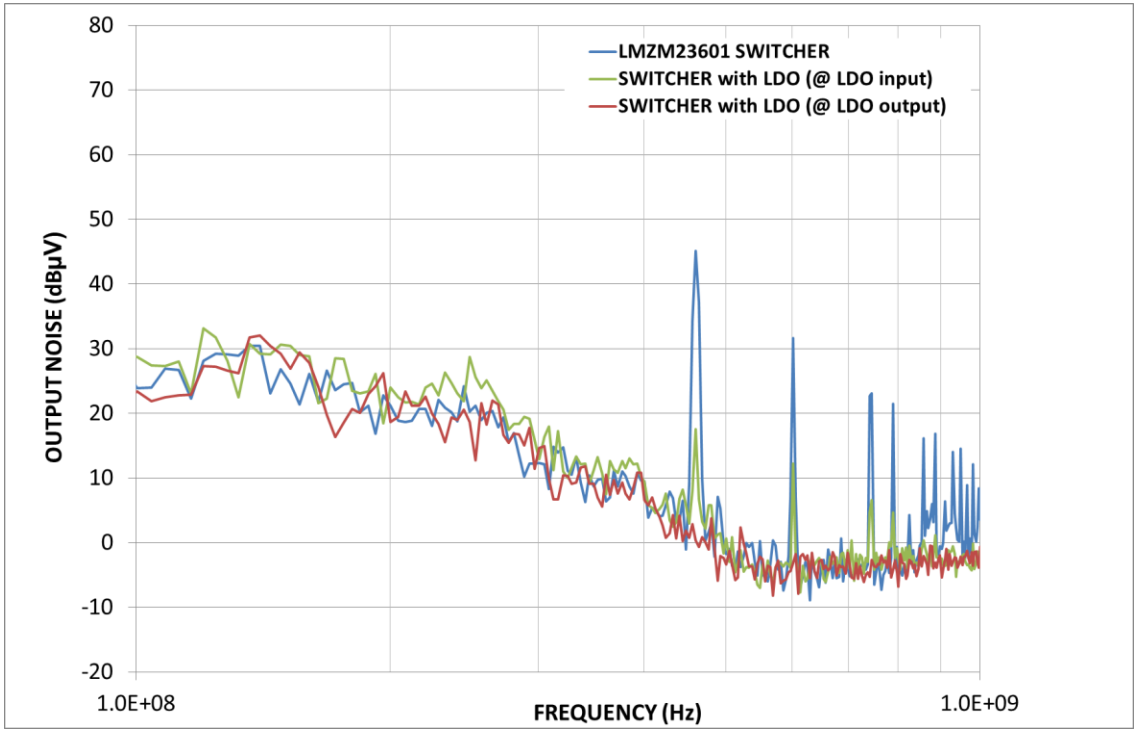
LMZM23601 + TPS7A4701 output noise

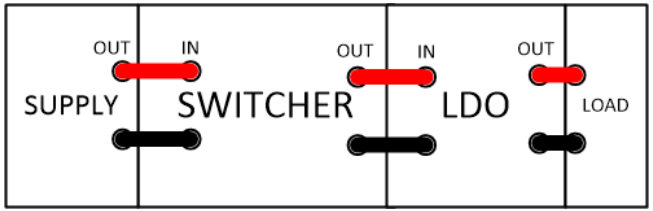




- Measurement shows attenuation of HF noise from 15.6mV to 6.4mV for a total of 7.6dB attenuation

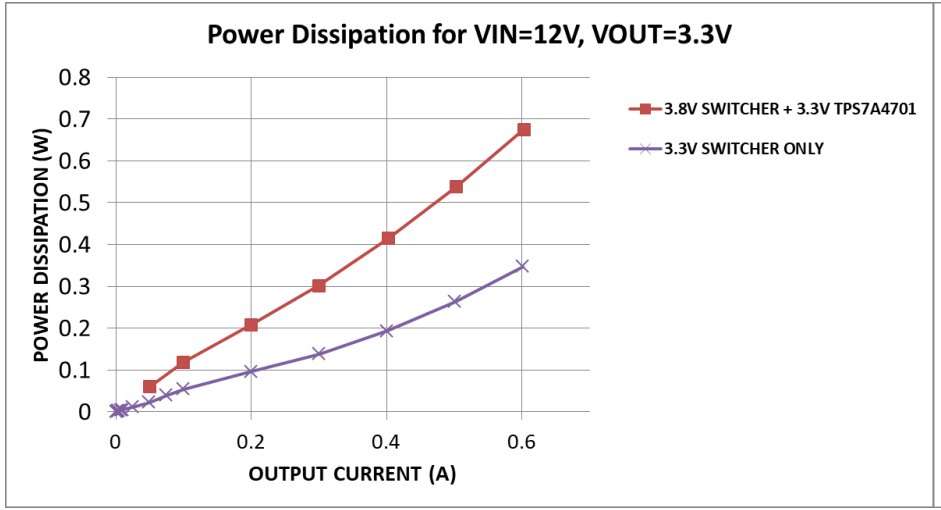
LMZM23601 + TPS7A4701 output noise in frequency domain

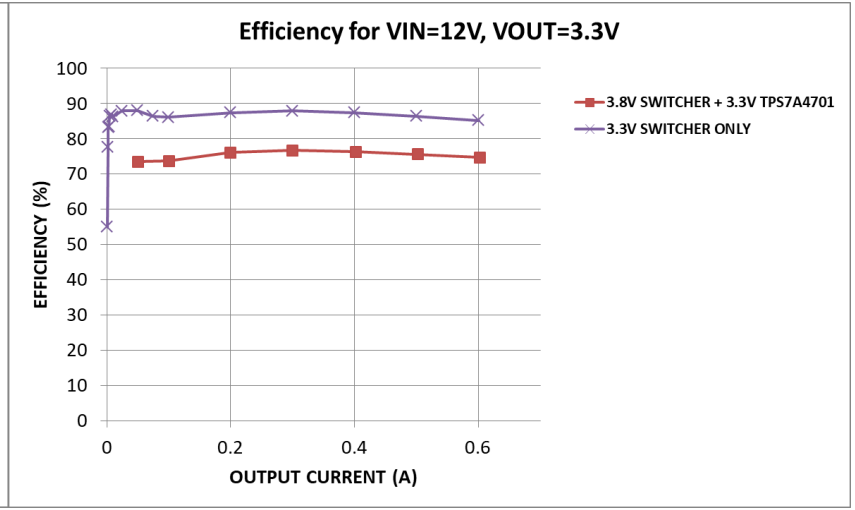




LDO as a filter tradeoffs (efficiency)

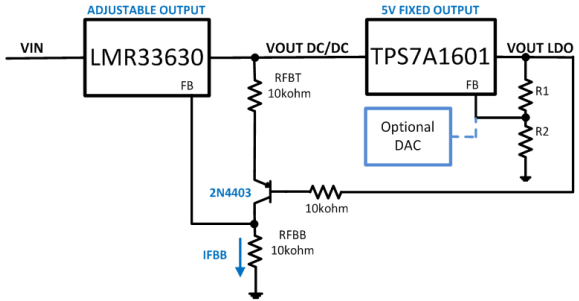
- Additional power dissipation – need to give the LDO some headroom to regulate VOUT.
- The additional dissipated power is V headroom x Load current





DAC adjustable low noise power supply

- Some test and measurement applications may require DAC adjustable and low noise power rail
- If LDO is used to “clean up” the power rail and the switcher output voltage is DAC adjustable, the voltage difference between the LDO input and output can be larger
- To avoid excessive power loss the switcher can be configured as a tracking pre-regulator.



Link: [Designing a pre-tracking regulator, part 1: for a positive-output LDO]

LDO as a filter tradeoffs (BOM)

- At a minimum, the LDO requires 3 components (Cin, LDO, Cout)
- Additional components could be FB resistors, reference filter cap

7.1 Schematic

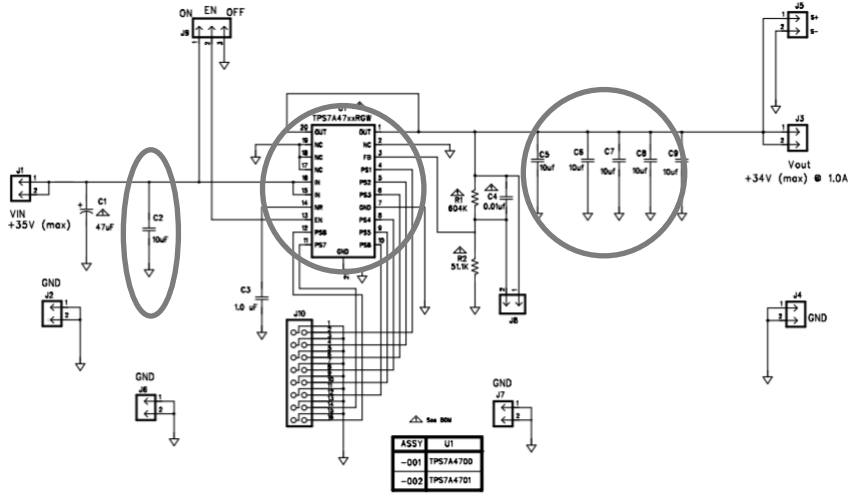
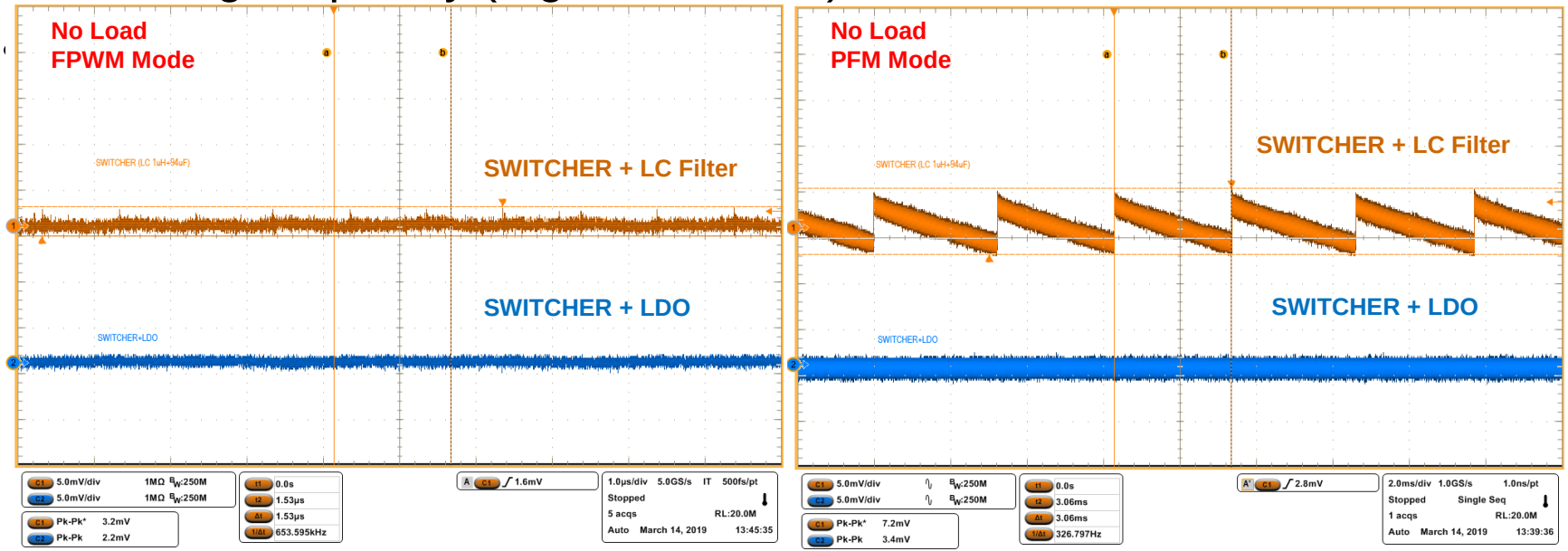


Figure 6. TPS7A47xxEVM-094 Schematic

Filtering performance at light load

- Many switchers have power savings mode at light load with reduced switching frequency (e.g. PFM mode).



LDO as a filter key takeaways

- Can help reduce both LF ripple and HF switching noise
- If the switcher has power savings mode with lower switching frequency at light load, the LDO will still work well
- HF switching noise reduction depends on the LDO PSRR at high frequency which depends on the LDO output capacitor
- Load regulation issues are mitigated with LDO
- Tradeoff is additional power loss, BOM count, and board space.

So, LDO or a 2nd stage filter?!

- LC filters can tricky at high frequency
  - The designer needs to consider the parasitic elements of the capacitor and inductor
  - Filter damping needs to be considered along with stability
  - It may require lower BOM count than LDO but it depends how many capacitors are used
- If power savings mode is employed, the LDO will definitely provide better filtering
- In terms of design, the LDO is straight-forward
- LDO can always be followed by “high frequency” capacitors to clean up the remaining switching noise.

TPS62913 converter + internal filter comp.

TPS6291x 3-V to 17-V, 2-A/3-A Low Noise and Low Ripple Buck Converter with Integrated Ferrite Bead Filter Compensation

1 Features

- Low output 1/f noise < 20 μV_{RMS} (100 Hz to 100 kHz)
- Low output voltage ripple < 10 μV_{RMS} after ferrite bead
- High PSRR of > 65 dB (up to 100 kHz)
- 2.2-MHz or 1-MHz fixed frequency peak current mode control
- Synchronizable with external clock (optional)
- Integrated loop compensation supports ferrite bead for second stage L-C filter (optional)
- Spread spectrum modulation (optional)
- 3.0-V to 17-V input voltage range
- 0.8-V to 5.5-V output voltage range
- 57-mΩ/20-mΩ R_{DSon}
- Output voltage accuracy of ±1%
- Precise enable input allows
  - User-defined undervoltage lockout
  - Exact sequencing
- Adjustable soft start
- Power-good output
- Output discharge (optional)

3 Description

The TPS6291x devices are a family of high efficiency low noise and low ripple synchronous buck converters. The devices are ideal for noise sensitive applications that would normally use an LDO for post regulation such as high speed ADCs, Clock and Jitter Cleaner, Serializer, De-serializer, and Radar applications.

The device operates at a fixed switching frequency of 2.2 MHz or 1 MHz, and can be synchronized to an external clock.

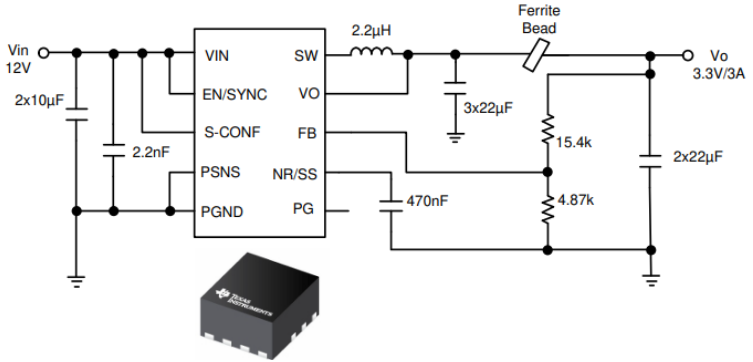
To further reduce the output voltage ripple, the device integrates loop compensation to operate with an optional second-stage ferrite bead L-C filter. This allows an output voltage ripple below 10 μV_{RMS}.

Low-frequency noise levels, similar to a low-noise LDO, are achieved by filtering the internal voltage reference with a capacitor connected to the NR/SS pin.

The optional spread spectrum modulation scheme spreads the DC/DC switching frequency over a wider span, which lowers the mixing spurs.

- Simplified solution with filter compensation taken care of for FPWM applications that require output filtering

- No V_{OUT} regulation penalty since LC filter is inside the feedback network



Summary

- Understanding the noise origin is important for noise mitigation
- The parasitic elements are usually the trouble makers
- Measuring noise properly can save us effort in trying to design filtering solutions
- There are many noise reduction techniques (e.g. layout, stackup, component placement, filtering, etc.)
- 2nd stage LC filters and LDOs can be used to “clean up” a noisy power supply
- LDOs may be preferred based on the tradeoffs discussed

References

- Design a Second-Stage Filter for Sensitive Applications
- Output Noise Filtering for DC/DC Power Modules
- Understanding, Measuring, and Reducing Output Noise in DC/DC Switching Regulators (Part 1)
- Understanding, Measuring, and Reducing Output Noise in DC/DC Switching Regulators (Part 2)
- You Think LDOs are Simple?

Any Questions?

Contact Information: j-hua@ti.com or use the TI E2E Forum (e2e.ti.com)

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