Robust design of delta-sigma ADC system inputs for EOS immunity – PLC analog input module

Dale Li
Applications, Data Converters – Precision ADC
Agenda

• EOS and fault conditions
  – EOS vs ESD
  – Fault conditions

• Diode and ADC input structure
  – Diode: Type and characteristic
  – ADC input protection structure

• Protection topologies for RTD in PLC AI module
  – Conventional TVS diode
  – TI flat-clamp TVS diode

• IEC testing (IEC61000-4-x) – RTD in PLC AI module
ESD vs. EOS – what’s the difference?

<table>
<thead>
<tr>
<th>ESD</th>
<th>EOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>• Electrostatic discharge</td>
<td>• Electrical overstress</td>
</tr>
<tr>
<td>• Short duration event (1-100ns)</td>
<td>• Longer duration event</td>
</tr>
<tr>
<td>• High voltage (kV)</td>
<td>– Milliseconds or more</td>
</tr>
<tr>
<td>• Fast edges</td>
<td>– Can be continuous</td>
</tr>
<tr>
<td>• Both “in-circuit” and “out-of-circuit”</td>
<td>• Lower voltage</td>
</tr>
<tr>
<td></td>
<td>– May be just beyond absolute maximum ratings</td>
</tr>
<tr>
<td></td>
<td>• “In-circuit” event only</td>
</tr>
</tbody>
</table>
EOS from fault or overdriven

- **Fault conditions**
  - Harsh electrical environment
  - High voltage circuit in the system
  - Improper power up sequencing
  - Hot-swap connection and disconnection
  - Loss of power supply but input signal is applied
  - Apply bipolar signal to unipolar input ADC
  - Miswiring
  - Other conditions violating the absolute maximum specifications

- **Key conditions to result in an EOS to RTD application:**
  - Miswiring power supply to RTD input
  - Connect high voltage signal from voltage channel to RTD input
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Unidirectional TVS Diode
(Transient voltage suppressor)

Symbol | Parameter
---|---
$V_{BR}$ | Breakdown voltage
$V_R$ | Stand-off voltage
$V_C$ | Clamping voltage
$V_F$ | Forward voltage drop
$I_{BR}$ | Breakdown Current @ $V_{BR}$
$I_R$ | Reverse Leakage @ $V_R$
$I_F$ | Forward Current @ $V_F$
$I_{PP}$ | Peak Pulse current @ $V_C$

TVS_Uni
Bidirectional TVS diode
(Transient voltage suppressor)

Symbol | Parameter
---|---
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$V_R$ | Stand-off voltage
$V_C$ | Clamping voltage
$V_F$ | Forward voltage drop
$I_{BR}$ | Breakdown Current @ $V_{BR}$
$I_R$ | Reverse Leakage @ $V_R$
$I_F$ | Forward Current @ $V_F$
$I_{PP}$ | Peak Pulse current @ $V_C$

TVS_Bi

![Bidirectional TVS diode graph](image)
Capacitance and leakage current on TVS diode

- **Capacitance**
  - Not constant, change with standoff voltage
  - Junction capacitance changes from hundreds pF up to 10-nF
  - Large power rating diode has higher capacitance and variation
  - Key impact to switch-capacitor input structure SAR ADC

- **Leakage Current**
  - Data sheet from most manufacturers only shows max leakage at room temperature.
  - Same PN from different manufacturers may have different leakage spec.
  - Leakage variation with temperature.
  - Key impact to RTD measurement.

<table>
<thead>
<tr>
<th>Manufacturers</th>
<th>PN</th>
<th>Leakage current (max at 25°C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bourns Inc.</td>
<td>SMBJ14CA</td>
<td>1μA</td>
</tr>
<tr>
<td>Littelfuse</td>
<td>SMBJ14CA</td>
<td>1μA</td>
</tr>
<tr>
<td>Vishay</td>
<td>SMBJ14CA</td>
<td>1μA</td>
</tr>
<tr>
<td>Diodes Inc.</td>
<td>SMBJ14CA</td>
<td>5μA</td>
</tr>
<tr>
<td>Taiwan Semi</td>
<td>SMBJ14CA</td>
<td>5μA</td>
</tr>
</tbody>
</table>
TVS vs. Zener

**TVS Diode**
- Solid state PN junction
- Designed for operation in reverse-breakdown region only during over-voltage events
- Junction area sized to conduct significant current and absorb significant power
- Specifically designed for large transients such as ESD
- Can react to overvoltage in pico-seconds

**Zener**
- Solid state PN junction
- Designed for full-time operation in reverse-breakdown region
- Ideal for voltage regulation
- Slower reaction time
- Lower current/power capability

Zener diode
Internal clamp/protection on data converters

1. Input steering diodes:

2. Back-to-back Zener diode:

3. SCR-based input:

*Bi-directional SCR example
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RTD (resistance temperature detector) sensor

- **PT-100** exhibits 100Ω resistance at 0°C and has wide temp range: -200°C to 850°C.
- R varies from **20Ω to 400Ω**, Currents are pumped into RTD and voltage is measured.
- Sensor with a predictable resistance vs. temperature.
- Measure the resistance and calculate temperature based on the resistance vs. temperature characteristics of the RTD material.
- Overstress (EOS) protection is an increasingly popular requirement from customers.
Typical block diagram: 2-wire RTD inputs

Circuit notes:
- 2 terminal input
- High-side reference (low-side is possible as well)
- One excitation current required
- No lead wire compensation
- \( R_{\text{REF}} \) is typically largest source of error

Key ADC Specs
- \(+ V_{\text{ref}}\) and \(+ V_{\text{RTD}}\)
- \(- V_{\text{error}}^+\) and \(- V_{\text{error}}^-\)

- Differential VREF inputs
- 1x current sources
- Low-noise
- Integrated gain stage

**From ADS124S08 EVM**
Typical block diagram: 3-wire RTD inputs

**Circuit notes**
- 3 terminal input
- High-side reference (low-side is possible as well)
- Excitation via 1x or 2x current sources (1x IDAC requires 2x measurements)
- Lead wire compensation is possible
- $R_{REF}$ is typically largest source of error

**Key ADC Specs**

1. $+V_{ref}$
2. $+V_{RTD}$
3. $-V_{error^+}$
4. $-0V^+$
5. $+V_{error^-}$

---

**From ADS124S08 EVM**
Typical block diagram: 4-wire RTD Inputs

Circuit notes:

- 4 terminal input
- High-side reference (low-side is possible as well)
- One excitation current required
- Inherent lead wire compensation
- $R_{\text{REF}}$ is typically largest source of error

Key ADC Specs

**From ADS124S08 EVM**
Design requirements

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input sensor</td>
<td>RTD: PT100</td>
</tr>
<tr>
<td>Measurement range</td>
<td>-200°C to 850°C (20Ω to 400Ω)</td>
</tr>
<tr>
<td>EOS fault protection</td>
<td>±30V on RTD input</td>
</tr>
</tbody>
</table>
| Resolution                        | ENOB: >20 bits
Noise-free resolution: >17 bits |
| Accuracy (TA = -40 to 85°C)       | ±0.1% at room, ±0.5% full temp range |
| IEC certifications                | ESD: IEC61000-4-2
EFT: IEC61000-4-4
Surge: IEC61000-4-5 |
Design block diagram: RTD measurement (IEC Testing)

Note: ADS124S08’s other channels are used for voltage and current measurement in this design.
Common 3-wire RTD measurement without protection

- **Ratiometric measurement:**
  IDAC noise and drift are cancelled.

- **Lead wire resistance cancellation:**
  - Lead resistance is related to length, material and cross-sectional-area of the conductor.
  - One IDAC needs two measurements.

- **Two IDACs need current chopping to minimize the effect of mismatched current sources.**

Note: 1-meter PT100 RTD sensor from Adafruit.
Why do we need two measurements

Two measurements by taking difference between $V_1$ and $V_2$:

- Cancel lead wire resistance.
- Cancel the offset of ADC.
- Low side reference requires two measurements.
- High side reference measurement only requires one measurement, however the resistor selections ($R_{RTD}$, $R_{ref}$ and $R_{bias}$) and IDAC current are limited by compliance voltage.

Note: $R_{RTD} = 100\, \Omega$, $R_{Lead1} = R_{Lead2} = R_{Lead3} = 10\, \Omega$
ESD / EOS Protection Design

**Design Goals**
- Assume continuous fault
- Limit $I_{ABS\_MAX} < 10\text{mA}$
- Minimize fault power dissipation in $R_{P1}$, $R_1$, and $T_4$
- Make sure normal operation of circuit is functional and has minimal error
  - Compliance limit
  - Leakage Errors
Protection: 3-wire RTD, low-side reference measurement

- Current limiting resistors:
  - $R_{P1}/R_{P2}/R_{P3}/R_{P4}$: limit current to TVS and ADC inputs
  - $R_1$ limits current to IDAC (no $R_{flt}$ on AIN5).
  - Large value $R_{P1}$ and $R_1$ limit current more:
    - Advantage: lower clamped voltage under fault condition.
    - Disadvantage: higher voltage under normal operation.
    (violate compliance voltage on IDAC).
  - Small value $R_{P1}$ and $R_1$ limit less current, have higher
    power dissipation on $R_{P1}$ and $R_1$.
  - Mismatching and drift affect accuracy.

- TVS diode considerations:
  - Proper standoff voltage (14V) -> tradeoff for $R_{P1}$ and $R_1$.
  - Bidirectional TVS instead of unidirectional TVS.
  - Leakage current is a key error contribution to accuracy.
  - Temp drift of leakage current affects accuracy.

### Absolute Maximum Ratings (Single 5V Power Supply)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Analog input voltage ($V_{in,\text{Abs}}$)</td>
<td>-0.3</td>
<td>+5.3</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Analog input current ($I_{in,\text{Abs}}$)</td>
<td>-10</td>
<td>+10</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>Normal input signal</td>
<td>0</td>
<td>+5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>AINx signal ($V_{n}$)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Maximum EOS: ±30W

Compliance voltage = 4.6V max

(*Common-mode capacitor not shown)
Voltage drop across Rp1 can not be acceptable and power dissipation on Rp1 can be a challenge.

Why do we use bidirectional TVS diode?

<table>
<thead>
<tr>
<th>Diodes Inc.</th>
<th>SMBJ14CA (Bidirectional)</th>
<th>SMBJ14A (Unidirectional)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_B$ (Breakdown Voltage)</td>
<td>$-15.6V$</td>
<td>$-0.7V$</td>
</tr>
<tr>
<td>$V_{RP} = V_{EOS} - V_B$ (Volts on Rp)</td>
<td>$-14.4V$</td>
<td>$-29.3V$</td>
</tr>
<tr>
<td>$P_P = \frac{V_{RP}^2}{R_{P1}}$ (Power Dissipation on Rp)</td>
<td>$\frac{(-14.4V)^2}{590\Omega} = 0.351W$</td>
<td>$\frac{(-29.3V)^2}{590\Omega} = 1.455W$</td>
</tr>
</tbody>
</table>
Solution 1: Choose $R_{P1}$ and $R_1$ with regular TVS diode

<table>
<thead>
<tr>
<th>Part number</th>
<th>MFG</th>
<th>Reverse standoff voltage($V_R$)</th>
<th>Breakdown voltage ($V_{BR}$)</th>
<th>Clamping voltage max ($V_{C@I_{PP}}$)</th>
<th>Reverse leakage max ($I_R\over V_R$) 25°C</th>
<th>Breakdown current ($I_{BR\over V_{BR}}$)</th>
<th>Peak pulse current ($I_{PP}$)</th>
<th>Peak power dissipation ($P_{PP}$)</th>
<th>Steady state power dissipation($P_{PP}$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SMBJ14CA</td>
<td>Bourns</td>
<td>14V</td>
<td>Min 15.6</td>
<td>Max 17.9</td>
<td>23.2V</td>
<td>1uA</td>
<td>1mA</td>
<td>25.9A</td>
<td>600W</td>
</tr>
</tbody>
</table>

Positive EOS: (+30V)

1. \[ R_{P1} \geq \frac{V_{EOS\_max} - V_{BR\_min}}{I_{fault}} = \frac{30V - 15.6V}{25mA} = 576\Omega \quad \text{(choose 590\Omega)} \]

2. \[ R_1 \geq \frac{V_{BR\_min} - V_{in\_max}}{I_{ADC}} = \frac{15.6V - 5.3V}{5mA} = 2.06k\Omega \quad \text{(choose 2.2k\Omega, 5mA < I_{in\_Abs})} \]

Negative EOS: (-30V)

1. \[ R_{P1} \geq \frac{V_{EOS\_max} - V_{BR\_min}}{I_{fault}} = \frac{-30V - (-15.6V)}{-25mA} = 576\Omega \quad \text{(choose 590\Omega)} \]

2. \[ R_1 \geq \frac{V_{BR\_min} - V_{in\_max}}{I_{ADC}} = \frac{-15.6V - (-0.3V)}{-5mA} = 3.06k\Omega \quad \text{(choose 3.4k\Omega, 5mA < I_{in\_Abs})} \]

Power

1. \[ P_{RP1} = \frac{(V_{EOS\_max} - V_{BR\_min})^2}{R_{P1}} = \frac{(-30V - (-15.6V))^2}{590\Omega} = 351mW \quad \text{(choose \geq 0.5W for P_{RP1})} \]

2. \[ P_{R1} = \frac{(V_{BR\_min} - V_{in\_max})^2}{R_1} = \frac{(-15.6V - (-0.3V))^2}{3.4k\Omega} = 68.85mW \]

Power

1. \[ P_{TVS\_max} = \frac{(V_{EOS\_max} - V_{BR\_min}) - V_{BR\_min} - V_{in\_max}}{R_{P1}} \cdot V_c = \frac{(-30V - (-15.6V) - 15.6V - (-0.3V))}{590\Omega \cdot 3.4k\Omega} \cdot 23.2V = 461mW \]

Select worst case!
Select reference resistor - $R_{\text{REF}}$

Parameters known:

<table>
<thead>
<tr>
<th></th>
<th>Min (-200°C)</th>
<th>Max (+850°C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>PT100</td>
<td>20Ω</td>
<td>400Ω*</td>
</tr>
<tr>
<td>Lead resistance</td>
<td>Min</td>
<td>Max</td>
</tr>
<tr>
<td></td>
<td>0Ω</td>
<td>10Ω</td>
</tr>
</tbody>
</table>

Components selected: $R_P = 590\Omega, R_1 = 3.4k\Omega$

* Approximate value.

Select $R_{\text{REF}}$ regarding maximum voltage across $R_{\text{RTD}}$:

1. Use $I_{\text{DAC}} = 0.5mA$ (lower sensor self-heating: $0.093\text{mW}<0.1\text{mW}$)
2. $V_{\text{RTD, max}} = I_{\text{DAC}} \cdot R_{\text{RTD, max}} = 0.5mA \cdot 400\Omega = 0.2V$
3. Use Gain = 4, $V_{\text{REF, min}} = V_{\text{RTD, max}} \cdot \text{Gain} = 0.2V \cdot 4 = 0.8V$
   $\Rightarrow V_{\text{REF}} = 1V$
4. $R_{\text{REF}} = V_{\text{REF}} / I_{\text{DAC}} = 1V / 0.5mA = 2k\Omega$

(*Common-mode capacitor not shown)
Compliance Voltage on I_{ref}

<table>
<thead>
<tr>
<th>Accuracy</th>
<th>-1.5%</th>
<th>1.5%</th>
</tr>
</thead>
<tbody>
<tr>
<td>EXCITATION CURRENT SOURCES (IDACS)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Current settings</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Compliance voltage^{(4)}</td>
<td></td>
<td></td>
</tr>
<tr>
<td>10 \mu A to 750 \mu A, 0.1% deviation</td>
<td>AVSS</td>
<td>AVDD - 0.4 V</td>
</tr>
<tr>
<td>1 mA to 2 mA, 0.1% deviation</td>
<td>AVSS</td>
<td>AVDD - 0.6 V</td>
</tr>
<tr>
<td>T_x = 25°C, 10 \mu A to 100 \mu A</td>
<td>-5%</td>
<td>±0.7%</td>
</tr>
</tbody>
</table>

\[ 5V - 0.4V = 4.6V \]

Need to confirm that IDAC input < 4.6V
Verify node voltage

Parameters Known:

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>PT100 (max)</td>
<td>400Ω</td>
</tr>
<tr>
<td>Lead Resistance (max)</td>
<td>10Ω</td>
</tr>
<tr>
<td>Excitation Current (I_{DAC})</td>
<td>0.5mA</td>
</tr>
<tr>
<td>Compliance voltage (V_C)</td>
<td>0.4V &lt; V_C &lt; 4.6V *</td>
</tr>
<tr>
<td>V_{(AINx)} (Gain=4)</td>
<td>0.45V &lt; V_{(AINx)} &lt; 4.55V *</td>
</tr>
</tbody>
</table>

Components Selected:

- R_P = 590Ω, R_1 = 3.4kΩ, R_{REF} = 2kΩ

* Limit calculated under specified conditions (Gain=4, AVDD=5V).

Verify Node Voltage under Normal Operation:

V_{AIN5} = I_{DAC} \cdot (R_1 + R_P1 + R_{Lead1} + R_{RTD} + R_{Lead3} + R_P5 + R_{REF}) =

0.5mA \cdot (3.4kΩ + 590Ω + 10Ω + 400Ω + 10Ω + 590Ω + 2kΩ) = 3.35V < 4.6V *

Compliance voltage = 4.6V max
Select $R_{flt}$ and $C_{flt}$ for differential and common-mode filter

- Keep bandwidth of differential filter $\geq 10 \times$ data rate.
- Keep differential capacitor $\geq 10 \times$ Common-mode capacitor.
- Keep input resistance $< 10k\Omega$ for proper input sampling.
- Higher resistance helps to limit current to ADC input.
- Keep resistance low on REFN0 since for single power supply.
- Set $R_{flt} = R_{flt\_ref} = 4.12k\Omega$, $C_{flt} = C_{ref} = 470pF$, $C_{flt\_Diff} = 4.7nF$.

<table>
<thead>
<tr>
<th>For ADC input filtering:</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>1 $f_{in_diff} = 1/([2 \cdot \pi \cdot C_{in_diff} \cdot (R_{RTD} + 2 \cdot R_{flt} + R_p)]) = 3.67kHz$</td>
<td></td>
</tr>
<tr>
<td>2 $f_{in_CM} = 1/[2 \cdot \pi \cdot C_{flt} \cdot (R_{RTD} + R_{flt})] = 74.9kHz$</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>For reference input filtering:</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>1 $f_{ref_filter} = 1/(2 \cdot \pi \cdot C_{ref} \cdot R_{flt_ref} + R_{flt})] = 82kHz$</td>
<td></td>
</tr>
</tbody>
</table>

*see RTD Ratiometric Measurements and Filtering Using the ADS1148 and ADS1248.*

*Protection circuitry not shown*
Calculated and simulated error with SMBJ14CA diode

- TVS leakage current are added:
  - I3 and I4 through both $R_{RTD}$ and $R_{REF}$.
  - I2 and I1 through $R_{REF}$ only.
- Leakage current on SMBJ14CA from Bourns: $I_{leak} = 1\mu A$
  (maximum at room temp, no spec over temp)

Additional error (maximum) at room temperature:

\[
\text{Ratio}_{-\text{Ideal}} = \frac{(I_{DAC} \cdot R_{RTD} \cdot \text{Gain})}{(I_{DAC} \cdot R_{REF})} = 400\Omega \cdot 4/2\,k\Omega = 0.8
\]

\[
V_1 = (I_{DAC} + I_3 + I_4) \cdot (R_{RTD} + R_{\text{lead1}}) + I_3 \cdot R_{RP2} - I_2 \cdot (R_{P3} + R_{\text{lead2}})
\]

\[
V_2 = (I_{DAC} + I_2 + I_3 + I_4) \cdot R_{\text{lead3}} + I_2 \cdot (R_{RP3} + R_{\text{lead2}}) - I_1 \cdot R_{RP4}
\]

\[
\text{Ratio}_{-\text{Actual}} = \frac{(V_{\text{meas.error}} \cdot \text{Gain})}{V_{\text{REF}}} = \frac{((V_1 - V_2) \cdot \text{Gain}))/\left((R_{REF} \cdot (I_{DAC} + I_1 + I_2 + I_3 + I_4 + I_5))\right)}{\left((I_{DAC} + 2I) \cdot R_{RTD} - 3I \cdot R_{\text{lead}} \cdot \text{Gain}))/\left((R_{REF} \cdot (I_{DAC} + 5I))\right) = 0.795^*\)
\]

\[
\text{Error} = \frac{(\text{Ratio}_{-\text{Actual}} - \text{Ratio}_{-\text{Ideal}})}{\text{Ratio}_{-\text{Ideal}}} \cdot 100\% = -0.625\%
\]

*Note: $I_1 = I_2 = I_3 = I_4 = I_5 = 1$

Accuracy desired: ±0.5%
Component mismatch - Monte Carlo simulation in TINA™-TI

Mismatch from:

- Current limiting resistors R_{px}
- Leakage current on TVS diodes.
- Temperature drift on diodes and resistors.

Monte Carlo Error Analysis PT100 RTD with SMBJ14CA-TSC
Component Mismatch - Monte Carlo Simulation - Cont’d

\[\text{TypError} = \frac{\text{standard deviation}}{\text{Mean}} \cdot 100 = \left( \frac{276.44474u}{-618.861022m} \right) \cdot 100 = \pm 0.045\% \]

For 68.26% of the population

\[\text{MaxError} = 3 \cdot \text{Typical} = 3 \cdot (\pm 0.045\%) = \pm 0.135\% \]

For 99.73% of the population
Error with low leakage current of TVS diode

<table>
<thead>
<tr>
<th>Part number</th>
<th>MFG</th>
<th>Reverse standoff voltage ($V_R$)</th>
<th>Breakdown voltage ($V_{BR}$)</th>
<th>Clamping voltage max ($V_{C@I_{PP}}$)</th>
<th>Reverse leakage ($I_R@V_R$)</th>
<th>Peak power dissipation W ($P_{PP}$)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Min</td>
<td>Typ</td>
<td>Min</td>
<td>Typ</td>
<td>Max at 27°C</td>
</tr>
<tr>
<td>TVS1401</td>
<td>TI</td>
<td>14V</td>
<td>17.1</td>
<td>17.6</td>
<td>22.2</td>
<td>1.1nA</td>
</tr>
<tr>
<td>SMBJ14CA</td>
<td>Bourns</td>
<td>14V</td>
<td>15.6</td>
<td>17.2</td>
<td>23.2</td>
<td>1uA</td>
</tr>
</tbody>
</table>

RTD system error calculated from leakage current:

<table>
<thead>
<tr>
<th>PN</th>
<th>MFG</th>
<th>Error</th>
<th>Temperature</th>
</tr>
</thead>
<tbody>
<tr>
<td>TVS1401</td>
<td>TI</td>
<td>-0.16%</td>
<td>85°C</td>
</tr>
<tr>
<td>SMBJ14CA</td>
<td>Bourns</td>
<td>-0.625%</td>
<td>25°C</td>
</tr>
</tbody>
</table>

Accuray desired: ±0.5%

Note: The error with TVS1401 at room temp is much smaller.
RTD measurement: accuracy vs. temperature

RTD - 100ohm (0°C)

RTD - 400ohm (850°C)

Conditions: 0.1% 10ppm/°C resistors for Rp and R1, 0.01%, 5ppm/°C resistor for Rref.

10x better than expected!
EOS protection verification on ADC input

Input Signal

Clamped Signal on ADC Input

60Vpp
Agenda

- EOS and fault conditions
  - EOS vs ESD
  - Fault conditions

- Diode and ADC input structure
  - Diode: Type and characteristic
  - ADC input protection structure

- Protection topologies for RTD in PLC AI module
  - Conventional TVS diode
  - TI flat-clamp TVS diode

- IEC testing (IEC61000-4-x) – RTD in PLC AI module
Electromagnetic compatibility (EMC) tests

IEC – International Electrotechnical Commission

• Promotes international cooperation on standardization
• Created test standards for electronics
• IEC 61000-4 standard
  – IEC 61000-4-2: Electrostatic discharge (ESD)
  – IEC 61000-4-3: Radiated electromagnetic interference (EMI)
  – IEC 61000-4-4: Electrical fast transients (EFT)
  – IEC 61000-4-5: Surge
  – IEC 61000-4-6: Conducted electromagnetic interference (EMI)

* Precision Labs - Op Amps: Electrical Overstress
Electrical fast transient (EFT) immunity

IEC61000-4-4
Simulates everyday switching transients caused by interruption of inductive loads, relay bounces, etc.

* Precision Labs - Op Amps: Electrical Overstress
### IEC 61000-4-4 threat levels

<table>
<thead>
<tr>
<th>Level</th>
<th>Power supply port</th>
<th>I/O, signal, data &amp; control lines</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Open-circuit voltage (kV)</td>
<td>Short-circuit current (A)</td>
</tr>
<tr>
<td>1</td>
<td>0.5</td>
<td>10</td>
</tr>
<tr>
<td>2</td>
<td>1</td>
<td>20</td>
</tr>
<tr>
<td>3</td>
<td>2</td>
<td>40</td>
</tr>
<tr>
<td>4</td>
<td>4</td>
<td>80</td>
</tr>
</tbody>
</table>

* Precision Labs - Op Amps: Electrical Overstress
IEC 61000-4 test setup – RTD hardware
IEC61000-4 tested RTD module with TVS1401 EOS protection solution

<table>
<thead>
<tr>
<th>Standard</th>
<th>Type</th>
<th>Level</th>
<th>Outcome</th>
<th>Grade</th>
</tr>
</thead>
<tbody>
<tr>
<td>ESD Immunity</td>
<td>Contact</td>
<td>±8kV</td>
<td>Passed</td>
<td>Class B</td>
</tr>
<tr>
<td></td>
<td>Air</td>
<td>±15kV</td>
<td>Passed</td>
<td>Class B</td>
</tr>
<tr>
<td>EFT Immunity</td>
<td>5kHz</td>
<td>±4kV</td>
<td>Passed</td>
<td>Class B</td>
</tr>
<tr>
<td></td>
<td>100kHz</td>
<td>±4kV</td>
<td>Planning</td>
<td></td>
</tr>
<tr>
<td>Surge Immunity</td>
<td>Planning</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Thank you!

Special thanks to:

Art Kay
Collin Wells
Bob Benjamin
Bryan Lizon
from PADC team

**TI Precision Labs – ADCs:** Electrical Overstress on Data Converters
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