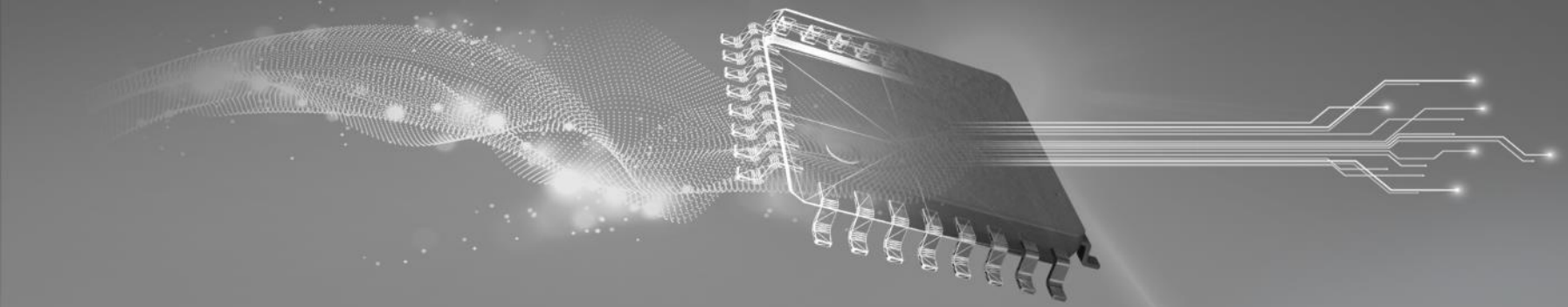
TI TECH DAYS



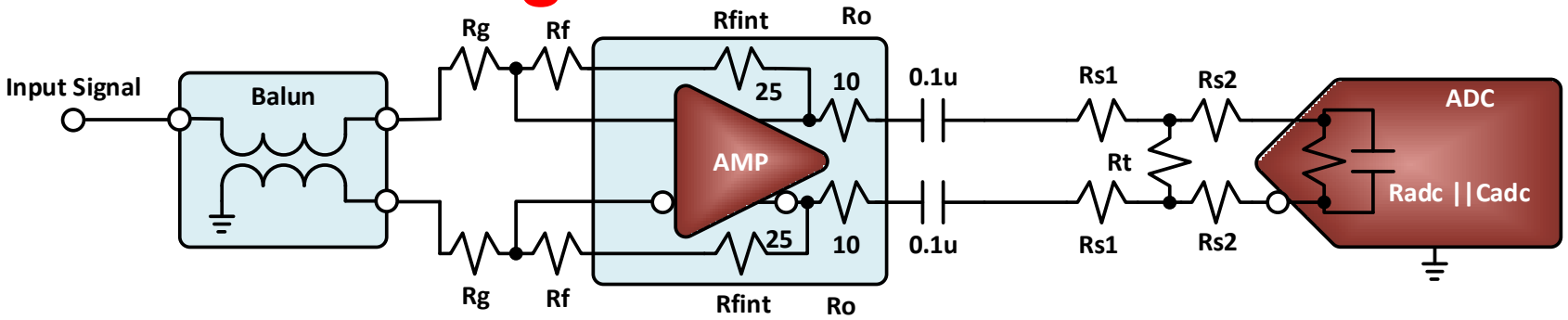
Unraveling the practical mysteries behind RF converter front ends

Rob Reeder

Data Converters – High-Speed Converters

Texas Instruments

Front-end background



- The term “front end” generally implies that this is a network or coupling circuit that connects between the last stage of the signal chain (usually an amplifier, gain block or tuner) and the converter’s analog inputs.
- In order to achieve DS performance the designer must understand the frontend goals.
- There are typically two types of front ends, they are passive or active.
- It must also be very linear, well balanced and properly laid out on the printed circuit board (PCB) in order to preserve the signal content properly.

Front-end goals & definitions

- Designing an input network is important because it allows for a complete evaluation over the converter's entire useable band.

- When designing the network there are five parameters to keep in mind:

  - **Input impedance / VSWR** (voltage standing wave ratio) is a unitless parameter that shows how much power is being reflected into the load over the bandwidth of interest. Input impedance of the network is specified value of the load, usually this is 50ohms.

  - **Passband flatness** is usually defined as the amount of fluctuation/ripple that can be tolerated within the specified bandwidth. 1.0dB, ±0.5dB, could be more, could be less, could be define with a slope

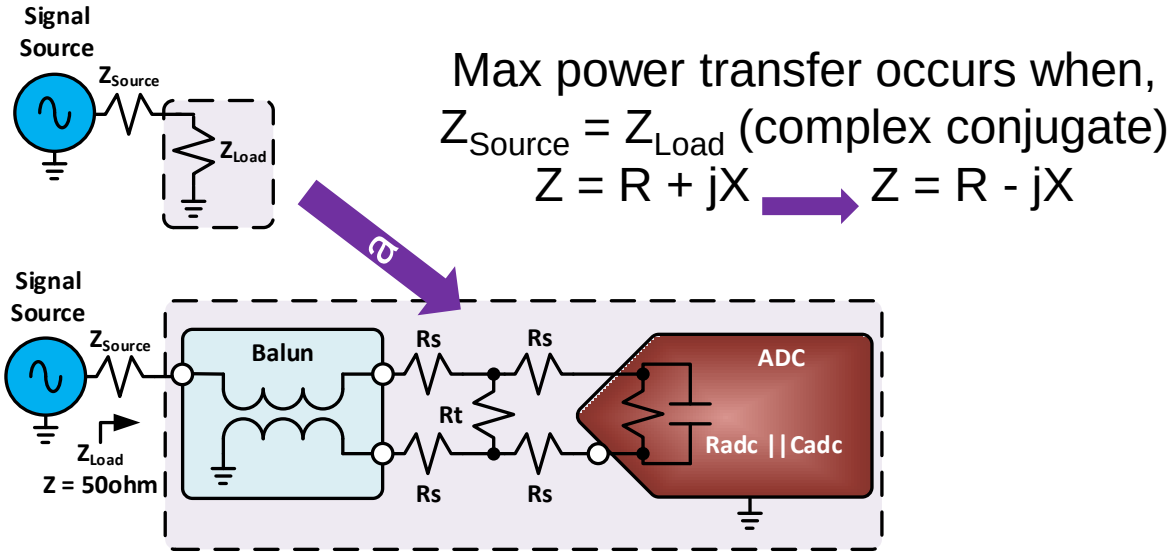
  - **Bandwidth** is simply the beginning and ending of the frequencies to be used in the system. Typically -3dB from some reference point.

  - **SNR** (signal-to-noise ratio) / **SFDR** (spurious free dynamic range)

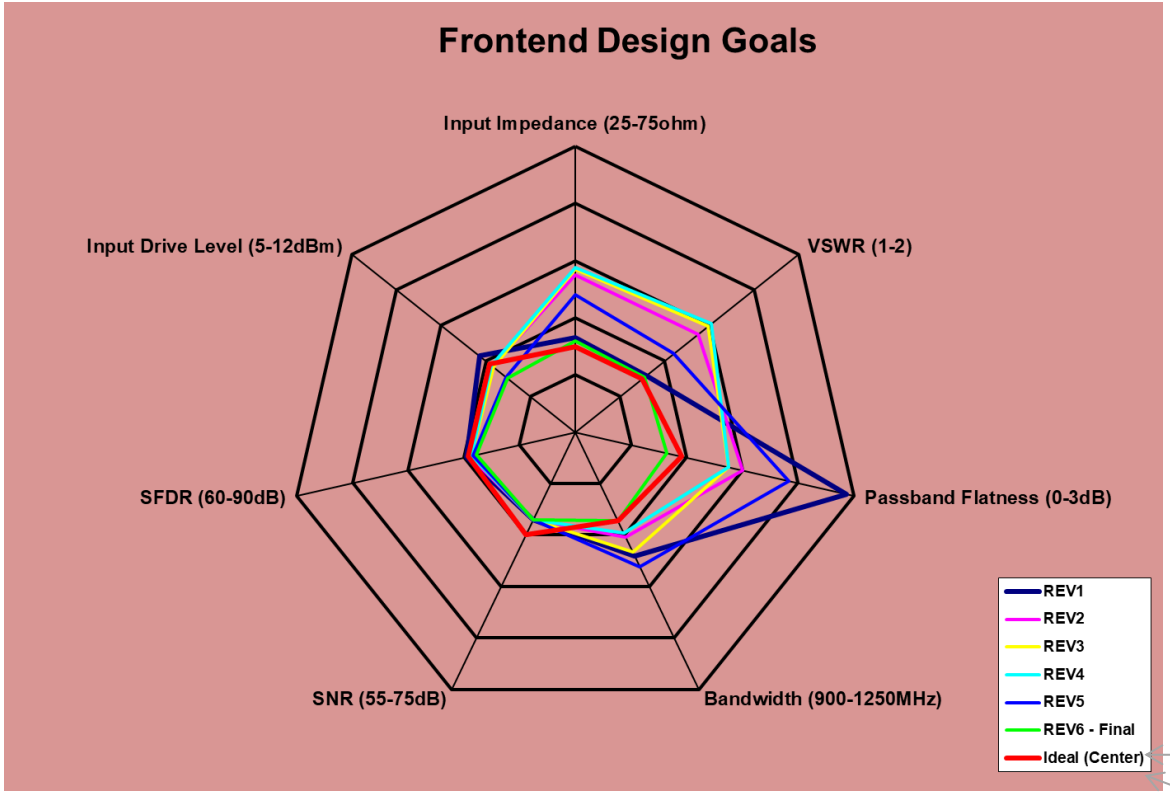
  - **Input drive level** is a function of the bandwidth, input impedance, and VSWR specifications. This sets the gain/amplitude required for a full-scale input signal at the converter. It is highly dependent on the frontend components chosen – i.e., transformer, amplifier, AAF – and can be one of the most difficult parameters to achieve.

Front-end goals & definitions: to match or not to match?

- The word “**match**” is a term that should be used wisely. Keep in mind an ADC is a voltage sensitive device that typically has poor VSWR and return loss on the analog input pins.
- Therefore, it is almost impossible to match a ADC front ends that samples at 100s of MSPS, let alone +1GSPS which are very popular today….the BWs are just too wide.
- The RF-term “**match**” should be positioned to mean…for an ADC: optimization yielding the best results given the front-end design and application.
- Keep in mind, the impedance is only one of the parameters on the list.



Front-end goals & definitions: one approach to “matching”…

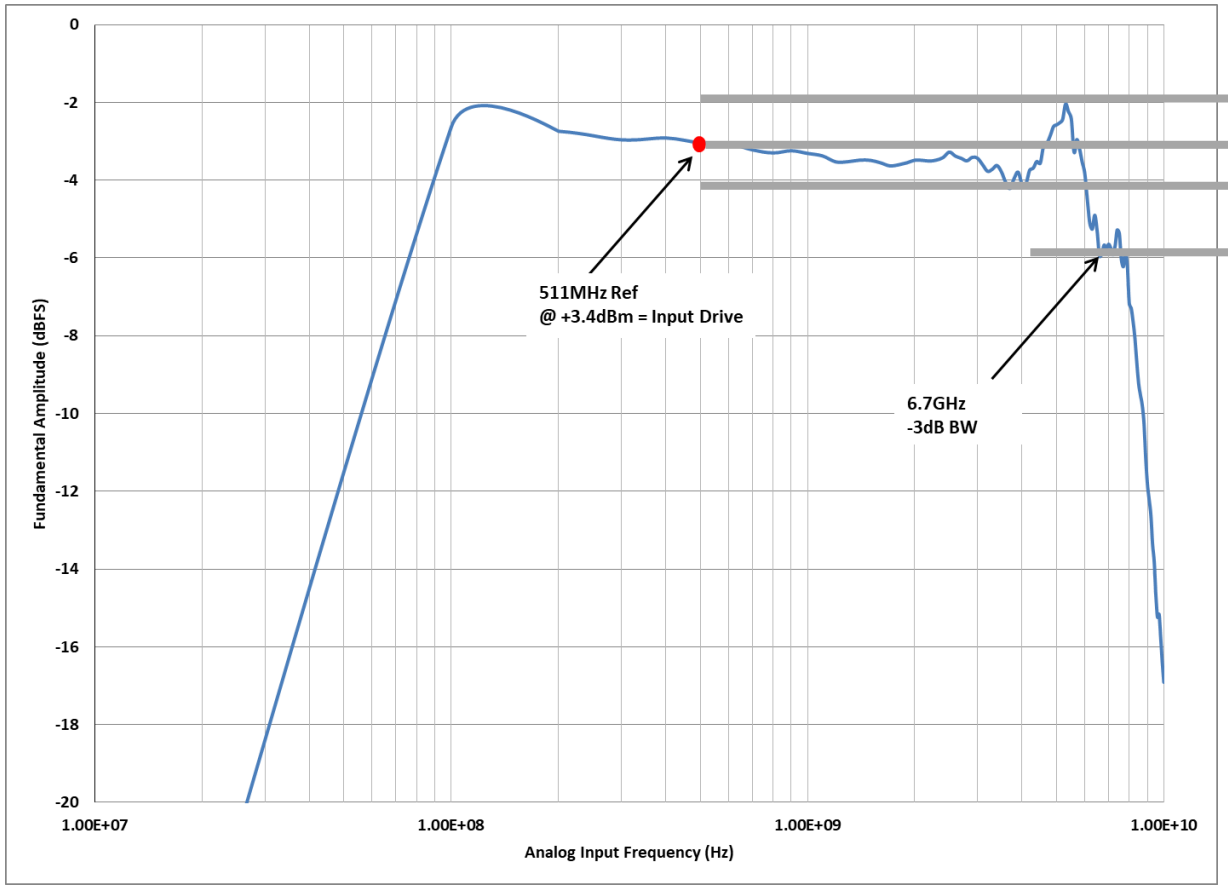


Final match

Ideal match

*Putting boundaries on each of these parameters can help quickly arrive to an expected/optimum frontend design.

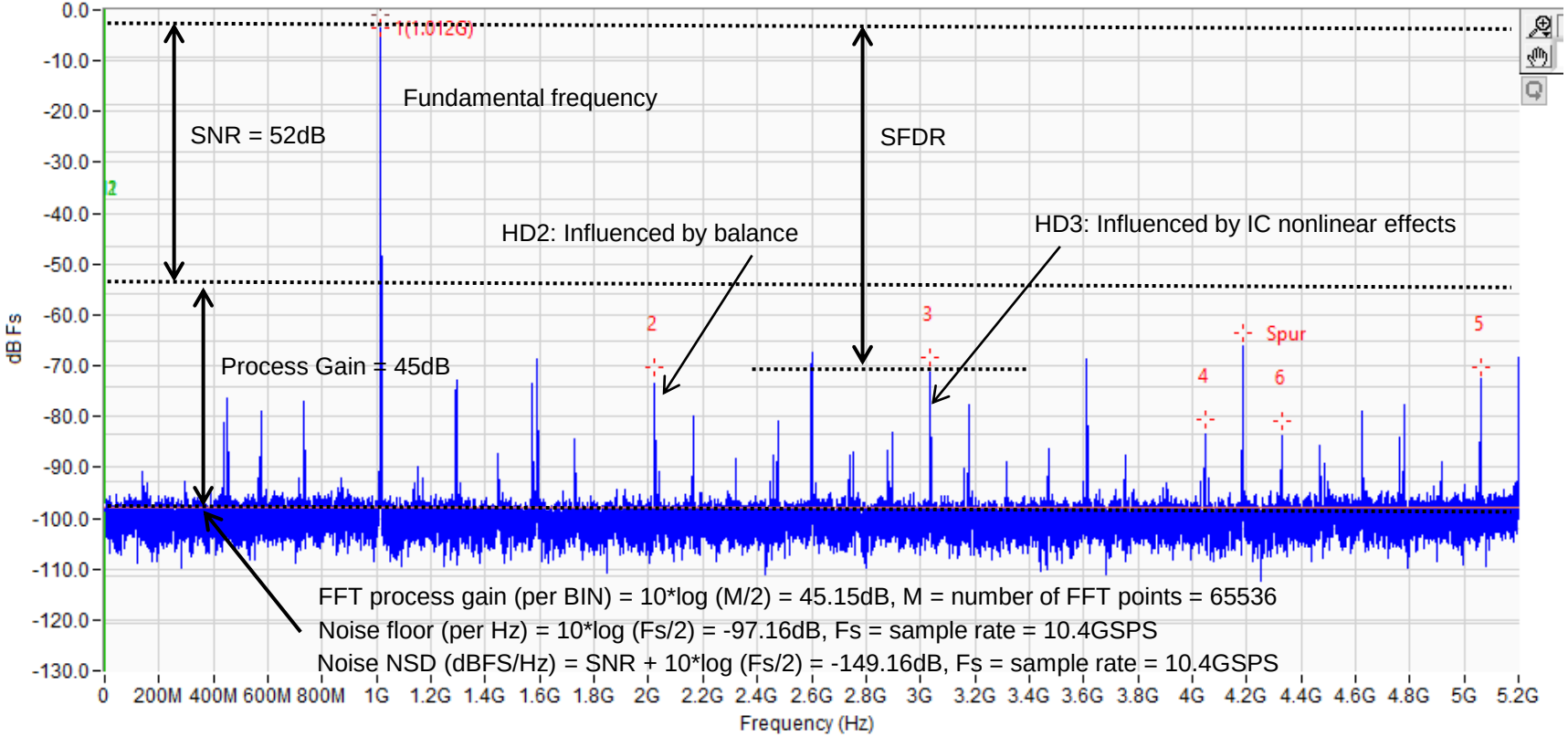
Front-end goals & definitions: passband flatness/bandwidth/drive level



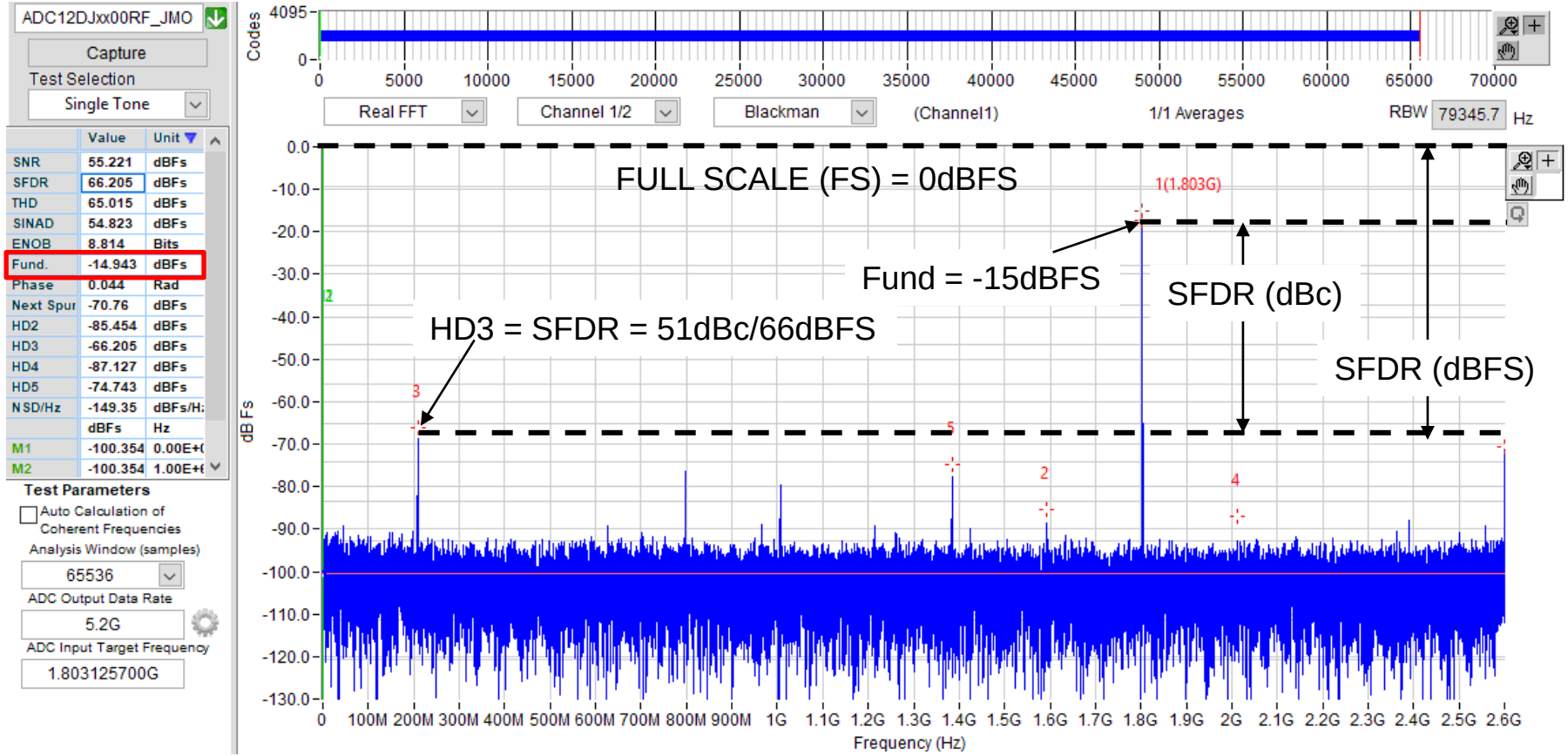
Bandwidth

Passband flatness ±0.5dB

Front-end goals & definitions: noise and distortion

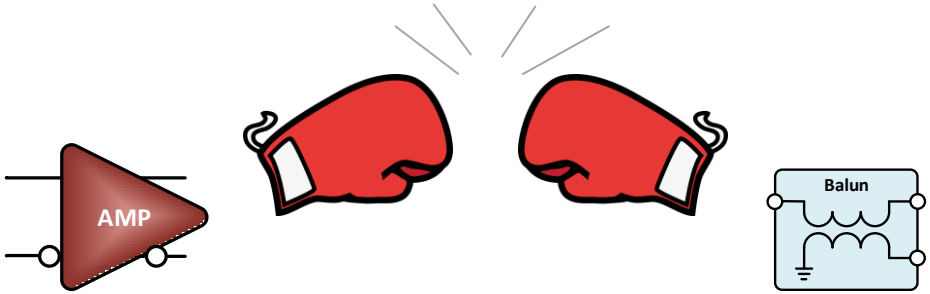


Front-end goals & definitions: dBc vs. dBFS



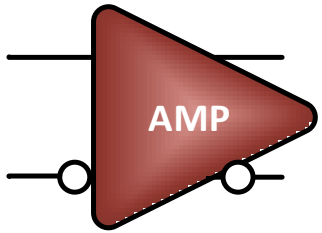
Front-end types: amplifier vs. transformer/balun

- Q: Who will win?
- A: It depends!
- The KEY is understanding the tradeoffs (i.e. – those goals we discussed in the previous slides) which are mostly set per the application
- An amplifier is active and a transformer is passive.
- Like all active devices, amplifiers consume power and transformers do not.
- However, both have dynamic effects that need to be dealt with.



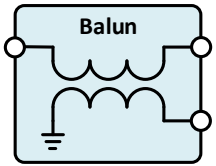
Front-end types: amplifier vs. transformer/balun

- Why use an amplifier?
  - Amplifiers preserve the DC content of the signal (in some cases)
  - Amplifiers preserve isolation between the previous stage and the ADC…on the scale of ~40-60dB.
  - Amplifiers are easier to work with in terms of gain and are not bandwidth dependent.
  - Amplifiers are less likely to ripple through the passband.
  - Can be used to convert single-ended signals to differential (in some cases)

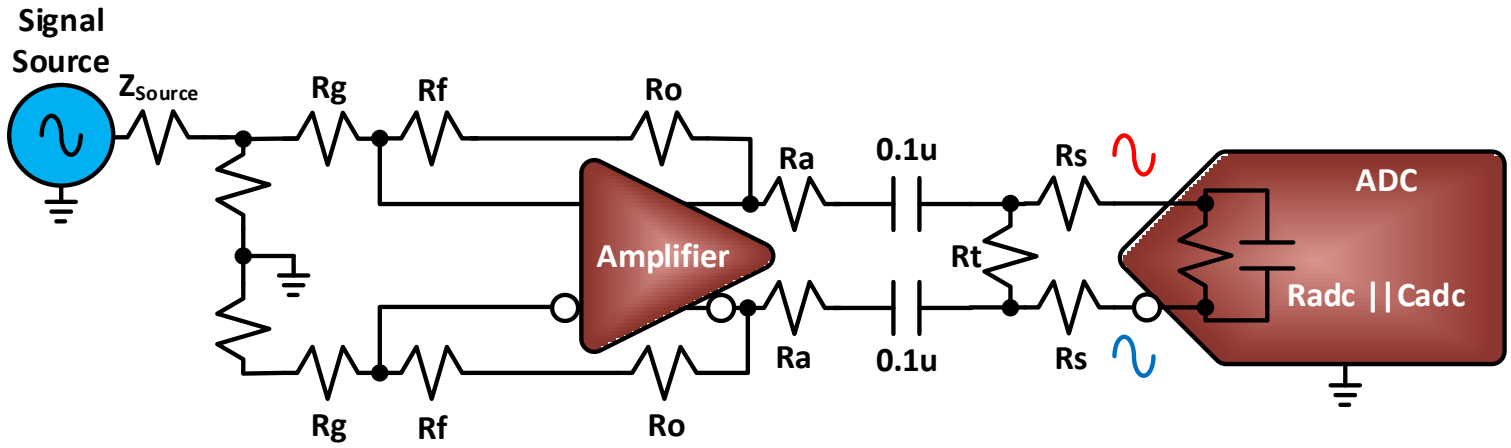


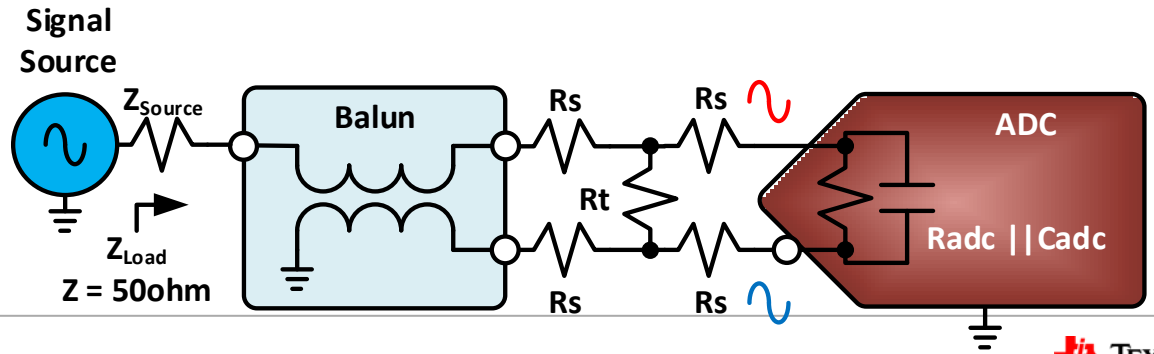
Front-end types: amplifier vs. transformer/balun

- Why use a transformer?
  - Transformers have the advantage of coupling higher IF frequencies without significant loss (>200MHz).
  - For this same reason transformers usually have more bandwidth.
  - Transformers don’t require a power supply and thus add no power increment to the overall signal chain.
  - Transformers don’t add noise to the system, they only gain the signal noise, if using a transformer with gain.
  - Transformers provide an inherent AC coupled circuit.
    - Baluns are not.
  - Can be used to convert single-ended signals to differential (in all cases)



Front-end types: examples





Front-end types: summary

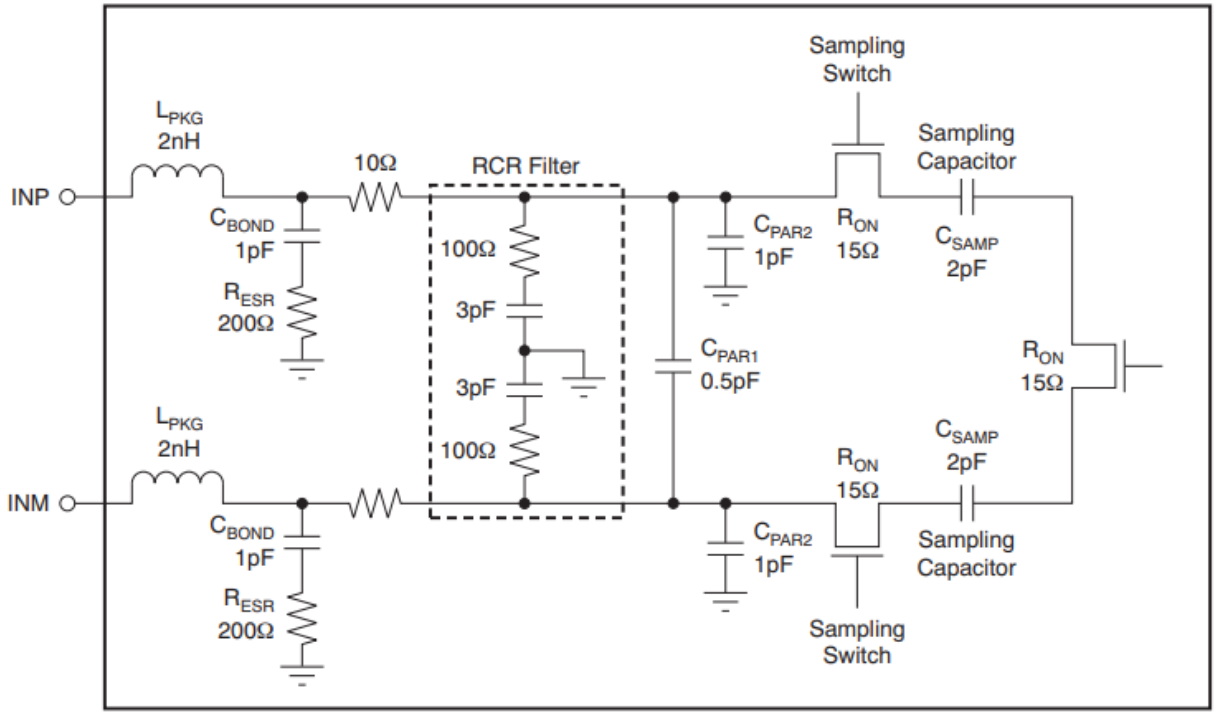
Parameter	Usual preference
Bandwidth	Transformer/balun
Gain	Amplifier
Passband flatness	Amplifier
Power requirement	Transformer/balun
Noise	Transformer/balun
DC vs. AC coupling	Amplifier (DC level preservation) Transformer/Balun (DC isolation)

ADC types: ADC internal input architectures

- Unbuffered
  - Input Impedance set by switched-capacitor design
  - Lower power
  - Input Impedance varies over time (sample clock – track and hold)
  - Charge injection from sample caps reflects back onto input network

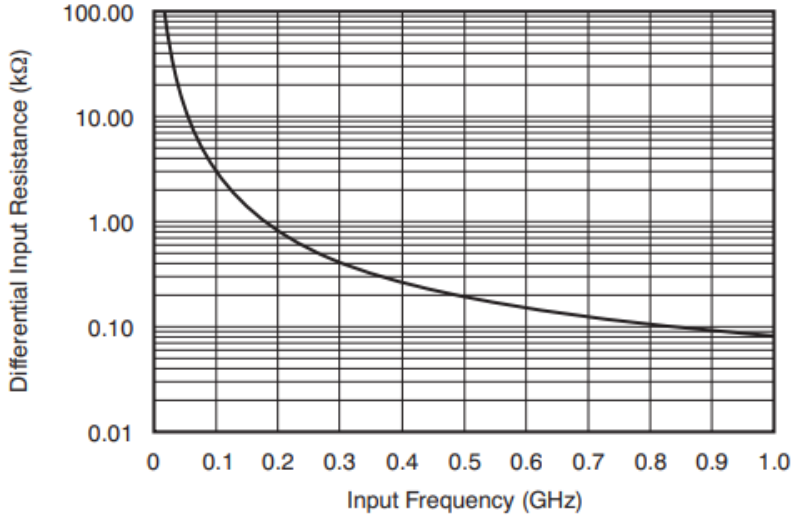
- Buffered
  - Highly linear buffer but requires more power
  - Generally have lower SNR, buffer = noise
  - Easier to design input network to interface high impedance buffer since it provides a fixed input termination resistance
  - Buffer provides isolation between sample caps and input network resulting in reduced charge injection transients

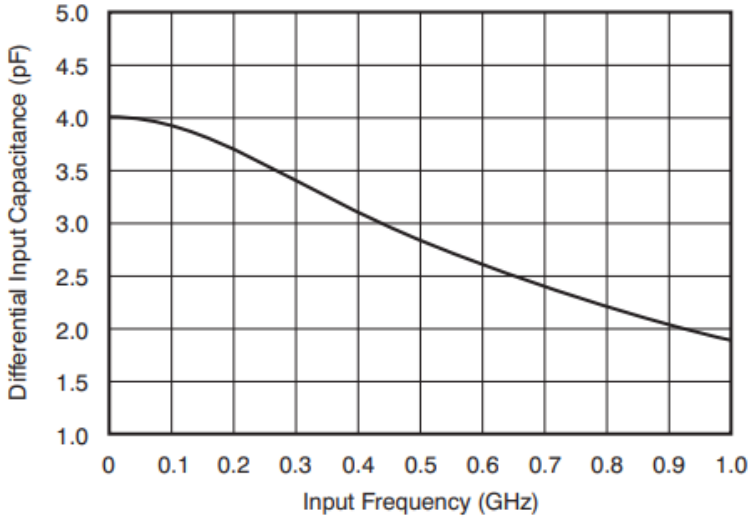
ADC types: unbuffered input architectures



ADS4149: unbuffered ADC input architecture, simplified

ADC types: unbuffered input architectures, cont. – input Z

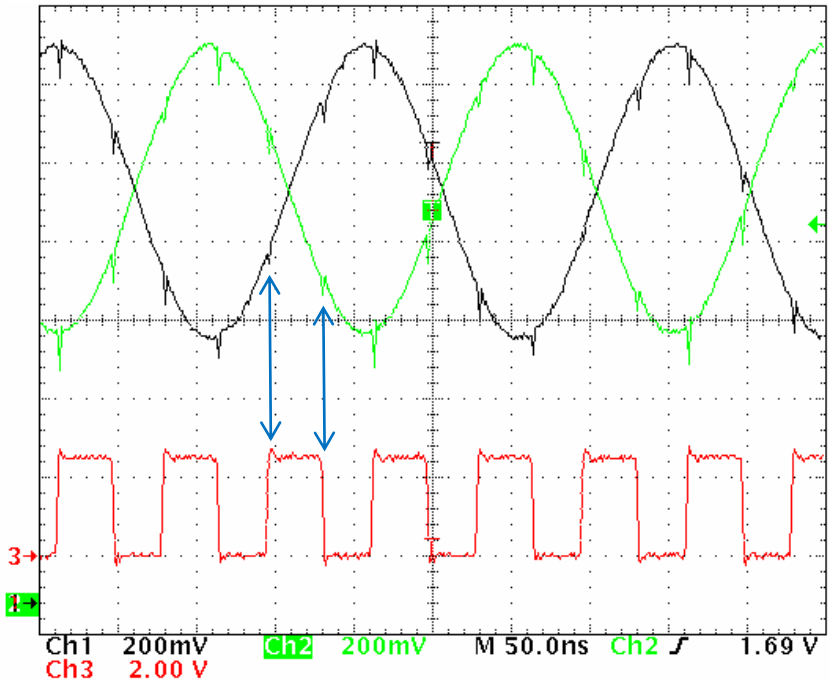




ADS4149: unbuffered ADC input Zin = Rin || Cin

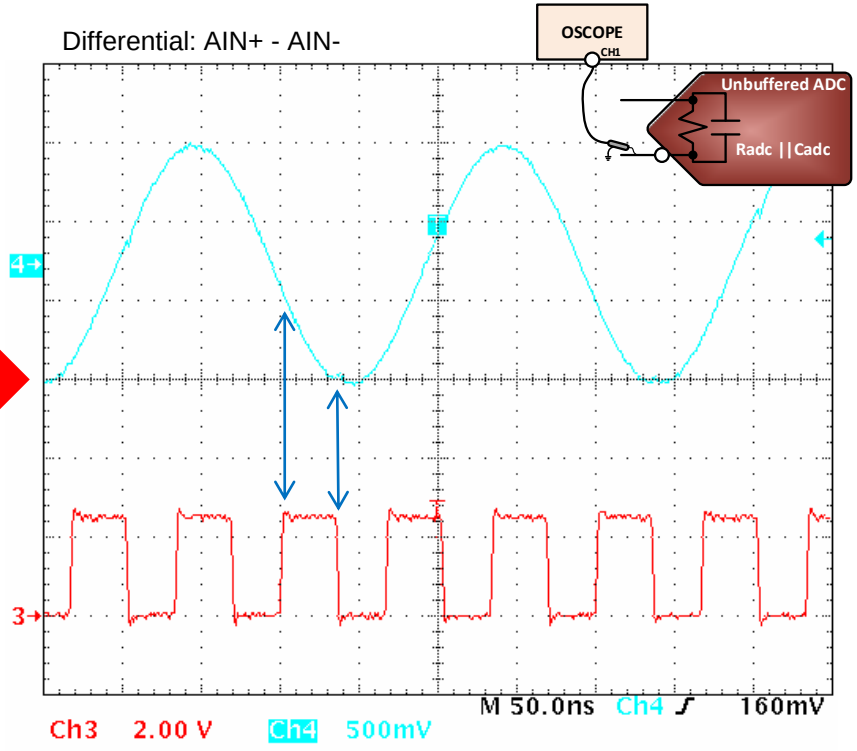
ADC types: unbuffered input architectures, cont. – TD

Single-Ended: AIN+ and AIN-



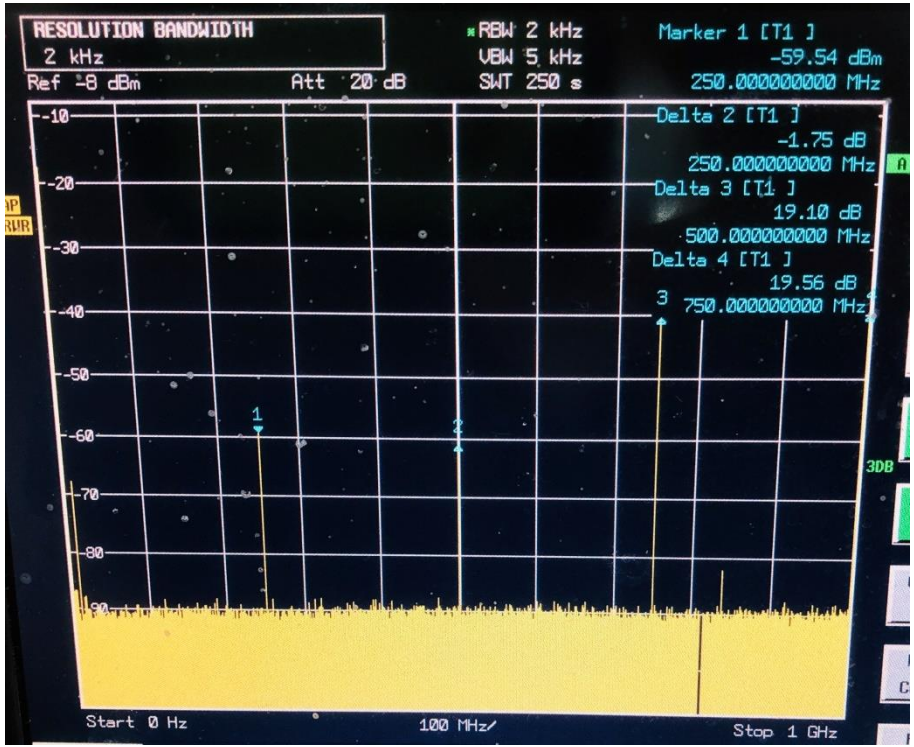
Charge injection glitches reflect back on the analog inputs relative to the sampling clock edges in the time domain.

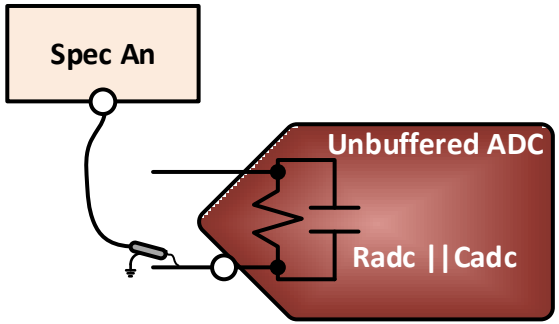
Differential: AIN+ - AIN-



Charge injection glitches subtract or common mode out on the analog input relative to the sampling clock edges.

ADC types: unbuffered input architectures, cont. – FD

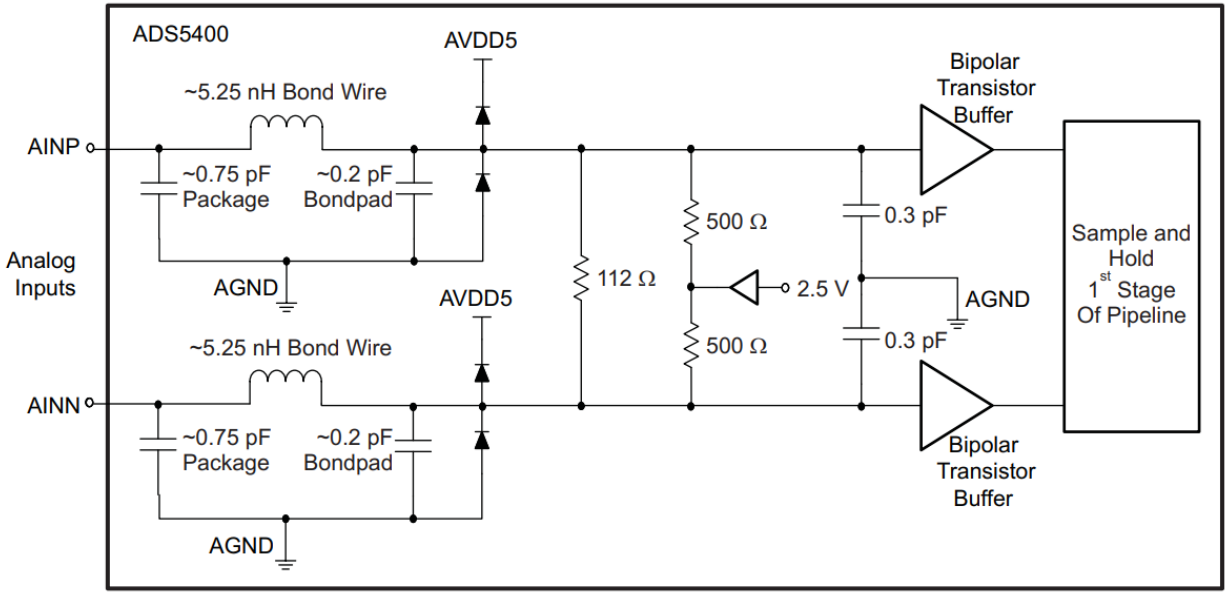




Fs = 250MSPS

Spectrum analyzer measurement at the analog inputs showing charge injection in the frequency domain

ADC types: buffered input architectures



ADS5400: buffered ADC input architecture, simplified

ADC types: buffered input architectures, cont. – input Z

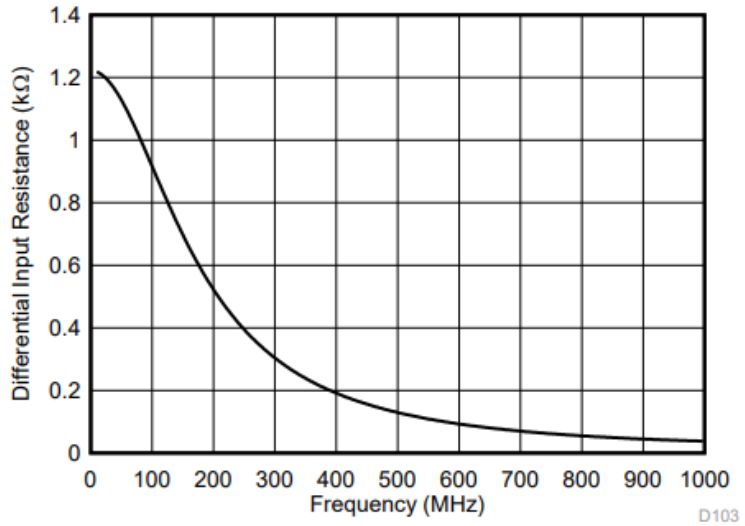


Figure 132. R_{IN} vs Input Frequency

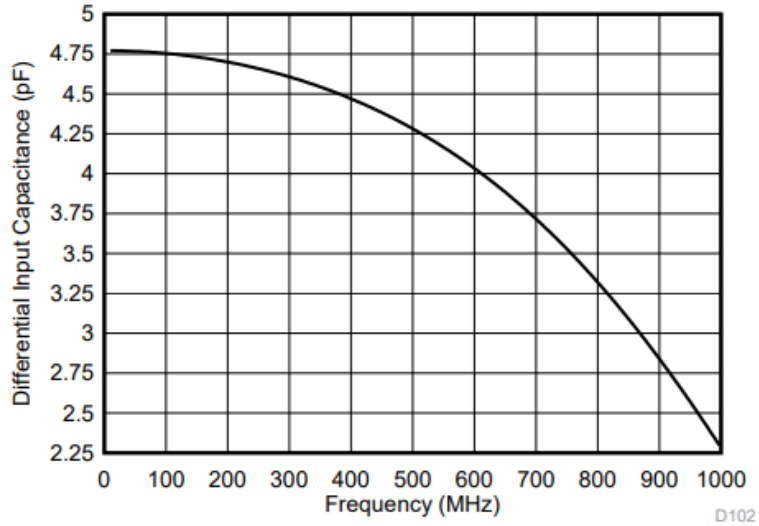
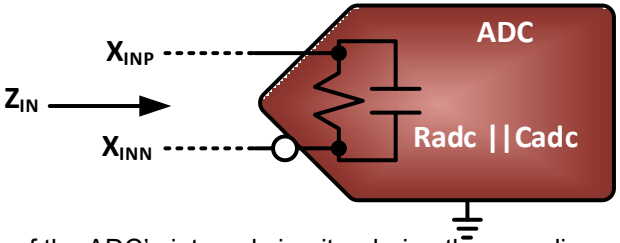


Figure 133. C_{IN} vs Input Frequency

ADS54J69: buffered ADC input Zin = Rin || Cin, measured

ADC types: ADC input architectures – quick input Z approx.



Note that the Rin & Cin values are a reflection of the ADC's internal circuitry during the sampling process in track mode—this is when the actual sample of the signal is taken. In hold mode, the sampling switch is open and isolates the input front-end circuitry from the internal sampling process or buffer.

If we derive the simple model and solve for the real and imaginary terms:
$Z_0 = R$, $Z_1 = 1/s*C$, $s = j*2*p*f$, f = frequency (1)

$Z_{IN} = 1/(1/Z_0 + 1/Z_1) = 1/(1/R + s*C) = 1/((1 + s*R*C)/R)) = R/(1 + s*R*C)$ (2)

Now sub in for s and multiply by the complex conjugate:
$Z_{IN} = R/(1 + j*2*p*f*R*C) = R/(1 + j*2*p*f*R*C)*((1 – j*2*p*f*R*C)/(1 – j*2*p*f*R*C)) = (R –j*2*p*f*R^2*C)/(1 + (2*p*f*R*C)^2)$ (3)

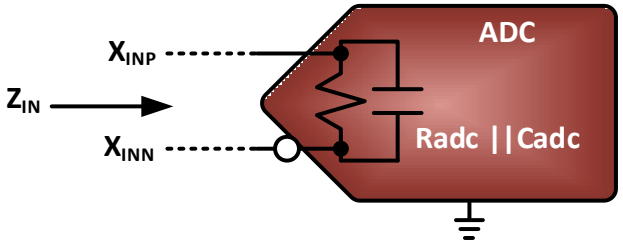
Now find the "real" and "imaginary" terms:
$Z_{IN} = Real + j*Imag = R/(1 + (2*p*f*R*C)^2) + j*(–2*p*f*R^2*C)/(1 + 2*p*f*R*C)^2)$ (4)

$Real = R/(1 + (2*p*f*R*C)^2)$ $Imag = (–2*p*f*R^2*C)/(1 + (2*p*f*R*C)^2)$ (5)

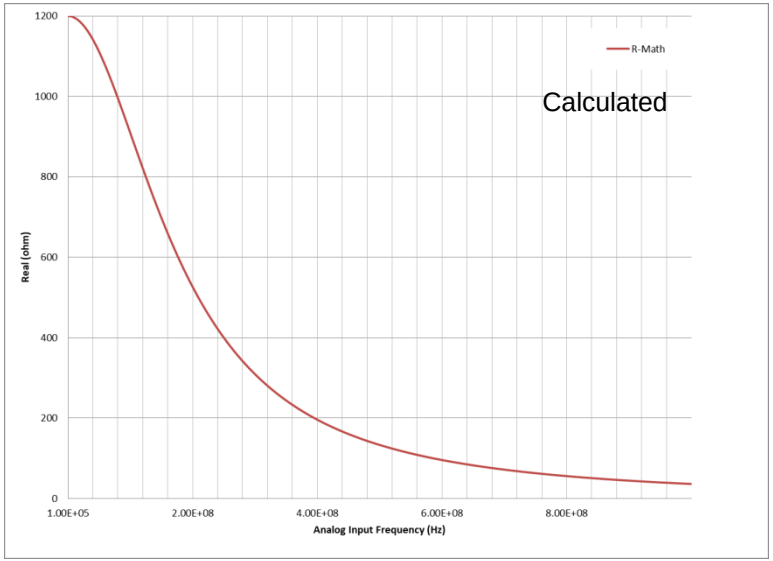
Spreadsheet calculator upon request

This mathematical model has proven to align well with the ac simulation in track mode.
The main source of error in this simple model is the settling level of the impedance at higher frequencies.

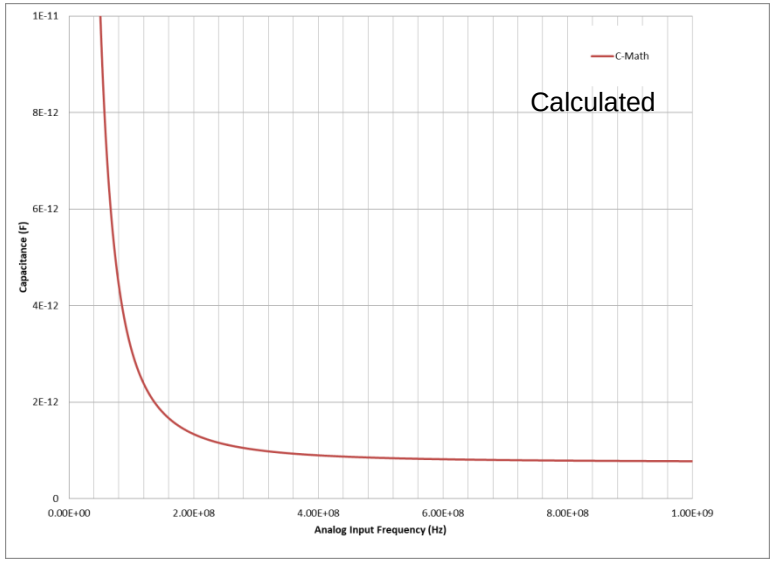
ADC types: ADC input architectures – quick input Z approx.



ADS54J69: Rin



ADS54J69: Cin

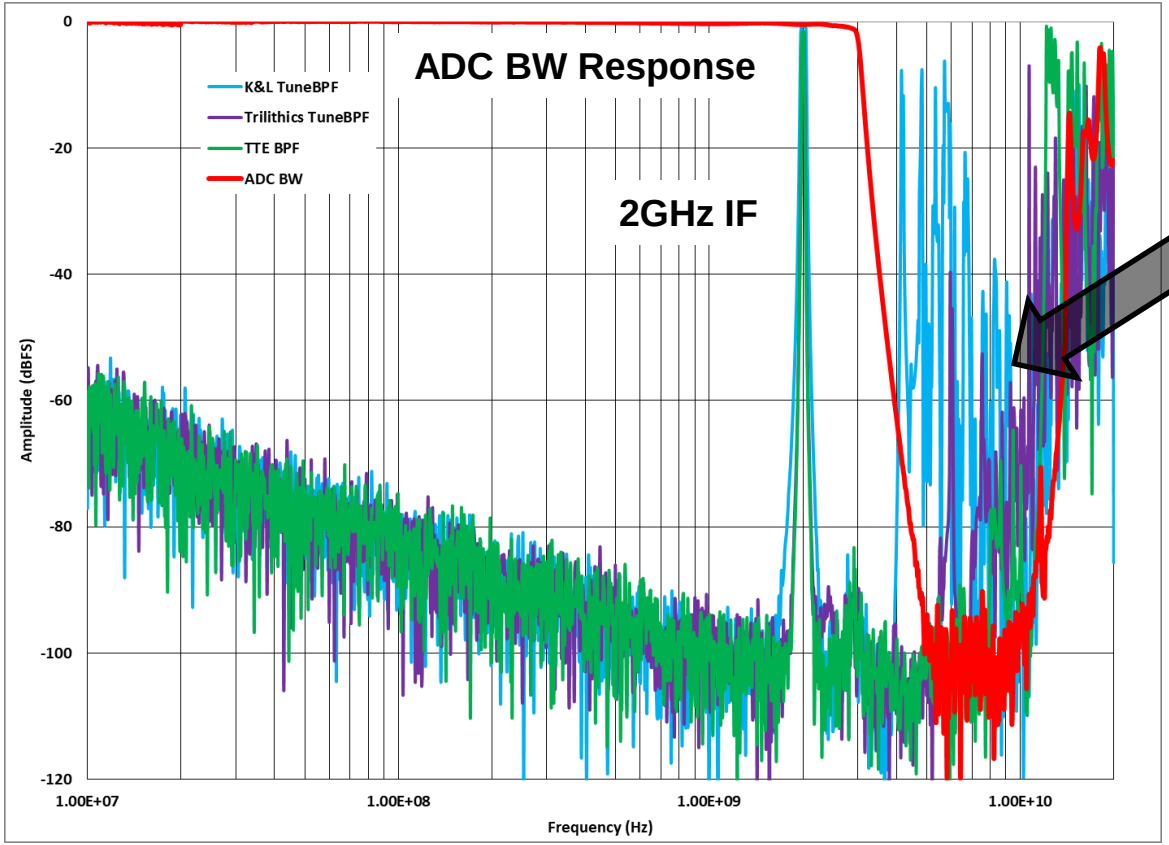


Spreadsheet calculator upon request

Anti-aliasing filters (AAF) – things to watch out for…

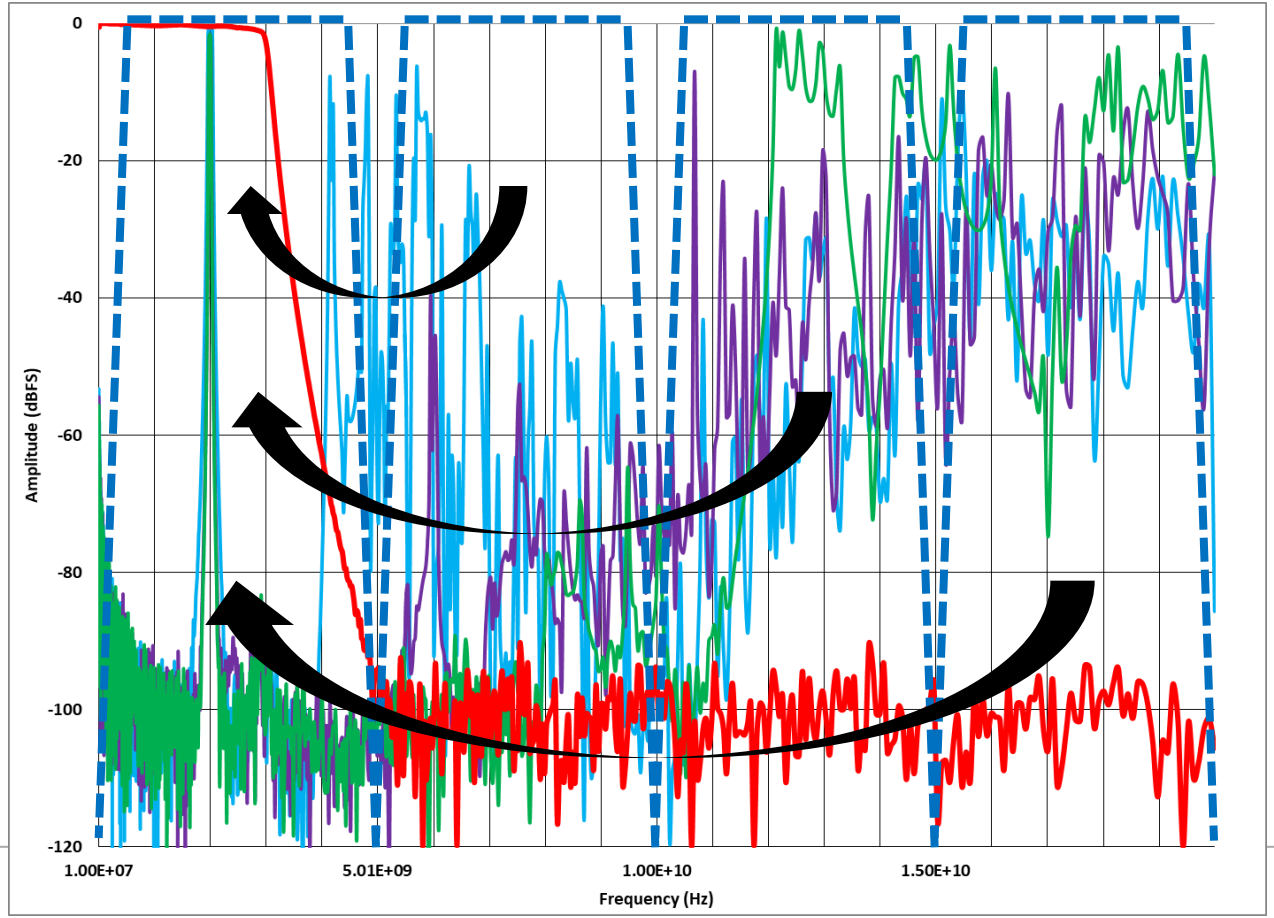
- Too many components in the AAF design can cause mismatches (component tolerance) in differential filters, therefore giving rise to even order distortions (HD2) due to imbalance
- Not all inductors are created equal, so model or simulate those inductors, so that, sim = pcb design
  - DL Sparameters, use Modelithics models or measure them on VNA
- Inductors can sometimes have assembly issues giving rise to poor connections due to hidden end tabs.
  - This can lead to distortion effects because of lop-sided filtering
- When designing an AAF or even using a filter to test an ADC, make sure the stopband region is specified to be flat, broadband noise can still fold back in-band, **see next slide…**

Anti-aliasing filters (AAF) – filter flyback example



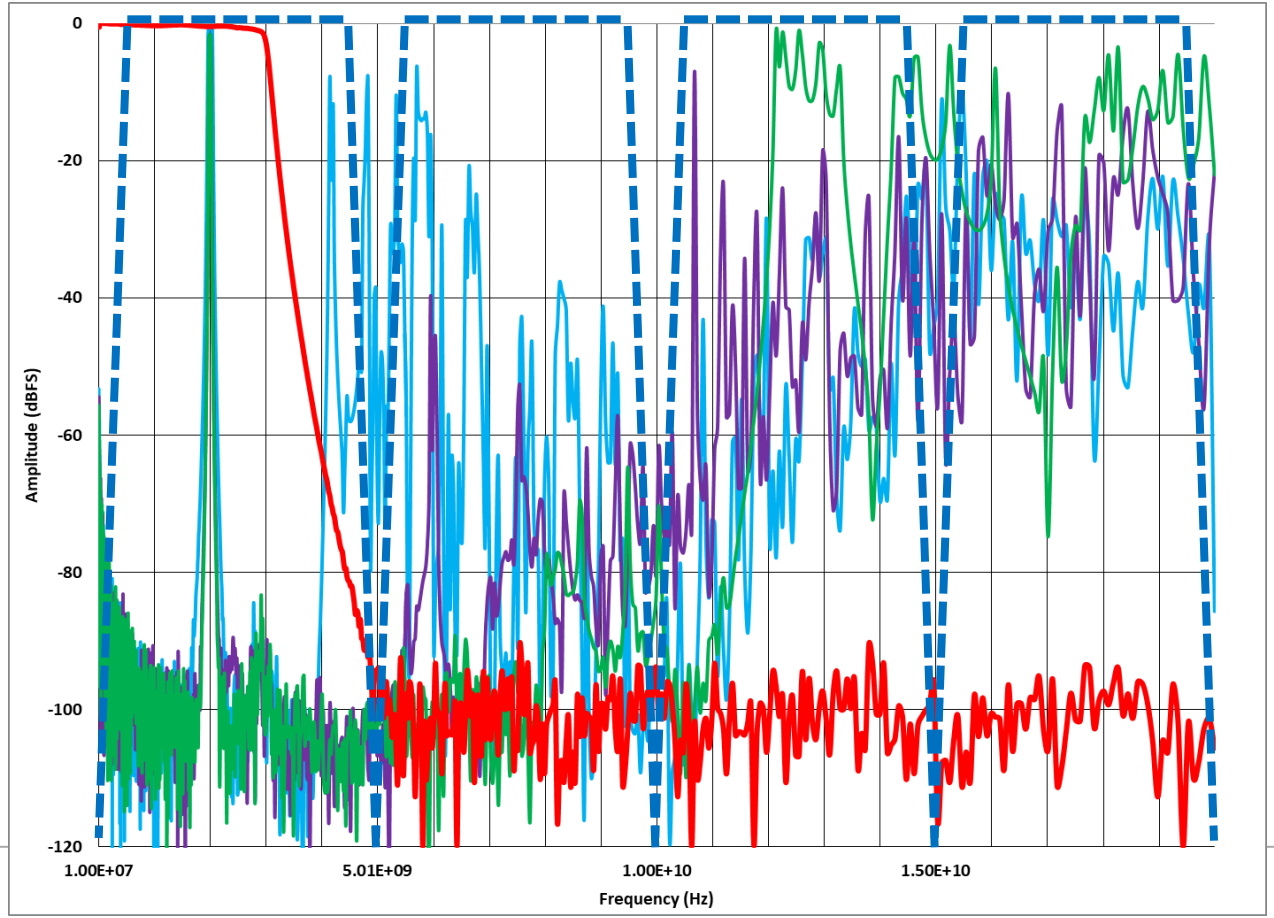
Filter flyback

Anti-Aliasing Filters (AAF) – Filter Flyback Example



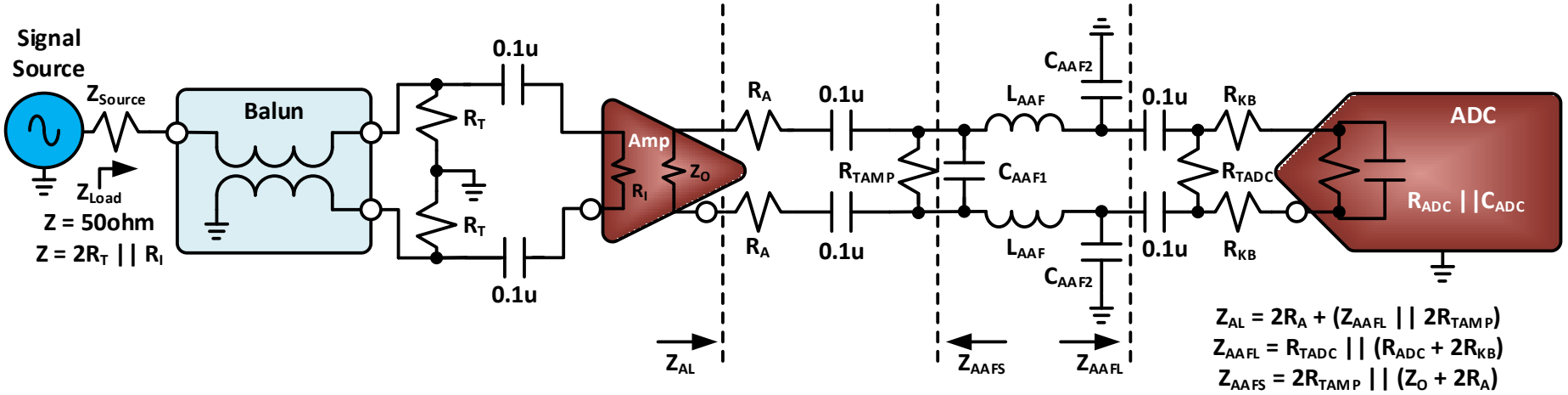
Fs = 10GSPS
Fs/2 = 5GHz = Baseband
IF = 2GHz

Anti-aliasing filters (AAF) – filter flyback example



Fs = 10GSPS
Fs/2 = 5GHz = Baseband
IF = 2GHz

Anti-aliasing filters (AAF) – design procedure



The amplifier should see the correct dc load recommended by the data sheet for optimum performance. 50ohm? 100ohm? 200ohm?, etc.

The correct amount of series resistance must be used between the amplifier and the load presented by the filter. This is to prevent undesired peaking in the pass band.

The input to the ADC should be reduced by an external parallel resistor, and the correct series resistance should be used to isolate the ADC from the filter. This series resistor also reduces peaking.

Anti-aliasing filters (AAF) – design procedure, cont.

The basic design process is as follows:
1) Select the external ADC termination resistor RTADC so that the parallel combination of RTADC and RADC is between 200 Ω and 400 Ω. This can help stabilize the filter design.
2) Select RKB based on experience and/or the ADC data sheet recommendations, typically between 5 Ω and 36 Ω.
3) Calculate the filter load impedance using: $ZAAFL = RTADC \parallel (RADC + 2RKB)$
4) Select the amplifier external series resistor RA.
    Make RA less than 10 Ω if the amplifier differential output impedance is 100 Ω to 200 Ω.
    Make RA between 5 Ω and 36 Ω if the output impedance of the amplifier is 12 Ω or less.
5) Select RTAMP so that the total load seen by the amplifier, ZAL, is optimum for the particular differential amplifier chosen using the equation: $ZAL = 2RA + (ZAAFL \parallel 2RTAMP)$.
6) Calculate the filter source resistance: $ZAAFS = 2RTAMP \parallel (ZO + 2RA)$.
7) Using a filter design program select the filter's source and load impedances, ZAAFS and ZAAFL, type of filter, bandwidth, and order. Use a bandwidth that is slightly higher than one-half the sampling rate to ensure flatness in the frequency span between dc and fs/2.
8) The internal ADC capacitance, CADC, should be subtracted from the final shunt capacitor value generated by the program. The program will give the value CSHUNT2 for the differential shunt capacitor. The final common-mode shunt capacitance is $CAAF2 = 2(CSHUNT2 - CADC)$.

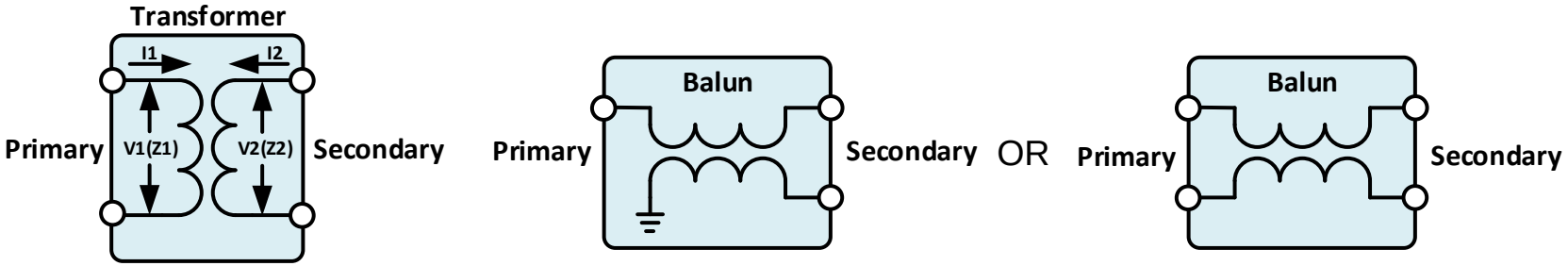
Anti-aliasing filters (AAF) – design procedure, cont.

After running these preliminary calculations, the circuit should be given a quick review for the following items.

1) The value of CAAF2 should be at least 10 pF so that it is several times larger than CADC. This minimizes the sensitivity of the filter to variations in CADC.
2) The ratio of ZAAFL to ZAAFS should not be more than about 7 so that the filter is within the limits of most filter tables and design programs.
3) The value of CAAF1 should be at least 5 pF to minimize sensitivity to parasitic capacitance and component variations.
4) The inductor, LAAF, should be a reasonable value of at least several nH.

In some cases, the filter design program may provide more than one unique solution, especially with higher order filters. The solution that uses the most reasonable set of component values should always be chosen. Also, choose a configuration that ends in a shunt capacitor so that it can be combined with the ADC input capacitance.

Transformers & baluns – The basics



Turns ratio

$n = N1/N2$

Defines the ratio of primary voltage to secondary voltage

Impedance ratio

$n^2 = Z1/Z2$

Seen as the primary reflected from the secondary, the square of the turns ratio

The transformer's signal gain

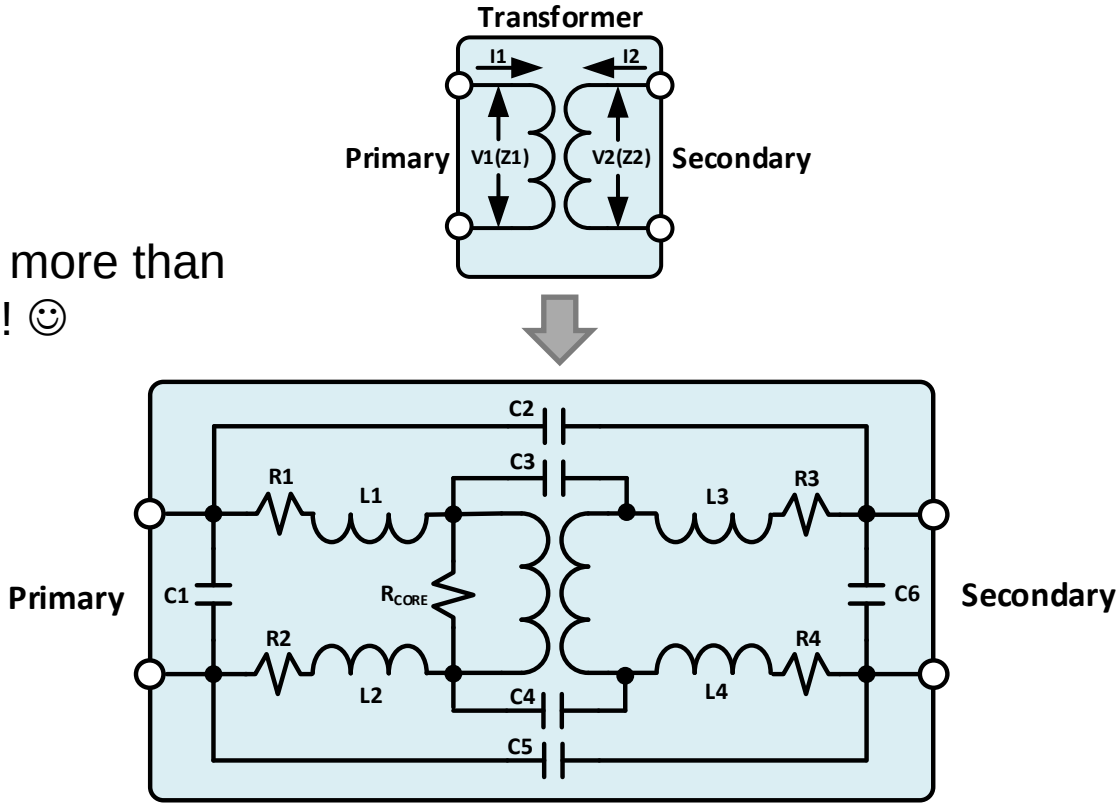
$20 \log (V2/V1) = 10 \log (Z2/Z1)$

A transformer with a voltage gain of 3 dB would have a 1:2 impedance ratio

This is good since data converters are voltage devices. Voltage gain is noise FREE!

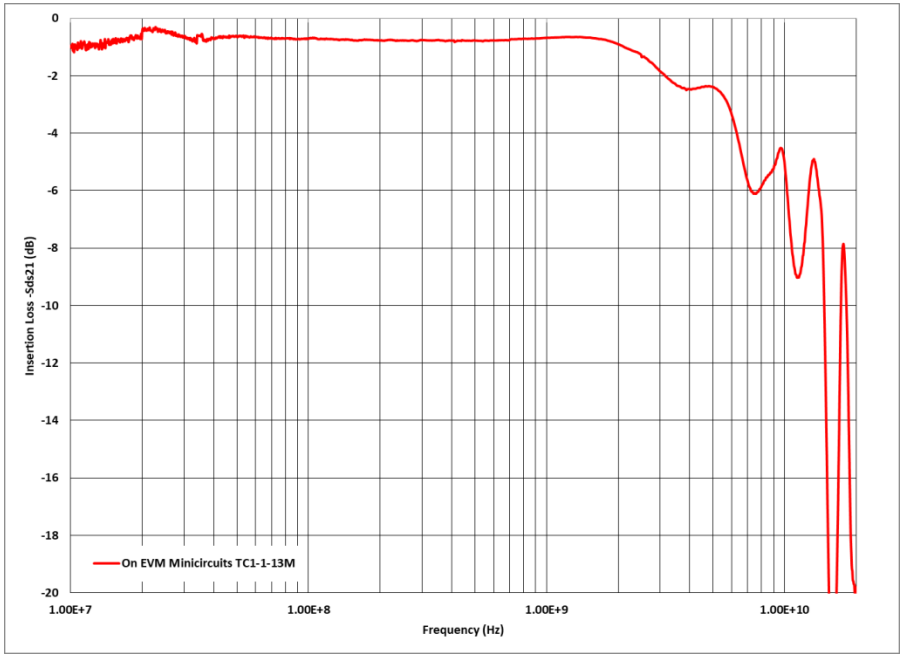
Transformers & baluns – models & parasitics

…as they say:
Transformers, more than meets the eye! ☺

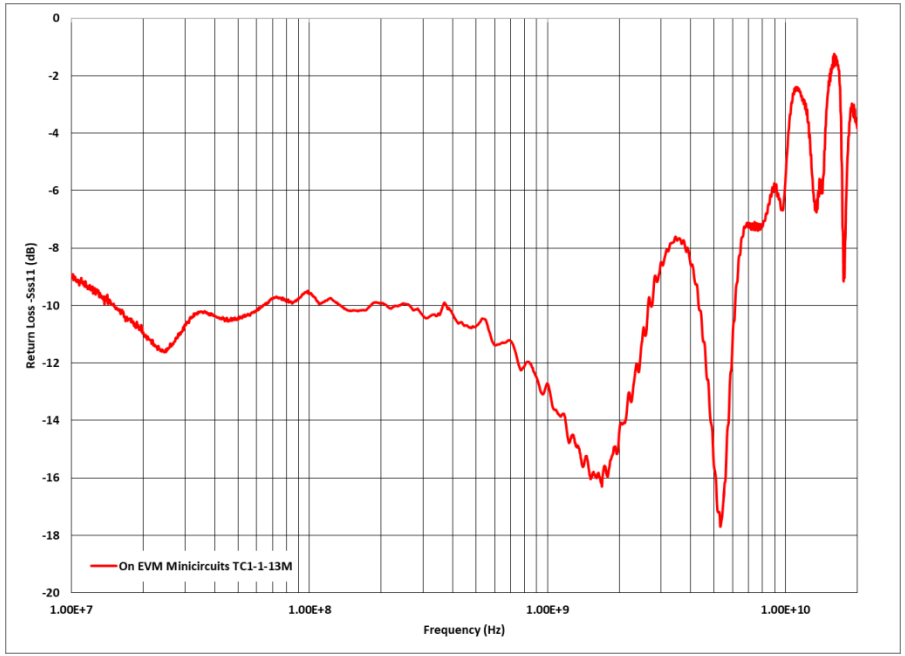


Transformers & baluns - specifications

Insertion loss

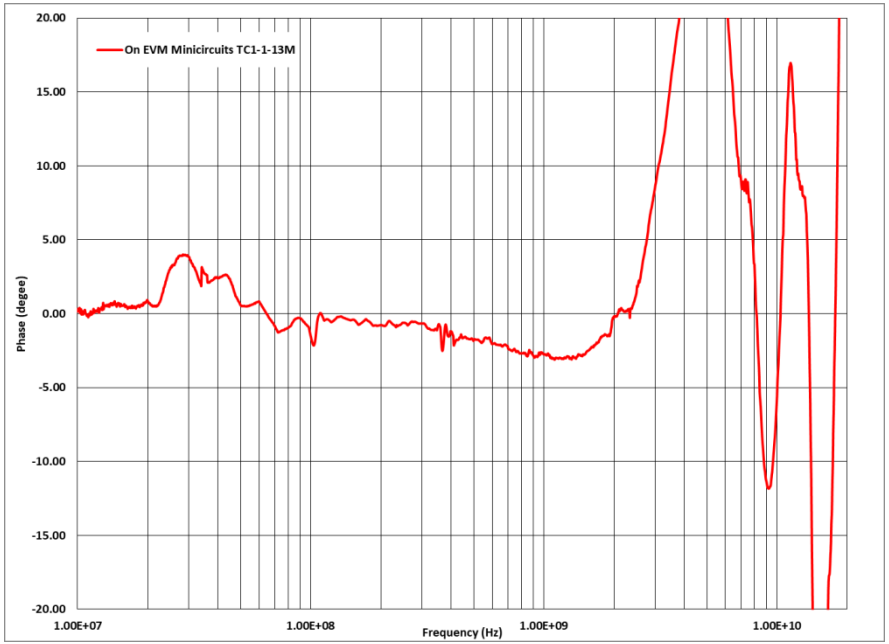


Return loss

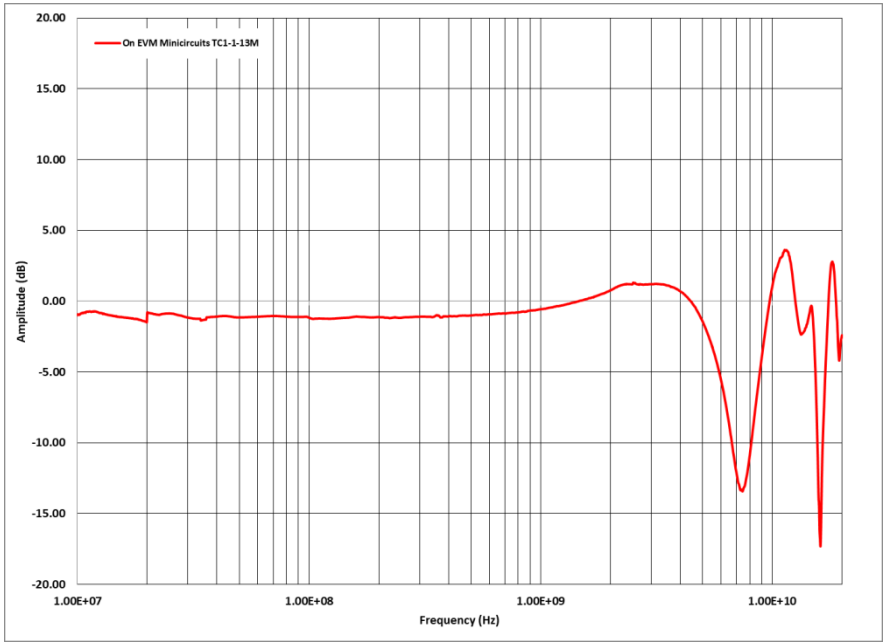


Transformers & baluns – specifications, cont.

PhaseImbal

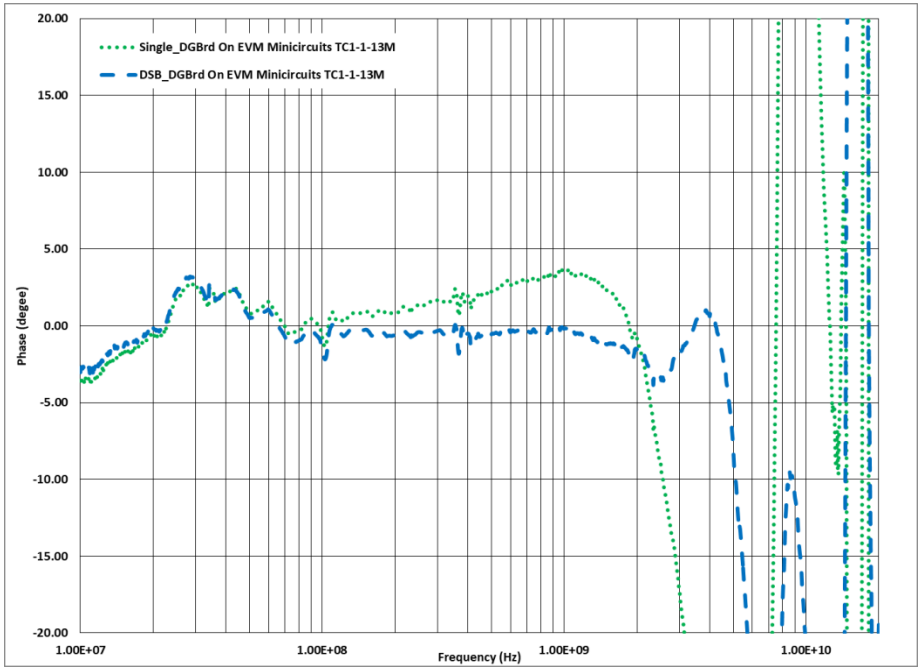


MagImbal

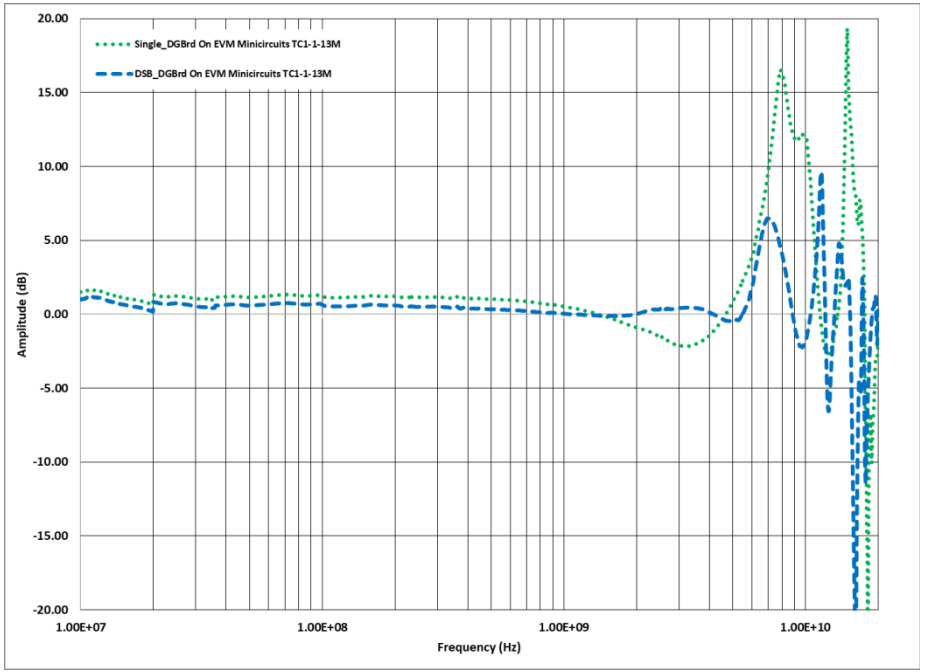


Transformers & baluns – balancing

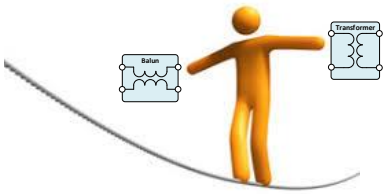
PhaseImbal – single vs. double



MagImbal – single vs. double



Transformers & baluns – balancing



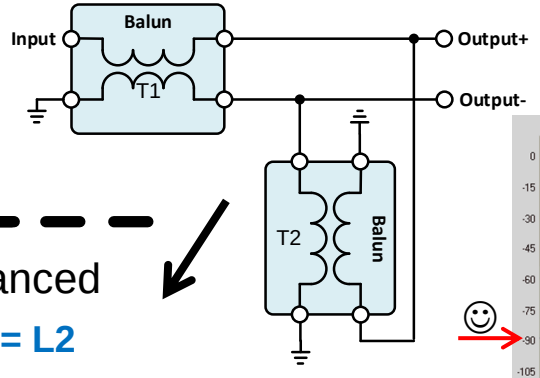
◆**Layout** is another variable that can wreak havoc on any frontend design.
Improper layout can literally mess up the frontend design causing unexpected performance.
Take the time to keep the layout sound and symmetrical.

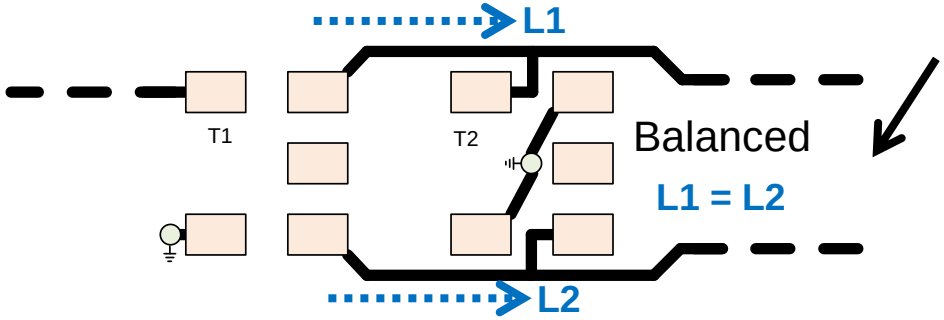
◆Keeping the frontend network symmetrical, forces return currents or ground references to be common.

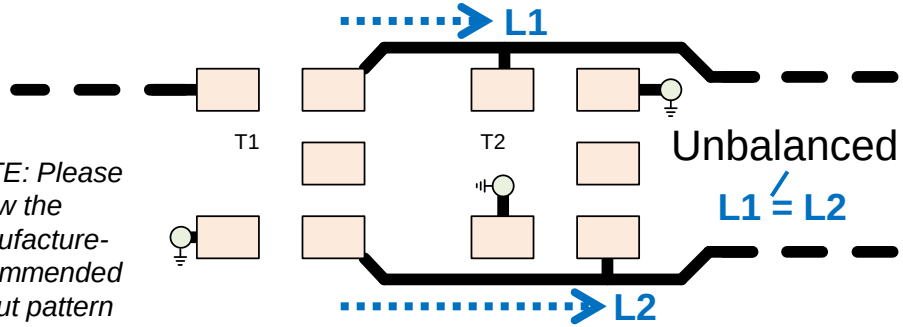
◆This next slide shows an example of an FFT performance plot, using the symmetrical layout:
This yielded a 2nd harmonic of 85dB with a 140MHz IF applied at -1dBFS.

◆The figure on the bottom shows the performance under these same conditions however, a non-symmetrical layout was used.
This consistently yields a 2nd harmonic of 79.5dB, more than 5dB lost in performance!

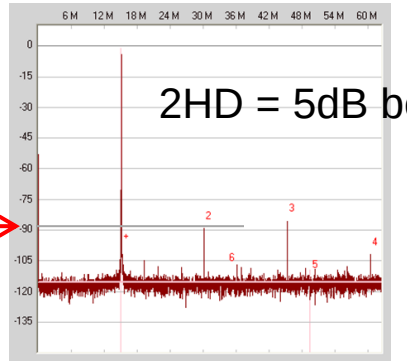
Transformers & baluns – balancing example

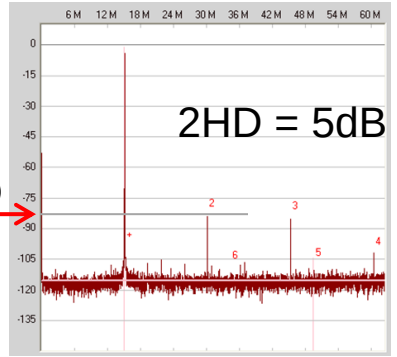






FFT performance results

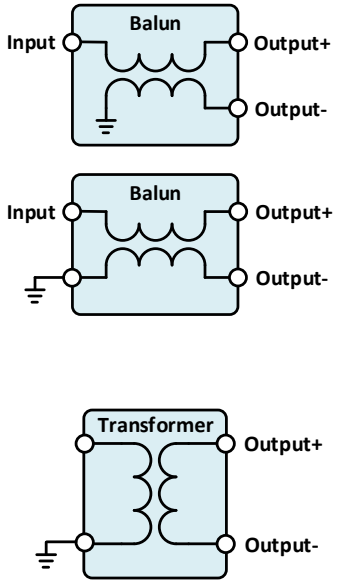




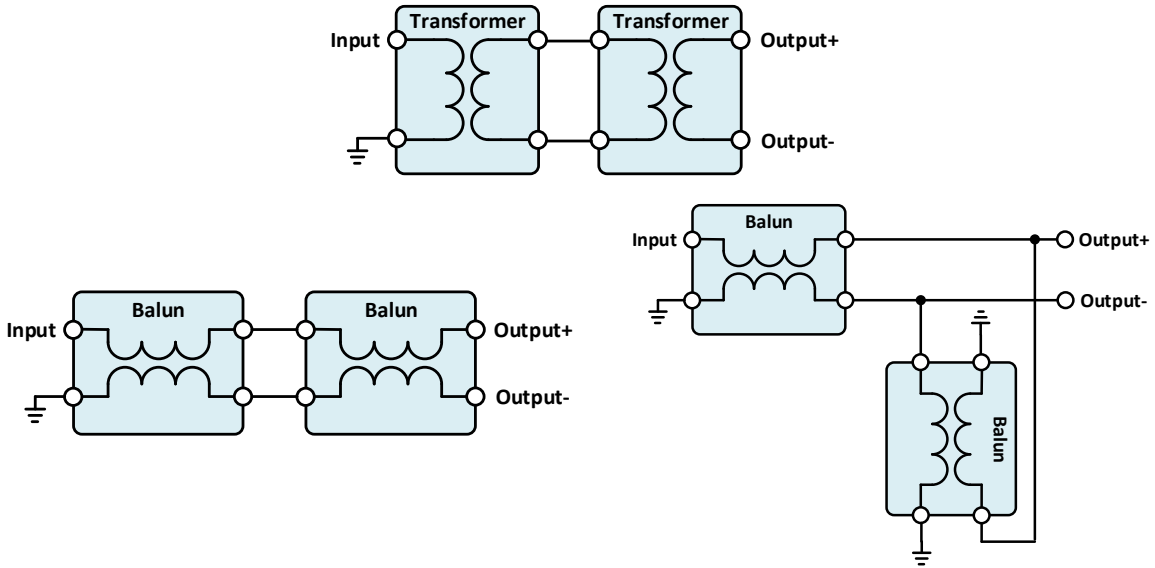
NOTE: Please follow the manufacture-recommended layout pattern

Transformers & baluns – configurations

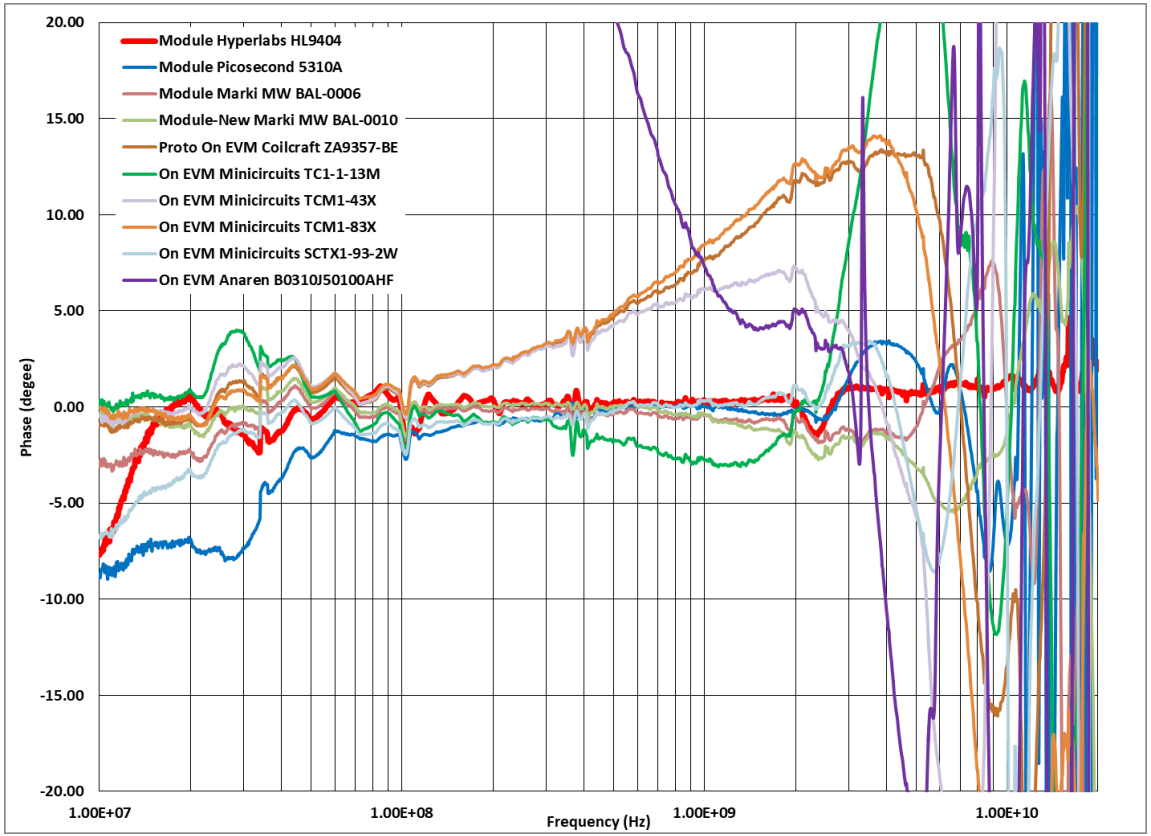
Single configurations



Double configurations (for improved phase imbalance)



Transformers & baluns - tradeoffs



Bottom line:
Find a better balun or use two baluns to help improve the HD2 specification

Amplifier – balancing

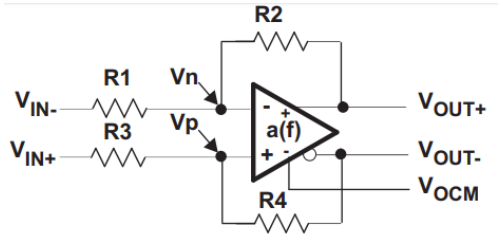
• Tolerances in passive components can hurt performance too. This can be seen at the summing nodes in the feedback loop of an amplifier and multi-pole anti-aliasing filters between amplifiers and converters. Simple mismatches here can be seen in the math.

• Take for example the differential amplifier analysis below. A common mode voltage mismatch can be developed if the component tolerances of R1(Rg) and R2(Rf) are not tight.

• Notice that beta (β) is the ratio of these two resistors on either side of the amplifier. Any mismatch here will cause the summing node Vacm to be slightly different as these resistors drift over the tolerance itself, the temperature variation and over life.

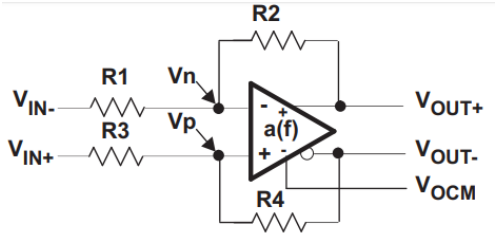
• A difference in Vn & Vp will ultimately cause Vout+ and Vout- to be different on the amplifier's outputs, giving rise to second order distortion.

• To combat this, make sure the component tolerances are low (<1%). If accuracy is important, specialized resistor packs can be procured that offer low ppm drifts and tight tracking tolerances. One of the reasons TI puts matched resistor gain networks inside our high-speed amplifiers is for this reason.



NOTE: Amplifiers with internal resistors are better matched

Amplifier – balancing, cont.



NOTE: SLVA417 – DC output errors in a fully differential amplifier

Quantity	Symbol	General Expression	Asymptotic Form
Feedback factors	β_1,β_2	$\beta_1 = R3/(R3 + R4)$, $\beta_2 = R1/(R1 + R2)$	
Coefficients	b_1,b_2	$b_1 = \left(1+\frac{1}{2CMRR}\right)$ $b_2=\left(1-\frac{1}{2CMRR}\right)$	
Equivalent resistances	R_{EQ1},R_{EQ2}	$R_{EQ1} = R1 \parallel R2$, $R_{EQ2} = R3 \parallel R4$	
Applied input common-mode	V_{ICM}	$V_{ICM} = \frac{(V_{IN-} + V_{IN+})}{2}$	
Desired output	$V_{OD,\ Desired}$	$V_{id}\frac{2 - (\beta_1+\beta_2)-\frac{1}{2CMRR}(\beta_1 - \beta_2)}{(\beta_1 + \beta_2) + \frac{1}{2CMRR}(\beta_1 - \beta_2) + \frac{2}{a}}$	$V_{id}\left(\frac{1-\beta}{\beta}\right)$

Frontend VCM - common mode voltage follies in ADCs

• Since converter supply ranges are between VDD and GND and the process nodes are getting smaller, this leave little room for headroom error.

•The ADC's analog inputs have an inherent common mode voltage (VCM) bias that establishes the "zero code" for the converter's input signal to swing around.

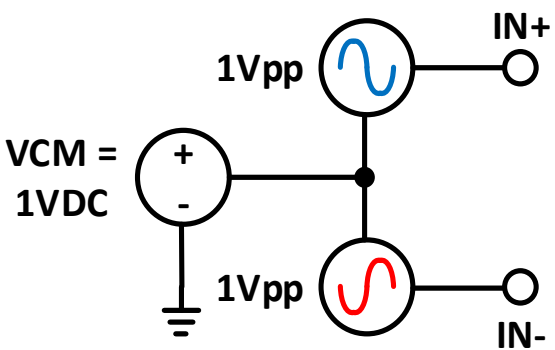
• Any deviation in the VCM voltage on either analog input, puts the converter's performance in serious jeopardy…

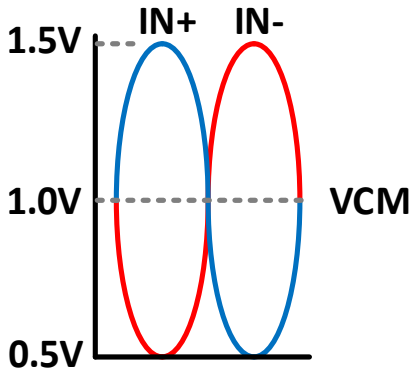
- •Why? Because the VCM helps establish the input fullscale range of the converter
- •Any deviation allow for clipping or over-ranging to occur early

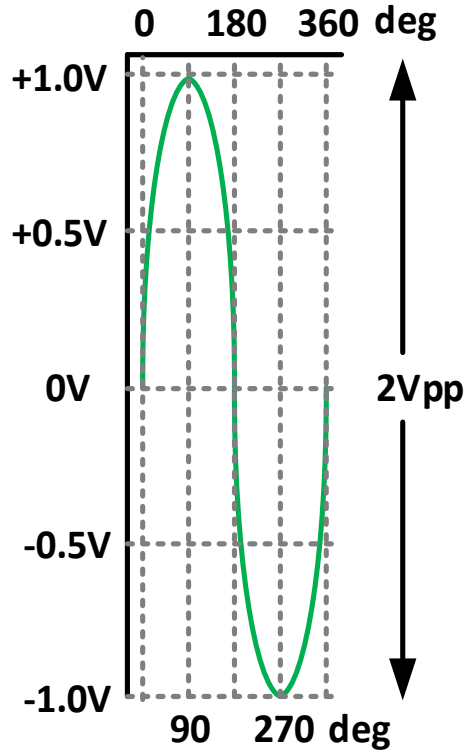
•A quick review of the converter's analog inputs signal is on the next slide….

Frontend VCM – analog input signal review

2Vpp differentially balanced signals







Vx(t) = Vpk * sin(wt) + VCM
= 1*sin(wt) @ 90 = +1Vpk
= 1*sin(wt) @ 270 = -1Vpk
= 2Vpp

Frontend VCM – buffered vs. unbuffered ADCs

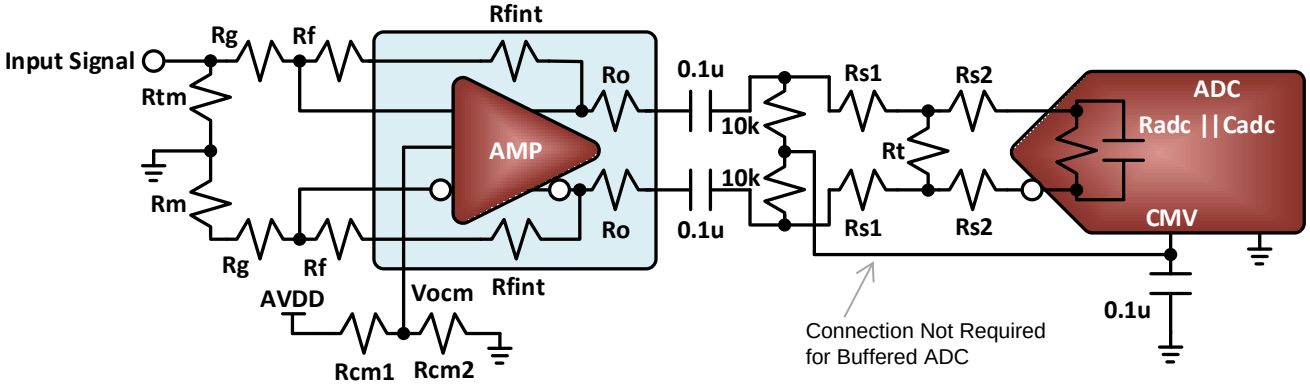
• Unbuffered converters (aka: switched-capacitor type) require an external VCM bias on the analog inputs, typically the VCM = AVDD/2 or half the analog supply

• Buffered converters typically have self-biased analog inputs and are set by the converter's internal buffer, VCM is typically half of the supply, plus a diode drop above or AVDD/2+0.7V

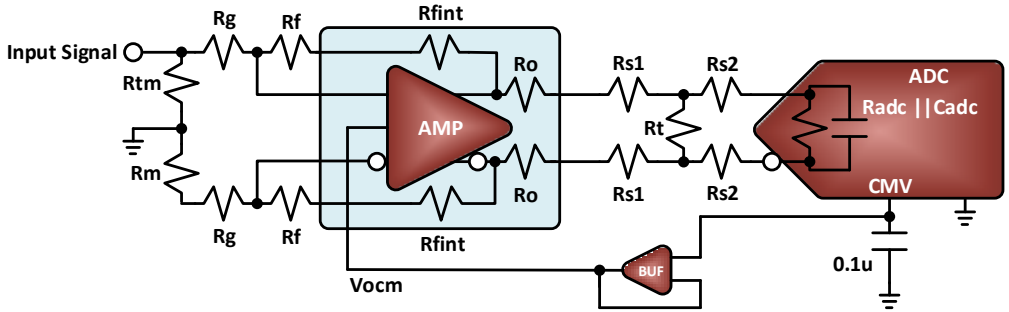
• DC coupled application notes:
  - Make sure the amplifier can meet the VCM requirement of the ADC
  - Any VCM mis-match between the amp and ADC or either input differential pin, even if small, can create performance issues, ie – early clipping
  - Adding a buffer amp between the ADC and Amp is preferred

Frontend VCM – AC vs. DC coupled examples

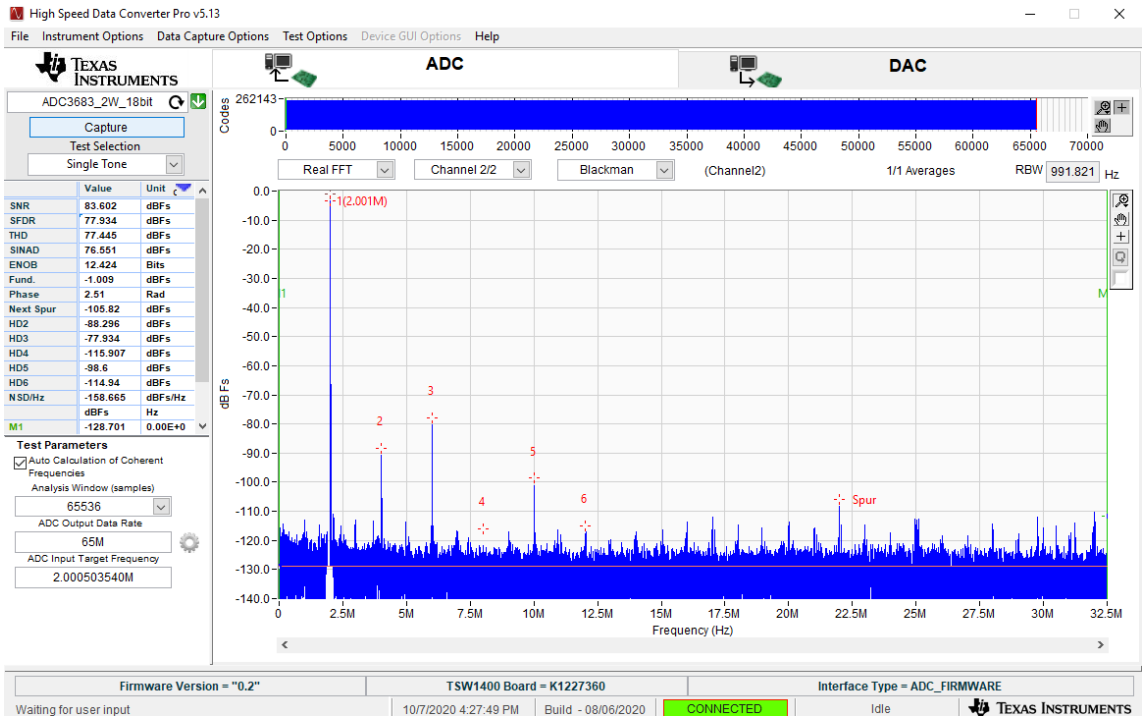
AC coupled

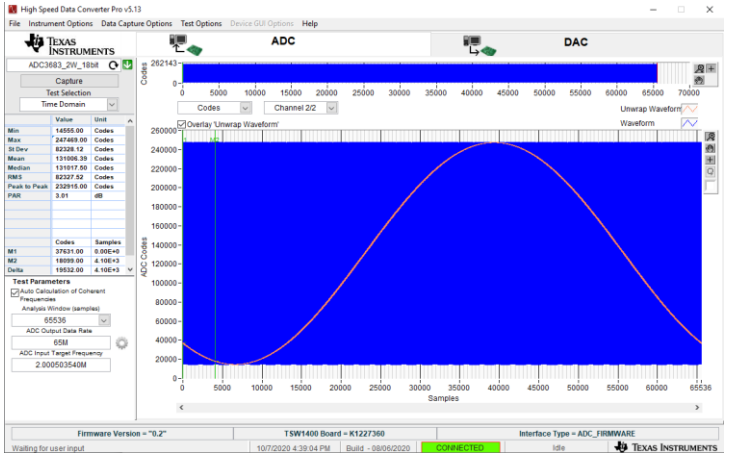


DC coupled

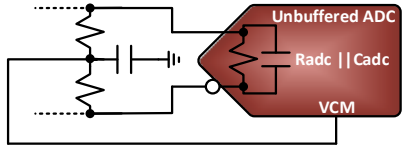


Frontend VCM – “common” issues, baseline

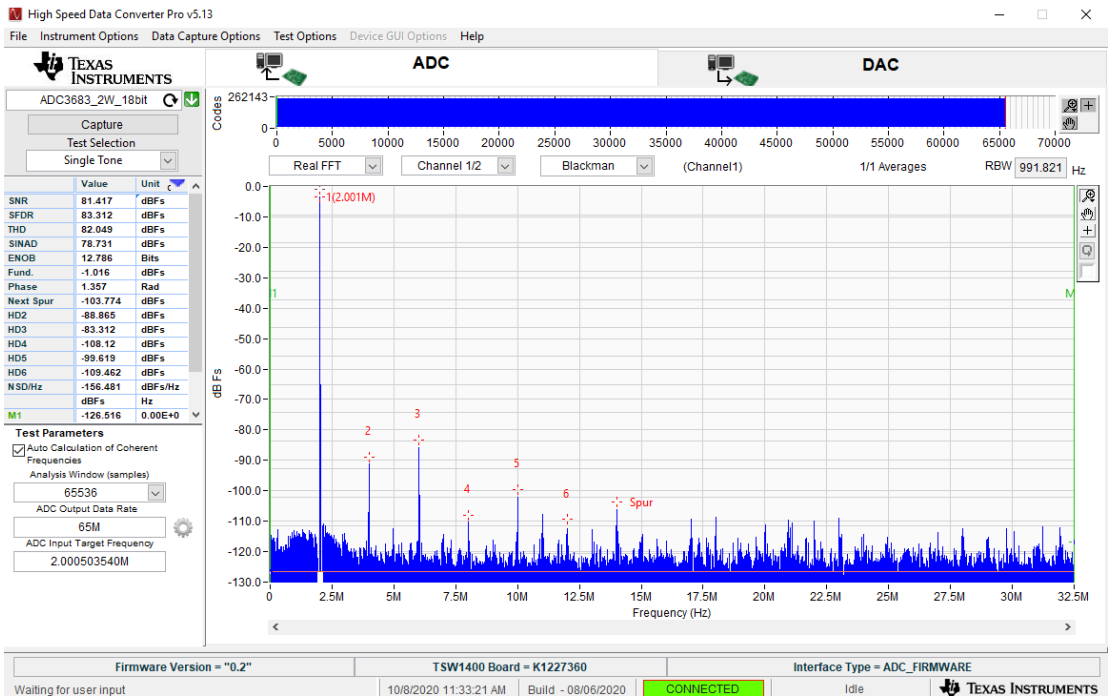


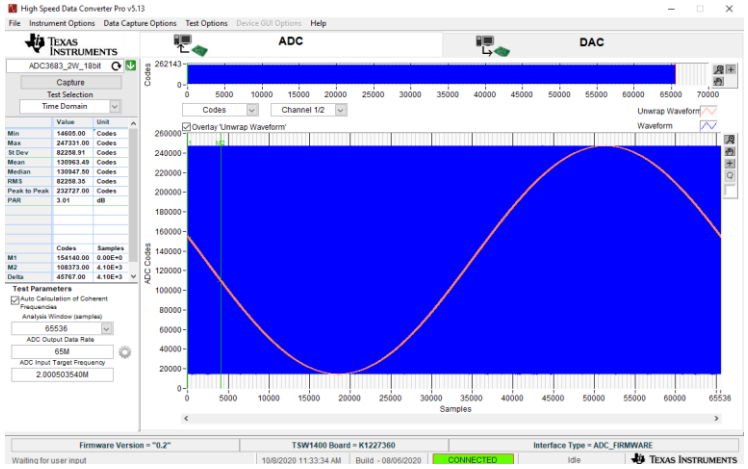


Baseline

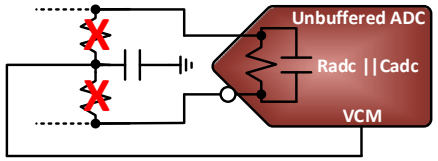


Frontend VCM – “common” issues, VCM floating

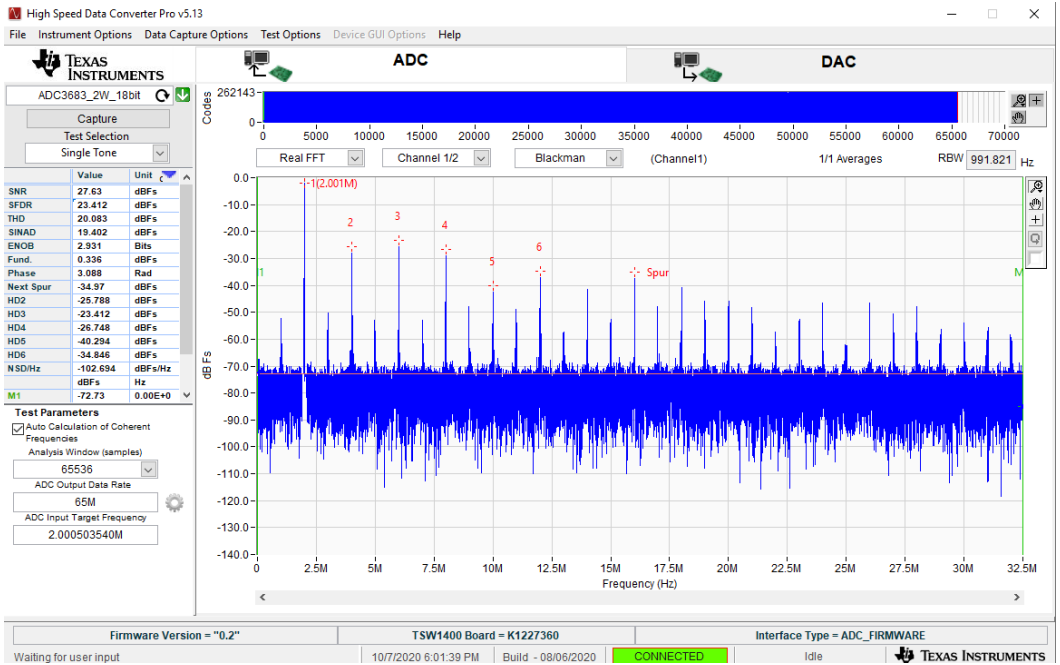


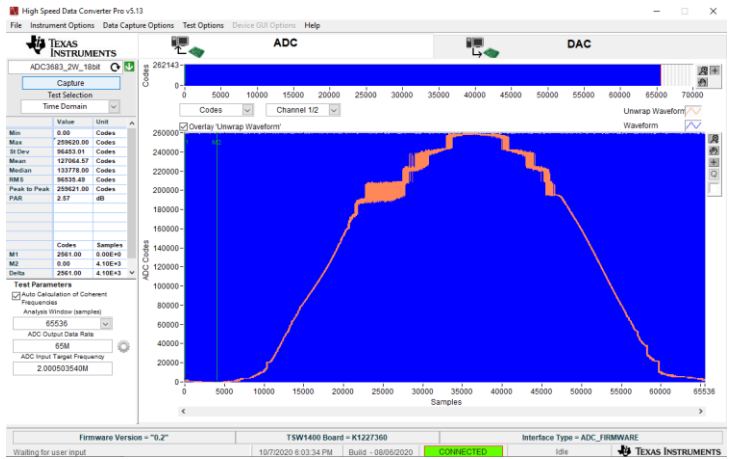


VCM Floating

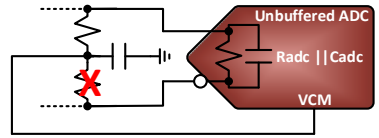


Frontend VCM – “common” issues, VCM mismatch

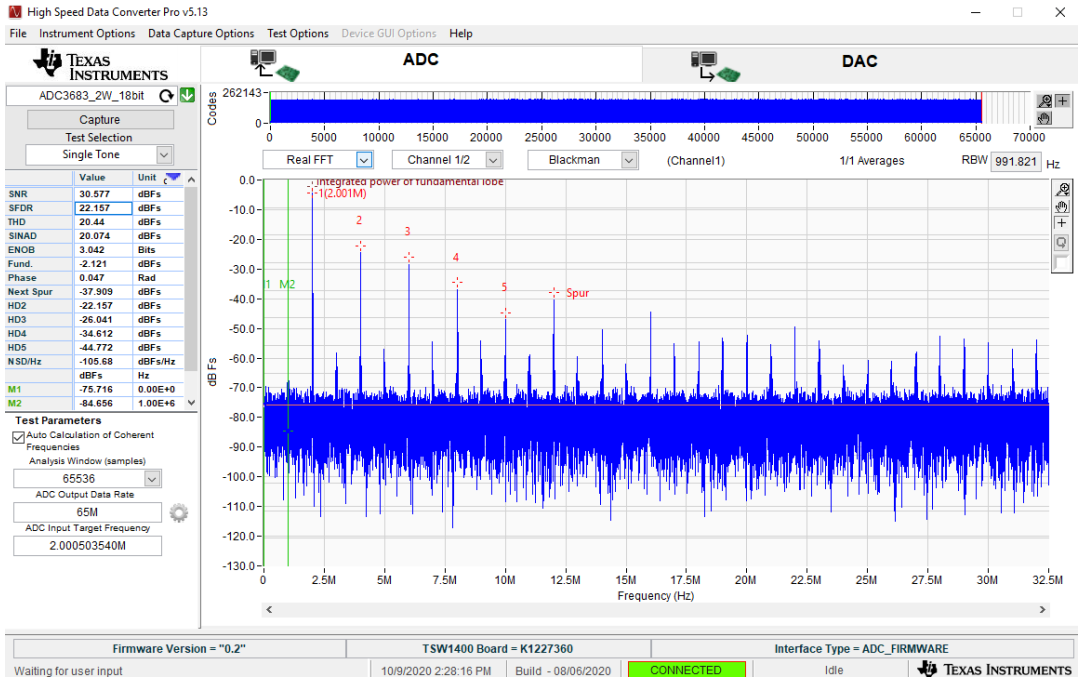


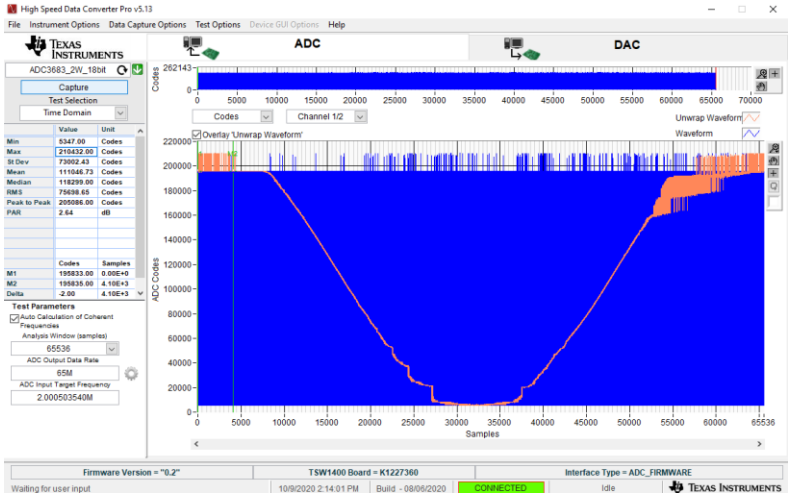


Unequal
VCM
AINP = AINN

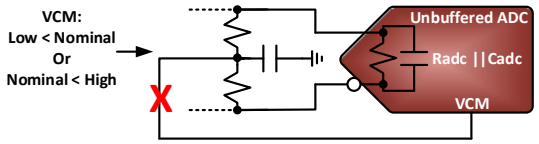


Frontend VCM – “common” issues, VCM too high or low



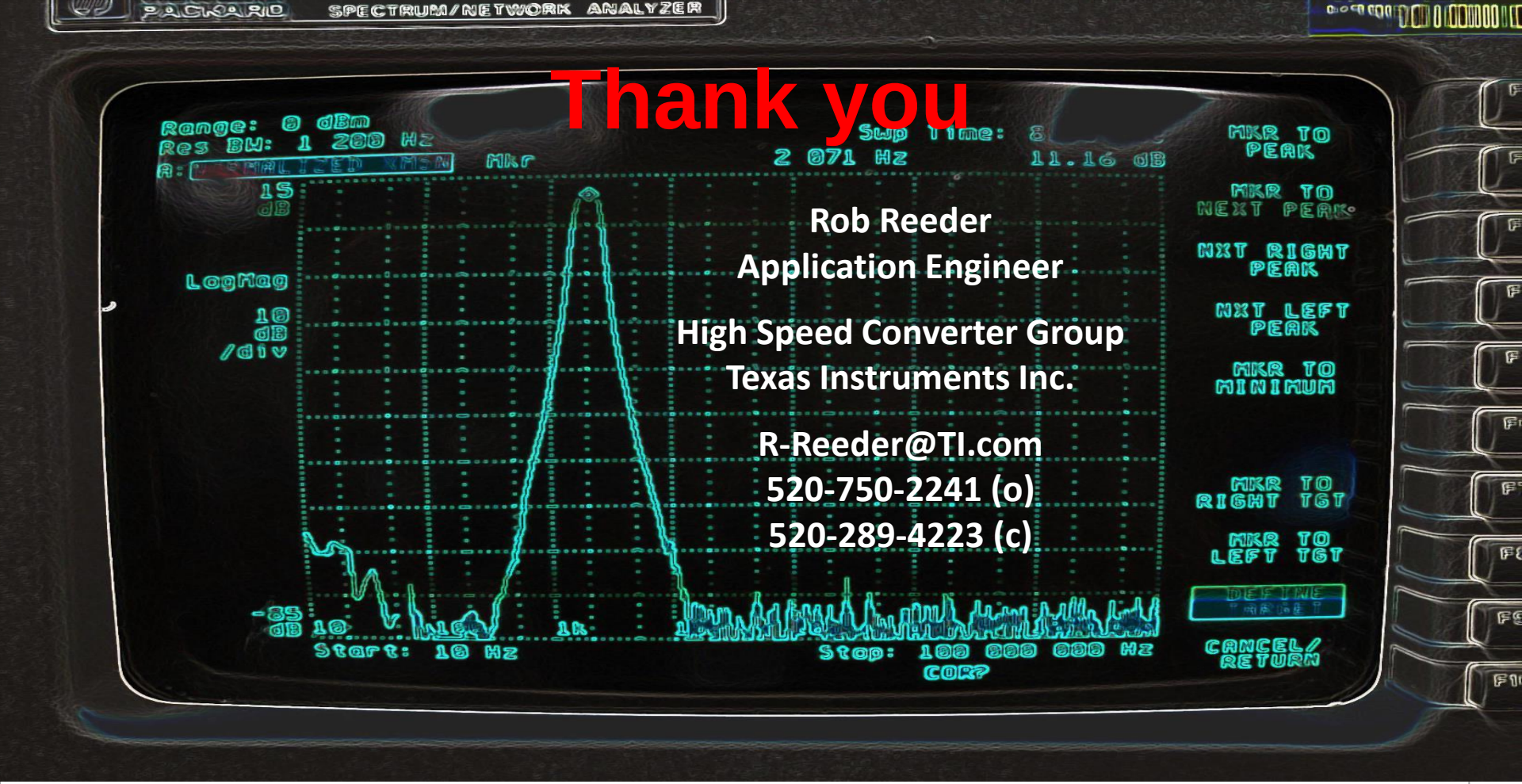


AINn VCM ≠ AINp VCM



Front-end eummary

- Understand and define the front-end design goals up front…
- “Matching” is just a fancy RF word which translates to ADC optimization…
- Understanding the application can zero in on the front-end amp or balun of choice….
- What’s your converter type? Buffered vs. unbuffered…
- A good impedance curves vs. frequency can be estimated by the ADC AIN internal R||C…
- Understand the AAF pitfalls and make sure your filters are filtering…
- Check for balancing issues, might need a better balun! Or lower tolerance resistors around the amp…
- Keep common modes common between amps and ADCs…don’t let them fight for VCM equilibrium…
- **It’s not really a mystery after all…☺**



Thank you

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520-750-2241 (o)

520-289-4223 (c)

Front-end references

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- AN-742: Frequency Domain Response of Switched Capacitor ADCs, Rob Reeder, Analog Devices, Inc.
- MT-230: Noise Considerations in High Speed Converter Signal Chains, Rob Reeder, Analog Devices, Inc.

Useful converter equations

Theoretical Signal-to-Noise Ratio (SNR)

RMS Signal =(FSR / 2)/ sqrt(2), RMS Noise = Qn = q/ sqrt(12)

SNR (dB) = RMS Signal / RMS Noise = $20*\log(2^{(n-1)}*\text{sqrt}(6)) = 6.02*n + 1.76$

Total Harmonic Distortion (THD)

THD (-dB) = $20*\log(\text{sqrt}((10^{(-2ND\ HAR/20)})^2 + (10^{(-3RD\ HAR/20)})^2 + \ldots (10^{(-6TH\ HAR/20)})^2)$

Signal-to-Noise Ratio and Distortion (SINAD)

SINAD (dB) = $-20*\log(\text{sqrt}(10^{(-SNR\ W/O\ DIST/10)} + 10^{(THD/10)}))$

Effective Number of Bits (ENOB)

ENOB (BITS) = (SINAD – 1.76 + 20*log(FSR/ActualFSR))/ 6.02

Theoretical Noise Floor

Noise Floor (-dB) = 6.02*n + 1.76 + 10*log (N/2),
(See Table1), Assume coherent sampling and no windowing

Noise Floor (-dB) = 6.02*n + 10*log (3*N/(π∗ENBW)),
Assume noncoherent sampling and no windowing

Noise Spectral Density (NSD)

NSD (dBFS/Hz) = SNR + 10*log (Fs/2), Fs = sampling clock rate

Table 1

FFT Points	12-BIT	14-BIT	16-BIT
1024	101	113	125
2048	104	116	128
4096	107	119	131
8192	110	122	134
16384	113	125	137
32768	116	128	140
SNR (dB)	74.0	86.0	98.1

Definitions / terms

Fs = Sampling Rate (Hz)
Fin = Input Signal Frequency (Hz)
FSR = Full Scale Range (V)
n = Number of Bits
q = LSB Size
Qn = Quantization Noise
LSB = Least Significant Bit = $FSR/2^n$
N = Number of FFT Points
ENBW = Equivalent Noise Bandwidth of window function (Example: Four-Term Blackman-Harris Window, ENBW = 2)

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