Unraveling the practical mysteries behind RF converter front ends

Rob Reeder

Data Converters – High-Speed Converters
The term “front end” generally implies that this is a network or coupling circuit that connects between the last stage of the signal chain (usually an amplifier, gain block or tuner) and the converter’s analog inputs.

In order to achieve DS performance the designer must understand the frontend goals.

There are typically two types of front ends, they are passive or active.

It must also be very linear, well balanced and properly laid out on the printed circuit board (PCB) in order to preserve the signal content properly.
Front-end goals & definitions

◆ Designing an input network is important because it allows for a complete evaluation over the converter’s entire useable band.

◆ When designing the network there are five parameters to keep in mind:

  ● **Input impedance / VSWR** (voltage standing wave ratio) is a unitless parameter that shows how much power is being reflected into the load over the bandwidth of interest. Input impedance of the network is specified value of the load, usually this is 50ohms.

  ● **Passband flatness** is usually defined as the amount of fluctuation/ripple that can be tolerated within the specified bandwidth. 1.0dB, ±0.5dB, could be more, could be less, could be defined with a slope.

  ● **Bandwidth** is simply the beginning and ending of the frequencies to be used in the system. Typically -3dB from some reference point.

  ● **SNR** (signal-to-noise ratio) / **SFDR** (spurious free dynamic range)

  ● **Input drive level** is a function of the bandwidth, input impedance, and VSWR specifications. This sets the gain/amplitude required for a full-scale input signal at the converter. It is highly dependent on the frontend components chosen – i.e., transformer, amplifier, AAF – and can be one of the most difficult parameters to achieve.
Front-end goals & definitions: to match or not to match?

- The word “match” is a term that should be used wisely. Keep in mind an ADC is a voltage sensitive device that typically has poor VSWR and return loss on the analog input pins.
- Therefore, it is almost impossible to match a ADC front ends that samples at 100s of MSPS, let alone +1GSPS which are very popular today….the BWs are just too wide.
- The RF-term “match” should be positioned to mean…for an ADC: optimization yielding the best results given the front-end design and application.
- Keep in mind, the impedance is only one of the parameters on the list.

Max power transfer occurs when, 
\[ Z_{\text{Source}} = Z_{\text{Load}} \text{ (complex conjugate)} \]
\[ Z = R + jX \quad Z = R - jX \]
Front-end goals & definitions: one approach to “matching”…

*Putting boundaries on each of these parameters can help quickly arrive to an expected/optimum frontend design.
Front-end goals & definitions: passband flatness/bandwidth/drive level

- Bandwidth
- Passband flatness $\pm 0.5\text{dB}$
Front-end goals & definitions: noise and distortion

- **SNR = 52dB**
- **Process Gain = 45dB**
- FFT process gain (per BIN) = $10 \log (M/2) = 45.15$dB, $M =$ number of FFT points $= 65536$
- Noise floor (per Hz) = $10 \log (Fs/2) = -97.16$dB, $Fs =$ sample rate $= 10.4$GSPS
- Noise NSD (dBFS/Hz) = SNR + $10 \log (Fs/2) = -149.16$dB, $Fs =$ sample rate $= 10.4$GSPS

**Fundamental frequency**

**HD2: Influenced by balance**

**HD3: Influenced by IC nonlinear effects**

**SFDR**

Noise floor (per Hz) = $10 \log (Fs/2) = -97.16$dB, $Fs =$ sample rate $= 10.4$GSPS

Noise NSD (dBFS/Hz) = SNR + $10 \log (Fs/2) = -149.16$dB, $Fs =$ sample rate $= 10.4$GSPS
Front-end goals & definitions: dBc vs. dBFS

- **FULL SCALE (FS) = 0dBFS**
- **HD3 = SFDR = 51dBc/66dBFS**
- **Fund = -15dBFS**

**SFDR (dBc)**

**SFDR (dBFS)**
Front-end types: amplifier vs. transformer/balun

• Q: Who will win?
• A: It depends!
• The KEY is understanding the tradeoffs (i.e. – those goals we discussed in the previous slides) which are mostly set per the application
• An amplifier is active and a transformer is passive.
• Like all active devices, amplifiers consume power and transformers do not.
• However, both have dynamic effects that need to be dealt with.
Front-end types: amplifier vs. transformer/balun

• Why use an amplifier?
  – Amplifiers preserve the DC content of the signal (in some cases)
  – Amplifiers preserve isolation between the previous stage and the ADC…on the scale of ~40-60dB.
  – Amplifiers are easier to work with in terms of gain and are not bandwidth dependent.
  – Amplifiers are less likely to ripple through the passband.
  – Can be used to convert single-ended signals to differential (in some cases)
Front-end types: amplifier vs. transformer/balun

• Why use a transformer?
  – Transformers have the advantage of coupling higher IF frequencies without significant loss (>200MHz).
  – For this same reason transformers usually have more bandwidth.
  – Transformers don’t require a power supply and thus add no power increment to the overall signal chain.
  – Transformers don’t add noise to the system, they only gain the signal noise, if using a transformer with gain.
  – Transformers provide an inherent AC coupled circuit.
    • Baluns are not.
  – Can be used to convert single-ended signals to differential (in all cases)
Front-end types: examples

**Amplifier Diagram:**
- Signal Source: $Z_{\text{Source}}$
- Amplifier: $R_f, R_g, R_o$
- ADC: $R_{tc}, R_s, \frac{R_{adc}}{R_{cadc}}$
- Load: $Z = 50\, \text{ohm}$

**Balun Diagram:**
- Signal Source: $Z_{\text{Source}}$
- Balun: $Z_{\text{Load}} = 50\, \text{ohm}$
- ADC: $R_{tc}, R_s, \frac{R_{adc}}{R_{cadc}}$
Front-end types: summary

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Usual preference</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bandwidth</td>
<td>Transformer/balun</td>
</tr>
<tr>
<td>Gain</td>
<td>Amplifier</td>
</tr>
<tr>
<td>Passband flatness</td>
<td>Amplifier</td>
</tr>
<tr>
<td>Power requirement</td>
<td>Transformer/balun</td>
</tr>
<tr>
<td>Noise</td>
<td>Transformer/balun</td>
</tr>
<tr>
<td>DC vs. AC coupling</td>
<td>Amplifier (DC level preservation) Transformer/Balun (DC isolation)</td>
</tr>
</tbody>
</table>
ADC types: ADC internal input architectures

• Unbuffered
  – Input Impedance set by switched-capacitor design
  – Lower power
  – Input Impedance varies over time (sample clock – track and hold)
  – Charge injection from sample caps reflects back onto input network

• Buffered
  – Highly linear buffer but requires more power
  – Generally have lower SNR, buffer = noise
  – Easier to design input network to interface high impedance buffer since it provides a fixed input termination resistance
  – Buffer provides isolation between sample caps and input network resulting in reduced charge injection transients
ADC types: unbuffered input architectures

ADS4149: unbuffered ADC input architecture, simplified
ADC types: unbuffered input architectures, cont. – input Z

ADS4149: unbuffered ADC input $Z_{in} = R_{in} \parallel C_{in}$
ADC types: unbuffered input architectures, cont. – TD

Charge injection glitches reflect back on the analog inputs relative to the sampling clock edges in the time domain.

Charge injection glitches subtract or common mode out on the analog input relative to the sampling clock edges.
ADC types: unbuffered input architectures, cont. – FD

Spectrum analyzer measurement at the analog inputs showing charge injection in the frequency domain

Fs = 250MSPS
ADC types: buffered input architectures

ADS5400: buffered ADC input architecture, simplified
ADC types: buffered input architectures, cont. – input Z

ADS54J69: buffered ADC input $Z_{in} = R_{in} \parallel C_{in}$, measured
ADC types: ADC input architectures – quick input Z approx.

Note that the Rin & Cin values are a reflection of the ADC’s internal circuitry during the sampling process in track mode—this is when the actual sample of the signal is taken. In hold mode, the sampling switch is open and isolates the input front-end circuitry from the internal sampling process or buffer.

If we derive the simple model and solve for the real and imaginary terms:

\[ Z_0 = R, \quad Z_1 = 1/s*C, \quad s = j*2*p*f, \quad f = \text{frequency} \]  

\[ Z_{IN} = \frac{1}{1/Z_0 + 1/Z_1} = \frac{1}{1/(1/R + s*C)} = \frac{1}{((1 + s*R*C)/R)} = R/(1 + s*R*C) \]  

\[ Z_{IN} = R/(1 + j*2*p*f*R*C) = \frac{R}{(1 + j*2*p*f*R*C)/(1 - j*2*p*f*R*C)} = \frac{R}{(1 + (2*p*f*R*C)^2)} \]  

Now find the “real” and “imaginary” terms:

\[ Z_{IN} = \text{Real} + j*\text{Imag} = \frac{R}{(1 + (2*p*f*R*C)^2)} + j*(-2*p*f*R^2*C)/(1 + 2*p*f*R*C)^2 \]  

\[ \text{Real} = \frac{R}{(1 + (2*p*f*R*C)^2)} \quad \text{Imag} = \frac{-2*p*f*R^2*C}{(1 + 2*p*f*R*C)^2} \]  

This mathematical model has proven to align well with the ac simulation in track mode. The main source of error in this simple model is the settling level of the impedance at higher frequencies.
ADC types: ADC input architectures – quick input Z approx.

ADS54J69: Rin

ADS54J69: Cin

Spreadsheet calculator upon request
Anti-aliasing filters (AAF) – things to watch out for…

- Too many components in the AAF design can cause mismatches (component tolerance) in differential filters, therefore giving rise to even order distortions (HD2) due to imbalance
- Not all inductors are created equal, so model or simulate those inductors, so that, sim = pcb design
  - DL Sparameters, use Modelithics models or measure them on VNA
- Inductors can sometimes have assembly issues giving rise to poor connections due to hidden end tabs.
  - This can lead to distortion effects because of lop-sided filtering
- When designing an AAF or even using a filter to test an ADC, make sure the stopband region is specified to be flat, broadband noise can still fold back in-band, see next slide…
Anti-aliasing filters (AAF) – filter flyback example

ADC BW Response

2GHz IF

Filter flyback
Anti-Aliasing Filters (AAF) – Filter Flyback Example

Fs = 10GSPS
Fs/2 = 5GHz = Baseband
IF = 2GHz
Anti-aliasing filters (AAF) – filter flyback example

Fs = 10GSPS
Fs/2 = 5GHz = Baseband
IF = 2GHz
Anti-aliasing filters (AAF) – design procedure

The amplifier should see the correct dc load recommended by the data sheet for optimum performance. 50ohm? 100ohm? 200ohm?, etc.

The correct amount of series resistance must be used between the amplifier and the load presented by the filter. This is to prevent undesired peaking in the pass band.

The input to the ADC should be reduced by an external parallel resistor, and the correct series resistance should be used to isolate the ADC from the filter. This series resistor also reduces peaking.
Anti-aliasing filters (AAF) – design procedure, cont.

The basic design process is as follows:
1) Select the external ADC termination resistor RTADC so that the parallel combination of RTADC and RADC is between 200 Ω and 400 Ω. This can help stabilize the filter design.
2) Select RKB based on experience and/or the ADC data sheet recommendations, typically between 5 Ω and 36 Ω.
3) Calculate the filter load impedance using: $Z_{AAFL} = RTADC \parallel (RADC + 2RKB)$
4) Select the amplifier external series resistor RA.
   Make RA less than 10 Ω if the amplifier differential output impedance is 100 Ω to 200 Ω.
   Make RA between 5 Ω and 36 Ω if the output impedance of the amplifier is 12 Ω or less.
5) Select RTAMP so that the total load seen by the amplifier, ZAL, is optimum for the particular differential amplifier chosen using the equation: $Z_{AL} = 2RA + (Z_{AAFL} \parallel 2RTAMP)$.
6) Calculate the filter source resistance: $Z_{AAFS} = 2RTAMP \parallel (ZO + 2RA)$.
7) Using a filter design program select the filter’s source and load impedances, ZAAFS and ZAAFL, type of filter, bandwidth, and order. Use a bandwidth that is slightly higher than one-half the sampling rate to ensure flatness in the frequency span between dc and fs/2.
8) The internal ADC capacitance, CADC, should be subtracted from the final shunt capacitor value generated by the program. The program will give the value CSHUNT2 for the differential shunt capacitor. The final common-mode shunt capacitance is $C_{AAF2} = 2(C_{SHUNT2} - CADC)$. 
Anti-aliasing filters (AAF) – design procedure, cont.

After running these preliminary calculations, the circuit should be given a quick review for the following items.

1) The value of CAAF2 should be at least 10 pF so that it is several times larger than CADC. This minimizes the sensitivity of the filter to variations in CADC.
2) The ratio of ZAAFL to ZAAFS should not be more than about 7 so that the filter is within the limits of most filter tables and design programs.
3) The value of CAAF1 should be at least 5 pF to minimize sensitivity to parasitic capacitance and component variations.
4) The inductor, LAAF, should be a reasonable value of at least several nH.

In some cases, the filter design program may provide more than one unique solution, especially with higher order filters. The solution that uses the most reasonable set of component values should always be chosen. Also, choose a configuration that ends in a shunt capacitor so that it can be combined with the ADC input capacitance.
Transformers & baluns – The basics

**Turns ratio**

\[ n = \frac{N_1}{N_2} \]

Defines the ratio of primary voltage to secondary voltage

**Impedance ratio**

\[ n^2 = \frac{Z_1}{Z_2} \]

Seen as the primary reflected from the secondary, the square of the turns ratio

**The transformer’s signal gain**

\[ 20 \log (\frac{V_2}{V_1}) = 10 \log (\frac{Z_2}{Z_1}) \]

A transformer with a voltage gain of 3 dB would have a 1:2 impedance ratio

This is good since data converters are voltage devices. Voltage gain is noise FREE!
Transformers & baluns – models & parasitics

...as they say:
Transformers, more than
meets the eye! 😊

Transformer

Primary

C2
C3
C1
C4
C5
C6
R2
R1 R3
R4
R
CORE
L1
L2
L3
L4

Secondary

Primary

C1

R1 L1 R_CORE
C2
C3
R2 L2
C4
C5
L3
L4 R3 R4
C6

Secondary

 Transformer

I1
V1(Z1)
I2
V2(Z2)

V1(Z1)
V2(Z2)

I1
I2

V1(Z1)
V2(Z2)

...as they say:
Transformers, more than
meets the eye! 😊

...as they say:
Transformers, more than
meets the eye! 😊
Transformers & baluns - specifications

Insertion loss

Return loss
Transformers & baluns – specifications, cont.

PhaseImbal

MagImbal
Transformers & baluns – balancing

**PhaseImbal – single vs. double**

**MagImbal – single vs. double**
Transformers & baluns – balancing

◆ **Layout** is another variable that can wreak havoc on any frontend design. Improper layout can literally mess up the frontend design causing unexpected performance. Take the time to keep the layout sound and symmetrical.

◆ Keeping the frontend network symmetrical, forces return currents or ground references to be common.

◆ This next slide shows an example of an FFT performance plot, using the symmetrical layout: This yielded a 2\textsuperscript{nd} harmonic of 85dB with a 140MHz IF applied at -1dBFS.

◆ The figure on the bottom shows the performance under these same conditions however, a non-symmetrical layout was used. This consistently yields a 2\textsuperscript{nd} harmonic of 79.5dB, more than 5dB lost in performance!
Transformers & baluns – balancing example

Balanced  \[ L_1 = L_2 \]

Unbalanced  \[ L_1 \neq L_2 \]

**NOTE:** Please follow the manufacture-recommended layout pattern.

FFT performance results

- **2HD = 5dB better**
- **2HD = 5dB worse**
Transformers & baluns – configurations

Single configurations

Double configurations
(for improved phase imbalance)
Bottom line: Find a better balun or use two baluns to help improve the HD2 specification
Amplifier – balancing

Tolerances in passive components can hurt performance too. This can be seen at the summing nodes in the feedback loop of an amplifier and multi-pole anti-aliasing filters between amplifiers and converters. Simple mismatches here can be seen in the math.

Take for example the differential amplifier analysis below. A common mode voltage mismatch can be developed if the component tolerances of R1(Rg) and R2(Rf) are not tight.

Notice that beta (\(\beta\)) is the ratio of these two resistors on either side of the amplifier. Any mismatch here will cause the summing node Vacm to be slightly different as these resistors drift over the tolerance itself, the temperature variation and over life.

A difference in Vn & Vp will ultimately cause Vout+ and Vout- to be different on the amplifier’s outputs, giving rise to second order distortion.

To combat this, make sure the component tolerances are low (<1%). If accuracy is important, specialized resistor packs can be procured that offer low ppm drifts and tight tracking tolerances. One of the reasons TI puts matched resistor gain networks inside our high-speed amplifiers is for this reason.

NOTE: Amplifiers with internal resistors are better matched
Amplifier – balancing, cont.

NOTE: SLVA417 – DC output errors in a fully differential amplifier

<table>
<thead>
<tr>
<th>Quantity</th>
<th>Symbol</th>
<th>General Expression</th>
<th>Asymptotic Form</th>
</tr>
</thead>
<tbody>
<tr>
<td>Feedback factors</td>
<td>$\beta_1, \beta_2$</td>
<td>$\beta_1 = \frac{R3}{(R3 + R4)}$, $\beta_2 = \frac{R1}{(R1 + R2)}$</td>
<td></td>
</tr>
<tr>
<td>Coefficients</td>
<td>$b_1, b_2$</td>
<td>$b_1 = \left(1 + \frac{1}{2\text{CMRR}}\right)$, $b_2 = \left(1 - \frac{1}{2\text{CMRR}}\right)$</td>
<td></td>
</tr>
<tr>
<td>Equivalent resistances</td>
<td>$R_{\text{EQ1}}, R_{\text{EQ2}}$</td>
<td>$R_{\text{EQ1}} = R1 \parallel R2$, $R_{\text{EQ2}} = R3 \parallel R4$</td>
<td></td>
</tr>
<tr>
<td>Applied input common-mode</td>
<td>$V_{\text{ICM}}$</td>
<td>$V_{\text{ICM}} = \frac{V_{\text{IN-}} + V_{\text{IN+}}}{2}$</td>
<td></td>
</tr>
<tr>
<td>Desired output</td>
<td>$V_{\text{OD, Desired}}$</td>
<td>$V_{\text{id}} \left(1 - \beta \right)$</td>
<td></td>
</tr>
</tbody>
</table>
Frontend VCM - common mode voltage follies in ADCs

• Since converter supply ranges are between VDD and GND and the process nodes are getting smaller, this leave little room for headroom error.

• The ADC’s analog inputs have an inherent common mode voltage (VCM) bias that establishes the “zero code” for the converter’s input signal to swing around.

• Any deviation in the VCM voltage on either analog input, puts the converter’s performance in serious jeopardy…
  • Why? Because the VCM helps establish the input fullscale range of the converter
  • Any deviation allow for clipping or over-ranging to occur early

• A quick review of the converter’s analog inputs signal is on the next slide…. 
Frontend VCM – analog input signal review

2Vpp differentially balanced signals

\[ V_x(t) = V_{pk} \times \sin(\omega t) + V_{CM} \]

- \( V_{pk} = 1 \) at 90° = +1Vpk
- \( V_{pk} = 1 \) at 270° = -1Vpk
- \( V_{pk} = 2 \) Vpp
Frontend VCM – buffered vs. unbuffered ADCs

- Unbuffered converters (aka: switched-capacitor type) require an external VCM bias on the analog inputs, typically the $V_{CM} = AVDD/2$ or half the analog supply

- Buffered converters typically have self-biased analog inputs and are set by the converter’s internal buffer, $V_{CM}$ is typically half of the supply, plus a diode drop above or $AVDD/2 + 0.7V$

- DC coupled application notes:
  - Make sure the amplifier can meet the VCM requirement of the ADC
  - Any VCM mis-match between the amp and ADC or either input differential pin, even if small, can create performance issues, ie – early clipping
  - Adding a buffer amp between the ADC and Amp is preferred
Frontend VCM – AC vs. DC coupled examples

AC coupled

DC coupled

Connection Not Required for Buffered ADC
Frontend VCM – “common” issues, baseline

Unbuffered ADC
Radc || Cadc
VCM
Baseline
Frontend VCM – “common” issues, VCM floating
Frontend VCM – “common” issues, VCM mismatch

Unequal VCM
AINP = AINN

Unbuffered ADC
Radc || Cadc
VCMX
Frontend VCM – “common” issues, VCM too high or low

AINn VCM ≠ AINp VCM
Front-end summary

• Understand and define the front-end design goals up front…

• “Matching” is just a fancy RF word which translates to ADC optimization…

• Understanding the application can zero in on the front-end amp or balun of choice….

• What’s your converter type? Buffered vs. unbuffered…

• A good impedance curves vs. frequency can be estimated by the ADC AIN internal R||C…

• Understand the AAF pitfalls and make sure your filters are filtering…

• Check for balancing issues, might need a better balun! Or lower tolerance resistors around the amp…

• Keep common modes common between amps and ADCs…don’t let them fight for VCM equilibrium…

• It’s not really a mystery after all…😊
Thank you

Rob Reeder
Application Engineer
High Speed Converter Group
Texas Instruments Inc.
R-Reeder@TI.com
520-750-2241 (o)
520-289-4223 (c)
Front-end references

• SLVA417: DC Output Errors in a Fully-Differential Amplifier, John Miller, TI.com
• Unraveling the full-scale mysteries of your RF converter’s analog inputs, Rob Reeder, Electronic Products, Nov 2019
• Breaking down accuracy errors in a precision high-speed ADC signal chain, Rob Reeder, Analog Design Journal, Sept 2020

• Achieve CM Convergence Between Amps And ADCs, Rob Reeder, Electronic Design, June 2010
• Wideband A/D Converter Front-End Design Considerations, Rob Reeder, Analog Dialogue, July 2008
• AN-935: Designing an ADC Transformer-Coupled Front End, Rob Reeder, Analog Devices, Inc., May 2007
• Wideband A/D Converter Front-End Design Considerations II, Rob Reeder, Analog Dialogue, Feb 2007
• Designing High Speed Analog Signal Chains from DC-to-Wideband, Rob Reeder, Analog Devices, Inc.
• CN-0227: High Performance, 16-Bit, 250 MSPS Wideband Receiver with Antialiasing Filter, Rob Reeder, Analog Devices, Inc.
• CN-0238: High Performance, 12-Bit, 500 MSPS Wideband Receiver with Antialiasing Filter, Rob Reeder, Analog Devices, Inc.
• Test high-speed ADCs for analog-input phase imbalance, Rob Reeder, T&M World, April 2011
• MS-2597: How to Design Wideband Front Ends for GSPS Converters, Rob Reeder, Analog Devices, Inc.
• High-Speed ADC Input Impedance: A Measured Versus A Mathematical Approach, Rob Reeder, Electronic Design, April 2011
• AN-742: Frequency Domain Response of Switched Capacitor ADCs, Rob Reeder, Analog Devices, Inc.
• MT-230: Noise Considerations in High Speed Converter Signal Chains, Rob Reeder, Analog Devices, Inc.
Useful converter equations

**Theoretical Signal-to-Noise Ratio (SNR)**

RMS Signal = (FSR / 2) / sqrt(2), RMS Noise = Qn = q / sqrt(12)

SNR (dB) = RMS Signal / RMS Noise = 20*log(2**(n-1)*sqrt(6)) = 6.02*n + 1.76

**Total Harmonic Distortion (THD)**

THD (-dB) = 20*log (sqrt((10^(-2ND HAR/20))^2 + (10^(-3RD HAR/20))^2 + ... (10^-6TH HAR/20))^2)

**Signal-to-Noise Ratio and Distortion (SINAD)**

SINAD (dB) = -20*log (sqrt(10^(-SNR W/O DIST/10) + 10^(-THD/10)))

**Effective Number of Bits (ENOB)**

ENOB (BITS) = (SINAD – 1.76 + 20*log(FSR/ActualFSR))/ 6.02

**Theoretical Noise Floor**

Noise Floor (-dB) = 6.02*n + 1.76 + 10*log (N/2),
(See Table1 ), Assume coherent sampling and no windowing

Noise Floor (-dB) = 6.02*n + 10*log (3*N/(π*ENBW)),
Assume noncoherent sampling and no windowing

**Noise Spectral Density (NSD)**

NSD (dBFS/Hz) = SNR + 10*log (Fs/2), Fs = sampling clock rate

<table>
<thead>
<tr>
<th>FFT Points</th>
<th>12-BIT</th>
<th>14-BIT</th>
<th>16-BIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>1024</td>
<td>101</td>
<td>113</td>
<td>125</td>
</tr>
<tr>
<td>2048</td>
<td>104</td>
<td>116</td>
<td>128</td>
</tr>
<tr>
<td>4096</td>
<td>107</td>
<td>119</td>
<td>131</td>
</tr>
<tr>
<td>8192</td>
<td>110</td>
<td>122</td>
<td>134</td>
</tr>
<tr>
<td>16384</td>
<td>113</td>
<td>125</td>
<td>137</td>
</tr>
<tr>
<td>32768</td>
<td>116</td>
<td>128</td>
<td>140</td>
</tr>
<tr>
<td>SNR (dB)</td>
<td>74.0</td>
<td>86.0</td>
<td>98.1</td>
</tr>
</tbody>
</table>

**Definitions / terms**

Fs = Sampling Rate (Hz)
Fin = Input Signal Frequency (Hz)
FSR = Full Scale Range (V)
n = Number of Bits
q = LSB Size
Qn = Quantization Noise
LSB = Least Significant Bit = FSR/2^n
N = Number of FFT Points
ENBW = Equivalent Noise Bandwidth of window function (Example: Four-Term Blackman-Harris Window, ENBW = 2)
IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING Datasheets), Design Resources (Including Reference Designs), Application or Other Design Advice, Web Tools, Safety Information, and Other Resources “As Is” and With All Faults, and Disclaims All WARRANTIES, Express and Implied, Including Without Limitation Any IMPLIED WARRANTIES OF MERCHANTABILITY, Fitness For a Particular Purpose or Non-Infringement of Third Party Intellectual Property Rights.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2020, Texas Instruments Incorporated