What will I get out of this session?

- The purpose of this session is to introduce the concepts needed to successfully layout a printed circuit board (PCB) for a switched-mode power supply (SMPS).

- This presentation is relevant to all SMPS PCB layouts, from 1 W to 10 kW.

- Part numbers mentioned:
  - UCC28180
  - UCC28742
  - UCC28710
  - UCC24612
  - UCC24610

- Reference designs mentioned:
  - TIDA-00443
Why is layout important?

• The best controller in the world cannot work well if embedded in a poor layout

• PCB layout for SMPS is extremely complicated!

• Same principles govern low and high power layouts
  – The difficulty is how to apply the principles in practice

• The PCB is often the most complex component in a design

How to translate a schematic into working hardware
Agenda

• The schematic
• Parasitics
  – Resistance
  – Inductance
  – Capacitance
• EMI & safety
• Grounding & signal routing
• Thermal management
• PCB layout example
• Summary
What are concerns for a power supply PCB layout?

• Safety
• EMI
• Parasitic inductance
• Parasitic capacitance
• Parasitic resistance
• Thermal performance
• High dv/dt
• High di/dt
• Grounding
• Noise
Understand the circuit, including the parasitic components!
Parasitic resistance

You mean copper is not a perfect conductor?

<table>
<thead>
<tr>
<th>Material</th>
<th>mΩ-cm</th>
<th>mΩ-in</th>
</tr>
</thead>
<tbody>
<tr>
<td>Copper</td>
<td>1.70</td>
<td>0.67</td>
</tr>
<tr>
<td>Gold</td>
<td>2.2</td>
<td>0.87</td>
</tr>
<tr>
<td>Lead</td>
<td>22.0</td>
<td>8.66</td>
</tr>
<tr>
<td>Silver</td>
<td>1.5</td>
<td>0.59</td>
</tr>
<tr>
<td>Silver (plated)</td>
<td>1.8</td>
<td>0.71</td>
</tr>
<tr>
<td>Tin-lead</td>
<td>15</td>
<td>5.91</td>
</tr>
<tr>
<td>Tin (plated)</td>
<td>11</td>
<td>4.33</td>
</tr>
</tbody>
</table>

\[ R = \frac{\rho \cdot l}{A} \]

\[ \rho = \text{resistivity} \]

\[ \rho(Cu) = 0.67 \text{ mΩ-in at 25°C} \]

\[ TCR_{Cu} \approx 4000 \text{ ppm/°C} (+40\% \text{ for 100°C rise}) \]

Impacts?
- Regulation
- Efficiency
- Temperature rise
# Parasitic resistance

## Counting squares

- **Current Flow**
- **Parasitic resistance**

\[
R = \frac{\rho \cdot l}{T \cdot l} = \frac{\rho}{T}
\]

Assume 1 oz. Cu

2 series squares = \(~1.0\ m\Omega\)
2 parallel squares = \(~0.25\ m\Omega\)

<table>
<thead>
<tr>
<th>Copper Weight (Oz.)</th>
<th>Thickness ((\mu\m /\mils))</th>
<th>m(\Omega) per square (25°C)</th>
<th>m(\Omega) per square (125°C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1/2</td>
<td>17.5/0.7</td>
<td>1</td>
<td>1.4</td>
</tr>
<tr>
<td>1</td>
<td>35/1.4</td>
<td>0.5</td>
<td>0.7</td>
</tr>
<tr>
<td>2</td>
<td>70/2.8</td>
<td>0.25</td>
<td>0.35</td>
</tr>
</tbody>
</table>
Parasitic resistance

Vias have resistance too

Typical rule of thumb is 1 A to 3 A per via

\[ R = \frac{\rho \cdot l}{A} \]

\[ R = \frac{\rho \cdot l}{\pi \cdot (r_o^2 - r_i^2)} \]

\[ R = \frac{(0.67 \, \mu\Omega \cdot \text{in}) \cdot (0.06 \, \text{in})}{\pi \cdot [(0.01 \, \text{in})^2 - (0.009 \, \text{in})^2]} = 0.67 \, \text{m\Omega} \]
Parasitic resistance

How many mΩ between L2 and J3?

Poor sense location

Sensing at output connector
Identifying high di/dt

Switched current loops

I/P loop (green)
- di/dt rates much lower
- Stray inductance is less critical
- $C_{\text{IN}}$ provides local low impedance source

O/P loop (blue/red)
- Inductor current alternates between MOSFET and diode paths
- Pulsating currents
- Stray inductance will cause voltage spikes
Identifying high \( \text{di/dt} \)

**Reverse recovery**

**Occurs when:**

- MOSFET turns ON during CCM operation (nearly every topology)
- Stray inductance will cause voltage spikes

**Mitigation:**

- Minimize loop inductance
- Use low \( Q_{RR} \) rectifiers –
  - SiC for high \( V_{OUT} \)
  - Schottky or ultra-fast diodes
  - Sync rectifiers with low \( Q_{RR} \)
Identifying high di/dt

Gate drives

High di/dt in loop (yellow)
- Stray inductance:
  - Limits drive current
  - Can cause ringing
- Minimize loop inductance

High dv/dt on gate (blue)
- Can couple to noise-sensitive nodes
- Minimize capacitance

Simplified PFC boost schematic

- \(I_{\text{GATE}}\)
- \(V_{\text{GATE}}\)
- \(V_{\text{OUT}}\)
- \(V_{\text{IN}}\)
- EMC Filter
- \(R_{\text{LOAD}}\)
Parasitic inductance

Self inductance of PWB traces

- Due to the natural logarithmic relationship, large changes in conductor width have minimal impact on inductance

\[
L = 2 \cdot l \cdot \left( \ln \left( \frac{l}{T + W} \right) + \frac{1}{2} \right) \text{nH/cm}
\]

\[
L = 5 \cdot l \cdot \left( \ln \left( \frac{l}{T + W} \right) + \frac{1}{2} \right) \text{nH/in}
\]

<table>
<thead>
<tr>
<th>W (mm/in)</th>
<th>T(mm/in)</th>
<th>Inductance (nH/cm or nH/in)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.25/0.01</td>
<td>0.07/0.0028</td>
<td>10/24</td>
</tr>
<tr>
<td>2.5/0.1</td>
<td>0.07/0.0028</td>
<td>6/14</td>
</tr>
<tr>
<td>12.5/0.5</td>
<td>0.07/0.0028</td>
<td>2/6</td>
</tr>
</tbody>
</table>
Parasitic inductance

PWB traces over ground planes

- Substantial inductance reduction
- Inductance inversely proportional to width

\[ L = \frac{2 \cdot h \cdot l}{w} \text{nH/cm} \]

\[ L = \frac{5 \cdot h \cdot l}{w} \text{nH/in} \]

<table>
<thead>
<tr>
<th>Metric</th>
<th>English</th>
</tr>
</thead>
<tbody>
<tr>
<td>h (cm)</td>
<td>h (in)</td>
</tr>
<tr>
<td>w (cm)</td>
<td>w (in)</td>
</tr>
<tr>
<td>Inductance (nH/cm)</td>
<td>Inductance (nH/in)</td>
</tr>
<tr>
<td>0.25</td>
<td>0.01</td>
</tr>
<tr>
<td>2.5</td>
<td>0.1</td>
</tr>
<tr>
<td>0.2</td>
<td>0.5</td>
</tr>
<tr>
<td>1.5</td>
<td>0.06</td>
</tr>
<tr>
<td>2.5</td>
<td>0.1</td>
</tr>
<tr>
<td>1.2</td>
<td>3.0</td>
</tr>
</tbody>
</table>
Parasitic inductance

Low series inductance

High series inductance

How much inductance in series with C39? (total length ~ 2 cm)
Identifying high $dv/dt$

Switched nodes

High $dv/dt$ at switched node (blue):
- Switched between 0V and $V_{OUT}$
- Stray capacitance can cause:
  - EMI problems
  - Noise injected to internal circuits
  - Reduced efficiency

Mitigation:
- Minimize $V_{SW}$ surface area
- Keep sensitive etch and components away from $V_{SW}$
- Ground the heatsink!

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The switched node paradox

- Increased surface area
  - Lower resistance
  - Lower inductance
  - Better cooling

- Decreased surface area
  - Lower capacitance

---

Simplified PFC boost schematic
Parasitic capacitance

Sample capacitance calculation

Consider two 10 mil traces crossing with 10 mil PWB thickness

\[ A = 0.00025 \text{ m} \times 0.00025 \text{ m} \]

\[ C = \frac{\varepsilon_r \cdot \varepsilon_0 \cdot A}{t} \]

\[ C = \frac{5 \cdot (8.85 \times 10^{-12} \text{ F/m}) \cdot (0.25 \text{ mm})^2}{2.5 \text{ mm}} \]

\[ C = 0.01 \text{ pF} \]

Not much capacitance but consider the area of all components connected to the feedback network.

Note: 10 mils = 0.00025 m
Parasitic capacitance

Chaos created by noise injection

Ten 0.05 x 0.02 in² pads can increase parasitic capacitance to 2 pF

Noise sensitive
Parasitic capacitance

At high frequency inductors turn into capacitors

Don’t route planes under common mode inductors!

**Diagram:**
- Inductor $L1 = 28$ mH
- Parasitic capacitance $C_{IND\_PARASITIC} = 23$ pF
- Plane capacitances $C_{PWBA} = 50$ pF, $C_{PWBB} = 50$ pF
- Ground Plane

**Graph:**
- Impedance vs Frequency
  - $L = 28$ mH
  - $C = 23$ pF
  - Frequency range: $1$ k to $1$ M Hz

**Note:**
- 3 cm$^2$ (0.5 in$^2$) area with 0.25 mm (0.01 in) thickness or 1 Layer of PWB
EMI considerations

Magnetic coupling

• External fields couple between inductors
• Can cause EMI issues
• Consider alternate orientation of second inductor to minimize coupling
• Use core shapes that provide better shielding
EMI considerations

Input filter layout

- Place components away from noise sources
- Common mode inductor T2 input pins do not cross output pins
- No GND plane under EMI filter
- Wide, short etch used to minimize losses
- Wide spacing between etches meets high-voltage requirements and minimizes coupling capacitance
**Safety**

Separate hazardous voltages from user accessible points

- Consult your safety expert!
- Create a very clear channel between primary and secondary
- Spacing depends on:
  - Type of insulation
  - Pollution degree
  - AC mains voltage
  - Working voltage
- Types of insulation:
  - Functional
  - Basic/supplementary
  - Reinforced

Partial Clearance Dimensions (mm) from UL60950-1, Section 2.10.3, Table 2H
Ground planes

Ground planes provide:

• Low resistance return paths
• Low inductance return paths
• Lateral heat spreading across board

General ground plane tips:

• Consider flooding empty areas with ground
• Avoid putting slots in GND planes
• Use jumpers on single layer boards to improve GND planes
• Place as much GND under the IC as possible
Signal routing/placement

Avoid coupling noise to sensitive nodes

**Bad**

- Maximize the separation
  - Move the source, reduce $C_{stray}$
- Place capacitors and resistors near pins
- Place GND vias near caps, resistors, and IC
- Minimize the unfiltered track length

**Good**
Data sheets normally contain PCB layout guidelines

10.1 Layout Guidelines

In order to increase the reliability and robustness of the design, TI recommends the following layout guidelines.

- **VREF pin**: Decouple this pin to GND with a good quality ceramic capacitor. A 1-uF, X7R, 25V capacitor is recommended. Keep VREF PCB tracks as far away as possible from sources of switching noise.
- **EA+ pin**: This is the non-inverting input to the error amplifier. It is a high impedance pin and is susceptible to noise pickup. Keep tracks from this pin as short as possible.
- **EA− pin**: This is the inverting input to the error amplifier. It is a high impedance pin and is susceptible to noise pickup. Keep tracks from this pin as short as possible.
- **COMP pin**: The error amplifier compensation network is normally connected to this pin. Keep tracks from this pin as short as possible.
- **SS/EN pin**: Keep tracks from this pin as short as possible. If the Enable signal is coming from a remote source then avoid running it close to any source of high dv/dt (MOSFET Drain connections for example) and add a simple RC filter at the SS/EN pin.
- **DELAB, DELCD, DELEF, TMIN, RT, ROFFM, DCM, ADELEF and ADEL pins**: The components connected to these pins are used to set important operating parameters. Keep these components close to the I/O and provide short, low impedance return connections to the GND pin.
- **CS pin**: This connection is arguably the most important single connection in the entire PSU system. Avoid running the CS signal traces near to sources of high dv/dt. Provide a simple RC filter as close to the pin as possible to help filter out leading edge noise spikes which will occur at the beginning of each switching cycle.
- **SYNC pin**: This pin is essentially a digital I/O port. If it is unused, then it may be left open circuit or tied to ground via a 1-kΩ resistor. If Synchronisation is used, then route the incoming Synchronisation signal as far away from noise sensitive input pins as possible.
- **OUTA, OUTB, OUTC, OUTD, OUTE and OUTF pins**: These are the gate drive output pins and will have a high dv/dt rate associated with their rising and falling edges. Keep the tracks from these pins as far away from noise sensitive input pins as possible. Ensure that the return currents from these outputs do not cause voltage changes in the analog ground connections to noise sensitive input pins. Follow the layout recommendation for Analog and Power ground Planes in Figure 4.5.
- **VDD pin**: This pin must be decoupled to GND using ceramic capacitors as detailed in the ‘Power Supply Recommendations’ section. Keep this capacitor as close to the VCC and GND pins as possible.
- **GND pin**: This pin provides the ground reference to the controller. Use a Ground Plane to minimize the impedance of the ground connection and to reduce noise pickup.
Thermal management

PCB cooling strategy

- Have **solid ground planes** to better spread heat across the layer
- **Avoid breaks in planes** as they substantially degrade lateral heat flow
- Use **thermal vias** to spread heat to other layers
- **Thermal pads** help to get the heat out of the IC into the PCB
- Use both sides of the board to cool

- Maximize the thermal paths with partial pours wherever practical
- **DO NOT** use switched node for cooling
Thermal management

Why is Board A hotter than Board B?

- Traces on the bottom layer prevent heat from spreading effectively.

- Removing horizontal trace for a more solid bottom layer reduces IC temp on board B.

- Hottest component on B is the catch diode.
PCB layout example

Gather information and place large components

Useful information:
- PCB size and (layers, layer spacing, material)
- Position of inlet and outlet connections
- Mechanical restraints (keep outs and height restrictions)
- Manufacturing process constraints
- Know the creepage and clearance requirements

Understand the circuit:
- High current paths
- High di/dt paths
- High dv/dt nodes
- Hot parts

Imagine a general ‘flow’
- Trunk packing algorithm

UCC28710/UCC24610 PSR flyback with SR
PCB layout example

Place remaining components

- Place the large parts in the power path first
- Reserve a ‘quiet’ location for the controller
  - NOT under transformer or node with high dv/dt
  - Place its associated parts nearby
- Reserve an area for the input filter
  - Keep filter input away from output
  - Rotate, reposition, reassign pins, repeat
PCB layout example

Route power and signal etch

Two layers:
- Bottom layer (red)
- Top layer (blue)

Route power path first
- Use wide etch and polygon pours
- Minimize high di/dt loop area
- Minimize high dv/dt surface area

Route signal etch last
- Keep away from high dv/dt nodes
- Keep noise sensitive etch short
- Shorten return paths

UCC28710/UCC24610 PSR flyback with SR
PCB layout example

Pour ground planes

Flood empty areas:
- Primary GND
- Secondary GND

Use vias to connect to GND planes
- Near caps/resistors
- Near GND pins of ICs

Check for blocked GND connections
- Move parts/etch as necessary
- Be mindful of parasitic resistance and inductance

UCC28710/UCC24610 PSR flyback with SR
Summary: keys to a successful SMPS layout

• Understand your circuit: **high current and di/dt paths, high dv/dt nodes**

• Understand how **parasitic resistance, inductance, and capacitance** are manifested

• Understand how layout can significantly affect **EMI**

• Understand the **safety requirements** for your product

• Understand **how heat is transferred** through the PCB

• Follow a logical procedure:
  – Place large parts, place small parts, power routing, signal routing, pour planes

• Have someone review your layout!
Summary: references


- **Why Should You Count Squares**; Brigitte; 2016 TI Power House Blog; [http://e2e.ti.com/blogs_/b/powerhouse/archive/2016/10/03/why-should-i-count-squares](http://e2e.ti.com/blogs_/b/powerhouse/archive/2016/10/03/why-should-i-count-squares)
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