

# HIGH VOLTAGE SEMINAR

## RAMANAN NATARAJAN

### GALLIUM NITRIDE

THE BENEFITS OF 650-V GaN FETS  
FOR 800-V POWER CONVERTERS



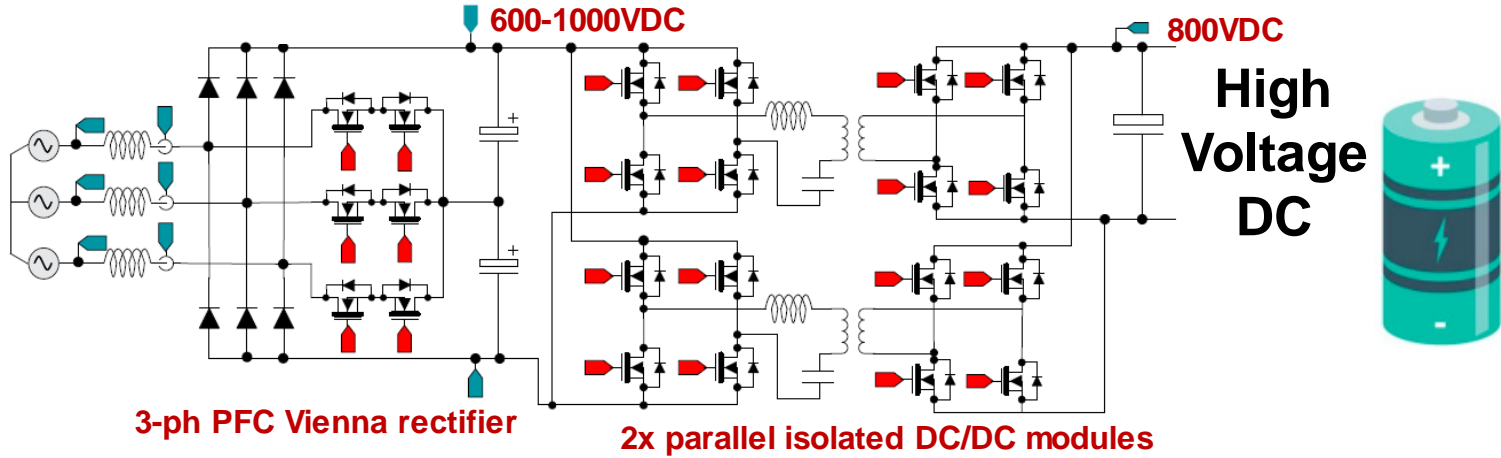
# Agenda

- Applications driving >800-V DC-link voltages & trends
- The case for 650-V GaN switches
  - Figure-of-merit for switching energy
- Power topologies enabling use of 650-V switches in 800-V converters
  - Stacked half-bridge arrangements
  - Multi-level power converters
- Conclusion

# Multi-kilowatt applications with 800-V DC-link

## 3-phase AC

L-L: 400VAC  
L-N: 230VAC



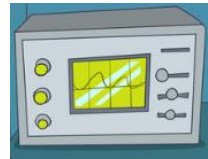
AC/DC battery  
chargers for energy  
storage



DC/AC grid tie  
inverters



Test & measurement  
equipment (eg. AC  
sources)



AC/DC onboard chargers, DC/AC  
vehicle-2-grid inverters, charging  
stations



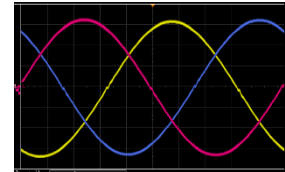
# Trend for higher operating frequency

- *Shrink the passives* i.e. inductors, transformers, storage capacitors to:
  - Reduce component cost
  - Reduce weight, height for better shock & vibration performance
  - Enable smaller PCB foot-prints
  - Create air-flow pathways for better cooling and higher efficiency
  - Better wave-shaping, lower distortion
  - Allow surface mount technology (SMT) components for automated assembly
- **Lower switching power loss & higher efficiency a pre-requisite for this**



## ***Electric vehicle onboard chargers***

- *power 6.6/7.2-kW to 11/22-kW with little-to-no increase in size*
- *density <2-kW/liter to >4-kW/liter*

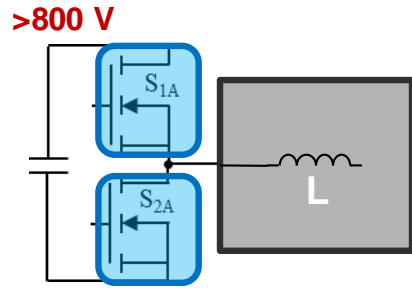


## ***Photovoltaic or battery inverter***

- *<1% harmonic distortion*

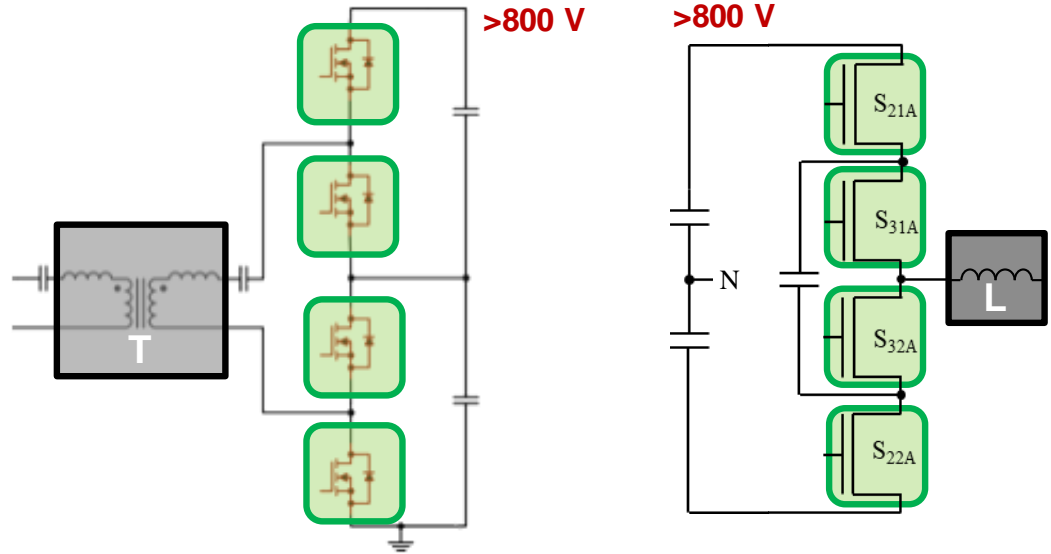
# Do 650-V devices make sense with 800-V DC link?


**Conventional wisdom**  
2-level converter



 1200-V switches

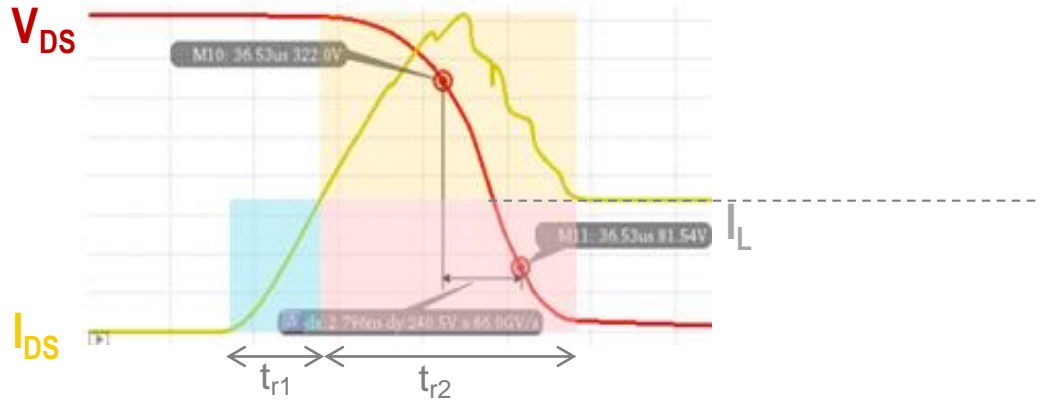
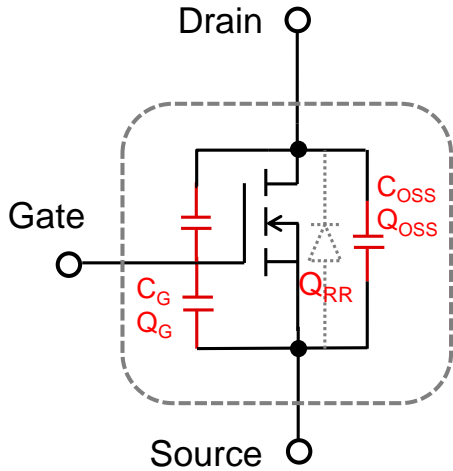
**Opportunities to differentiate**  
stacked 1/2-bridges, multi-level converters



 650-V devices

# Power switch attributes influencing switching loss

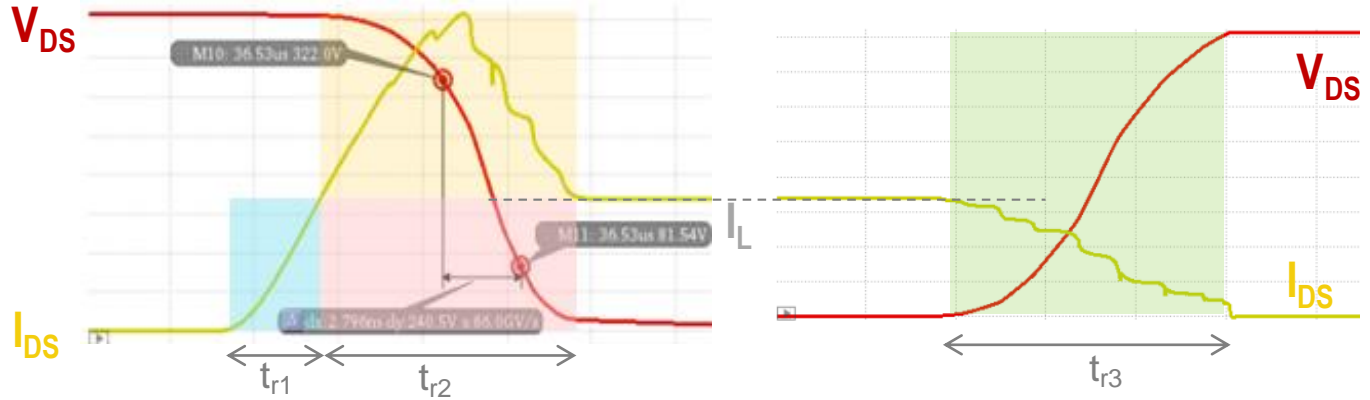
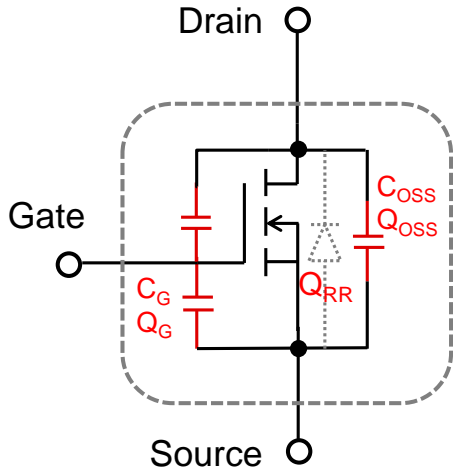
## Energy loss during hard-switching turn-on and turn-off



- Turn-on  $dI_{DS}/dt$  loss  $\approx V_{ds} * I_L / 2 * t_{r1}$
- Turn-on  $dV_{DS}/dt$  loss  $\approx V_{ds} / 2 * I_L * t_{r2}$
- Turn-on  $Q_{RR}, C_{OSS}$  loss =  $Q_{OSS} * V_{ds} + Q_{RR} * V_{bus}$

# Power switch attributes influencing switching loss

## Energy loss during hard-switching turn-on and turn-off



- Overlap losses influenced by *gate-source*, *gate-drain charge* & gate driver capability

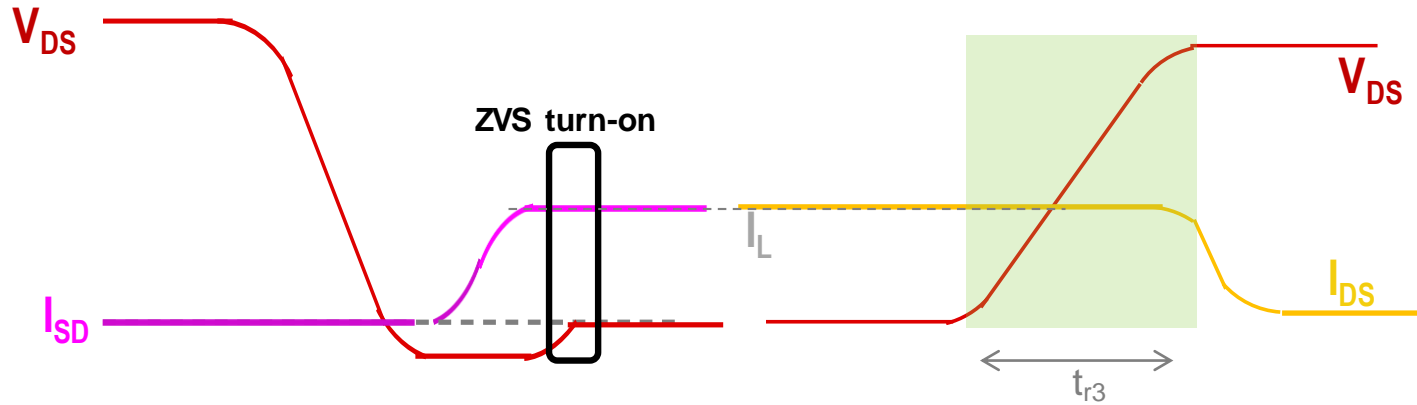
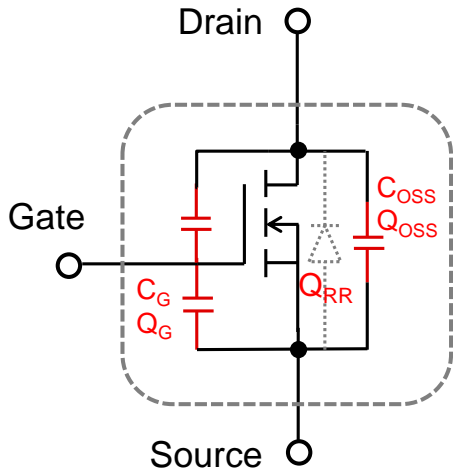


- Turn-on  $dI_{DS}/dt$  loss  $\approx V_{ds} * I_L / 2 * t_{r1}$
- Turn-on  $dV_{DS}/dt$  loss  $\approx V_{ds}/2 * I_L * t_{r2}$
- Turn-on  $Q_{RR}, C_{OSS}$  loss =  $Q_{OSS} * V_{ds} + Q_{RR} * V_{bus}$
- Turn-off  $d(I_{DS}, V_{DS})/dt$  loss  $\approx \int V_{DS}(t) * I_{DS}(t) * dt$

- Other losses related to *device output capacitance and stored reverse recovery charge*

# Power switch attributes influencing switching loss

## Energy loss during soft-switching turn-on (ZVS) and turn-off



- Overlap losses influenced by *gate-source*, *gate-drain charge* & gate driver capability

- Turn-on  $dI_{DS}/dt$  loss  $\approx V_{ds} * I_L / 2 * t_{r1}$
- Turn-on  $dV_{DS}/dt$  loss  $\approx V_{ds} / 2 * I_L * t_{r2}$
- Turn-on  $Q_{RR}, C_{OSS}$  loss  $= Q_{OSS} * V_{ds} + Q_{RR} * V_{bus}$
- Turn-off  $d(I_{DS}, V_{DS})/dt$  loss  $\approx \int V_{DS}(t) * I_{DS}(t) * dt$

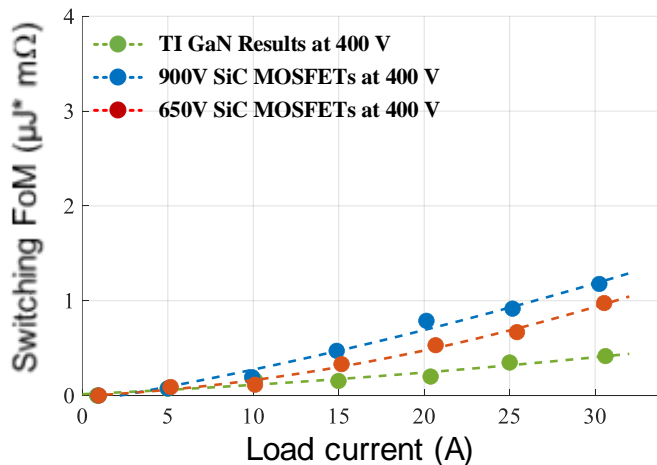
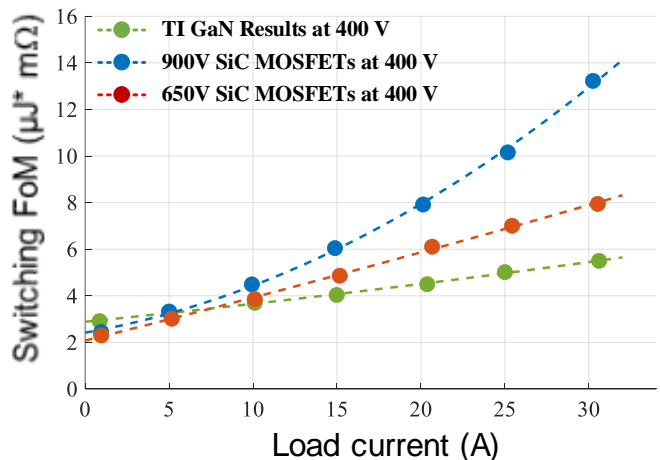




# Figure-of-merit for switching energy: GaN excels!

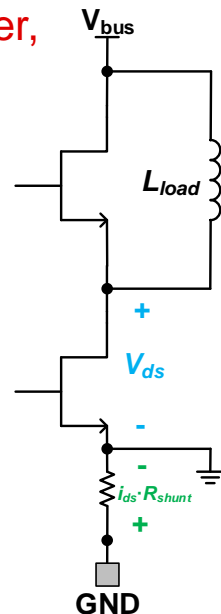
Figure-of-Merit = Switching Energy ( $\mu\text{J}$ ) \*  $R_{\text{DS,ON}}$  @125°C (m $\Omega$ )

The smaller,  
the better!



Turn-on Figure-of-Merit (*turn-on and turn-off losses, plus Coss & QRR losses*)

Turn-off Figure-of-Merit (*turn-off losses only; ZVS at turn-on*)



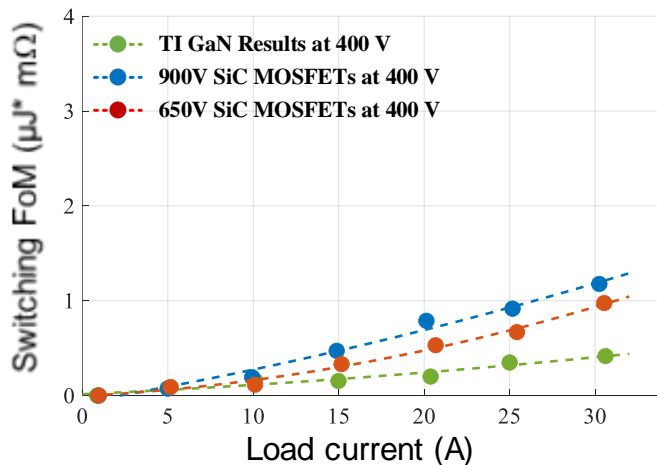
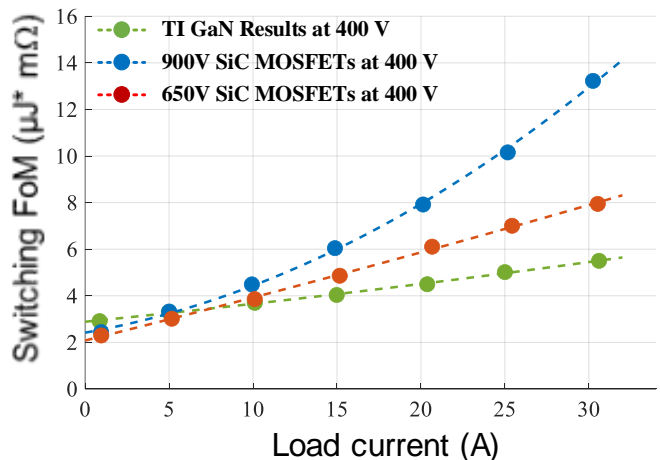
Double Pulse Test

Switching energy loss increases with higher switch voltage rating as expected, since associated device capacitances increase

# Figure-of-merit for switching energy: GaN excels!

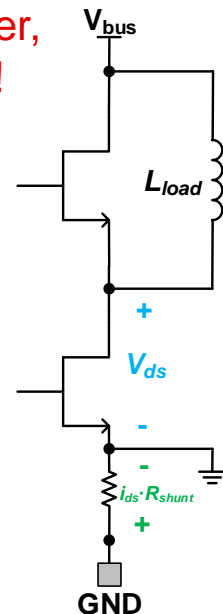
Figure-of-Merit = Switching Energy ( $\mu\text{J}$ ) \*  $R_{\text{DS,ON}}$  @125°C (m $\Omega$ )

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Turn-on Figure-of-Merit (*turn-on and turn-off losses, plus Coss & QRR losses*)

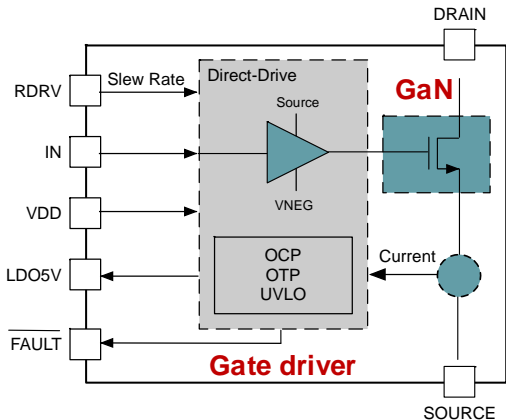
Turn-off Figure-of-Merit (*turn-off losses only; ZVS at turn-on*)



Double Pulse Test

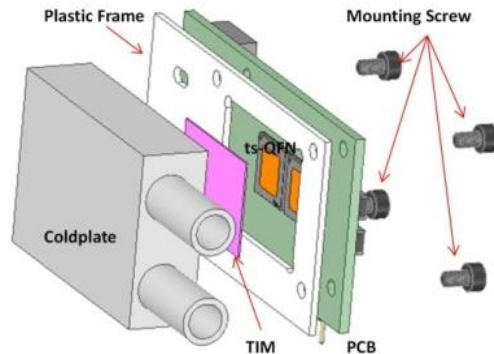
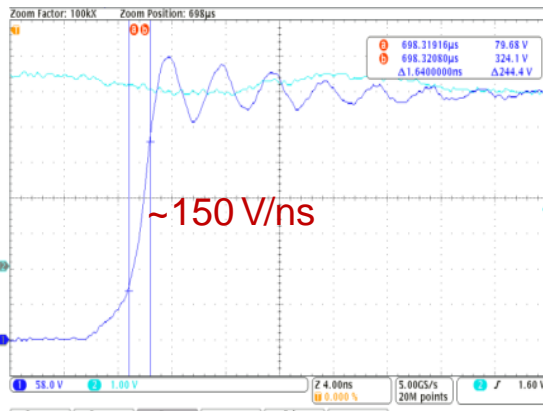
With lowest switching energy loss & zero reverse recovery, 650-V GaN offers the best opportunity for high-frequency operation!

# GaN FET engineered for high-frequency, high-power

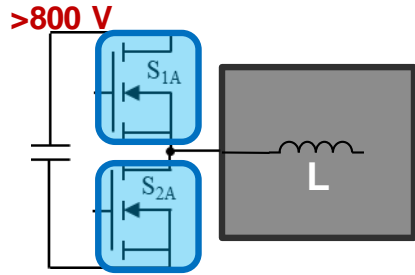



Standard Power Package	Kelvin Source Power Package	TI: GaN FET + Gate driver
Common Source: 2nH - 10nH	Common Source: <1nH	Common Source: <1nH
Gate loop: 5nH - 20nH	Gate loop: 5nH - 20nH	Gate loop: 1nH - 4nH

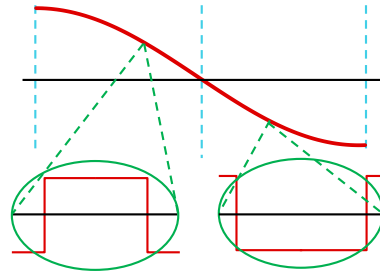
- Integrated gate driver offering up to 150-V/ns  $dV_{DS}/dt$
- 12x12mm QFN with lowest common source inductance
- Top-side thermal pad enables 1.6-2°C/W (>30W/package)
- Integrated protections



# Power topologies for 1200-V devices



: 1200-V devices



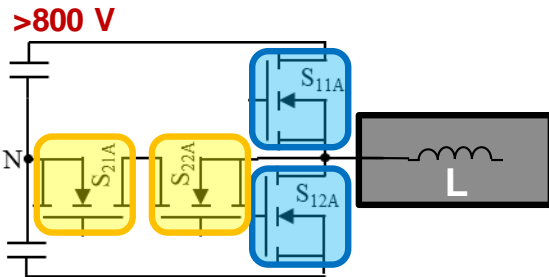
Two level


## Pros:

- Lowest device cost, fewest # of switches
- Well understood analysis and modulation

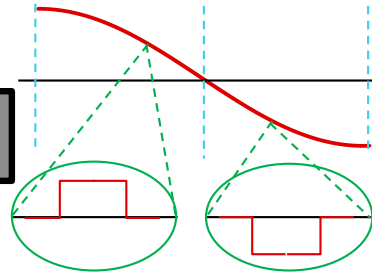
## Cons:

- 1200-V devices needed, higher losses
- 100% of bus voltage on switch resulting in high voltage stress & switching losses
- Highest Volt-sec on inductor resulting in large magnetics



: 600-V devices

: 1200-V devices



T type

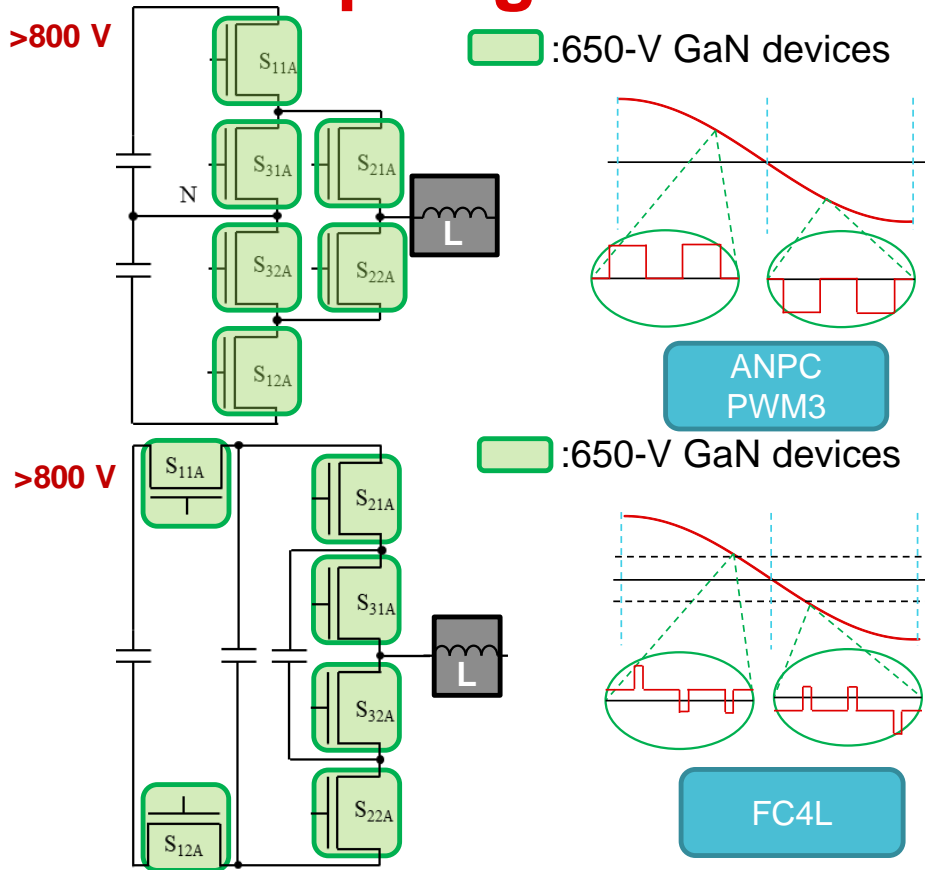
## Pros:

- 50% Volt-sec on inductor (assuming same frequency) allows smaller magnetics
- Higher efficiency with same frequency
- Lower voltage distortion due to 3-level

## Cons:

- 1200-V devices needed, higher losses
- Increased bus capacitance & # of switches
- Uneven loss distribution, more heatsink area

# Power topologies for 650-V devices (multi-level)



## Pros:

- 50% of bus voltage on FET allows for efficient 650-V devices
- Low Volt-sec due to 2X equivalent frequency at 50% bus voltage enables smaller inductor with simplified isolation
- Lower voltage distortion due to 3-level

## Cons:

- Increased bus capacitance, control complexity to balance neutral point
- Uneven loss distribution

## Pros:

- 3X equivalent frequency on inductor at 33% bus voltage allows smallest inductors (4-level)
- 33% of DC bus voltage on each switch
- Even loss distribution, lower distortion

## Cons:

- Increased conduction loss
- Increased control complexity

# 800-V/6.6-kW 3-phase bi-directional ANPC 3-level converter

## Features

- Power stage for three phase DC-AC inverter & AC-DC power factor correction converter
- Uses 650-V GaN FETs switches in 800-V system due to 3-level operation
- Shunt based current sense (high accuracy & linearity over temp.)
- Bidirectional operation with <1 ms direction changeover
- C2000 DSP control

## Target Applications

- Energy Storage Systems (Storage Ready Inverters)
- Bi-directional EV Charging Stations

## Tools & Resources

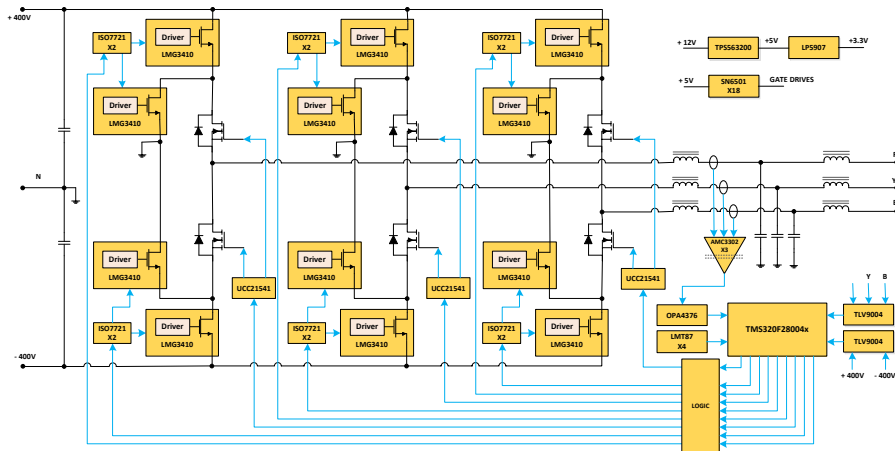


### Devices used:

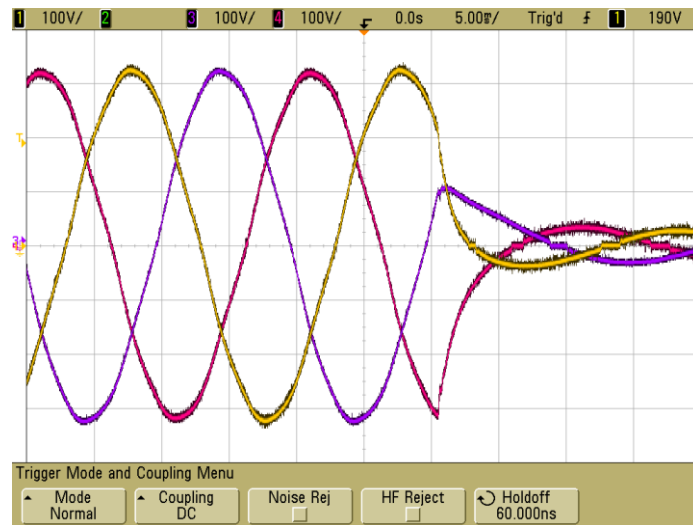
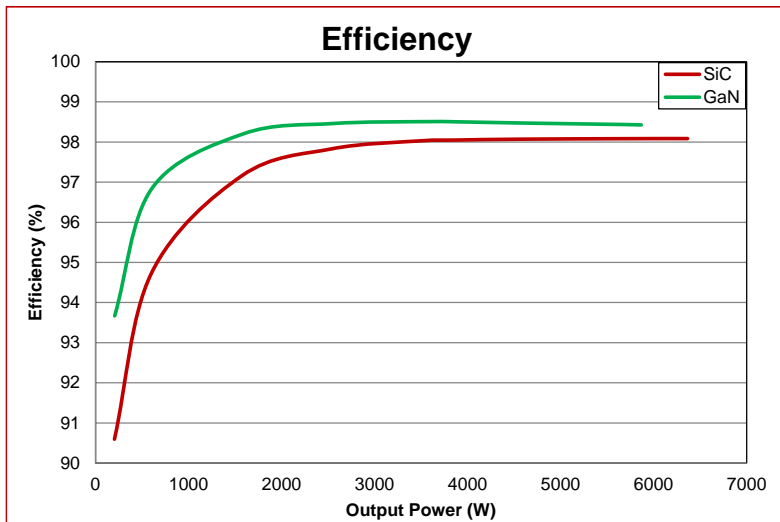
- [UCC21530](#)
- [AMC3302](#)
- [UCC21541](#)
- [LMT87](#)
- [TLV9004](#)
- [TPS563200](#)
- [LP5907](#)
- [SN6501](#)
- [OPA4376](#)
- [TMS320F28004x](#)

## Benefits

- **High power density** due to
  - high switching frequency (100kHz)
  - high efficiency (>98% at full load)
- **Low component stress** helps to improve system reliability
- **Optimized control scheme** needs 6 PWMs vs. 9 PWMs
- **Reduced cost** only 4 high-frequency FETs (out of 6) per leg



# 800-V/6.6-kW 3-phase bi-directional ANPC 3-level converter

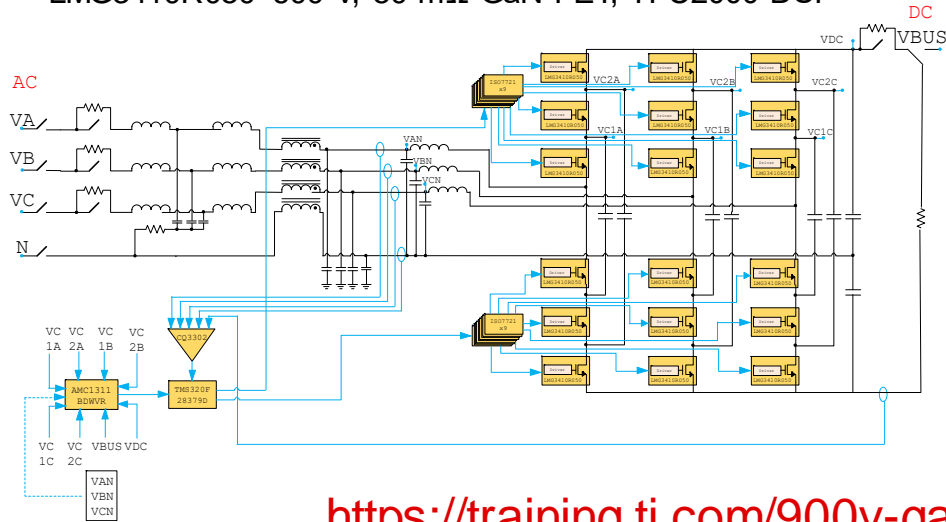


- ~98.5% efficiency above 1.5 kW with >90% efficiency at 200-W light load
  - GaN vs SiC efficiency improvement: 0.5% @ full load, 2-3% at light loads
- Clean sinusoidal voltage waveforms with <3% THD (total harmonic distortion)
- Stable transient response, settling time ~5ms
- 80° phase margin and 18dB gain margin with around 200Hz loop bandwidth

# 900-V/5-kW 3-phase bi-directional 4-level converter

## Features

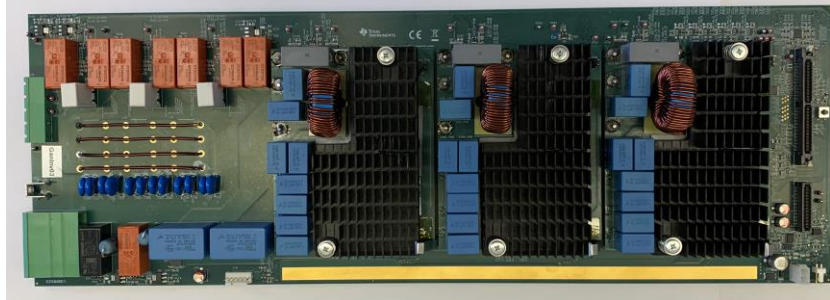
- AC voltage up to 480 V L-L, DC voltage up to 1400 V
- Peak efficiency of 99.2%
- Convection cooled with no fan
- Scalable 4-level flying capacitor multi-level solution
- Total harmonic distortion (THD) < 3%
- LMG3410R050 600-V, 50-mΩ GaN FET, TI C2000 DSP



## Benefits

- **3X power density improvement over IGBT** and 1.25X over SiC

Typical Operating conditions	IGBT	SiC	TI-GaN
Frequency (kHz)	20	100	<b>140</b>
Open-frame power density (W/in <sup>3</sup> )	73	170	<b>211</b>
Efficiency (%)	98.3	98.9	<b>99.2</b>

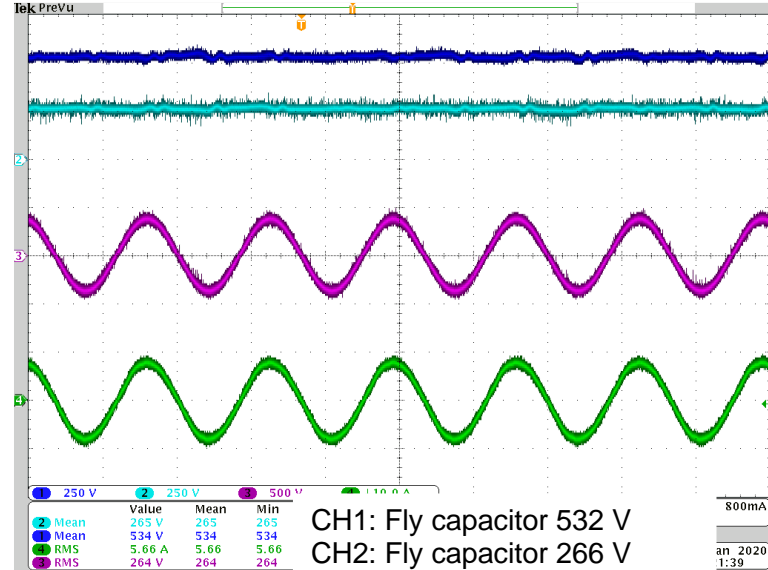
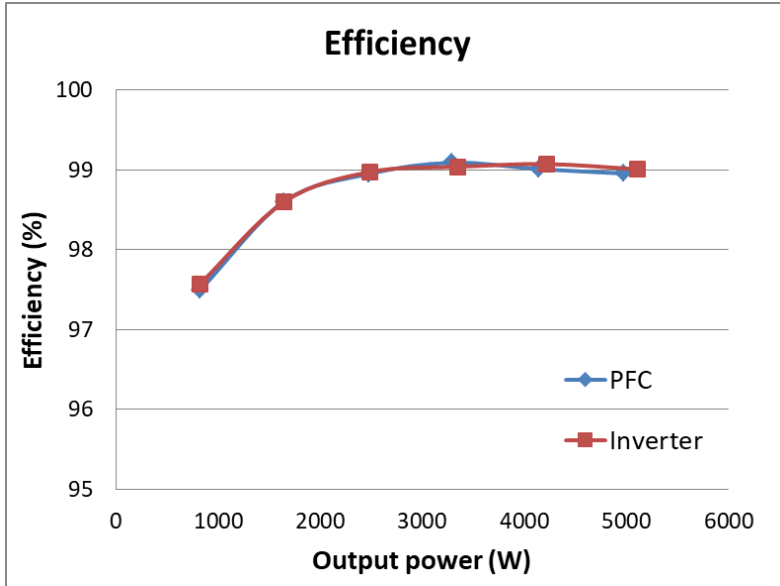


470 mm x 162 mm x 51 mm

<https://training.ti.com/900v-gan-solution-grid-and-beyond>



# 900-V/5-kW 3-phase bi-directional 4-level converter

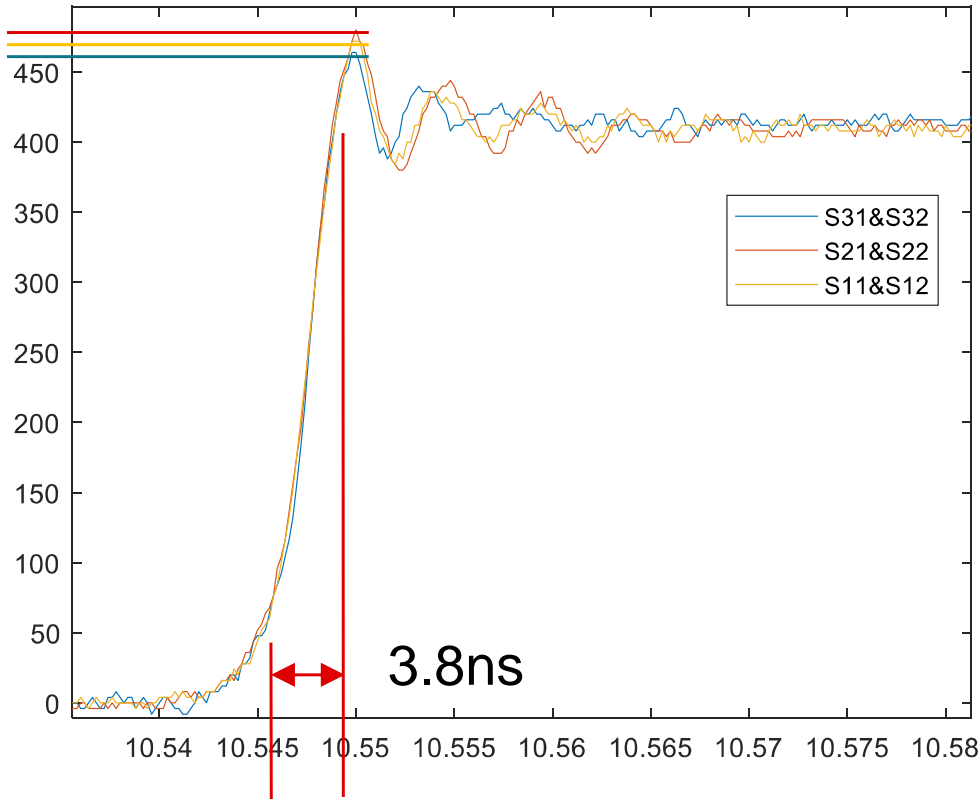


CH1: Fly capacitor 532 V  
CH2: Fly capacitor 266 V  
CH3: Grid voltage 270 V  
CH4: Grid current 6 A

- Peak efficiency of 99.2%
- Total harmonic distortion (THD) < 3%

# 900-V/5-kW 3-phase bi-directional 4-level converter

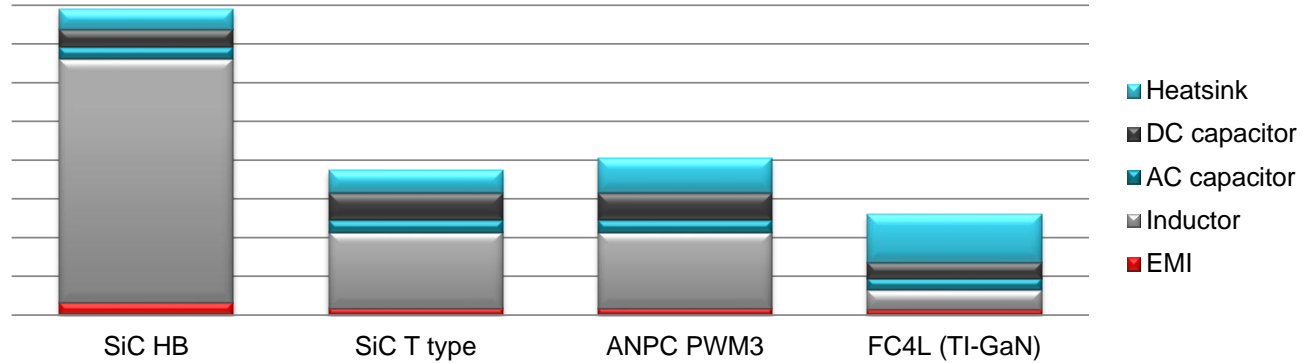
480 V  
472 V  
464 V



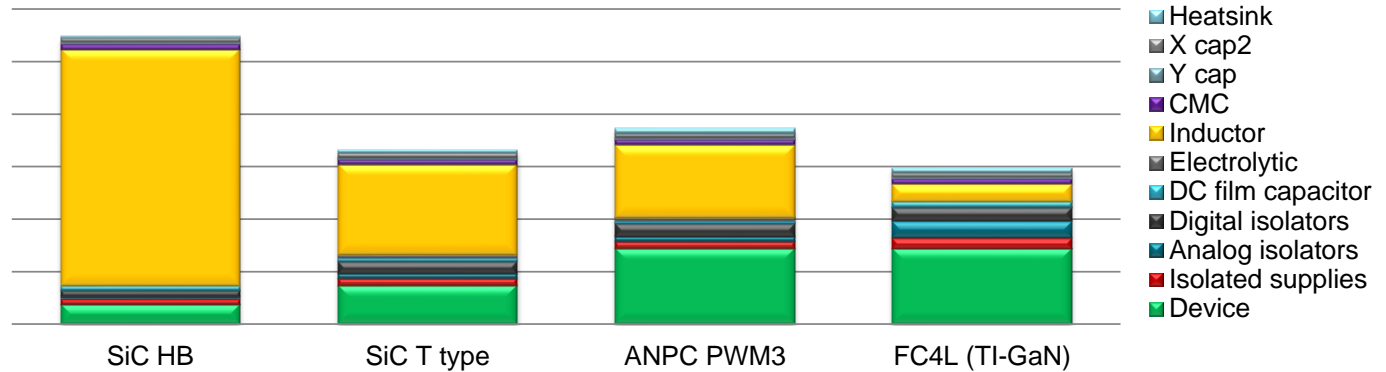
- 100V/ns  $dV_{DS}/dt$  of GaN FET contributes to low I-V overlap losses during switching enabling 10kHz operating frequency
- Low-inductance package mitigates voltage spikes during fast-switching transients

# 900-V/5-kW 3-phase bi-directional 4-level converter

**Inverter relative volume breakdown**

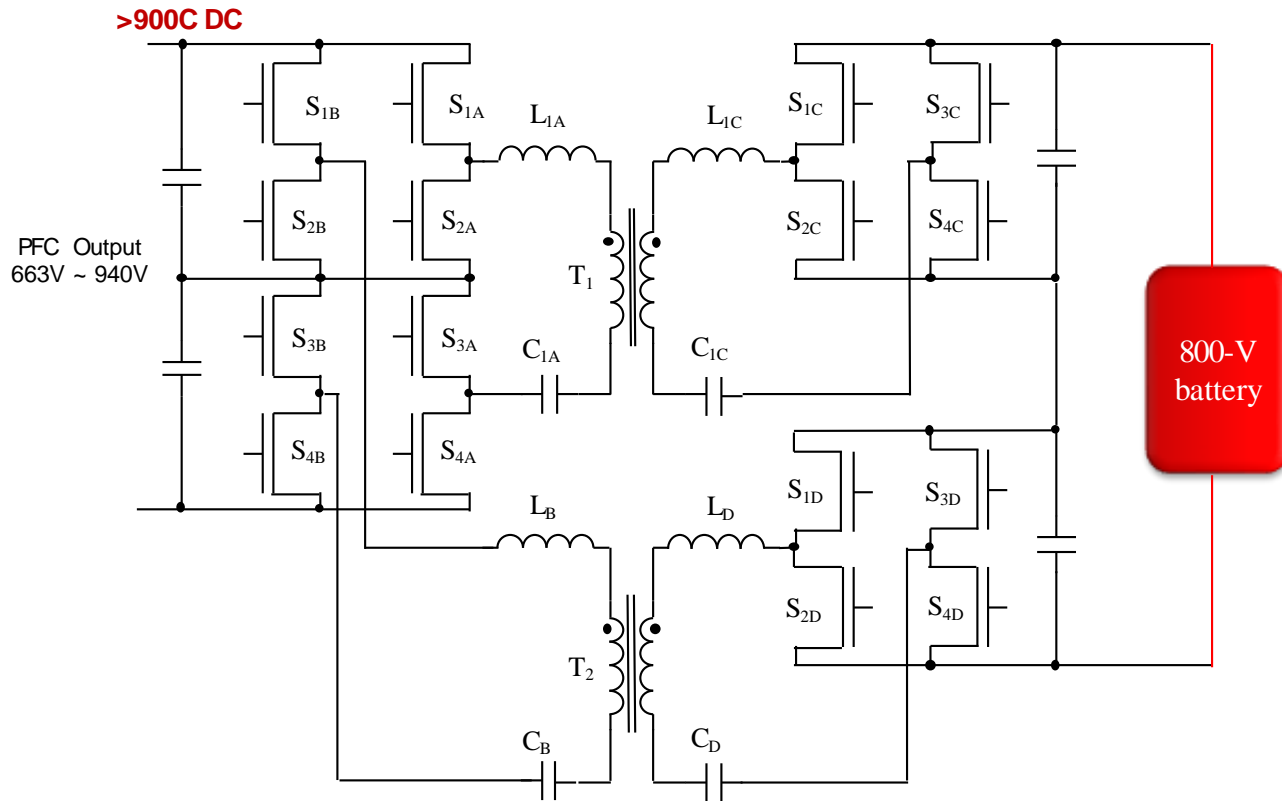


**Inverter relative cost breakdown**



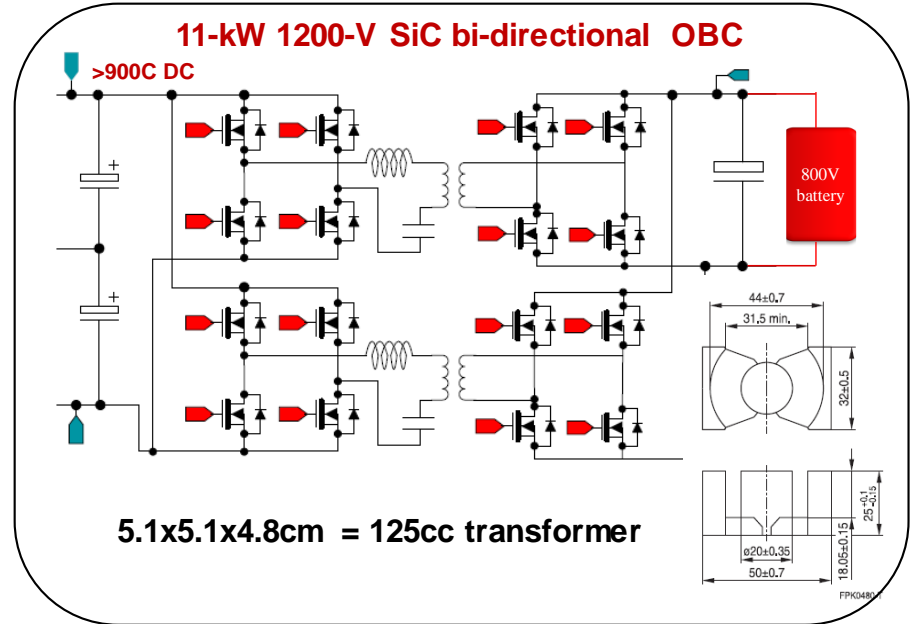
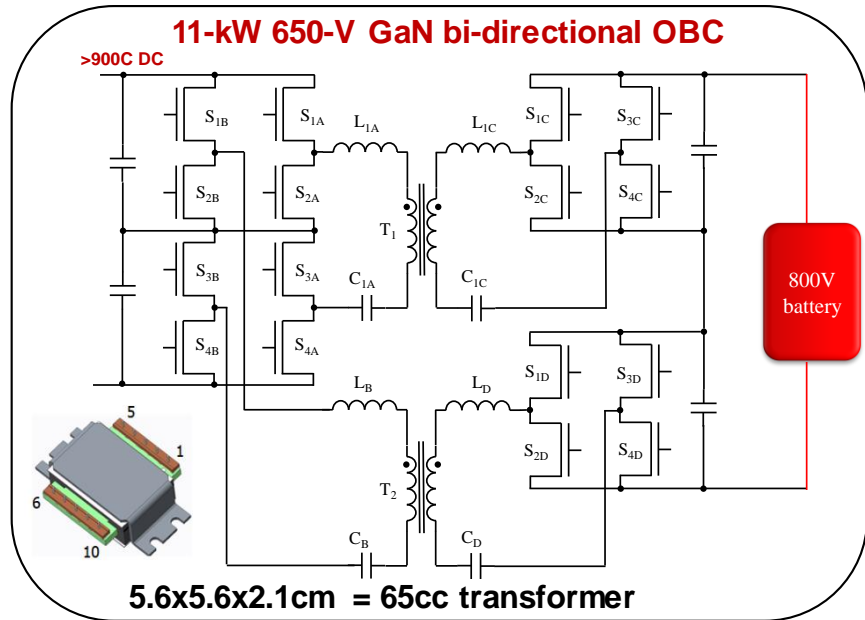
- Lowest system cost for 4-level solution, despite higher semiconductor cost

# Power topologies for 650-V devices (stacked 1/2-br)



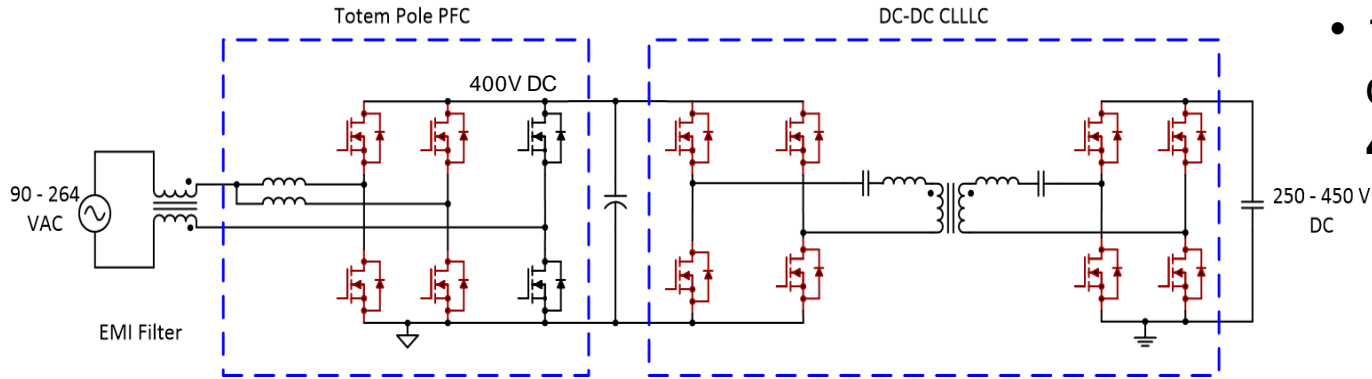
- Split DC bus capacitors enables series stacked 1/2-bridge arrangement of 650-V GaN-FETs
- Output connection reconfigurable for series or parallel operation (800-V or 400-V batteries)

# 11-kW onboard charger: 650-V GaN vs. 1200-V SiC



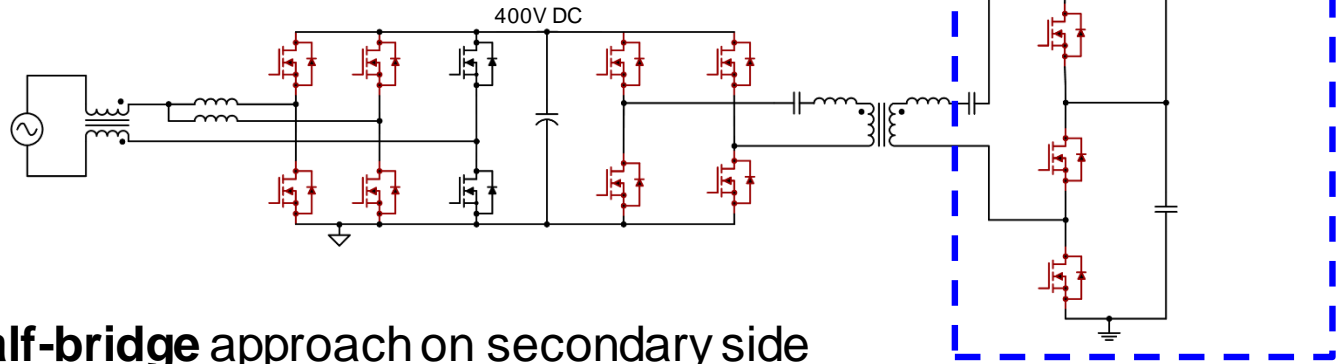
- 2X 5.5-kW modules comprising equal number of transformers (2X) and switches (16X)
- **Series stacked half-bridge** approach with GaN FETs; lower  $R_{DS,ON}$  for minimizing conduction losses due to higher current
- >3x frequency (~750kHz) enables **50% smaller planar transformers with GaN**

# Power topologies for 650-V devices (stacked 1/2-br)



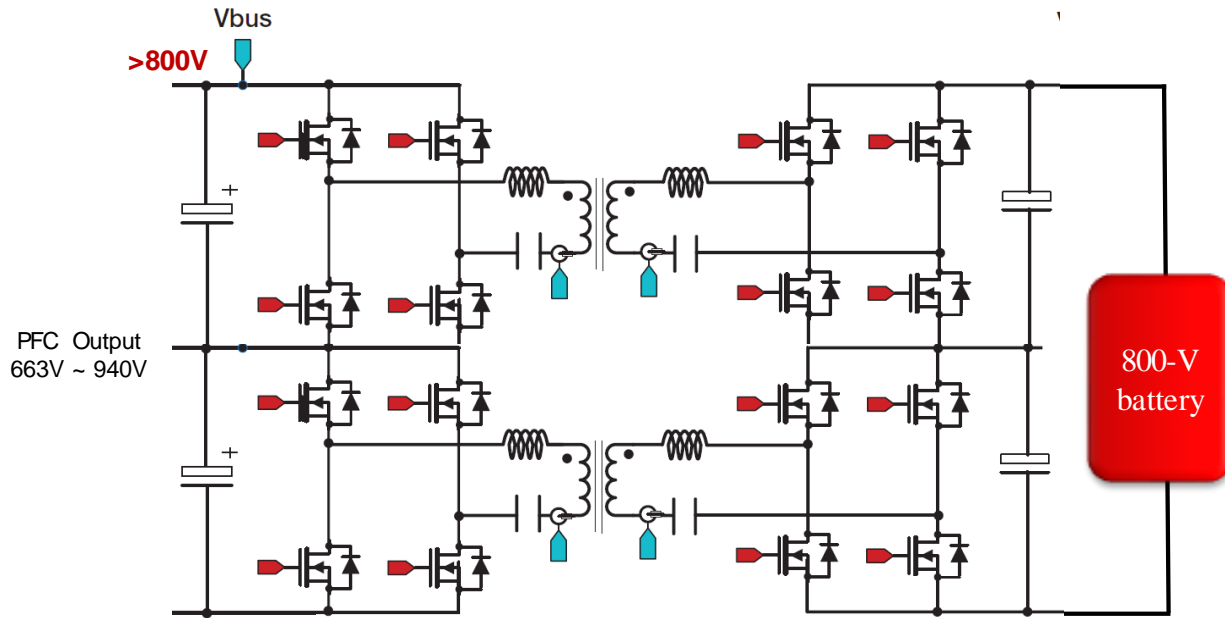
- 1-phase AC, 6.6-kW onboard charger for **400-V** battery

- 1-phase AC, 6.6-kW onboard charger for **800-V** battery



- **Series stacked half-bridge** approach on secondary side

# Power topologies for 650-V devices (stacked 1/2-br)



- Variant of series stacked half-bridge, with a completely symmetrical structure
- DC bus capacitor balancing needed simultaneously on both primary and secondary sides

# Conclusions

- Superior switching performance of 650-V GaN FETs provide an exciting opportunity to increase converter operating frequency
  - Challenge conventional approach to use 2-level converters with 1200-V IGBTs and SiC MOSFETs
  - 650-V GaN bring merits to both hard-switching and soft-switching converters
- Clever manipulation of power topologies easily enables use of 650-V FETs in converters with very high DC-link voltages (>800-V)
  - Fairly well-understood power topologies and related control algorithms
  - Mature eco-system of DSP control solutions, isolation products (isolators, bias power supplies) and total reference designs becoming available





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