Best practices for half-bridge gate drivers for HEV/EV
Agenda

• **Mid-voltage half-bridge design considerations**
  – Bootstrap supply design consideration
  – Switch node noise handling
  – Ground noise handling
  – Traditional half-bridge driver architecture vs. new UCC2792x

• **Using half-bridge driver for high side switch control**
  – Introduce the design circuit
  – Application examples

---

**Part numbers mentioned:**

- UCC27282(-Q1)
- UCC27284(-Q1)
- UCC27289
- UCC27212(-Q1)
- UCC27928A(-Q1)
- UCC27925B-Q1
Bootstrap supply design consideration

Basic bootstrap circuit operation

LO on to charge $C_{boot}$

Discharge $C_{boot}$ to supply high side HO on-pulse drive duration
Bootstrap supply design consideration

Bootstrap cap selection

<table>
<thead>
<tr>
<th>Bootstrap cap value</th>
<th>Potential issue</th>
</tr>
</thead>
</table>
| Too small           | • Higher output ripple voltage  
                      • Inadequate charge to drive high side FET  
                      • High dv/dt at initial bootstrap charge up |
| Too large           | • High bootstrap Ipeak  
                      • Take longer time to charge, require longer low side on time |

**Rule of thumb:** \( C_{\text{boot}} \geq 10 \times \text{FET gate capacitance} \)

**More detail calculation:**

\[
C_{\text{boot}} \geq \frac{Q_{\text{total}}}{\Delta V_{\text{HB}}}
\]

\[
Q_{\text{total}} = Q_g + I_{\text{HBS}} \times \left( \frac{D_{\text{Max}}}{f_{\text{sw}}} \right) + \left( \frac{I_{\text{HB}}}{f_{\text{sw}}} \right)
\]

\[
\Delta V_{\text{HB}} = V_{\text{DD}} - V_{\text{DH}} - V_{\text{HBL}}
\]

**Also to consider**

- Boot capacitor
  - low ESR, ESL, X7R cap for better temperature coefficients
- Very high fsw such as >1MHz
  - Can add a low value, high frequency bypass cap in parallel of \( C_{\text{boot}} \)
- Low fsw such as ~10kHz in motor drive application
  - take account for Rgs loading or any other leakage path from HS to VSS
- VDD bypass capacitor
  - \( \geq 10 \times C_{\text{boot}} \)
  - Reduce VDD ripple and avoid driver UVLO
Bootstrap supply design consideration

Bootstrap diode selection

Bootstrap diode consideration:
- Use fast reverse recovery or Schottky diode
  - Reduce risk of current supplies back to driver supply from bootstrap capacitor
- Able to take Ipeak during initial bootstrap cap startup
- Voltage rating shall take into account Vbus transient

During boot diode reverse recovery
- Undershoot can cause driver shutdown
- Can also increase switch node ringing

High dv/dt cause by high Ipeak
- Can cause undesired pulse on outputs
- Or may damage to driver
Bootstrap supply design consideration

Bias supply startup sequence

Optimum startup sequence

Control inputs switch before UVLO delay expire

- Controller should allow driver bias UVLO delay to expire before driving starting pulse
- Bootstrap cap value shall take into account the high side bias UVLO delay to ensure adequate capacitance is considered in the design
Switch node noise handling

What’s causing the negative spike?

Possible issues:
- Driver malfunction (faulty input pulse translation with increased ground noise)
- Bootstrap diode overcurrent
- High side bias (HB-HS) overvoltage

Cause of negative spike
1. While high side turning off, low side turning on
2. Current flow in the inductance, low side current rising
3. Power device/pcb layout parasitic inductance causes the –ve voltage on the switch node

\[ L_{ss} \cdot \frac{di}{dt} \]

What’s causing the negative spike?
Switch node noise handling

How to reduce negative spike?

• Reduce parasitic inductance
  – Most parasitic inductance is from the layout

- Parasitic inductance from low side FET source to capacitor

Add a ceramic cap across the power MOSFET
  ➢ Reduce the parasitic inductance from low side FET source to capacitors

Bulk cap usually is not close to the power FETs
Switch node and drive output noise handling

How to reduce negative spike?

- Clamp the negative spike
  - Add a zener diode between HB-HS
  - Prevent HB-HS overvoltage

- Limit current into HS (With internal $D_{boot}$)
  - Place small resistor (e.g. 2Ω) at the switch node
  - Reduce switch node slew rate and noise

- Reduce current in discharge paths
Ground noise handling

Drive input noise

1. Ideal case: current from low side FET source to return to the system ground (to the bulk capacitors)

2. The ground noise can affect the driver input signals through the low side FET source to driver ground connection

May result with undesired input signal translates to output pulse
Ground noise handling

Mitigate Drive input noise: schematic layout

1. Add small RC filter on the input signal pins
2. RC filter should be placed on a clean ground close to the driver input pins

1. Increase impedance connection on between the controller and power train grounds
2. Narrow layout trace width connecting the controller and power grounds
Ground noise handling

Mitigate Drive input noise: driver features

• Minimum input pulse rejection
  – UCC27282/284: 20ns
  – UCC27925/928: 20ns

• Input interlock and deadtime
  – UCC27282: Interlock
  – UCC27925: resistor programmable 60x deadtime
  – UCC27928: resistor programmable 10x deadtime

• Negative voltage transients support
  – UCC27282/284:
    • Switch node HS @ -14V for <100ns
    • Input pins HI, LI, EN @ -5V
  – UCC27925/928:
    • Switch node @ -200V
    • Split input and power grounds @ +/-200V
**Half-bridge driver architecture vs. new UCC2792x**

- **Traditional HB driver architecture**
  - LO: Low side output
    - drive the ground reference MOSFET
    - Gate voltage = VDD
  - HO: High side output
    - Floating driver with HS as reference
    - Gate voltage = VDD – boot diode $V_f$ w.r.t. HS

- **UCC2792x architecture**
  - Split grounds with +/-200V
  - Level shifter on both high and low side output
    - Excellent ground noise immunity
  - Low side power by VDD2
  - High side powered by VDD1 (can be bootstrap from VDD2)
    - Excellent switch node noise tolerance
  - **UCC27925A-Q1**: 8V UVLO, 60x Deadtime
  - **UCC27928A-Q1**: 4V UVLO, 10x Deadtime
UCC2792x: bootstrap supply design

Short VDD UVLO delay + high startup dv/dt tolerance

Test setup

VDD UVLO delay: spec typ 2us
- Fast start up allows faster switching

VDD dv/dt delay: spec max 0.5V/ns
- Higher dv/dt tolerance improve driver robustness
UCC2792x Switch node noise handling

Robust driver operation under excess switch node noise

- Test is set up to push switch node ringing to ~300Vp-p
- **High side input**: Apply PWN signal
- **Low side input**: Remain LOW for through the test
- **Expected result**: No undesired pulse on low side output

![Graph showing switch node noise and driver operation](image)

No undesired pulse on both high and low-side channels

- **Expected result**: No undesired pulse on low side output
- **High side output**: Apply PWN signal
- **Low side output**: Remain LOW for through the test

![Zoom-in graph showing dv/dt at ~180V/ns](image)
UCC2792x ground noise handling

Split grounds and application examples

Application with single ground, suffering
- Severe ground bounds
- Ground shifted because of a use of current sense resistor

Example: Half-bridge in 48-V motor drive design

With <0.01uA max leakage
UCC2792x ground noise handling

Split grounds and application examples

Example: Unidirectional 48V-12V DC/DC

48V side Power MOSFET

12-V side controller

Allow clean 48-V & 12-V ground layout design

Configure as dual low side
- Use as SR driver for best ground bounce immunity

Example: bi-directional 48V-12V DC/DC

Example: Unidirectional 48V-12V DC/DC

Configure as dual low side

UCC27928A-Q1 as half-bridge x2

UCC27928A-Q1 as dual low side
Using half-bridge driver as high-side switch control

Why mechanical relay is being replaced by solid state solution

• **What is high side switch?**
  – Switches placed between voltage source and load

• **Why using high side switch?**
  – No floating voltages at load
  – System is pulled to ground

• **Mechanical relay constraints**
  – Good
    • can control high voltage system from a low power single
  – Bad
    • subject to wear out due to friction/oxidation
    • shorter cycling lifetime comparing solid state relay
    • slower reaction time

➢ Use high side driver + MOSFET
Using half-bridge driver as high-side switch control

Gate driver and MOSFET as solid state disconnect switch

- **High power, high current application challenge**
  - Integrated MOSFET/driver cannot support high current
  - System has multiple MOSFETs in parallel
    - Higher gate charge \( (Q_g) \)
    - Still requires fast switching
  - 12V, 48V system require different driver voltage rating

- **Driver requirements**
  - Support 100% duty cycle
  - Strong drive strength
  - Different driver voltage rating options
  - Cost effective solution

- Charge pump
- Self-oscillate circuit
- Half-bridge driver + external charge pump
Using half-bridge driver as high-side switch control

How does a half-bridge work as a high-side DC driver?

- LI rising to driver VIH threshold, LO is off
- LO rise drives FET, LI falls from VIH to VIL threshold, LO is on

VIH

VIL

LI

LO

Switch Input

Optional diode: Turn off CP w/ HI low

12V_Aux

48V_Aux

48V_OR

CONTROL

DRIVE

HI

LO

HB

HO

HS

LIC27284-Q1

VDD

VSS

LO Charge Pump Oscillator

Oscillator

Optional diode:

Turn off CP w/ HI low
Using half-bridge driver as high-side switch control

How does a half-bridge work as a high-side DC driver?

- **LO high Transition:**
  Source current from CP cap into HB

- **LO low Transition:**
  Restore charge, voltage across CP cap

- The charge pump coupling capacitor will have a DC voltage ~ VBus
- The peak to peak voltage to charge HB cap is VDD – 2 Vf

- Additional initial charge path of HB cap is thru boot diode from VDD
Using half-bridge driver as high-side switch control

Driver selection

- **Half-bridge driver selection**
  - For charge pump operation, both HO & LO need to be on
    - Select driver without interlock
  - LI input has oscillator ramp waveform
    - Select driver with sufficient VIH and VIL hysteresis

- **Example drivers for the application**

<table>
<thead>
<tr>
<th>Device</th>
<th>Input Hyst</th>
<th>VHS Max</th>
<th>Driver Current</th>
<th>VDD UVLO Max</th>
</tr>
</thead>
<tbody>
<tr>
<td>UCC27284(-Q1)</td>
<td>1.0 V</td>
<td>100 V</td>
<td>2.5/3.5 A</td>
<td>5.4</td>
</tr>
<tr>
<td>UCC27289</td>
<td>1.0 V</td>
<td>100 V</td>
<td>2.5/3.5 A</td>
<td>8</td>
</tr>
</tbody>
</table>

- **Alternative circuit for driver with interlock function**
  - Bypass interlock with TLV1805 (high voltage comparator) as charge pump oscillator
  - **UCC27712-Q1**: 600V, 2A with interlock
IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (https://www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2021, Texas Instruments Incorporated