

**TI *Live!* BATTERY MANAGEMENT
SYSTEMS SEMINAR**

DAN TORRES

48-V BATTERY MONITORS IN xEV BMS

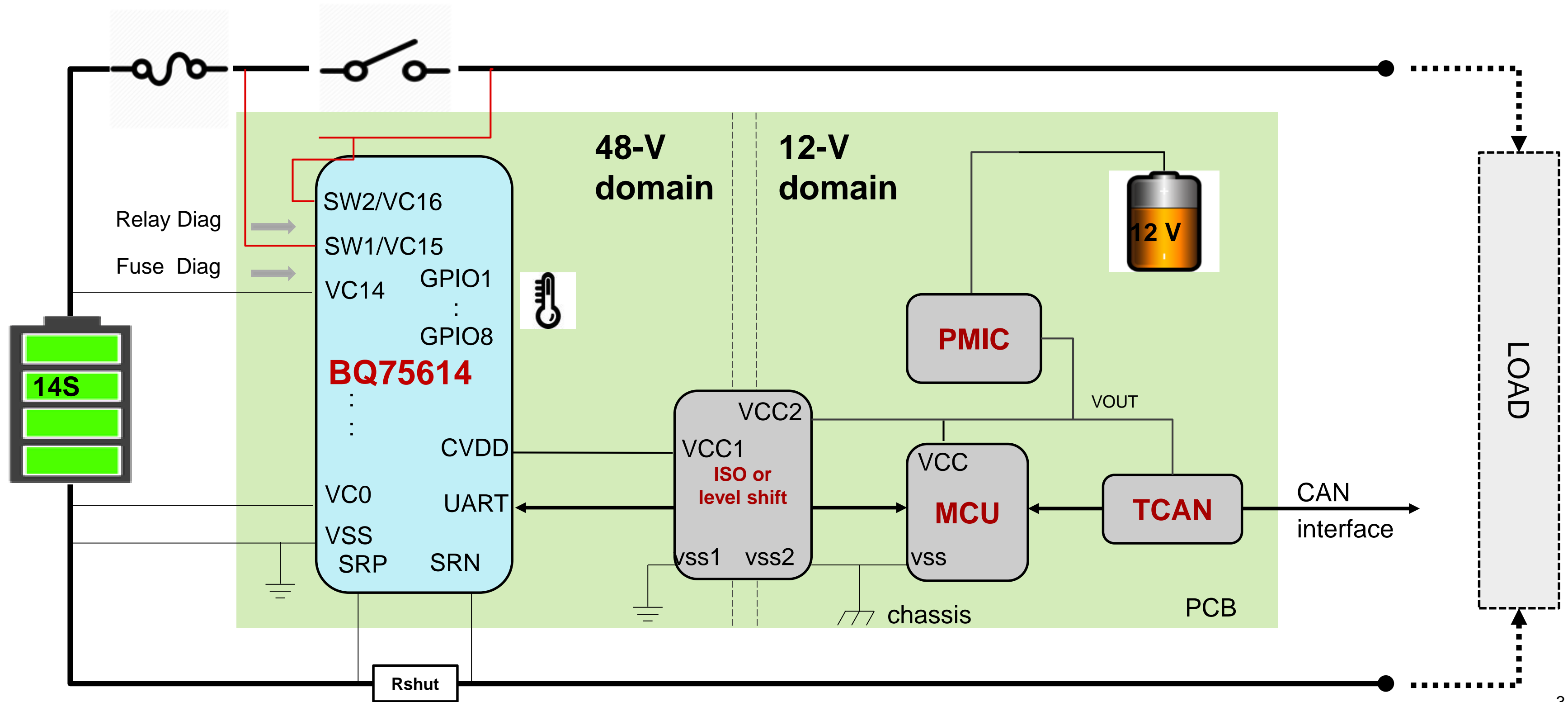


Agenda

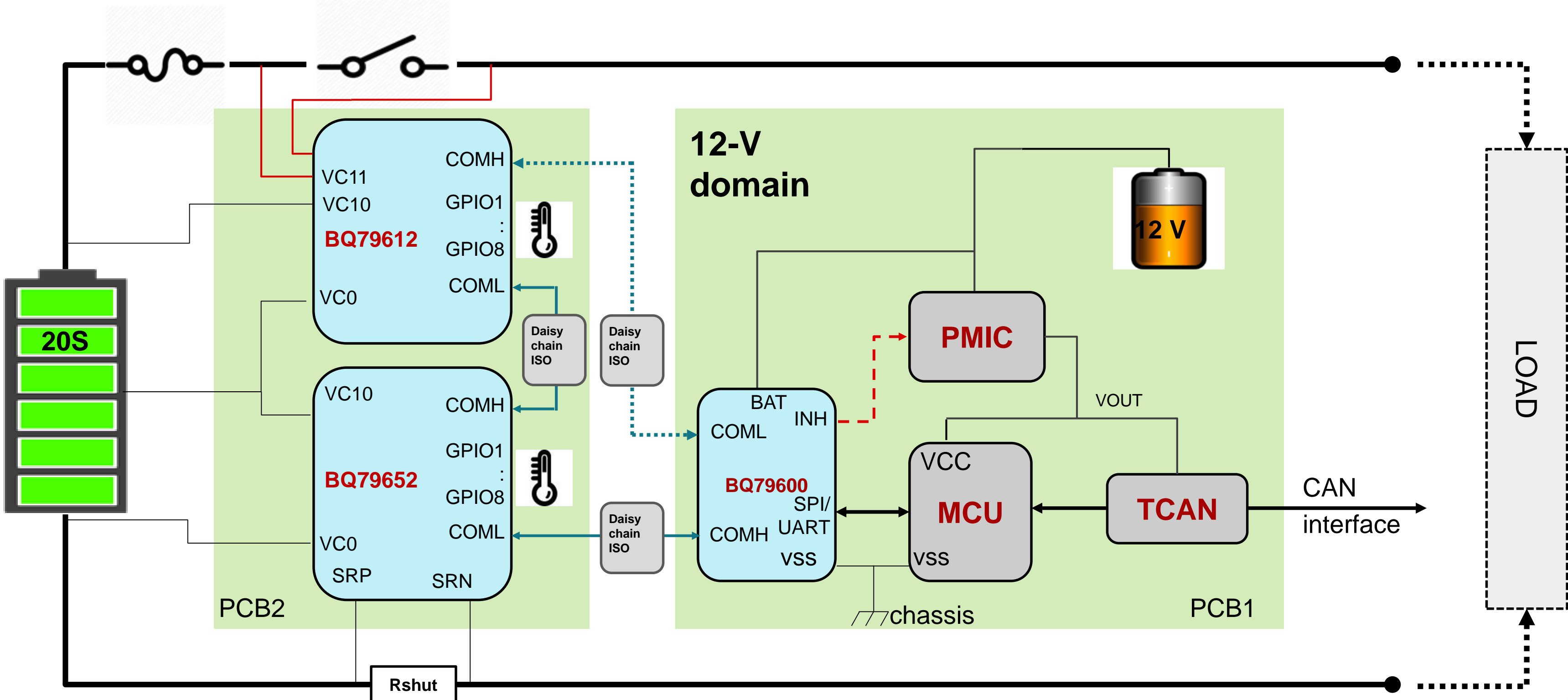
- 48-V battery-management system architectures
- BQ75614-Q1 overview
- Voltage and current measurement, and synchronization
- Reference schematic and hotplug
- Cell balancing and thermal management

48-V system architecture

- Topology variation:
- Microcontroller (MCU) on 48-V side, isoCAN



48-V system architecture with lithium-titanate battery



BQ75614-Q1 overview

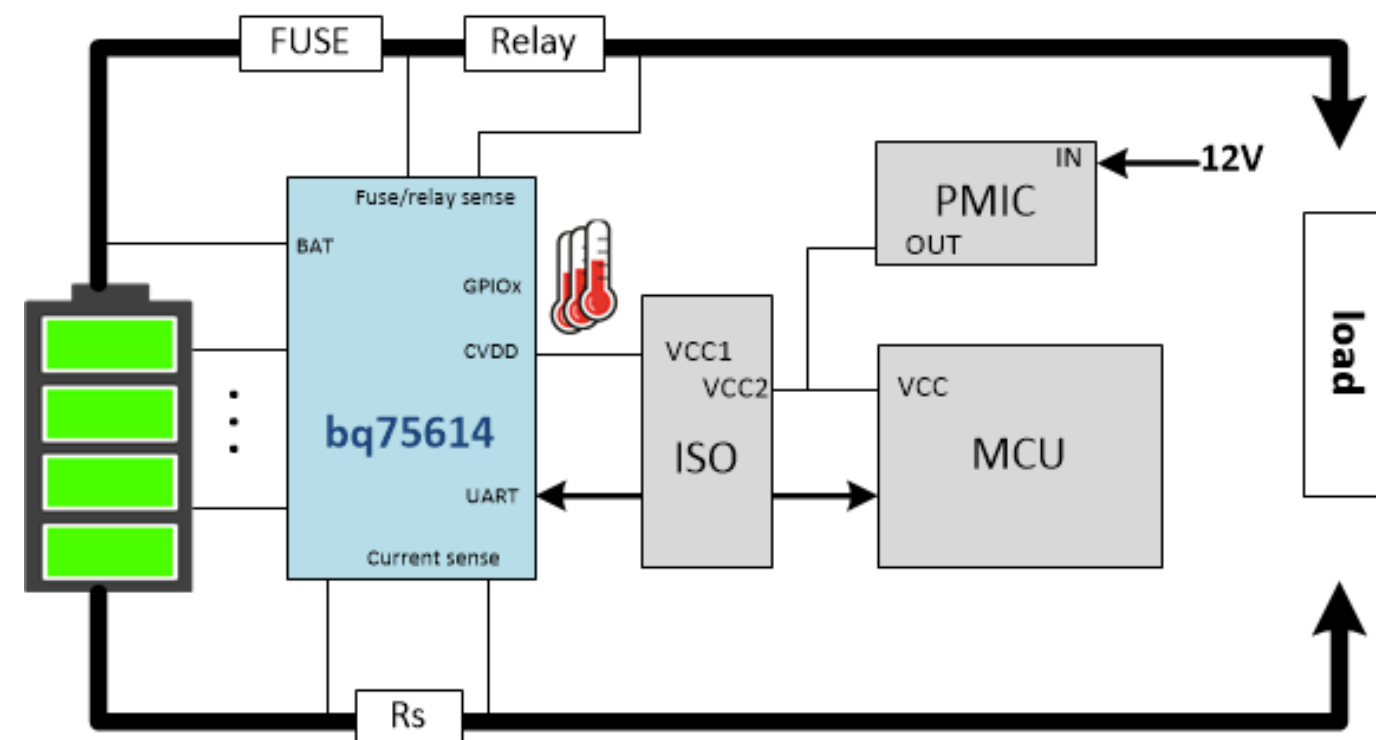
BQ75614: 48-V 14S to 16S battery monitor

Features

- **ASIL-D Voltage/temperature** measurement and **communication**
- **ASIL-D current** measurement with dedicated 16-bit sigma-delta ADC
- **Integrated current sensing:**
 - Input range = **+/-100mV** with **0.75ms to 12ms** conversion time options
 - Synchronized current & cell voltage measurements
 - Accuracy of **+/-0.3%** (>300uV input); **1.5uV** (<=300uV input)
- **Integrated fuse & relay diagnostic**
- **Voltage Accuracy +/-3.5mV** over full temperature range post soldering
 - **All 14 cell voltage measurements** complete in **112us**
 - **Integrated front end RC filters** on voltage measurement path
 - **Integrated post ADC digital low pass filters** w/ as low as $6.5\text{Hz } f_{\text{cutoff}}$
- **Built-in 2nd level protector** for OV/UV/OT/UT
- **Fault interrupt signal** to system MCU for quick action
- **UART communication** to system MCU
- **External load support** to power digital isolator
- **Internal cell balancing** with integrated balancing FET
 - Optional device controlled odd/even duty cycle w/out constant host system monitoring, or
 - Complete MCU controlled balancing
 - Option to **pause CB progress** at OT detection and **automatically resume** when temp drops
- **100ms FDTI mode**
- **Package: 64-pin QFP**

Benefits

- **Provide device level ASIL-D. No special SW requirement from MCU.**
 - Part of the ASIL-D family with 16S, 14S, 12S monitor for HV system and 48V system
 - All devices sharing same package/pinout, functional control and register map
 - Learn one, learn all. Maximize MCU code reuse and system level fault analysis.
- **Similar time average between current and cell voltage measurements for more accurate SOC calculation**
 - **Similar timing options** on current sense conversion time and cell voltage LPF setting
 - **Integrated post ADC low pass filters** provides high integrity level of DC voltage measurement by filtering out system noise (e.g. inverter/charger/heater/motor rotation etc) for best SOC calculation
- **Built-in 2nd level protector** with user programmable OV/UV/OT/UT threshold independent of ADC measurement



BQ75614 block diagram

Current ADC

- High accuracy
- Fast data rate
- SINC3 low pass filter

Main ADC

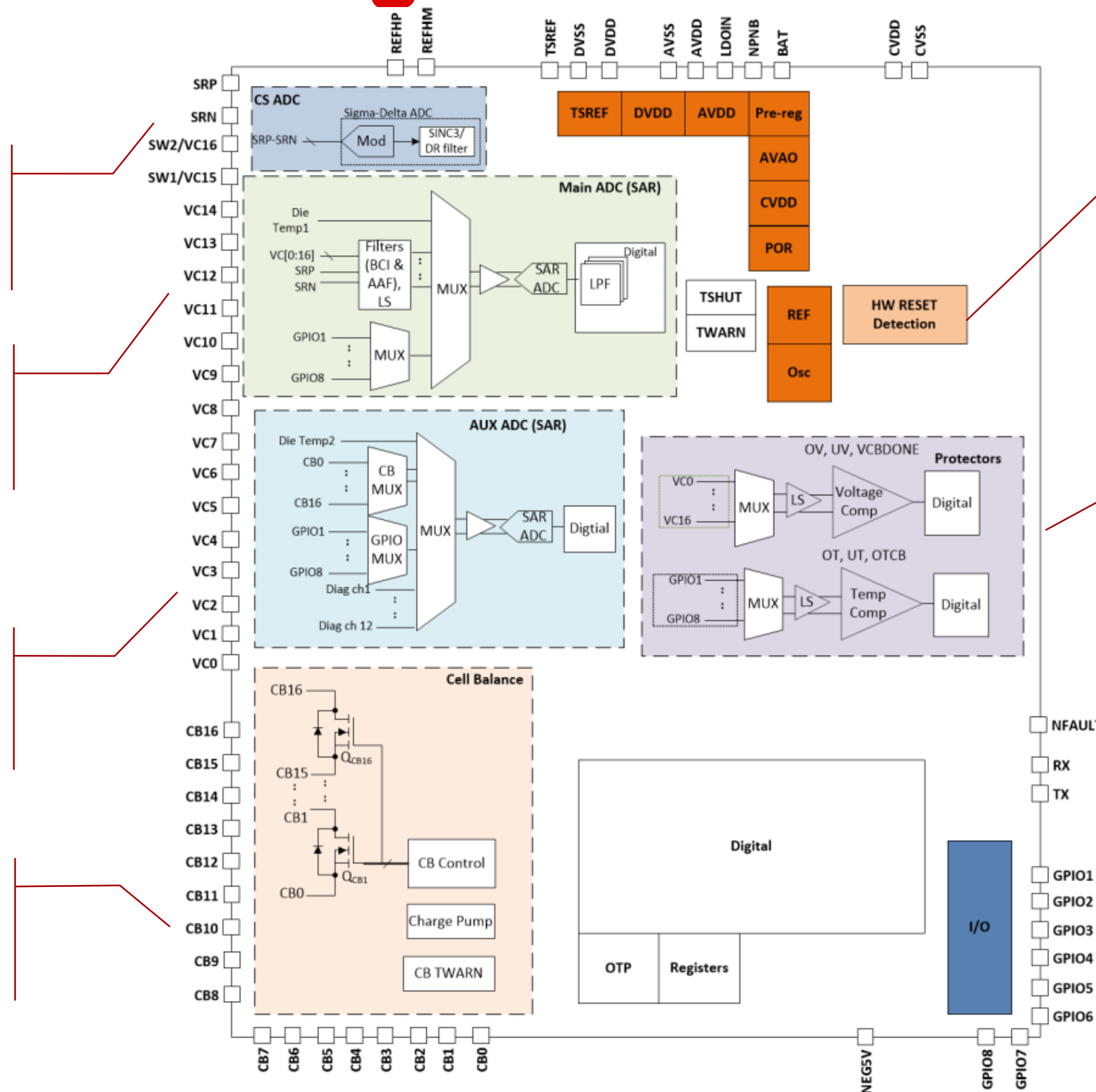
- Vcell measurement
- Temperature measurement

AUX ADC

- Redundant path
- Diagnostic channel
- Measure VBAT etc.

Cell balancing

- 300-mA balancing @ 60 C
- Dynamic thermal management



Hardware reset

- Emulate POR reset
- pure analog
- Available in all power modes

Secondary hardware protectors

- Hardware comparators independent of ADC
- OV, UV, OT, UT
- Operate in sleep mode

GPIOs

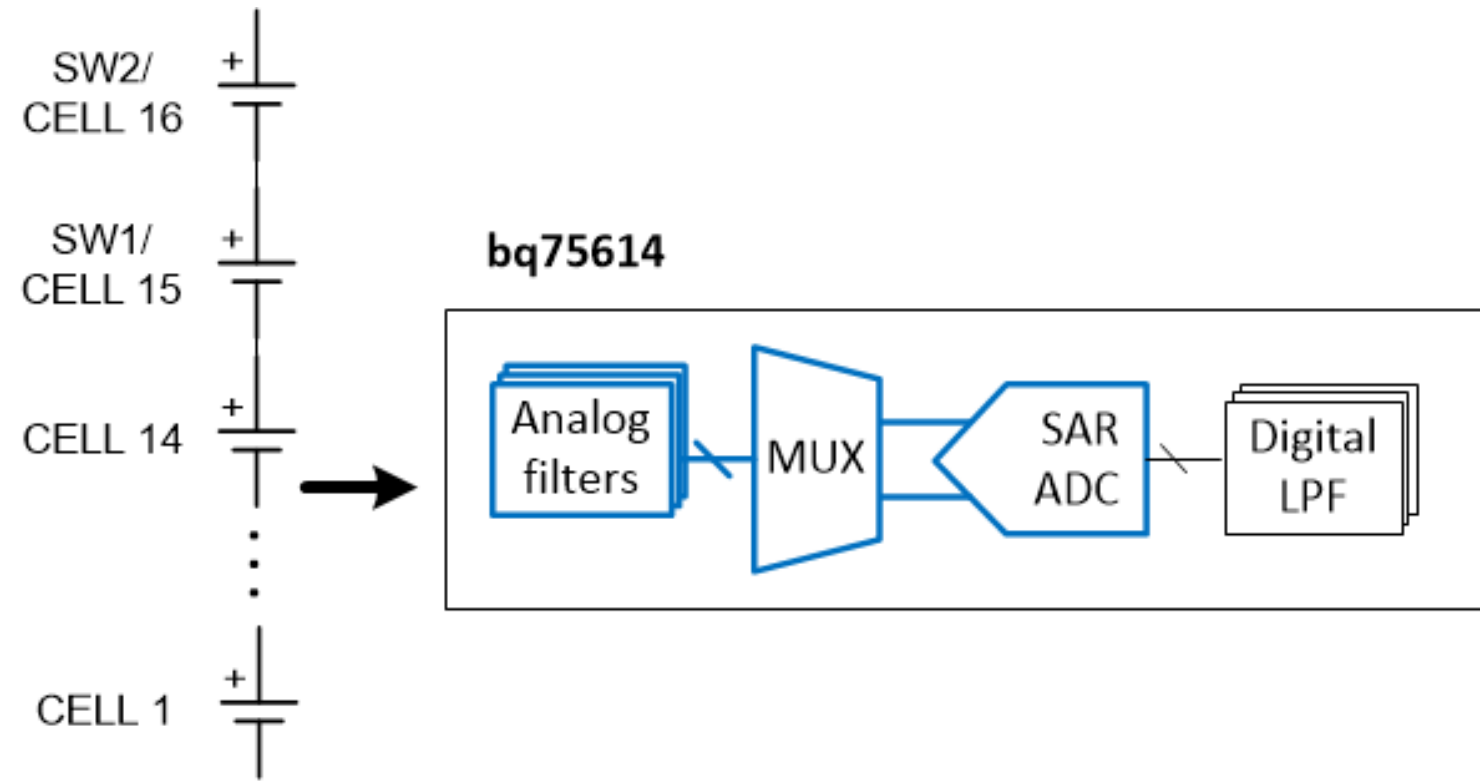
- 8 GPIOs
- NTC thermistor
- Analog voltage input
- SPI master

Voltage & current measurement

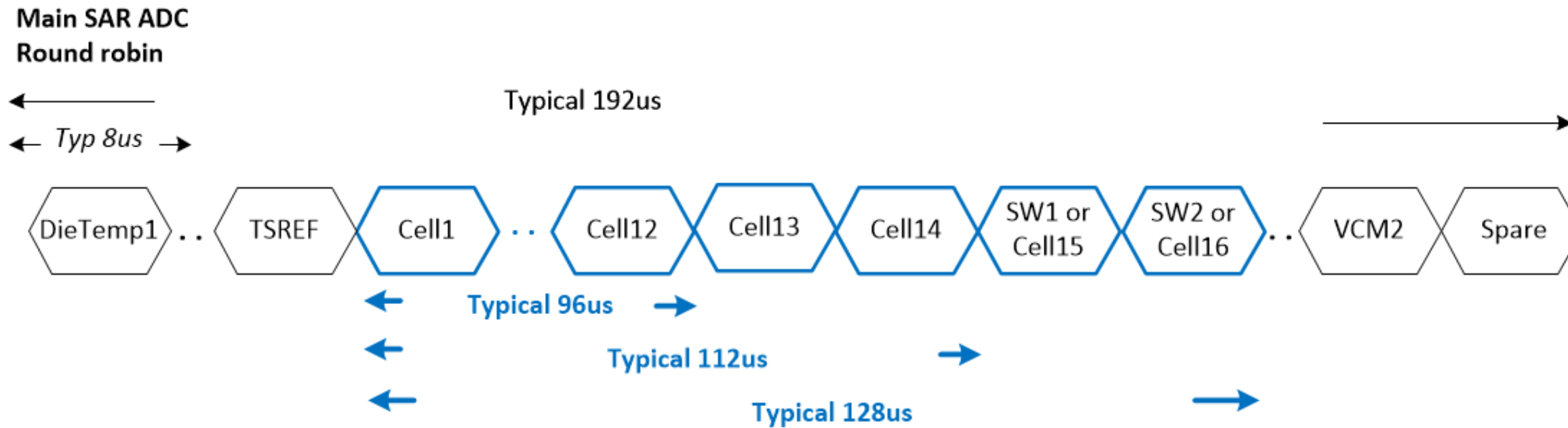
Why measure voltage and current?

- Continuous current measurement and timing synchronization allows system to optimize coulomb counting calculation.
- Synchronized V and I measurement allows system to execute optimized SOC/SOH algorithm.
- Accurate cell voltage and pack current measurements provide the best SOC/SOH estimations.

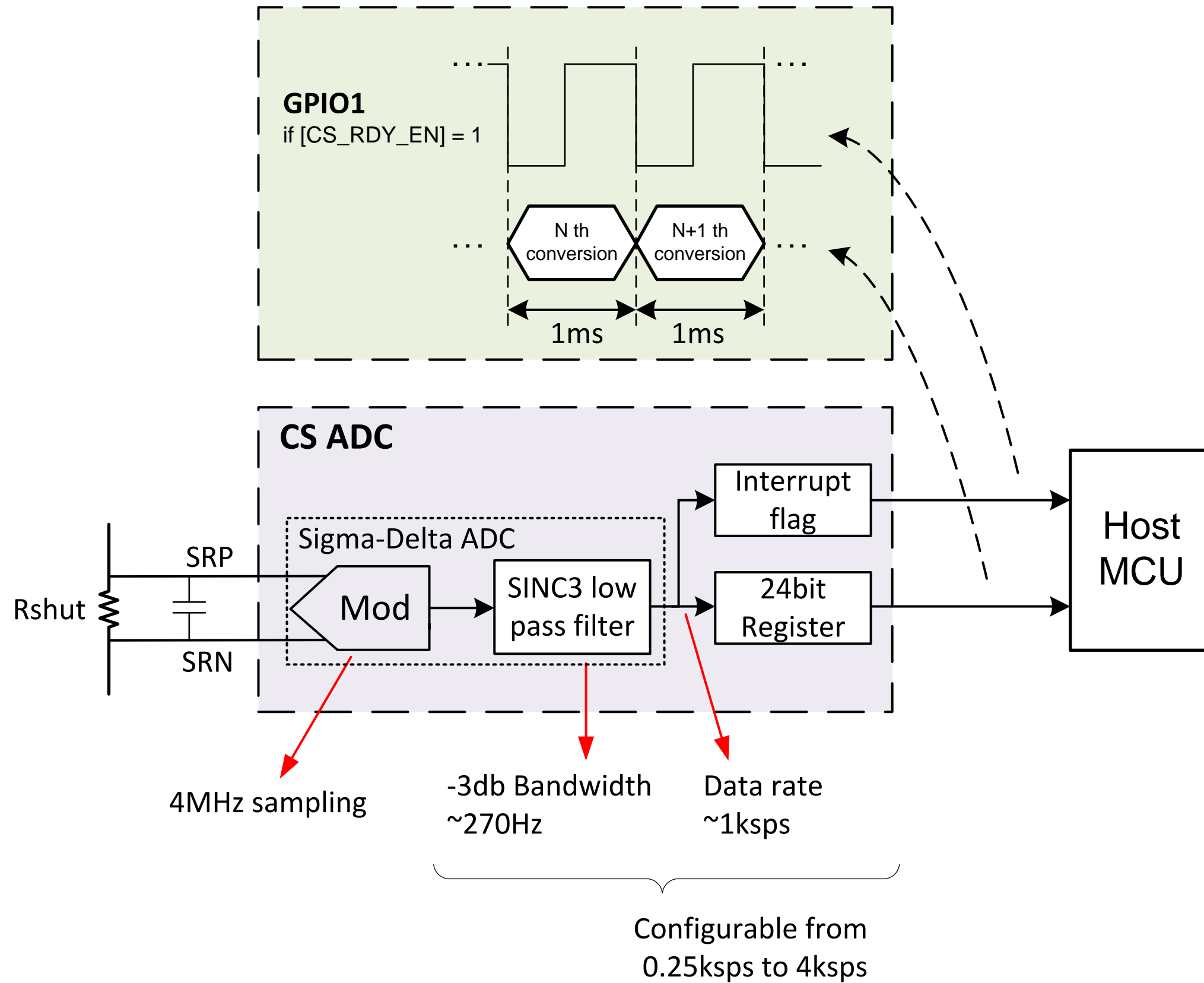
Cell voltage measurement



- Cell voltage is synchronized with in 112 us
- Cell voltage is refreshed every 192 us
- Integrated digital low-pass filter (6.5 Hz, 53 Hz, etc. configurable)

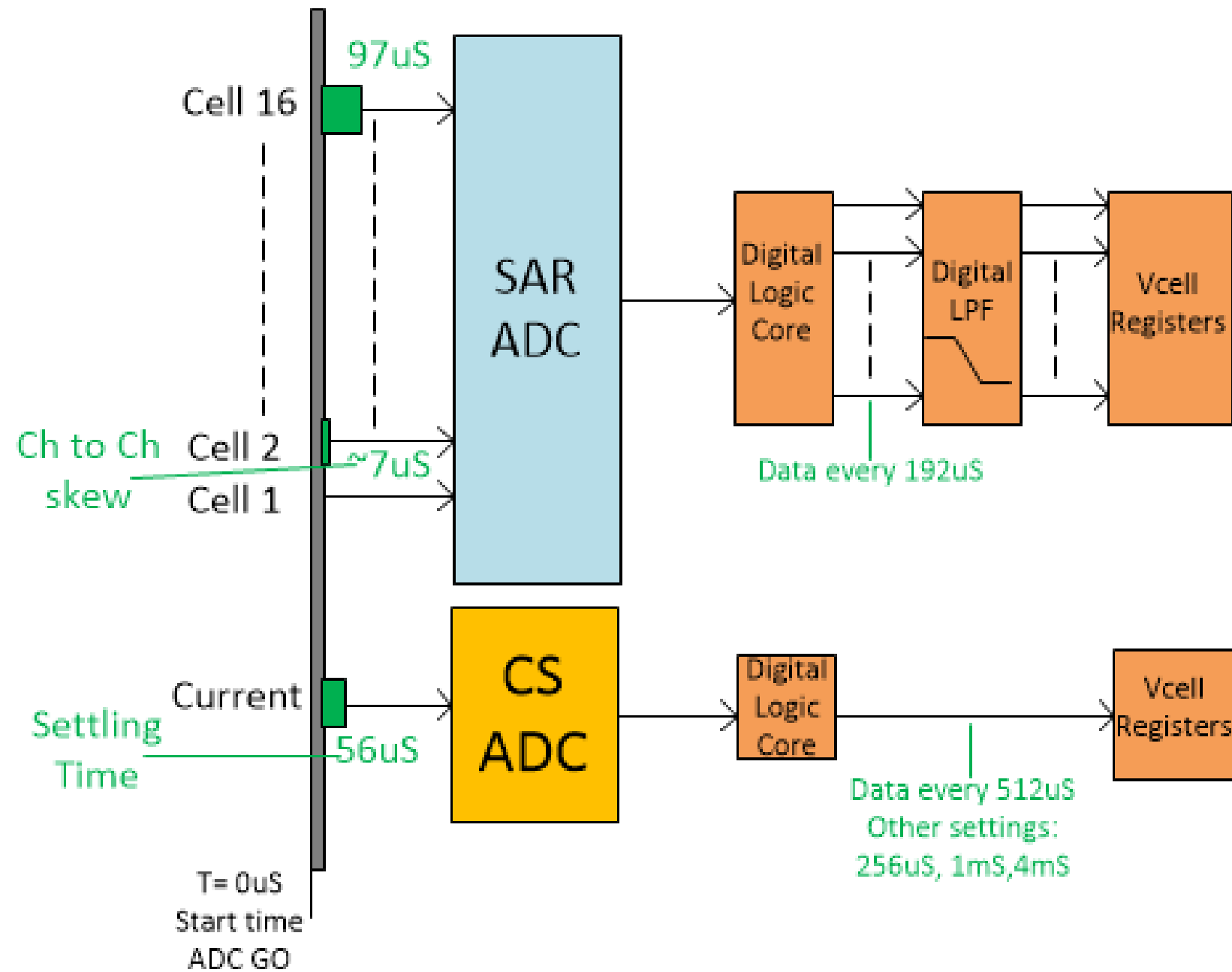


Current measurement



Parameter	Value	Comment
Input range	+/- 122.5 mV	
Offset	+/- 1.5 uV	Full temp range
Gain error	+/- 0.4%	Full temp 0.3%
Effective number of bits (ENOB)	16.5 bits	@ 1 ksps
Data rate	1 ksps	Configurable
Resolution	14.6 nV/LSB	24-bit result

VI signal path

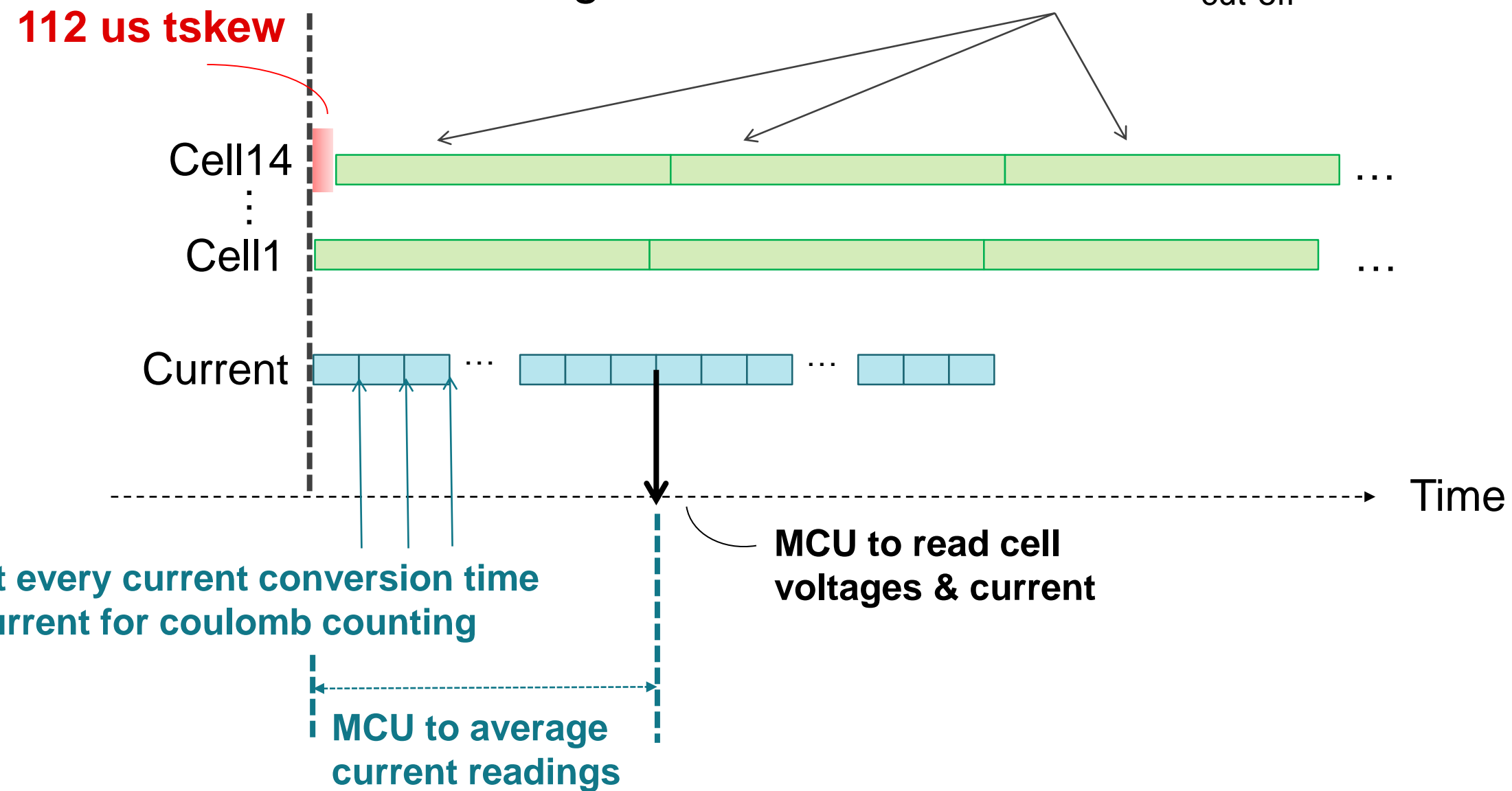


- Vcell analog-to-digital converter (ADC) has a digital low-pass filter (LPF) in the data path. This LPF needs to be accounted for when considering accuracy of voltage measurement.
- For accurate voltage and current sync, the current measurement needs to have the same amount of filtering as the voltage.
- This filter time constant can be much greater than the difference between V and I data readout rates.

Voltage/current synchronization

Cell voltage average through digital low-pass filter

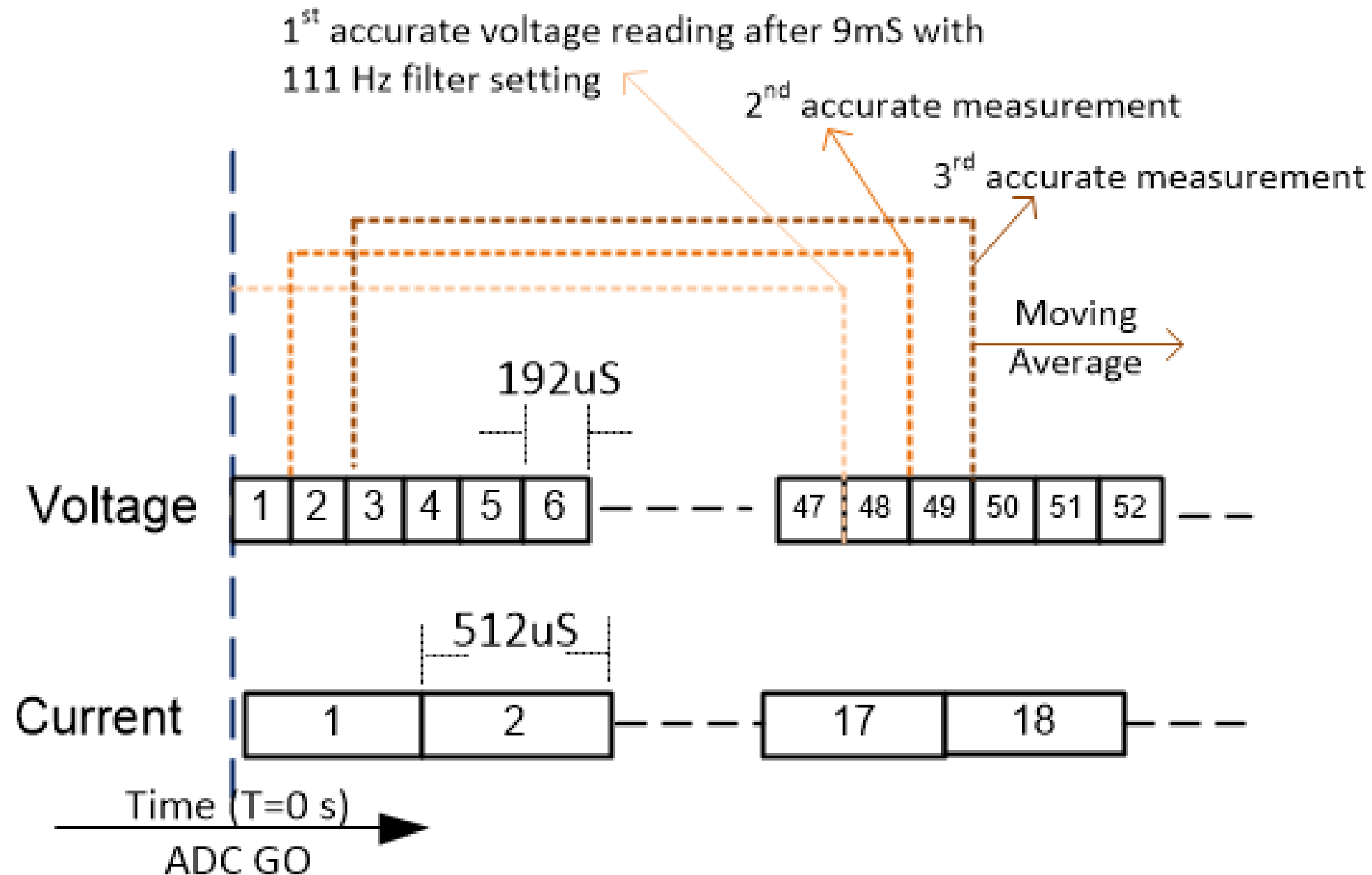
Average time based on selected $f_{\text{cut-off}}$



MCU to read current at every current conversion time

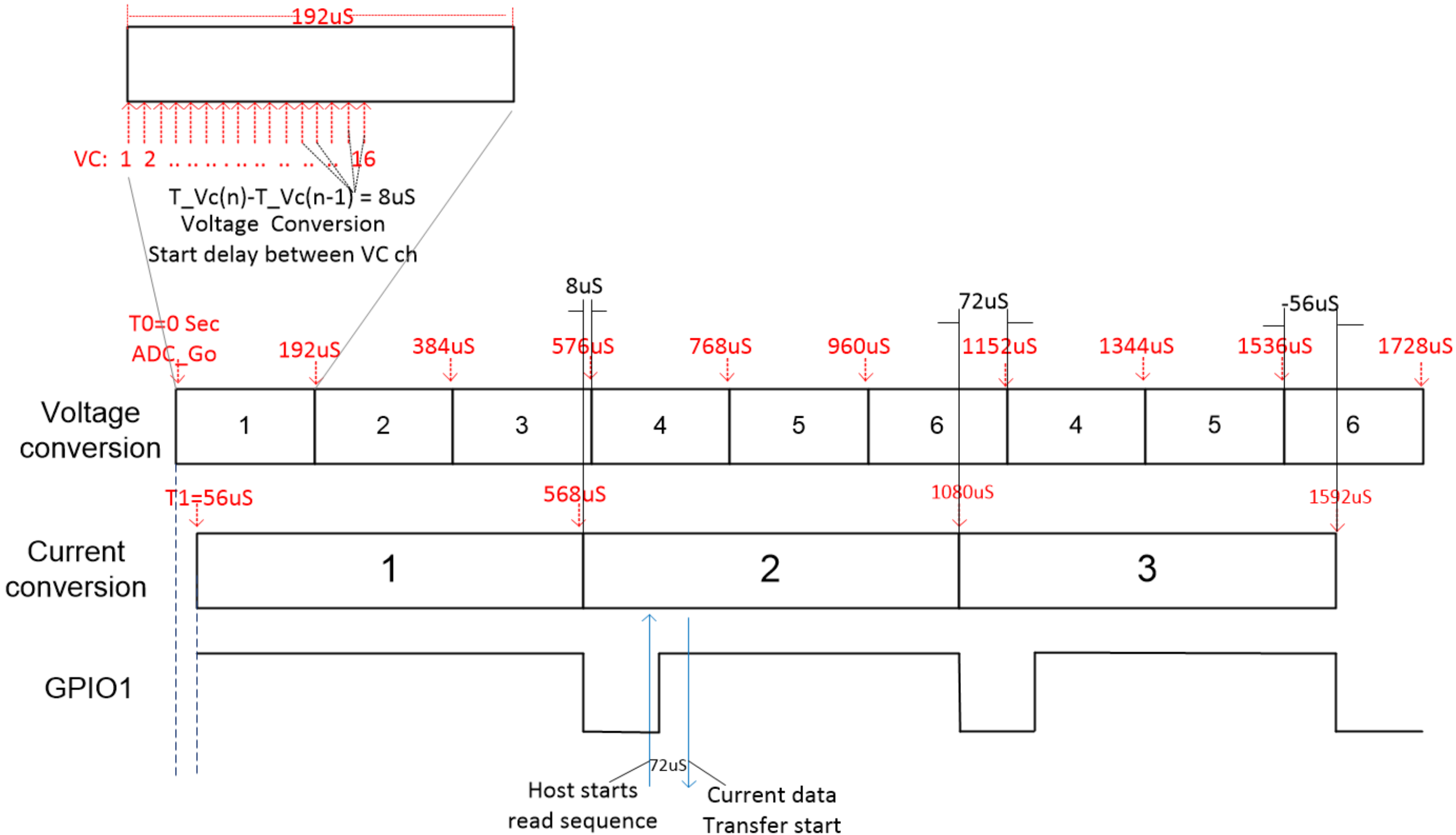
- MCU to integrate current for coulomb counting

Vcell filter impact on voltage and current synchronization



- Example with 111-Hz Vcell filter setting shown.
- When filter is used for accurate voltage measurement, its settling time is much larger than the readout time delta between voltage and current. Filter settling time is also larger than the conversion rates.
- For accurate average current measurement over this same period (Vcell filter time constant), the current averaging can be done using the micro controller over this time.

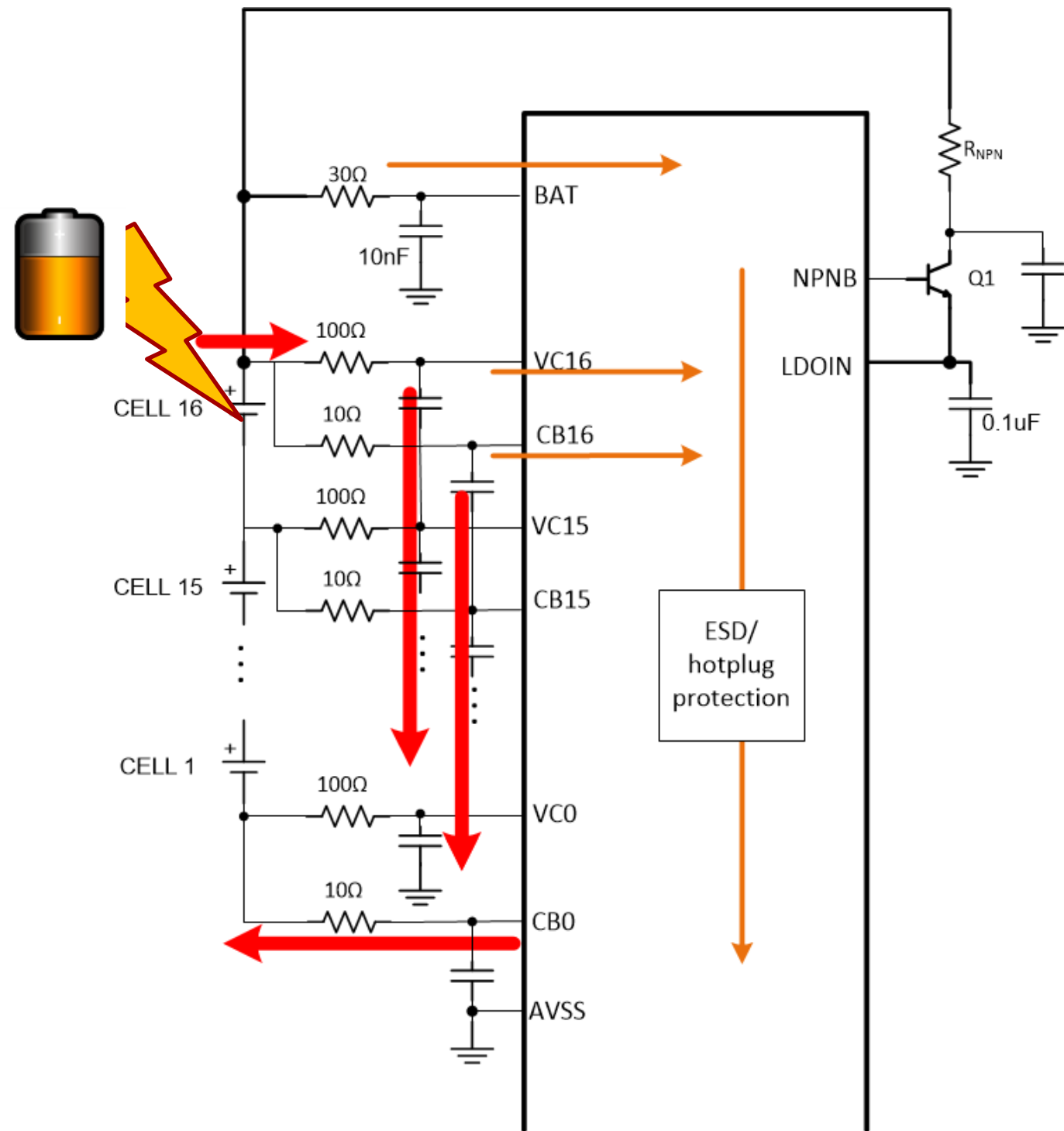
Time delay between voltage and current readout



- The sync delay at the end of the current sense (CS) ADC ready is 8 uS, 72 uS and -56 uS respectively for the first 3 CS ADC readouts. 8 uS, 72 uS and -56 uS delay cycles in this order for subsequent CS ADC readouts.
- The max delay between V and I readout is therefore 72 uS.

Reference schematic and hotplug

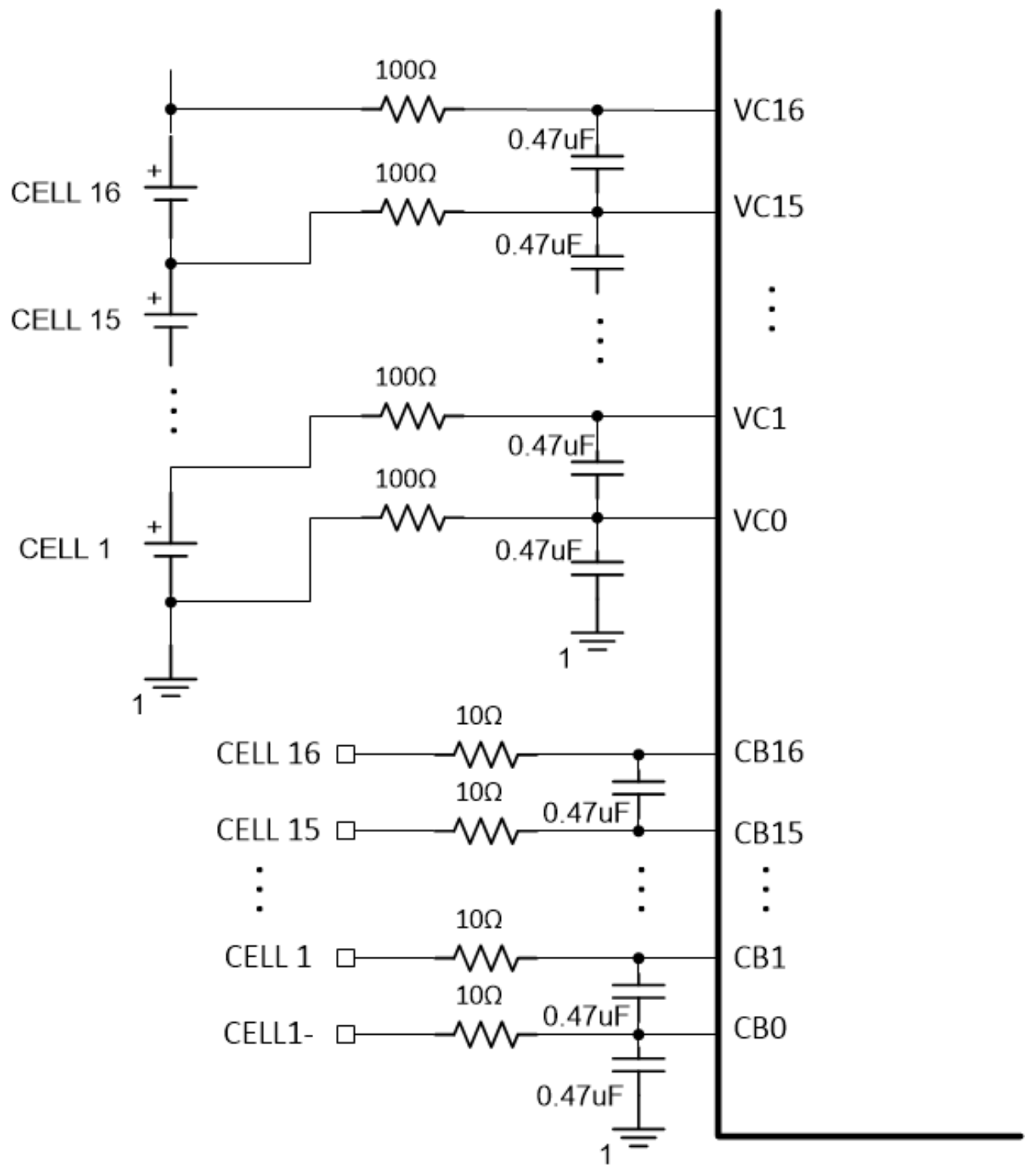
What is a hotplug event?



- A hotplug event is different than an electrostatic discharge (ESD) event in several ways:
 - The input voltage in a hotplug event doesn't collapse as in an ESD event (because a battery cell is an energy source).
 - The current path, peak current and RC response in a hotplug event varies depending on the hotplug path.
- To protect from a hotplug event, the goal is to size the RC constant and control the ESD/hotplug protection circuit so that the majority of the current flow is routed through the external RC components.
- Device pins absolute max rating are also sized with the goal to sustain during the hotplug event.

Reference schematic – hotplug

- Support hotplug with only simple different RC filters:
 - Low voltageage and <1-uF cap (16-V rated cap)
 - No diode clamp
 - No single-ended high-voltage cap
 - No additional cell-side differential cap



Two options on cell sensing pins RC:

	Option 1	Option 2
VC pins	R = 100 Ω C = 0.47 uF/16 V	R = 100 Ω C = 0.1 uF/16 V
CB pins	R = base on balancing current C = 0.47 uF/16 V	R = base on balancing current C = 1 uF/16 V

BQ75614 reference schematic

8 GPIOs

All can be used for thermistor connection, or option to take 1 GPIO to single MCU whenever current conversion is done (for coulomb counting calculation)

CVDD to power digital isolator

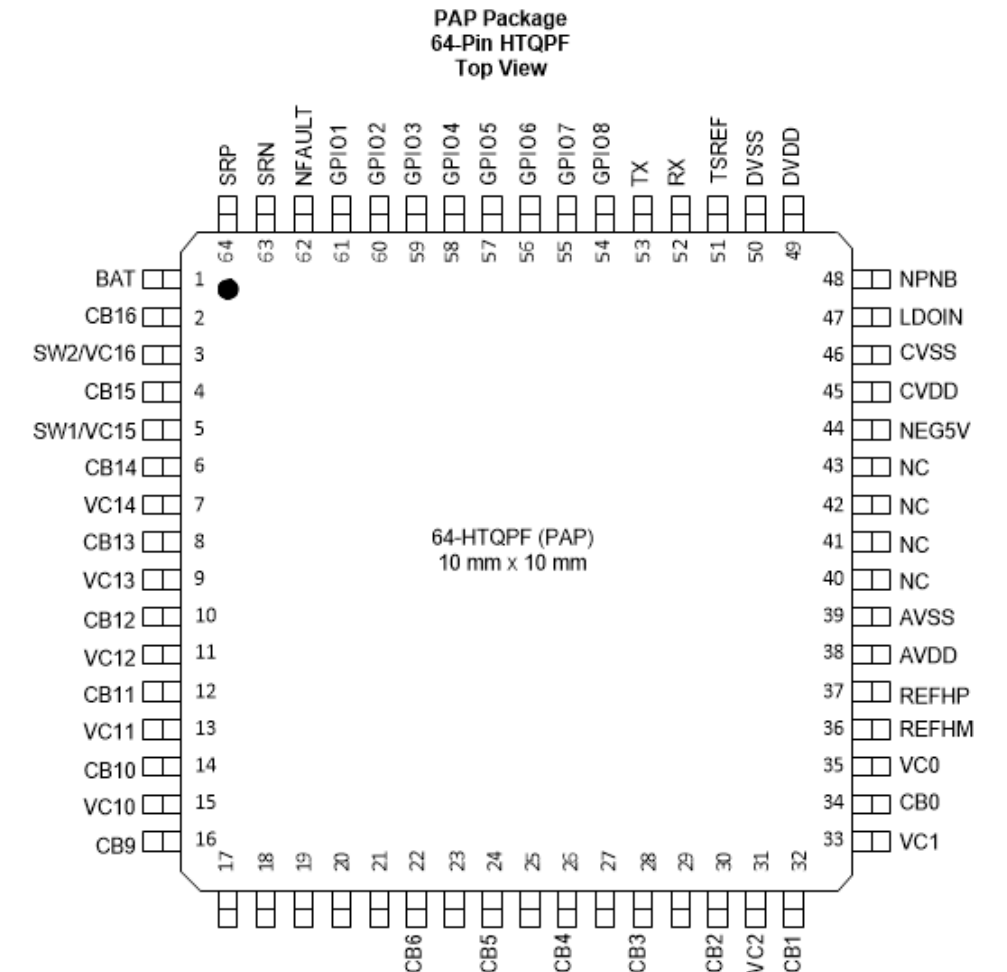
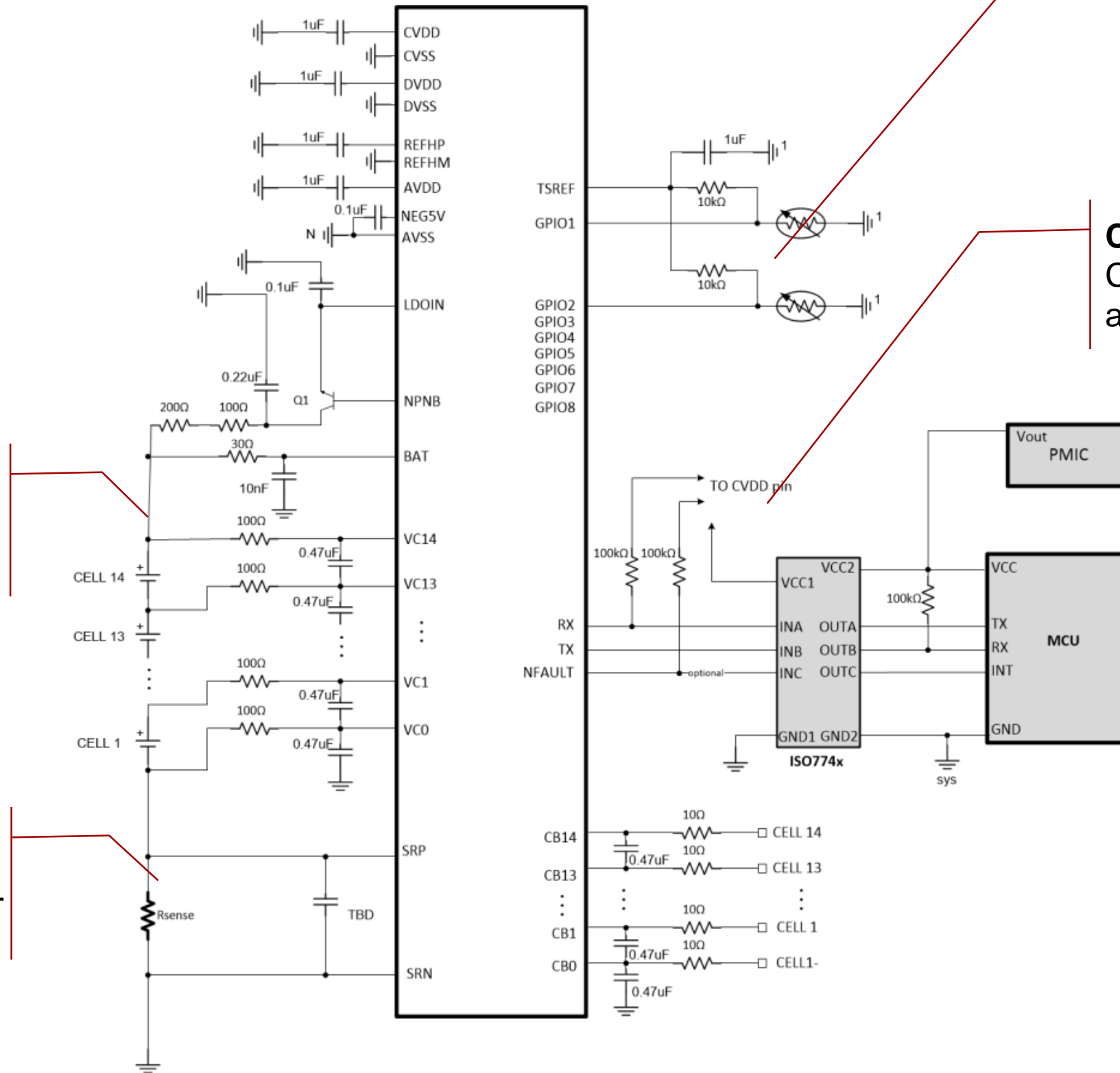
CVDD can support up to 5 mA in **shutdown** and 10 mA in **active** and **sleep** modes

Filtered Vcell measurements

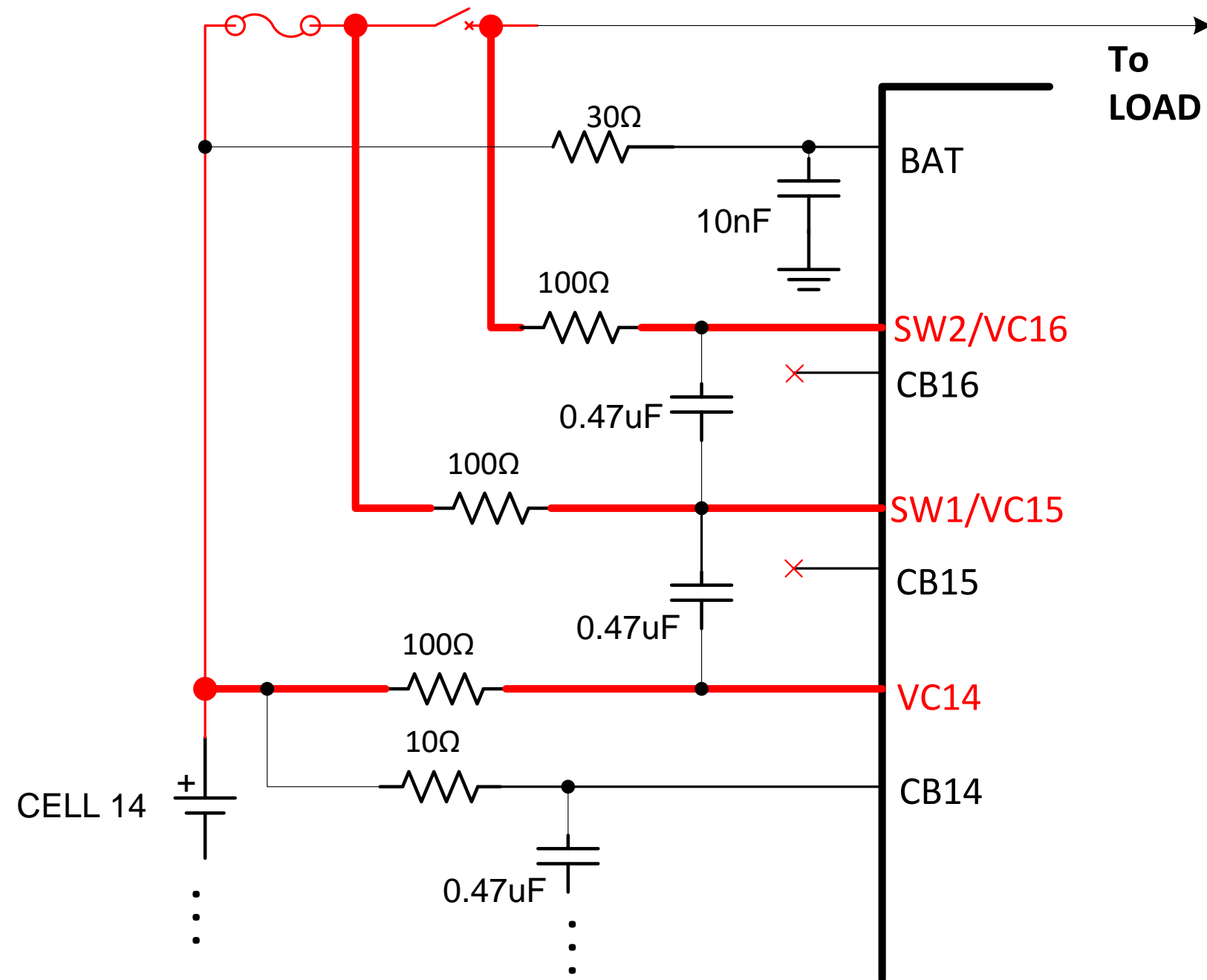
Built-in front-end filters + programmable post ADC digital LPF for best SOC/SOH calculation

Integrated current sense

Sync'd current and cell voltages measurements for best SOC/SOH calculation

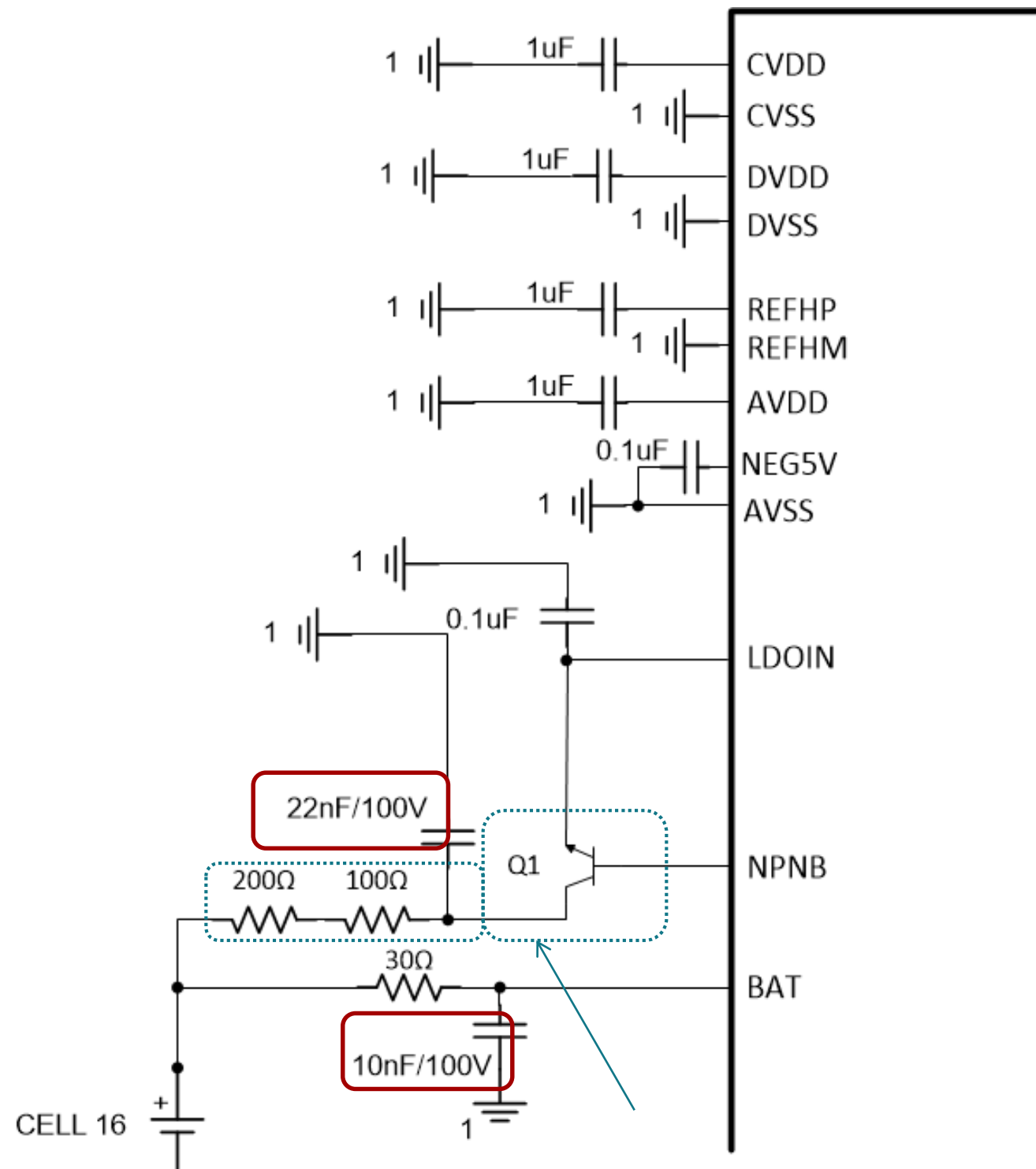


BQ75614 fuse and relay diagnostic



Diagnostic	Open/blown	Close
Fuse	$(SW1-VC14) \ll 0V$ <ul style="list-style-type: none"> SW1 will be pull down by the load 	$SW1-VC14 = \sim 0V$ <ul style="list-style-type: none"> Depends on current flow and fuse impedance (e.g. +/-0.3V)
Relay	$(SW2-SW1) \ll 0V$ <ul style="list-style-type: none"> SW2 will be pull down by the load 	$(SW2-VC1) = \sim 0V$ <ul style="list-style-type: none"> Depends on current flow and fuse impedance (e.g. +/-0.3V)

Reference schematic – power supplies



Keep a minimum 8 V at the NPN collector to ensure enough headroom for device pre-regulation

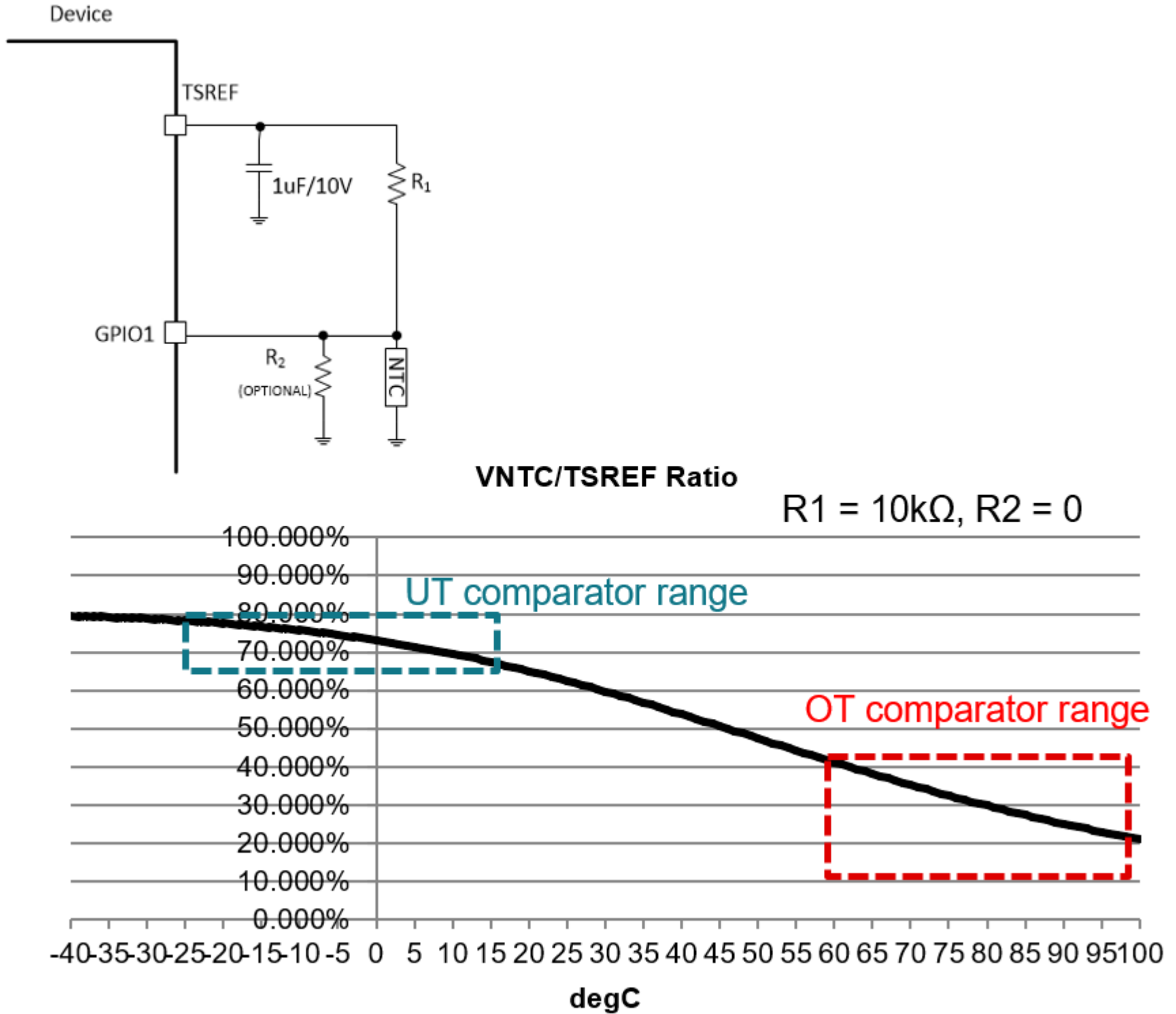
Power-supply capacitors:

- 100-V cap (10 nF on BAT and 22 nF on NPN collector)
 - Device designed to work with small capacitance to minimize bill of materials (BOM) cost of the 100-V cap.
- The rest of the power supplies capacitors are low-voltage rating (10-V rated).

NPN transistors and resistor on NPN collector:

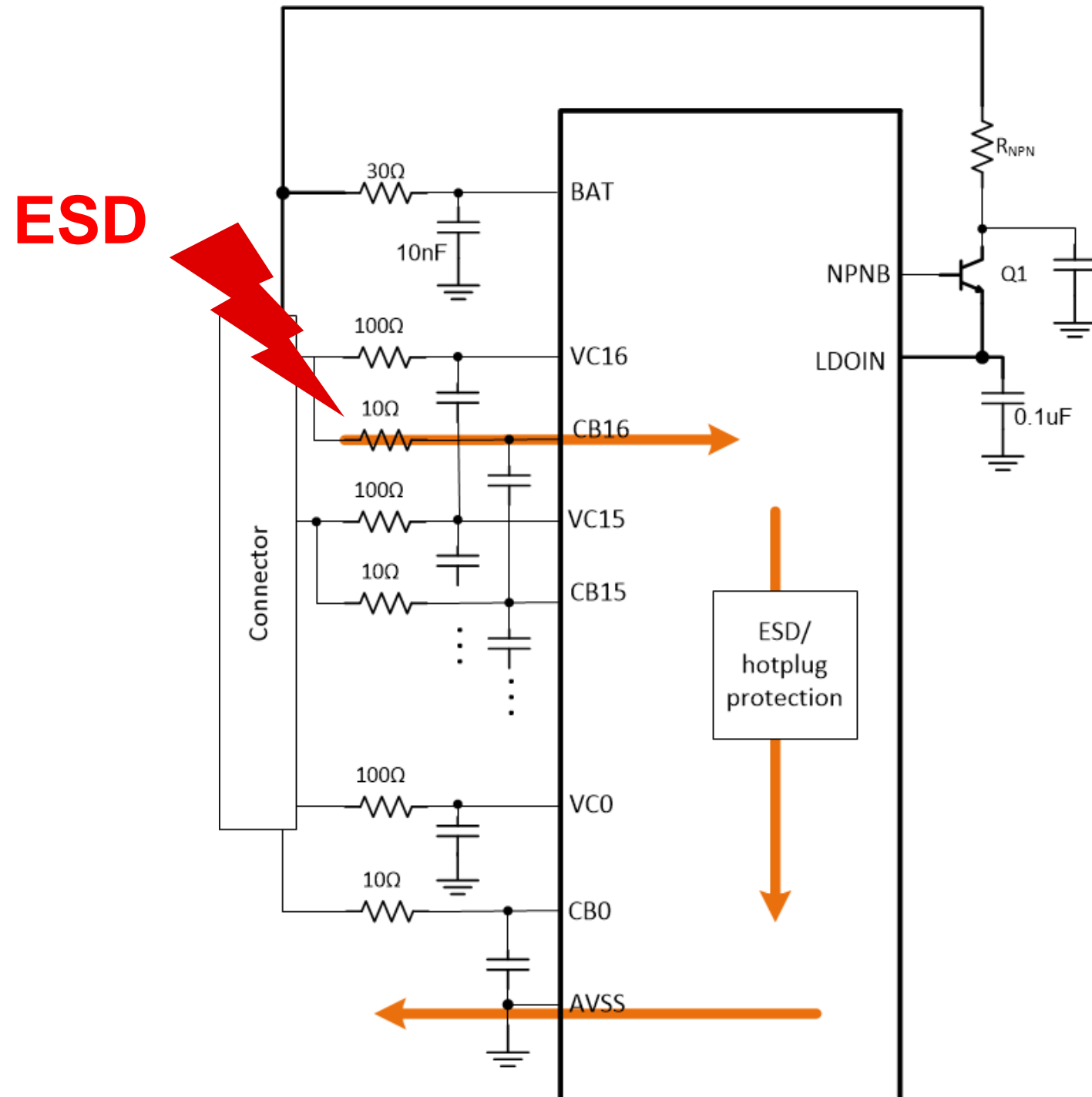
- Resistor values and NPN transistor can be further optimized (from the reference schematic values) based on the min and max module voltages for different projects.
- Choosing R on the NPN collectors:
 - System shall ensure the NPN collector will have ≥ 8 V.
 - Equation: R on collector = $(\text{Min } V_{\text{module}} - 8 \text{ V}) / 20 \text{ mA}$
- Choosing NPN transistor:
 - Voltage rating = $\text{max } V_{\text{module}} - R_{\text{collector}} I_{\text{R drop}} - V_{\text{LDOIN}}$
 - $R_{\text{collector}} I_{\text{R drop}} = (\text{Max ACTIVE mode current} * R_{\text{collector}})$
 - $V_{\text{LDOIN}} = 6\text{V}$
 - System designer shall also add additional margin for transient.
 - DC gain (equal to hfe) shall be >100 .
 - Power rating = $(\text{Max } V_{\text{module}} - R_{\text{collector}} I_{\text{R drop}} - V_{\text{LDOIN}}) / \text{Max ACTIVE current}$

Reference schematic – thermistor



- Use pull-up resistor to TSREF to form a negative temperature coefficient (NTC) thermistor connection.
- Device supports ratiometric measurement through the ADC.
- The integrated OT, UT comparators have a wide range of programmable threshold to support different R₁ and R₂ resistor ratio.

ESD protection



- In an ESD event, the on-chip ESD production circuit provides a low impedance path to discharge the ESD strike.
- The input voltage (spike voltage) collapses as the ESD protection is triggered, resulting in short event.
- Current flow path in an ESD is similar on each pin.

Cell balancing & thermal management

Why cell balancing?

- Helps extend runtime and ensure safe battery operation.
- Corrects imbalances in the battery itself. It helps to equalize aging of the cells.
- A battery can only deliver a charge until its weakest cell has discharged completely, even though other cells may have plenty of charge left.
- Increases battery life by maximizing the capacity of the battery pack and ensuring that all of its energy is available
- Ensures safe operation of the battery by preventing cell overcharge and overdischarge, both of which can lead to accelerated cell degradation and create potentially hazardous operating scenarios.
- There are two common approaches to cell balancing: active cell balancing and passive cell balancing.

Cell balancing control

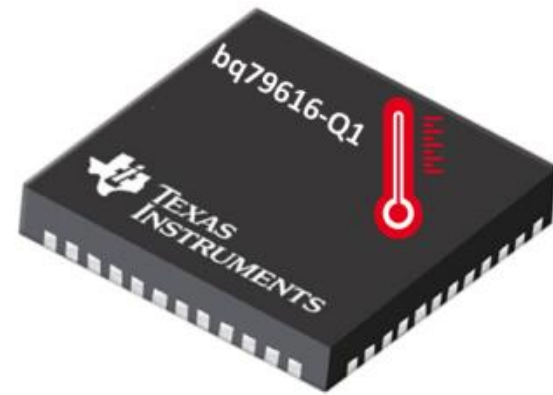
	Auto CB control	Manual CB control
Control	Always duty cycle between odd and even	Only turn on the channels that are enabled
Stop conditions	Timers (up to 10 hr) and cell voltage threshold	Timers (up to 10 hr) and cell voltage threshold
Thermal pause	Yes	Yes

C B 1	C B 2	C B 3	C B 4	C B 5	C B 6	C B 7	C B 8	C B 9	C B 10	C B 11	C B 12	C B 13	C B 14	C B 15	C B 16	Valid or Invalid setting	Manual CB control
Green	Green	Green	Green	Green	Green	Green	Green	Green	Green	Green	Green	Green	Green	Green	Green	Invalid setting	Total enabled channels >, or > 2 consecutive channels are enabled
Green	Green	Grey	Grey	Green	Green	Green	Green	Green	Green	Green	Green	Green	Green	Green	Green	Valid	Ok, device turns on the enabled channels
Green	Grey	Grey	Grey	Grey	Green	Grey	Grey	Green	Grey	Grey	Green	Grey	Grey	Green	Grey		

- **Auto CB control** can support all the configurations listed above.

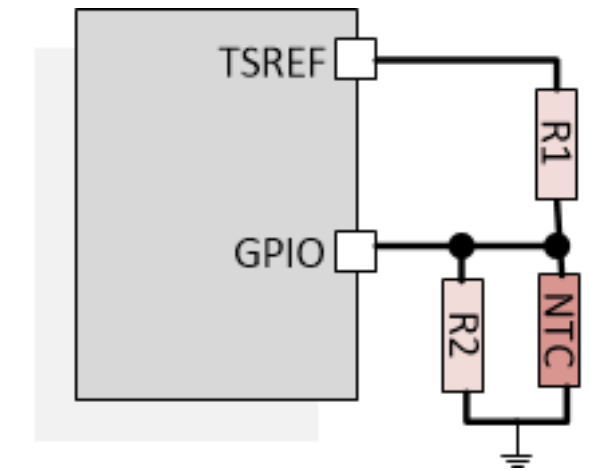
CB thermal pause

CB TWARN



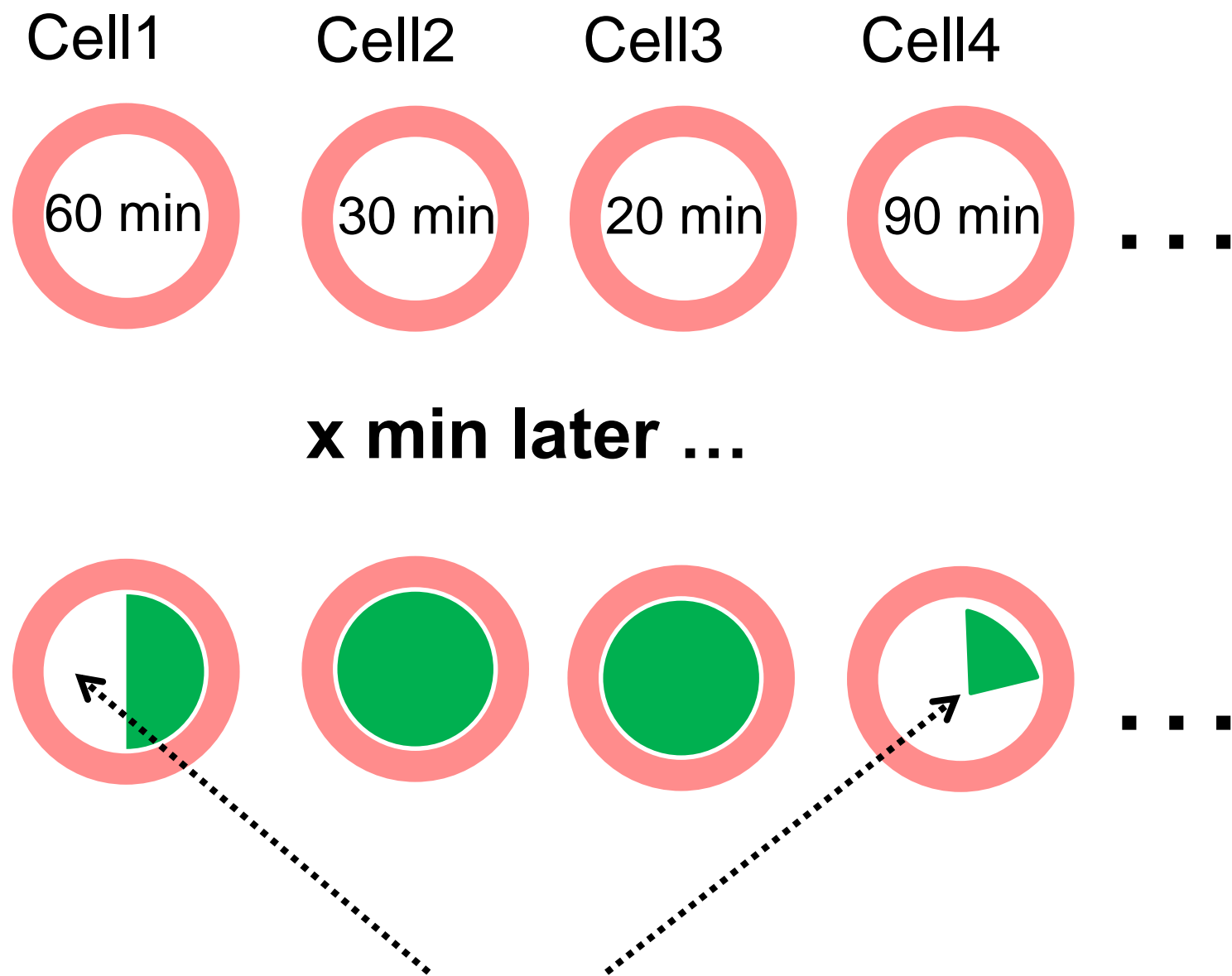
- Monitor through internal die temperature.
- Pause CB if die temp $> 105^{\circ}\text{C}$.
- Recover with 10°C hysteresis.
- Always on.

Thermistor OTCB



- Monitor through external thermistor.
- Pause CB if thermistor measurement $>$ OTCB threshold (programmable).
- Resume CB with COOLOFF hysteresis (programmable).
- Register bit enable.

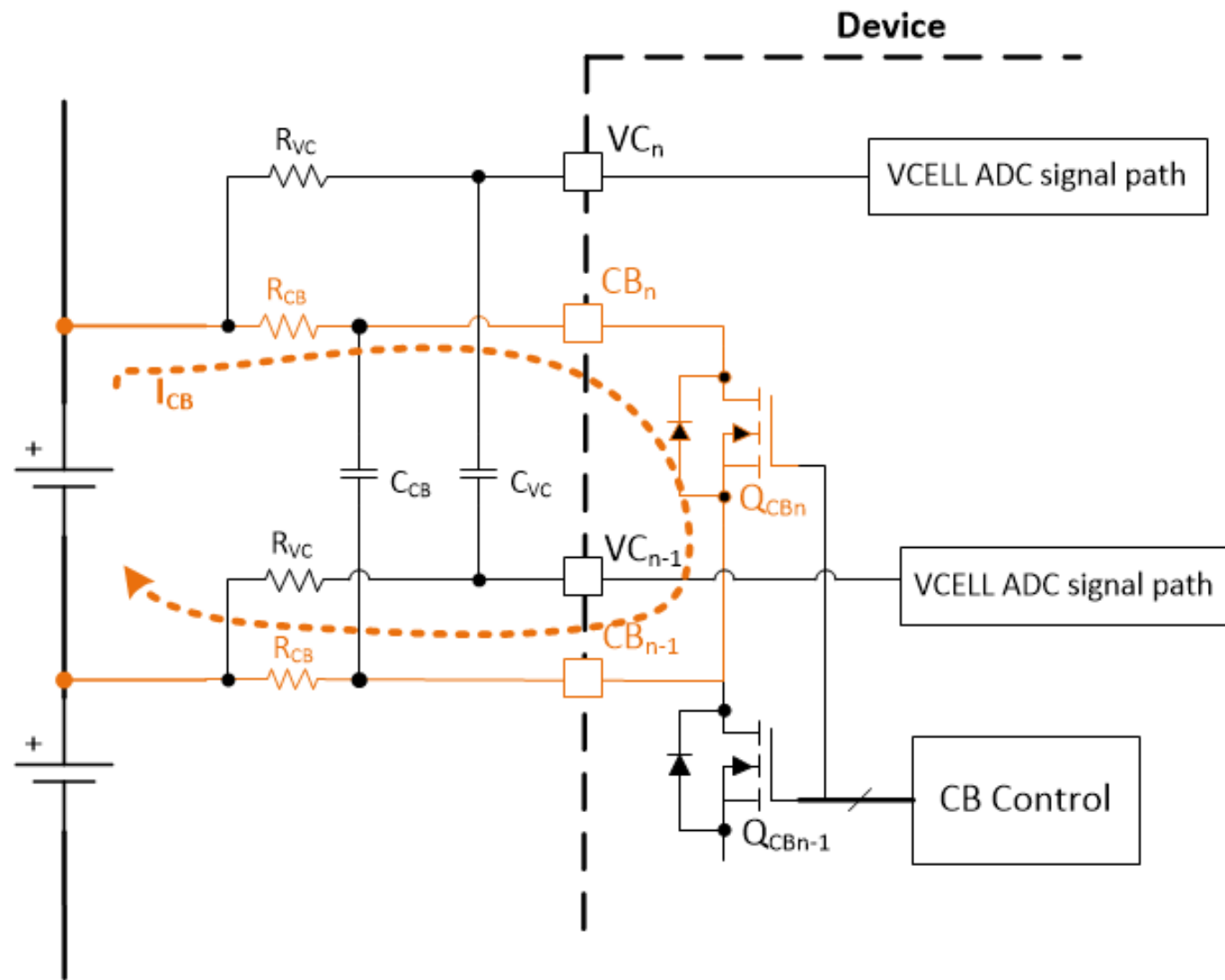
CB remaining timers



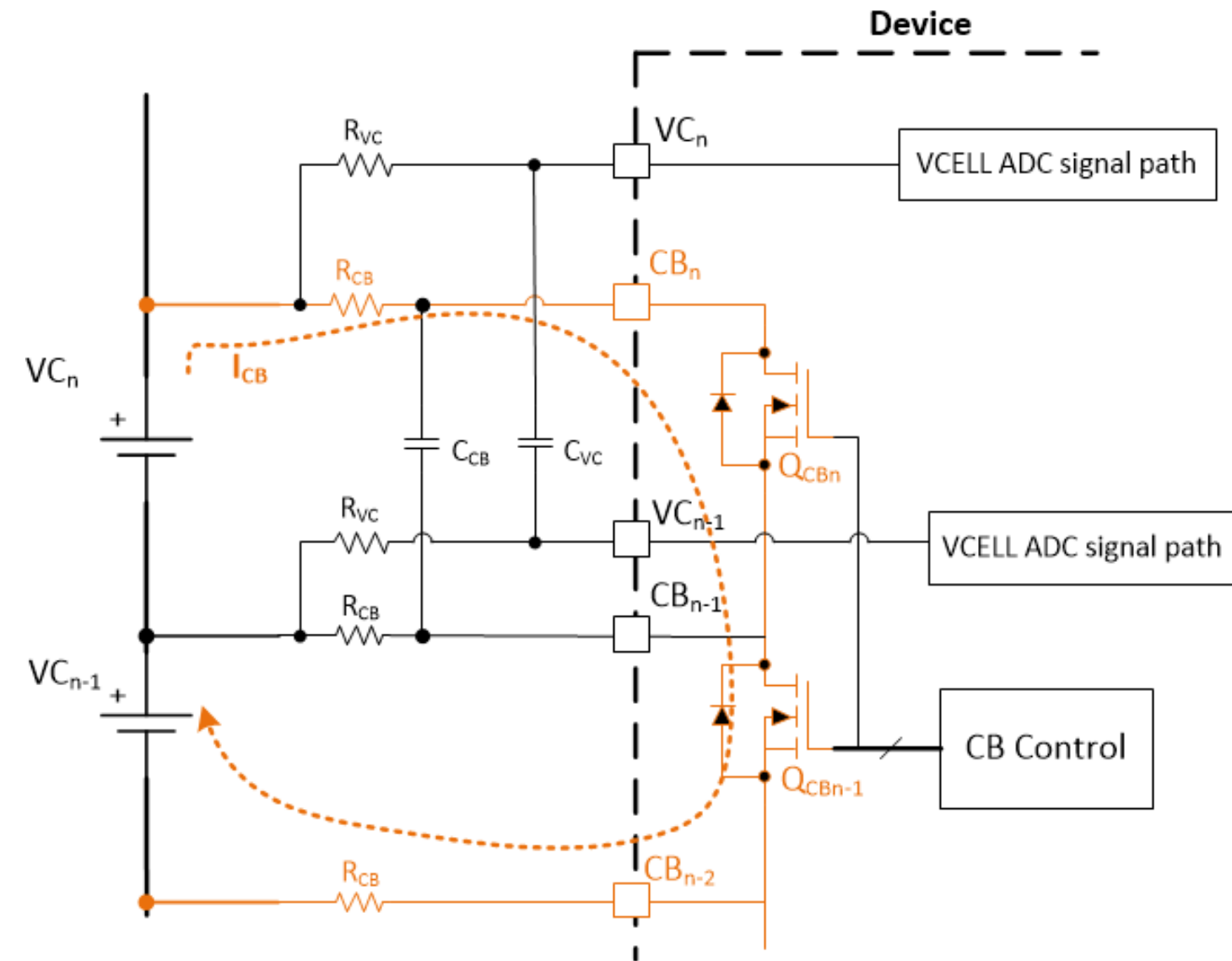
MCU can read out the remaining balancing time.
Better balancing time tracking and capacity estimation.

- Each cell can set with a different balancing time.
- CB thermal pause function:
 - Good for hardware thermal control.
 - But system may lose track of the total balancing time for SOC calculation.
- CB remaining timers:
 - Keep track of the remaining balancing time on each cell.
 - MCU can read this information anytime (only valid if CB is running).

Cell balancing current



$$I_{CB} = \frac{V_{Cell}}{(2 \times R_{CB}) + R_{dson_{Q_{CB}}}}$$



$$I_{CB} = \frac{\text{Sum of two } V_{CELL}}{(2 \times R_{CB}) + R_{dson_{Q_{CBn}}} + R_{dson_{Q_{CBn-1}}}}$$

Conclusion

- 48-V systems are trending in automotive, micro-mobility and energy storage because they provide:
 - Higher output than 12-V systems.
 - Higher power capability.
 - Lower load currents compared to 12 V.
- When designing 48-V systems, there are a few challenges to consider:
 - Accurate and synchronous on V/I measurement to enable accurate SOC/SOH.
 - Avoid thermal runways with ASIL rated HW protector.
 - Proper balancing the voltage of the cells in the pack to extend the runtime and battery life.
 - Avoid hotplug issues that could damage the cell monitor.
- The BQ75614-Q1 offers a robust and best-in-class performance solution to monitor and balance 48-V battery-management systems.



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