AEC-Q100 GaN: FUTURE FOR ON-BOARD CHARGING AND HIGH-VOLTAGE DC/DC
What will we cover?

• GaN FET basics
• TI GaN devices
  • Direct drive architecture
  • Automotive qualification
  • Reliability and rigorous testing
• Design tools and reference solutions
  • Resources for top-side, cooled packages
  • 6.6-kW on-board charger (OBC) reference design
  • Design concepts for 22 kW and 800 V
HEV/EV trends OBC & high-voltage DC/DC

- **High power density**: 1-2 kW/Liter ➔ 3-5 kW/Liter
- **Lower cost**: Higher operating frequencies → Smaller magnetics
  - Smaller magnetics → Size, cost, weight reductions
- **Fast time-to-market**: Solutions that easily scale from 3.3-22 kW, 400-800V OBCs, while delivering on performance metrics
  - Expertise in many different fields: control + power stage + magnetics
- **Reliability**: Component level and power supply level reliability
  - Confidence for adopting new wide band-gap technologies
  - Robust components for higher system reliability

New challenges for system-level design
- **On-board charger**: Increasing power density, support bidirectional power flow for V2G/V2L, support 800V batteries
- **DC/DC**: Size and cost reductions, redundant designs for ASIL, active monitoring of system thermals and performance
GaN FET basics

Low $C_G, Q_G$ gate capacitance/charge (1 nC-$\Omega$ vs Si 4 nC-$\Omega$)
✓ Faster turn-on and turn-off, higher switching speed
✓ Reduced gate drive losses

Low $C_{OSS}, Q_{OSS}$ output capacitance/charge (5 nC-$\Omega$ vs Si 25 nC-$\Omega$)
✓ Faster switching, high switching frequencies
✓ Reduced switching losses

Low $R_{DSON}$ (5 m$\Omega$-cm$^2$ vs Si >10 m$\Omega$-cm$^2$)
✓ Lower conduction losses

Zero $Q_{RR}$ No ‘body diode’
✓ No reverse recovery losses
✓ Reduces ringing on switch node and EMI
GaN vs SiC: Ideal switching comparison

Figure-of-merit = switching energy (µJ) * $R_{DS,ON}@125^\circ C$ (mΩ)

The smaller, the better!

Hard-switching figure-of-merit (turn-on and turn-off losses, plus Coss & QRR losses)

Soft-switching figure-of-merit (turn-off losses only; ZVS at turn-on)
TI’s approach to GaN

Features and reliability
LMG352xR030-Q1 GaN FET with integrated driver, protection & reporting

650-V GaN FET 30mΩ

Integrated 2.2-MHz gate driver
- Minimizes parasitic inductances (<1nH common source; <4H gate-loop)
- Adjustable slew rate (30 - 150 V/ns)

Internal buck-boost and LDO
- Support for 7.5-18-V unregulated supply
- 5-V regulated output for powering digital isolator and peripherals

Integrated protection features:
- GaN FET temperature digital PWM reporting for active power management
- Over-current (OCP), over-temperature (OTP) and short-circuit protections (SCP)

https://www.ti.com/product/LMG3522R030-Q1
What is direct drive?

**Typical cascode dMode GaN**

- **Cascode** $C_{oss}$ is sum of $C_{oss}$ of silicon FET and $C_{gs}$ of GaN FET
- High $C_{oss}$ when $V_{ds} < 10V$; high losses if ZVS is not achieved

**TI direct drive**

- **Direct-Drive** reduces $Q_{oss}$ by at least 20% at 400V operation
- Allows <100ns dead-time
**TI GaN qualification & reliability summary**

**Reliable in power supply**
- JESD47, JEP-180 and AEC-Q100 Grade 1 qualification
- Every GaN product qualified inside power supply running at high voltage/current/temp against charge trapping

**Intrinsically reliable GaN**
- <1 FIT over 10-years at 125°C, from 1.8Mhours of reliability test data for time dependent breakdown
- Over 1 billion years switching lifetime under hard-switching against hot-electron wear-out

**Robust by design**
- Designed to withstand 720-V voltage surge
- Integrated over-current and over-temperature protection for every GaN FET
LMG352xR030-Q1 automotive qualification strategy

Why AEC-Q100 instead of AEC-Q101?

1. AEC-Q100 Grade 1 qualification for core device function, integrated driver and features
   i. Leverage TI’s expertise with power management ICs with an integrated switch
   ii. Coverage of early life failure rate (ELFR), latch-up (LU) and NVM power cycling that would otherwise not be included in Q101 qualification

2. Additional testing based on AEC’s power MOS qualifications
   i. HTOL and HAST testing with $V_{ds}$ at recommended max operating voltage
   ii. Additional testing to max specs of the integrated gate driver on the GaN gate

3. Additional testing at power supply level, based on emerging GaN standards and failure modes
   i. Dynamic $R_{ds(on)}$ stability and dynamic HTOL
   ii. Board-level reliability testing
Designing with GaN

Benefits and reference designs
**TI GaN: 6.6-kW, 400-V bi-directional on-board charger**

**Design Features**
- 2-ph interleave PFC + CLLLC with bi-directional power flow
- Single DSP control for both stages using C2000
- Multi-mode control algorithm for DC/DC enables high operating frequency in DC/DC – frequency/phase modulation/burst mode
- Resonant inductor integrated in transformer reduces BoM count
- Coupled inductor for 2-ph interleave PFC reduces BoM count
- Concept scalable to 800-V battery OBCs

**Design Benefits**
- 59% smaller DC/DC magnetics offering lower cost vs SiC
- Higher power density vs SiC

<table>
<thead>
<tr>
<th>Typical operating conditions</th>
<th>SiC</th>
<th>TI-GaN</th>
</tr>
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<tbody>
<tr>
<td>PFC switching frequency (kHz)</td>
<td>67</td>
<td>125</td>
</tr>
<tr>
<td>DC/DC switching frequency (kHz)</td>
<td>148-300</td>
<td>250-800</td>
</tr>
<tr>
<td>Open frame power density</td>
<td>(W/in³)</td>
<td>54</td>
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<tr>
<td></td>
<td>(kW/liter)</td>
<td>3.3</td>
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<tr>
<td>Efficiency (%)</td>
<td>96.5</td>
<td>97+</td>
</tr>
</tbody>
</table>
Ti GaN: 6.6-kW, 400-V, bi-directional on-board charger

Coupled inductor for 2-ph interleave PFC

Totem-pole PFC GaN FETs

CLLLC GaN FETs (pri)

500-kHz CLLLC transformer with heatsink

CLLLC GaN FETs (sec)
6.6-kW OBC: Test results

PFC Efficiency

- Voltage: $V_{IN} = 240$ VAC
- Output: $V_{OUT} = 400$ VDC
- Frequency: $f_s = 120$ kHz

CLLLC Efficiency

- Voltage: $V_{IN} = 400$ VDC
- Output: $V_{OUT} = 350$ VDC
- Frequency: $f_s = 500$ kHz

High $dV_{DS}/dt$ for low I-V overlap loss

500kHz CLLLC operation

ZVS in <60ns deadtime
6.6-kW OBC: Test results

[Graphs showing system efficiency, loss vs. $P_{OUT}$, total harmonic distortion, and $V_{OUT}$ regulation accuracy with and without bias.]

Search PMP22560 on TI.com for the full test results
### Design features

- Supports **800-V battery** using LMG3522R030-Q1 650-V/30-mΩ GaN FET with integrated driver & protection
- 6.6-kW from single phase AC input
- Utilize **series stack of GaN FETs** on secondary side of CLLLC DC/DC Converter
  - Concept scalable to three-phase AC input 11-kW/22-kW modular OBCs
- Two-phase CCM totem pole PFC converter

### Design benefits

- High power density, low solution cost due to high switching frequency
- >500kHz operation enabled by **superior switching capability of 650-V GaN** (vs 1200-V FETs)
  - Better switching figure-of-merit \( (C_{OSS(TR)} \times R_{DS}) \)
  - Zero reverse recovery for GaN FETs
- **Integrated fault protection/reporting for every GaN FET** offers redundancy and simplifies compliance

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**Series-stacked FET architecture using 650-V GaN for 800-V battery**

All devices shown are 650-V rated
Building toward three-phase AC, 11/22-kW OBC

**Modular OBC**

| DC Bus voltage / PFC & primary FET | 400-450-V DC bus / 650-V FET |

3x 3.6-kW in parallel = 11-kW OBC  
3x 7.2-kW in parallel = 22-kW OBC

**Benefits**

- Reusable components and effort across one and three-phase designs
- Better light load efficiency by only enabling one ‘module’ when connected to one-phase AC sources
- Balanced approach for managing transformer thermals and system cost
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