Texas Instruments

TI POWER

TI *Live!* BATTERY MANAGEMENT SYSTEMS SEMINAR

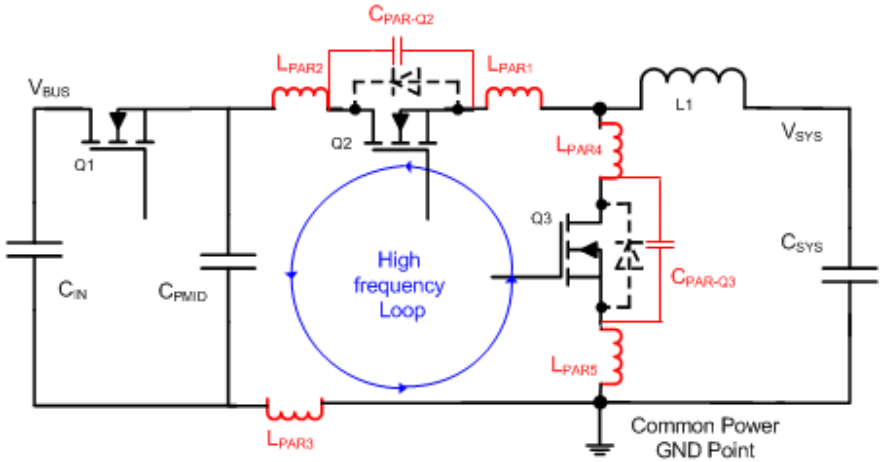
TIGER ZHOU

SWITCHING CHARGER PCB LAYOUT TIPS AND EXAMPLE

Content

- Switching charger layout key considerations
- Optimize electrical performance with minimized circuit noise
  - Noise sources and parasitics
    - di/dt loop, dv/dt coupling
  - Solutions:
    - Components placement, shielding, bypassing, ground partition, routing sensitive signal
- Optimize thermal performance
- Layout optimization examples
  - Buck-boost EVM, 5S power tools, notebook charger
- Summary

Key considerations of switching chargers

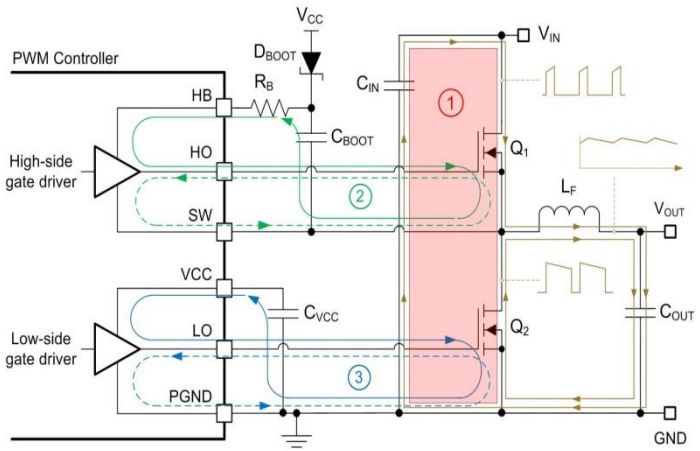


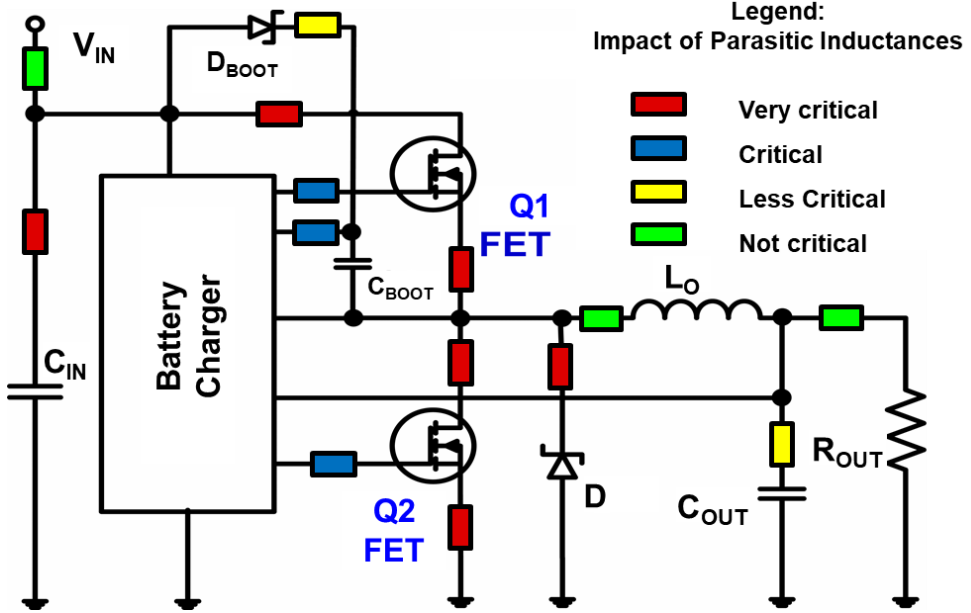
Layout is key to achieve the optimal electrical and thermal performance:

- Goals: low noise operation, low EMI, high accuracy, high efficiency, low temp
- Issues: high slew rate of di/dt or dv/dt, parasitic, noise, etc.
- Solutions: minimize coupling, optimize ground and improve the accuracy

Key to a successful layout is to understand the circuit, including the parasitic components.

Noise source –high di/dt loop

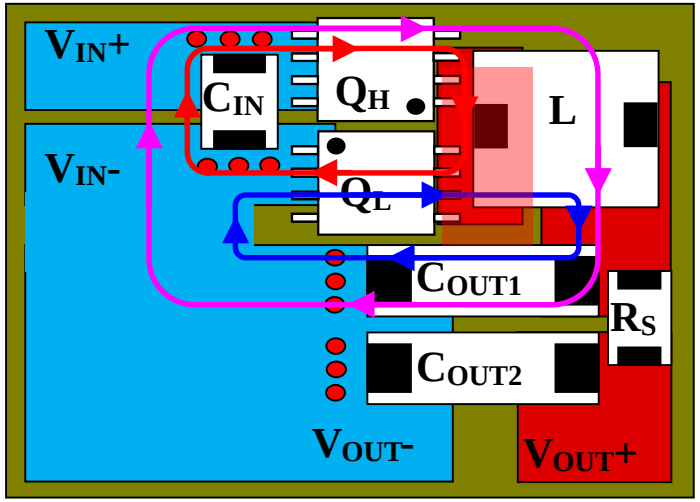


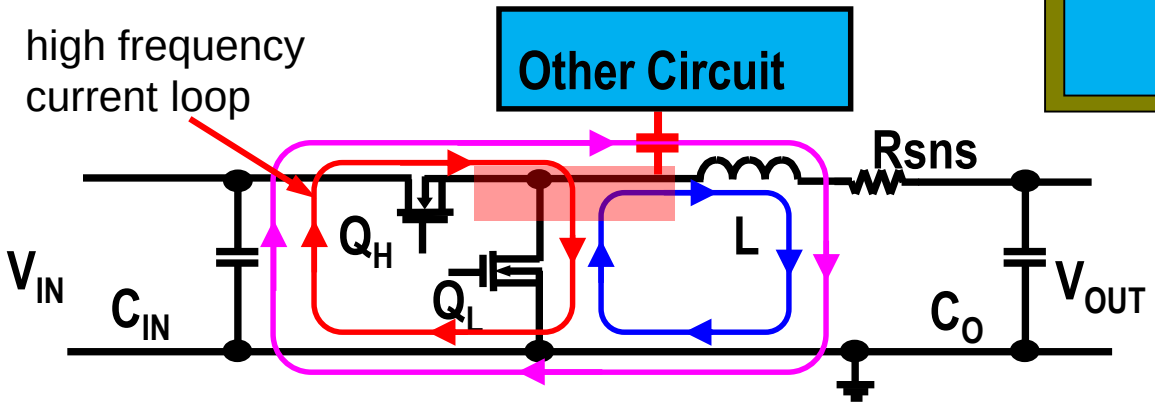


- Identify high di/dt loops
- Prioritize component placement to reduce high di/dt loop area

Components placement example

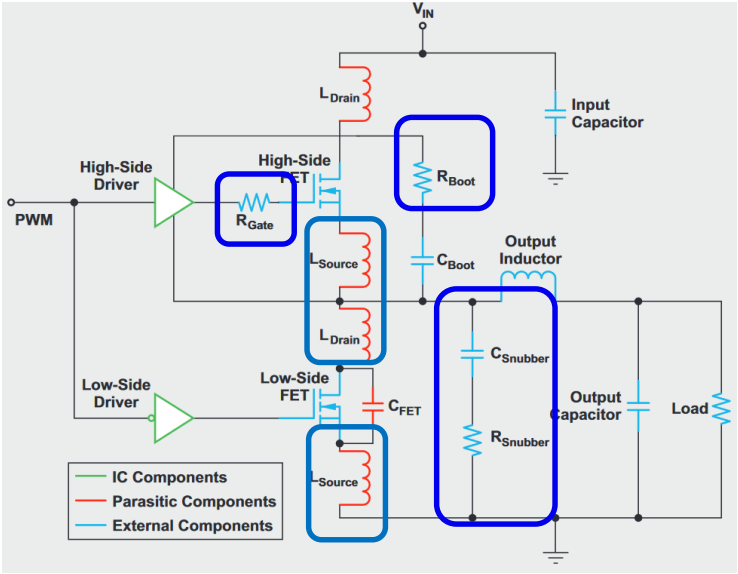
- Small high frequency current loop

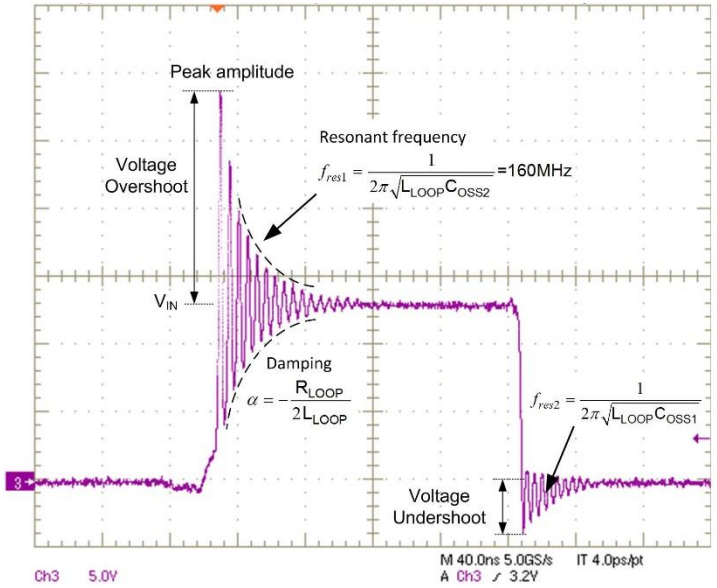


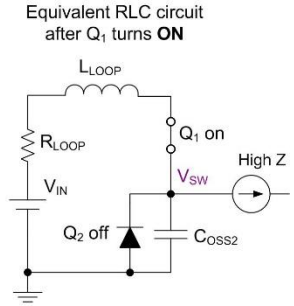


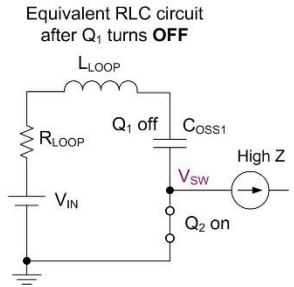
Noise source –dv/dt coupling

- The buck converter switch node rising edge ringing is related to L_{Drain}, L_{Source}, low side C_{FET} and input capacitor. The falling edge ringing is related to high side FET's Coss and low side FET's parasitic inductance.





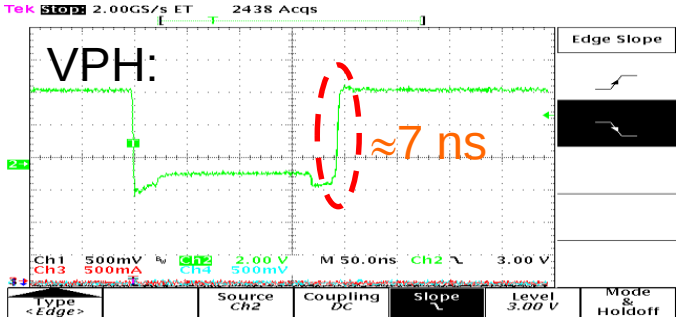




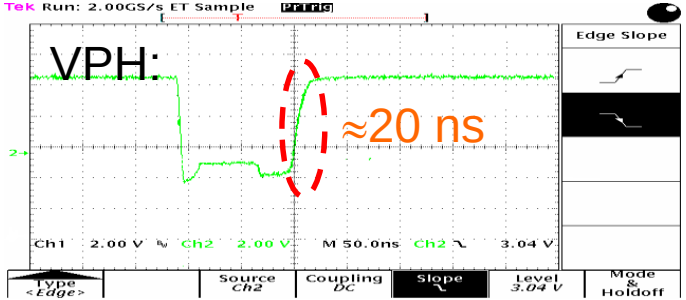
http://www.ti.com/lit/an/slyt465/slyt465.pdf

Reduce EMI noise by suppressing switch node ringing

- Suppress switch node ringing
  - Add Rboot
  - Add RC snubber
  - Add Rgate
  - Reduce parasitic inductance



15-dB noise reduction



Parasitic resistance

All conductors exhibit resistance – (except superconductors)

- Simple formulae exist for specific geometries
- Sheet Resistivity: $R_{sheet} = \rho \frac{l}{A}$
- ≈ 500 µΩ per square for 1 oz (34 µm) copper

This is important where currents are high

Current sensing resistors – 10 mΩ typical

Copper has a large temperature co-efficient of resistance $TCR_{cu} \approx 4000\, ppm\, °C^{-1}$ (+40% for 100 °C rise)

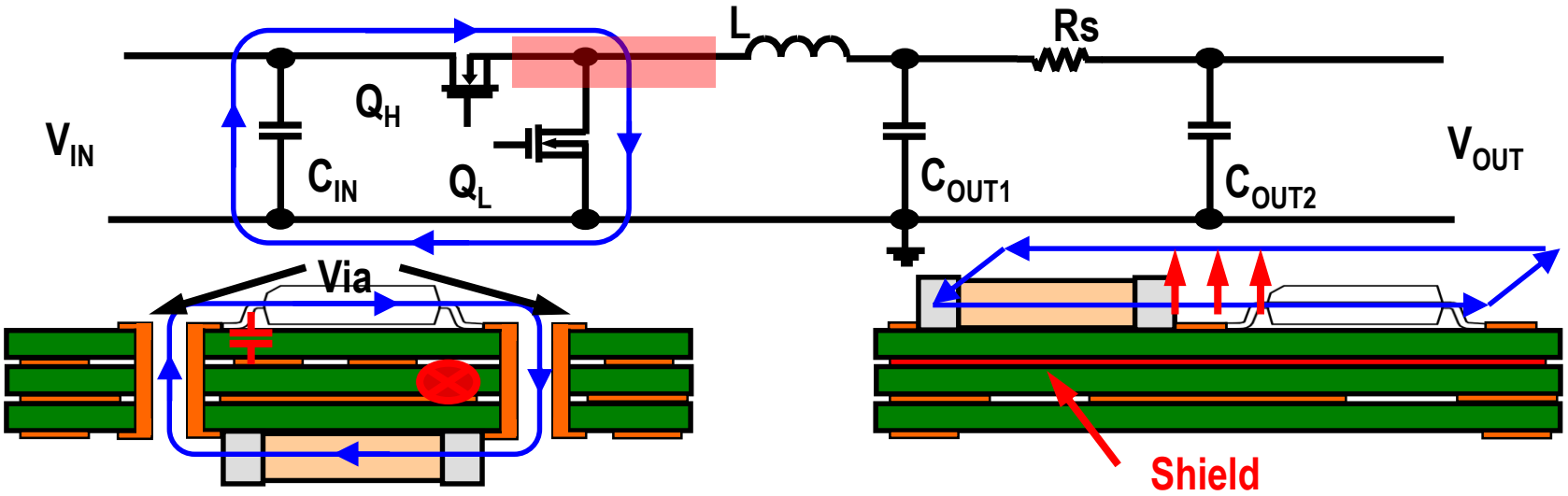
Copper Weight (Oz.)	Thickness (mm/mils)	mΩ per Square (25 °C)
1/2	0.02/0.7	1.0
1	0.04/1.4	0.5
2	0.07/2.8	0.2

4*500 µΩ = 2 mΩ

Layout tips

1. Same layer components placement reduces parasitic

- Put power components on the same layer and use ground layer to shield switching noise

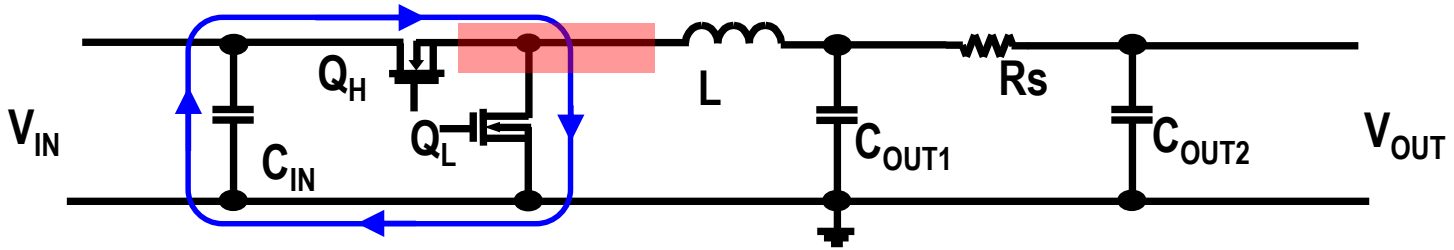


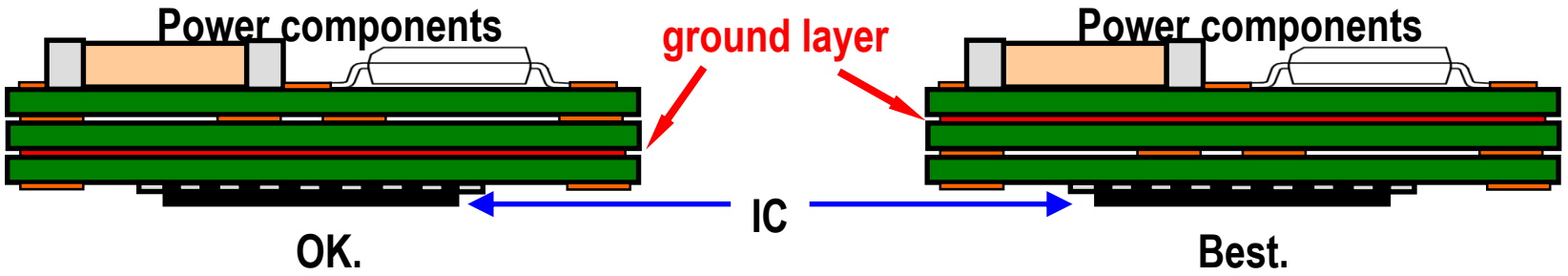
Internal layer trace has coupling (inductive and capacitive)

Can use ground plane to reduce inductive and capacitive coupling.

2. Noise shielding with ground layer

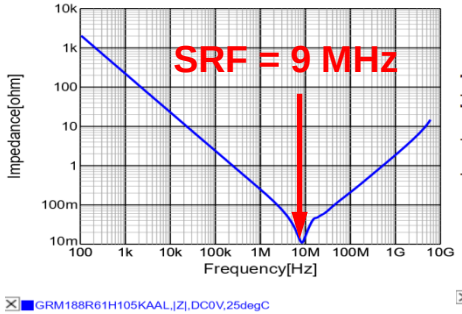
- Ground layer near power component layer can reduce:
  - Inductive and capacitive coupling noise
  - High frequency current loop area





3. Coupling minimization with ceramic capacitors

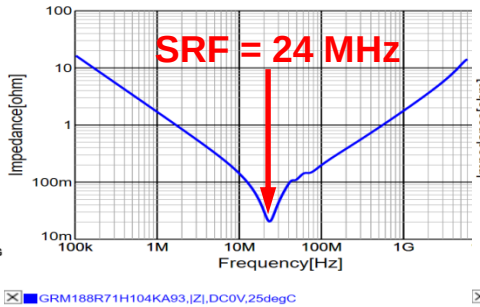
- A small capacitor can provide lower impedance at high frequency
- Put 10-nF ceramic capacitor between HS FET's drain and LS FET's source



1 µF, 50 V, X5R, 0603

SRF = 9 MHz (Z_C = 20 mΩ)

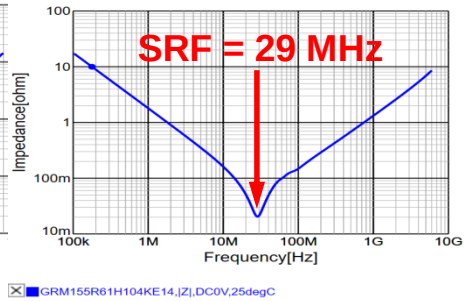
Z_C = 200 mΩ @ 100 MHz



0.1 µF, 50 V, X7R, 0603

SRF = 24 MHz (Z_C = 20 mΩ)

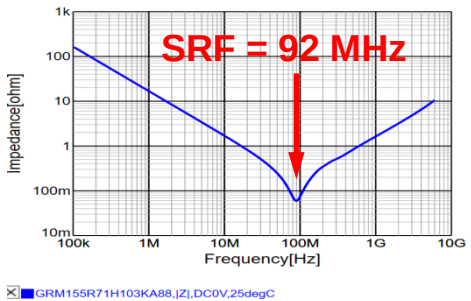
Z_C = 200 mΩ @ 100 MHz



0.1 µF, 50 V, X7R, 0402

SRF = 29 MHz (Z_C = 20 mΩ)

Z_C = 100 mΩ @ 100 MHz



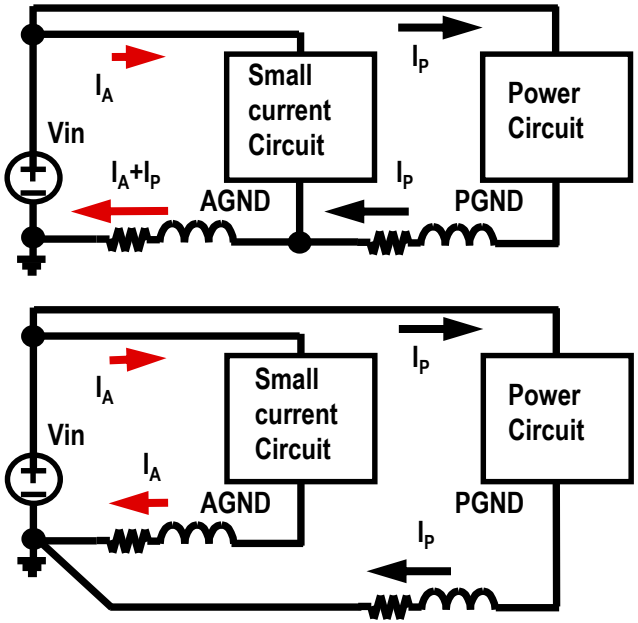
0.01 µF, 50 V, X7R, 0402

SRF = 92 MHz (Z_C = 20 mΩ)

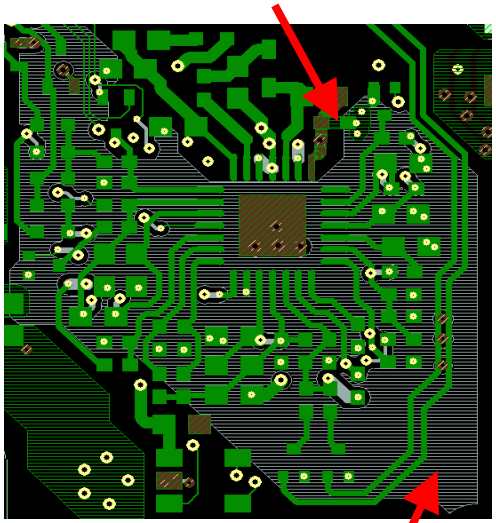
Z_C = 80 mΩ @ 100 MHz

[*] Murata Simsurfing tool, http://ds.murata.co.jp/software/simsurfing/en-us/index.html

4. Grounding – separate PGND and AGND



AGND and PGND single connection point

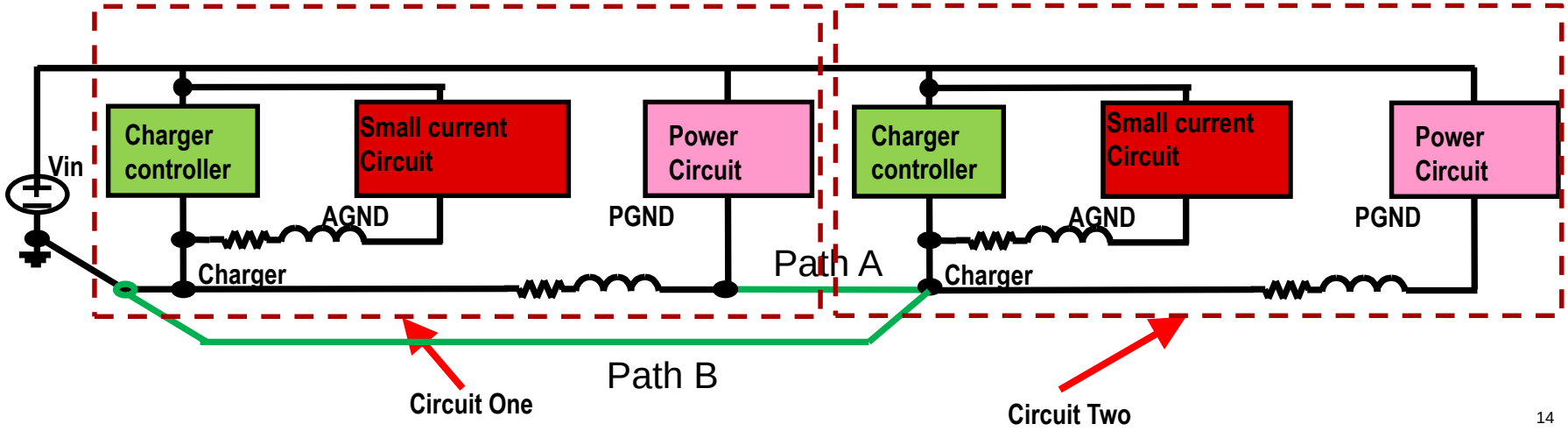


Analog ground copper pour

- Separate PGND (high current ground) and AGND (small current ground) first to avoid small signal ground coupling high current (high di/dt) ground noise
- Make PGND and AGND joint together near charger IC

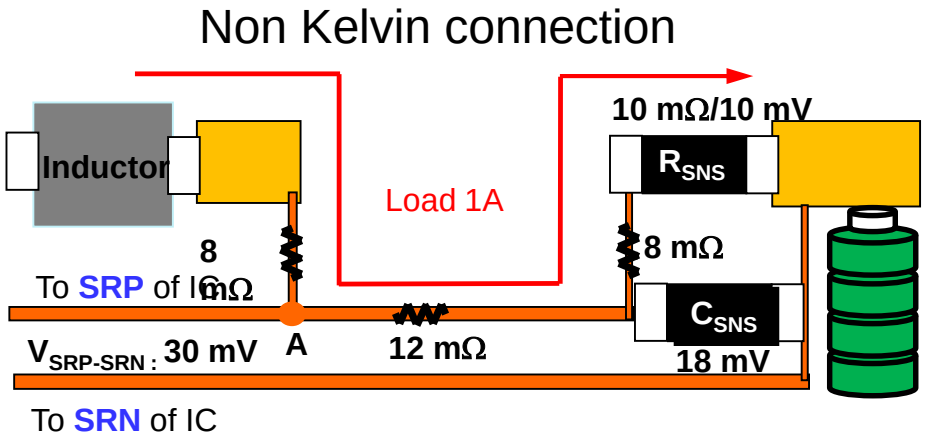
5. Grounding – PGND as common ground

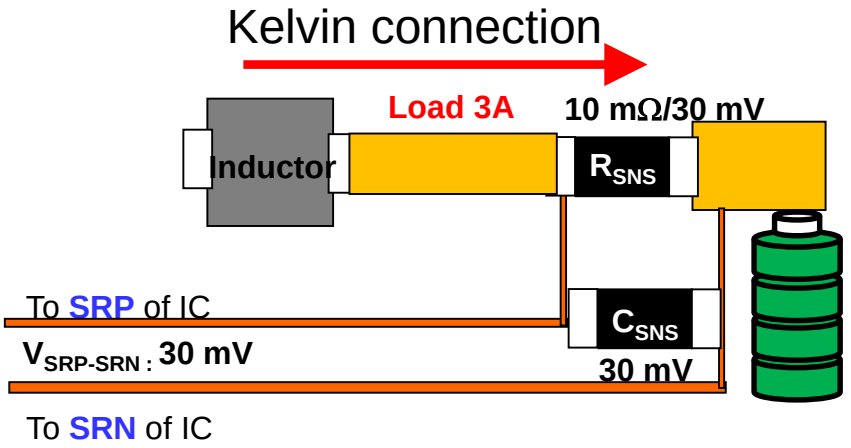
- Separate PGND and AGND first to avoid small signal ground coupling high current (high di/dt) ground noise.
- Make PGND and AGND joint together near charger IC.
- Use PGND as common ground for different sub-circuit, such as: pathA or pathB.



6. High accuracy with Kelvin sensing circuit

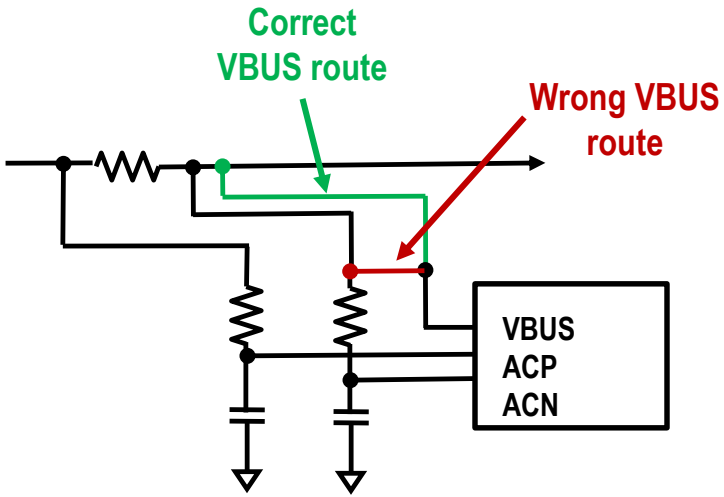
- The thin trace causes an unexpected voltage drop on the board.
- Non-Kelvin connector causes the SRP-SRN is different than V_{RSNS}.
- Kelvin connection is needed for current sensing.
- Voltage sensing trace doesn't allow high current path.

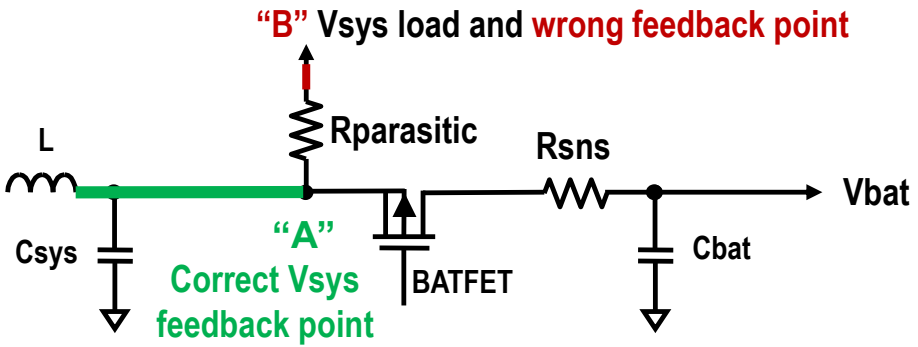




7. High accuracy with minimization of parasitic impact

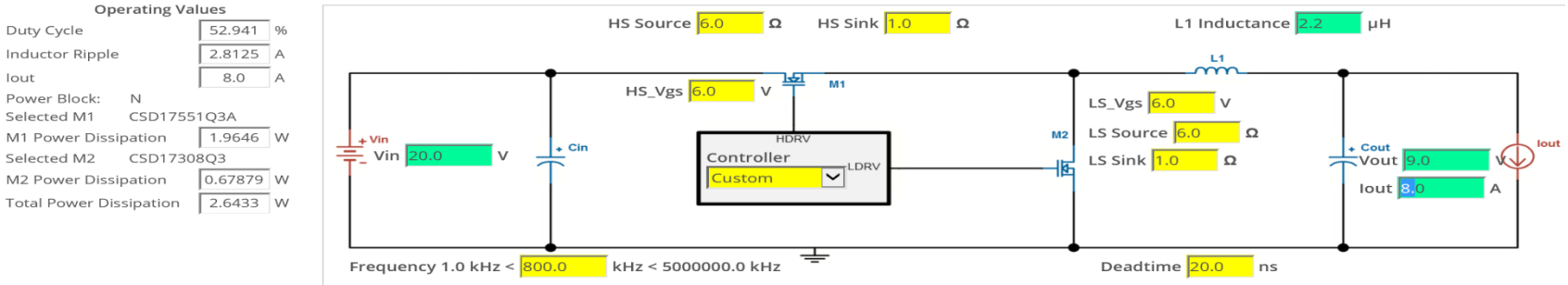
- Avoid V_{BUS} share same trace with V_{ACN} (Separate V_{ACN} trace and V_{BUS} trace)
- Avoid high parasitic resistance from the BATFET to VSYS load and feedback point (separate VSYS trace from IC VSYS pin to BATFET's source or on the green trace)





Thermal performance optimize - FETs

- Use Webench tool customize setup to estimate the power loss.
- Check the FET's thermal resistance in 3x3-mm and 5x6-mm package.
- Check the thermal performance at the worst case.
- If single FET cannot meet the thermal performance, we may have to use two FETs in parallel.



3. https://webench.ti.com/wb5/FETs_Selection/FETPBWizard.jsp

Thermal performance optimize - FETs

- TI app note-power loss calculation considering the FET parasitic inductance.[4]
- Dual FET reduces the parasitic inductance between top FET and bottom FET.

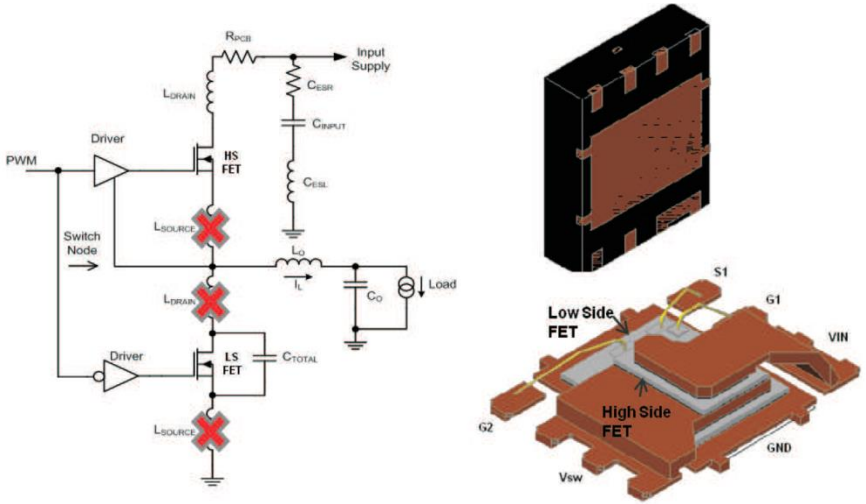


Figure 7. Schematic for Converter 2 – TI Power Block Solution

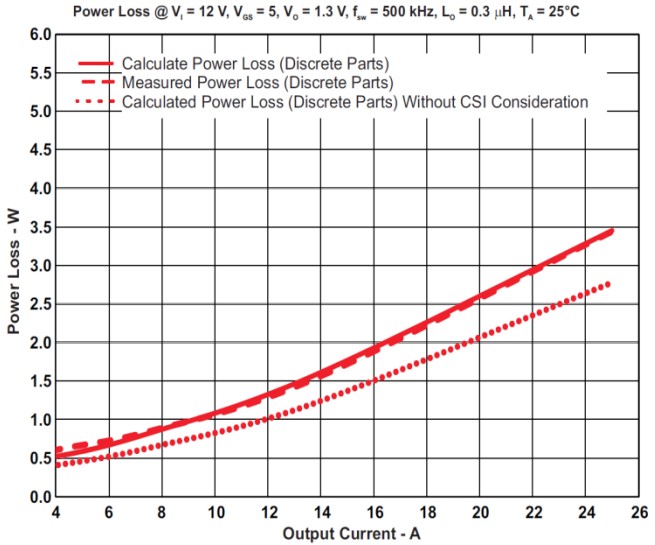


Figure 9. Power Loss Calculation Comparisons With/Without CSI Consideration

4. http://www.ti.com/lit/an/slpa009a/slpa009a.pdf

Thermal performance optimize - inductor

Use vendor calculation tool[5] to estimate the power loss and thermal performance.

Choose Calculator Type: Buck

Choose Available Series: IHLP-5050CE-01

IHLP-5050CE-01 - 2.2 Buck µH Ind. Loss Calculator

Inputs: Enter data into yellow fields

Frequency =	800000	Hz		
I_{ind} =	8	Amps		
Ambient Temp =	55	°C		
Volts In =	20	Volts		
Volts Out =	9	Volts		
V_{SW} =	0.025	Volts		
V_D =	0.025	Volts		
ET_{100} =	2.10	V-usec		
B_{pk} =	294.8	G		
A	0.520	Inch	13.2	mm
B	0.508	Inch	12.9	mm
C	0.138	Inch	3.5	mm
Reference Cost	1.5			

Outputs

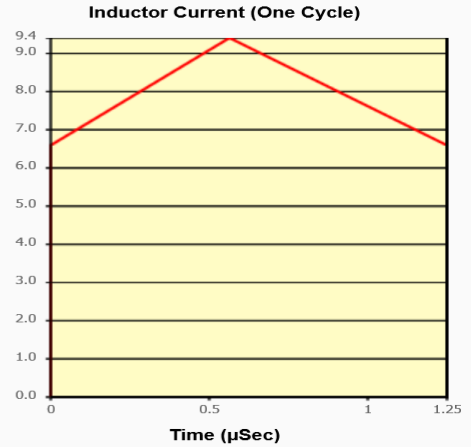
ET_{ckt}	6.19	V-usec
F(eff)	514183.8	Hertz
Res	0.009142	Ohms
I_{max}	9.41	Amps
I_{min}	6.59	Amps
I_{ripple}	2.81	Amps
Duty	0.45	
P_{core}	0.345	Watts
P_{dc}	0.585	Watts
P_{ac}	0.641	Watts
P_{tot}	1.571	Watts
Temp. Coeff.	18.8	°C/W
Temp Rise	29.5	°C
Comp Temp	84.5	°C
Compared to IHLP-2525CZ-01		

Select Inductance:

- 0.1 µH
- 0.15 µH
- 0.22 µH
- 0.33 µH
- 0.47 µH
- 0.6 µH
- 0.68 µH
- 0.82 µH
- 1 µH
- 1.5 µH
- 1.8 µH
- 2.2 µH (selected)
- 3.3 µH
- 4.7 µH
- 5.6 µH
- 6.8 µH
- 8.2 µH
- 10 µH

Ratings

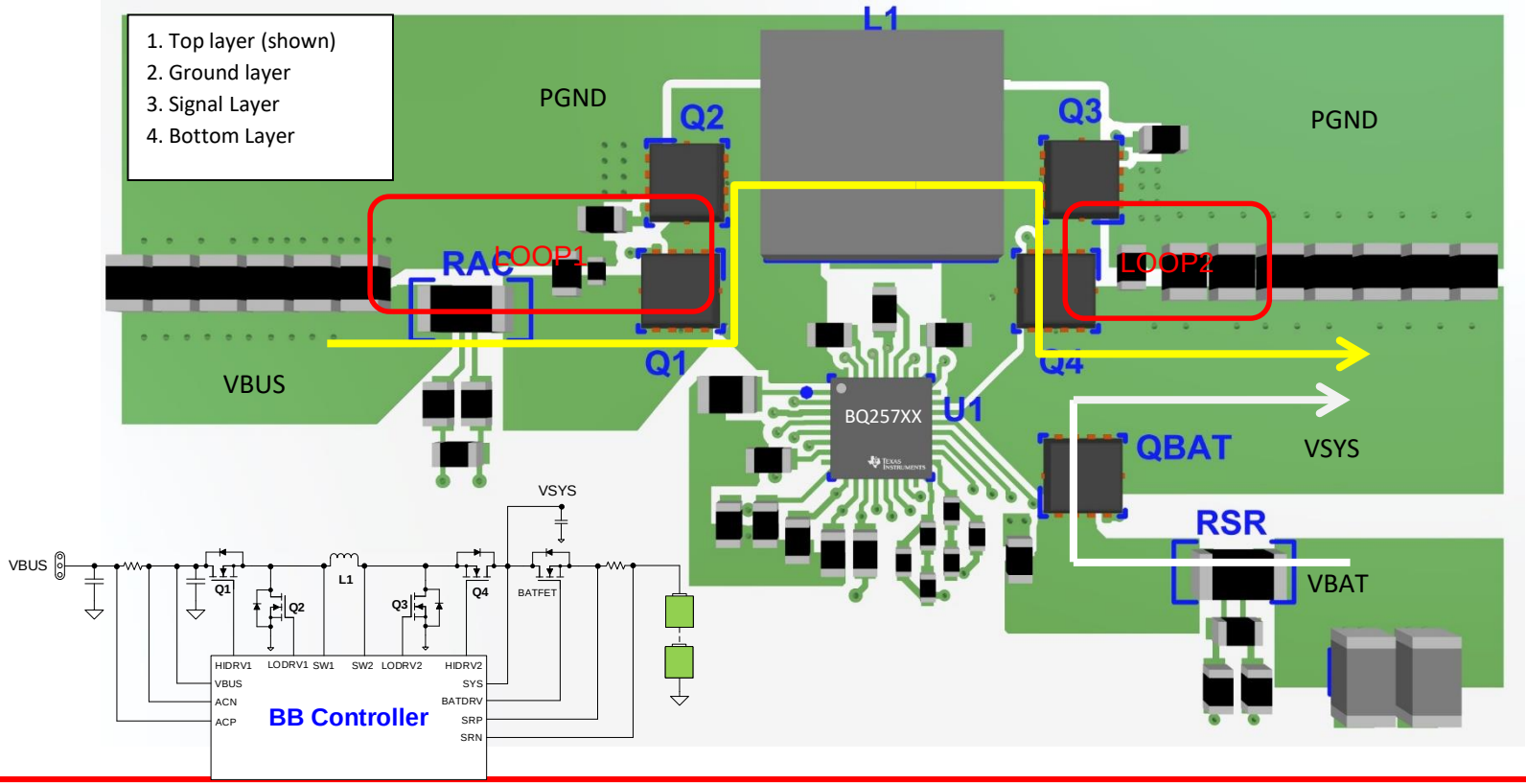
Inductance	2.2	µH
25° C DC Res	0.0072	Ohms
Isat	29	Amps
I(Heat)	16	Amps



5. https://www.vishay.com/inductors/calculator/calculator/

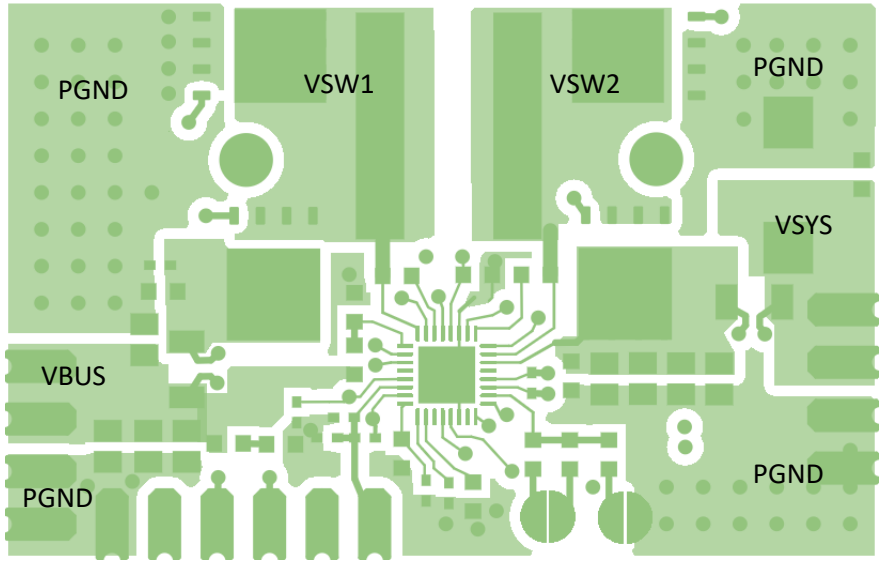
Layout examples

Example: A buck-boost charger EVM layout



Example: Inner traces and single point grounding

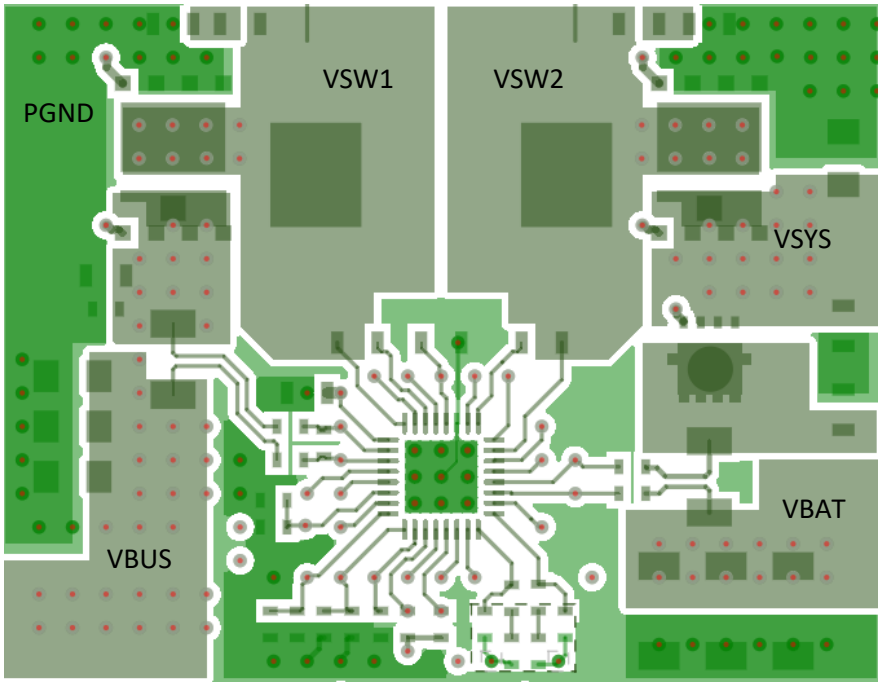
24-Vin, 240-W, 5S power tool



PMP22085

- High power 5 to 24 VIN and 240 W
- High efficiency of 98%
- Compact size of 1.08 inches x 1.68 inches (27.4 mm x 42.7 mm)
- USB on-the-go power bank
- Supports 1 to 5S battery
- Wide input range USB Type-C PD compliance

130-W high density notebook charger



- High power 5 to 24 VIN and 130 W
- Dual-FET for high density
- Compact size of 1.01 inches x 1.30 inches
- Supports 1 to 4S battery
- Wide input range USB Type-C PD compliance

Summary

- Switching charger layout key considerations
- Optimize electrical performance with minimized circuit noise
  - Minimize the noise source, reduce or shield coupling
  - AGND and PGND design considerations
  - Achieve high accuracy signal sensing
- Optimize thermal performance
  - Loss estimation with modeling
  - Component selection
  - Layout design with thermal performance

Details on the layout guideline

Priority	Components	Function	Impact	Comment
1		PCB layer stack up	Thermal, efficiency, signal integrity	Multi- layer PCB is suggested. Allocate at least one ground layer. The BQ257XXEVM uses a 4-layer PCB (top layer, ground layer, signal layer and bottom layer).
2	CBUS, RAC, Q1, Q2	input loop	High frequency noise, ripple	VBUS capacitors, RAC, Q1 and Q2 form a small loop 1. It is best to put them on the same side. Connect them with large copper to reduce the parasitic resistance. Move part of CBUS to the other side of PCB for high density design. After RAC and before Q1 and Q2 power stage, it is recommended to put two decoupling capacitors (10 nF, 1 nF, 0402 package) as close as possible to IC to decouple switching loop high frequency noise.
3	RAC, Q1, L1, Q4	current path	Efficiency	The current path from VBUS to VSYS, through RAC, Q1, L1, Q4, has low impedance. Please pay attention to via resistance if they are not on the same side. The number of vias can be estimated as 1 to 2A/via for a 10mil via with 1 oz copper thickness.
4	CSYS, Q3, Q4	output loop	High frequency noise, ripple	VSYS capacitors, Q3 and Q4 form a small loop 2. It is best to put them on the same side. Connect them with large copper to reduce the parasitic resistance. Move part of CSYS to the other side of PCB for high density design.
5	QBAT, RSR	current path	Efficiency, battery voltage detection	Place QBAT and RSR near the battery terminal. The current path from VBAT to VSYS, through RSR and QBAT, has low impedance. Please pay attention to via resistance if they are not on the same side. The device detects the battery voltage through SRN near battery terminal.
6	Q1, Q2, L1, Q3, Q4	power stage	Thermal, efficiency	Place Q1, Q2, L1, Q3 and Q4 next to each other. Please allow enough copper area for thermal dissipation. The copper area is suggested to be 2x~4x of the pad size. Multiple thermal vias can be used to connect more copper layers together and dissipate more heat.
7	RAC, RSR	current sense	Regulation accuracy	Use Kelvin-sensing technique for RAC and RSR current sense resistors. Connect the current sense traces to the center of the pads, and run current sense traces as differential pairs.
8	small caps	IC bypass caps	Noise, jittering, ripple	Place VBUS cap, VCC cap, REGN caps near IC.
9		ground partition	Measurement accuracy, regulation accuracy, jittering, ripple	Separate analog ground(AGND) and power grounds(PGND) is preferred. PGND should be used for all power stage related ground net. AGND should be used for all sensing, compensation and control network ground for example ACP/ACN/COMP1/COMP2/CMPIN/ CMPOUT/IADPT/IBAT/PSYS. Connect all analog grounds to a dedicated low-impedance copper plane, which is tied to the power ground underneath the IC exposed pad. If possible, use dedicated COMP1, COMP2 AGND traces. Connect analog ground and power ground together using power pad as the single ground connection point.

- Priority, the function in the circuit, the impact and explanations

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