Welcome!
Texas Instruments New Product Update

- This webinar will be recorded and available at www.ti.com/npu
- Phone lines are muted
- Please post questions in the chat or contact your TI sales contact or field applications engineer

LEARN ABOUT TI'S AUTOMOTIVE PMIC PORTFOLIO AND TPS65219-Q1 FOR POWERING SITARA AM62X-Q1

New Product Update

Lakshmi Sriraman
- Product Marketing Engineer

Agenda

- PMIC Overview
- TI Automotive PMIC Summary
- PMIC Recommendations for Sitara Auto MPU
- TPS65219-Q1 Overview
- TPS65219-Q1 One – pager
- TPS65219-Q1 Value proposition
- Schedule
- Power trees

Please feel free to “chat” Brenda Dias, Product Marketing Engineer, who is available to answer any questions you have throughout this presentation.

PMIC overview

■ Why TI PMIC preferred at world wide?

Strategy: Scalable and differentiated PMIC solutions for high TAM SoC platforms (TI and Non-TI attach) in automotive to grow faster than market.

Our scalable power management integrated circuits (PMICs) harness our leading edge power technology to reduce system complexity with fewer components. Built-in LDO regulators, DC/DC regulators, sequencers, load switches, supervisors, BISTs and logic help simplify your design compared to a fully discrete solution. Using a PMIC can reduce component count and system size without sacrificing efficiency or thermal performance.

Problems we are solving

- **Scalable & Optimized** power solution across high & low power variants
- **Reduced BOM** through integration of monitoring and sequencing features, minimize external components.
- **Reduced "hidden cost"** of Safety critical applications with functional safety-compliant devices (HW & SW support + safety documentation).
- **Reduction in board space** due to integration
- **Plug and play** solutions with validated reference designs for SoCs

TI automotive PMIC summary

Scalable and fast time to market PMIC solutions for SoC platforms (SoC, FPGAs, MCU, MPU, and modules) with Hardware/ Software support

Automotive-qualified functional and non functional safety, targeting a broad range of applications

Highly integrated solutions, that are optimized for board space and cost

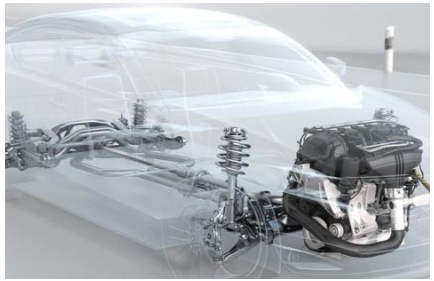
Advanced driver assistance systems (ADAS)

TPS65033x-Q1, LP8774-Q1, LP876x-Q1, TPS6594x-Q1, LP8772-Q1

Infotainment & Cluster

TPS65224-Q1, TPS65219-Q1, TPS6593-Q1 TPS659038, TPS65917, LP8756/2

Hybrid, electric & powertrain systems

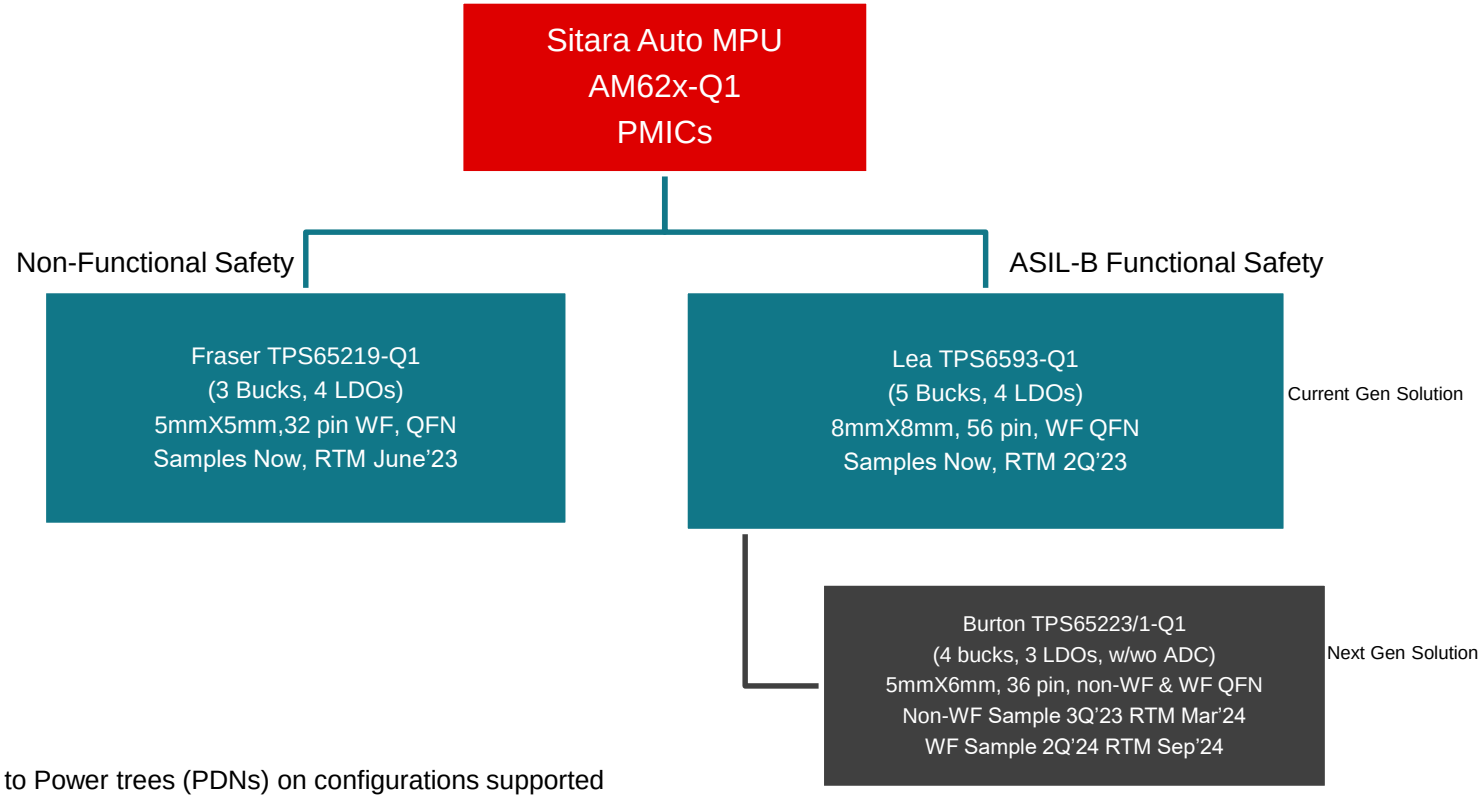


TPS65381x-Q1,TPS65385x-Q1, TPS653851x-Q1, TPS65386x-Q1, TPS65387x-Q1

Body electronics & lighting

TPS6594x-Q1, TPS65320-Q1

Sitara auto MPU | PMIC recommendations



*Please refer to Power trees (PDNs) on configurations supported

Fraser (TPS65219-Q1)

Target end equipment's

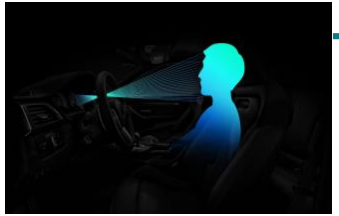

Cockpit Domain Controller


TCU


eMirror (CMS)


Rear Seat Entertainment


Display Modules


Driver Monitoring System
(NCAP DMS, OMS/IMS)

Target loads

TI SoCs

Non-Functional Safety Applications of
- AM62x-Q1
- AM62A-Q1

Non-TI SoCs

- Xilinx FPGAs Spartan-7, Artix-7
- Xilinx SoCs Zynq-7000 and Zynq Ultrascale+

General purpose loads

- FPDLink SERDES
- Ethernet Switches
- Ethernet PHYs
- PCIe Switches

TPS65219-Q1: 3x step-down DC-DC, 4x LDO, configurable PMIC

Features

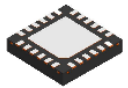
- 3 buck converters at 2.3 MHz fixed switching frequency
  - 1x VIN: 2.5 V – 5.5 V, Iout: 3.5 A; Vout 0.6 V – 3.4 V
  - 2x VIN: 2.5 V – 5.5 V, Iout: 2 A; Vout 0.6 V – 3.4 V
- 2 LDOs (configurable as load switch/bypass-mode, supporting SD-card)
  - 2x VIN: 1.5 V – 5.5 V, Iout: 400 mA; Vout: 0.6 V – 3.4 V
- 2 LDOs (configurable as load switch)
  - 2x VIN: 2.2 V – 5.5 V, Iout: 300 mA; Vout: 1.2 V – 3.3 V
- Dynamic voltage scaling on Buck1 and Buck2
- LowIQ/PFM / PWM-mode (fixed or quasi-fixed frequency)
- Programmable power sequencing and default voltages
- I2C interface
- Optimized for systems requiring 7-14 rails (1 or 2x TPS65219-Q1)
- 6 configurable GPIOs / multi-function pins (MFPs)
- EEPROM programmability
- 5 x 5 mm^2 QFN, 0.5mm pitch, 32 pin-wettable flank
- AEC-Q100-qualified, Functional Safety Capable**

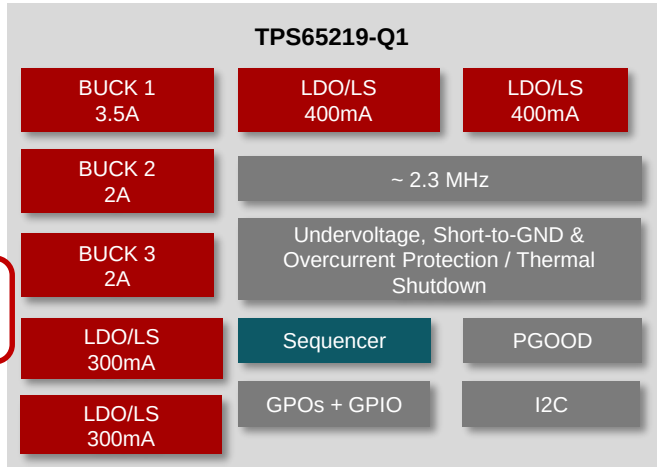
Applications

- Low power automotive MPUs e.g.: AM62x-Q1,AM62A-Q1
- Digital Cluster, Telematic Control Units, Lidar Proc.
- DMS/OMS, eMirror & CMS
- ISP & Deep Learning

Benefits

- Integrated step-down converters and 2.3 MHz switching frequency reduces external component and total solution size
- Fully programmable sequencing and output voltages
- Flexible to power many subsystems, processors and peripherals
- High efficiency over wide I_{OUT} range
- Monitoring of output voltage/current mitigates failures





**FIT rate, FMD, pin FMA documentation provided

Fraser TPS65219-Q1 value proposition

Small Solution Size and Cost

- TPS65219-Q1 with 3 Bucks and 4 LDOs
  - Optimized rail count and feature set to power **Automotive MPUs** for Non-Functional Safety Applications
  - Flexible PMIC with programmable sequencing and output voltages for wide variety of non-TI SoCs, ASICs and **FPGAs**
  - **5mmX5mm, 0.5mm pitch Wettable Flank (WF)** package for automotive applications

Automotive Grade

- **AEC Q100 Grade 1** Automotive Qualification
  - Operating Temperature Range **-40C to 125C Ta** (Tj upto 150C)
  - Wettable Flanks to help with AOI (automatic optical inspection) during automotive assembly
  - TI Functional Safety Capable device (FIT rate, FMD and pin FMA documentation provided)

Design Support

- TI recommended PMIC to supply for Non-Functional Safety Applications
  - **Power Trees available** showing processor and PMIC power and interfacing
  - **Hardware Reference design boards** available for certain MPUs + PMICs
  - Software **PMIC drivers** available to work with certain MPUs

Fraser TPS65219-Q1 schedule

Milestone	Date
Engineering Samples	Samples Available Now*
Preliminary Short Datasheet	Available now
Preview Release on ti.com (APL) OPN: PTPS6521920WRHBRQ1	Jan, 2023
Release to Market (RTM) OPN: TPS6521920WRHBRQ1	June, 2023
PPAP OPN: TPS6521920WRHBRQ1	July, 2023

*Sample generation time is 6 weeks (from placing a ZS order) for existing OTPs. Can be up to 10 to 12 weeks for new OTPs – because of additional time to define and validate the new NVM configuration.

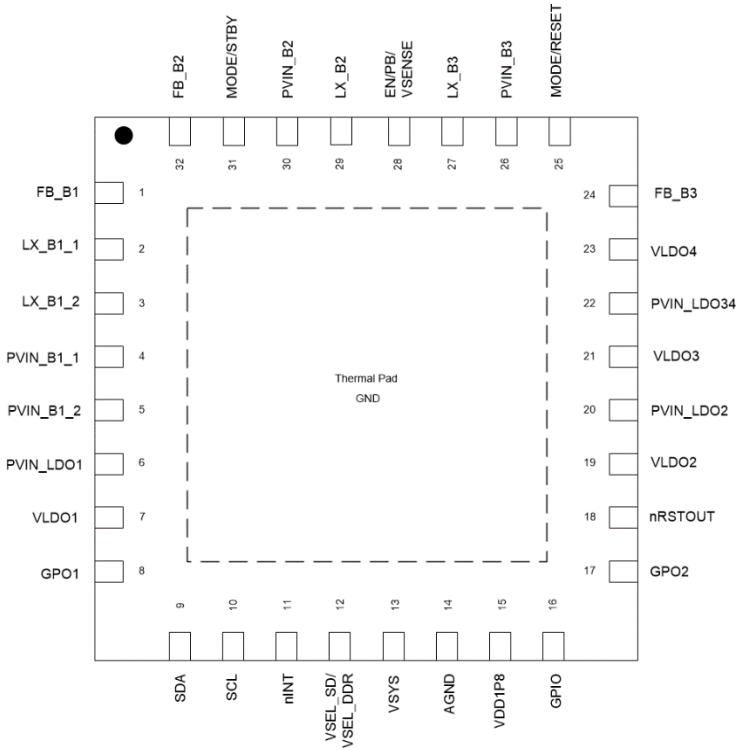
TPS65219-Q1 multi-function pins (MFP)

- **EN/PB/VSENSE (On-request inputs):**
  - Configured as EN:
    - Device enable pin, high level is ON-request, low-level is OFF-request.
  - Configured as PB:
    - Push-button monitor input. 600 ms high-level is an ON-request, 8 s high level is an OFF-request.
  - Configured as VSENSE:
    - Power-fail comparator input. Set sense voltage using a resistor divider connected from the input to the pre-regulator to this pin to ground. Detects rising/falling voltage on pre-regulator and triggers ON- / OFF-request.
- **GPO1, GPO2, GPIO:**
  GPO:
  – General Purpose Open-Drain Output. Configurable in the power-up and power-down-sequence to enable an external rail.

  GPIO configured as GPIO:
  – Synchronizing I/O. Used to synchronize two or more TPS65219.
- **MODE/RESET:**
  – Configured as MODE:
    - Connected to SoC or hard-wired pull-up/-down. Forces the Buck-converters into PWM or permits auto-entry in PFM-mode
  – Configured as RESET:
    - Connected to SoC. Forces a cold reset, sequencing down all enabled rails and power up again. Polarity is configurable.
- **MODE/STBY:**
  – Configured as MODE:
    - Connected to SoC or hard-wired pull-up/-down. Forces the Buck-converters into PWM or permits auto-entry in PFM-mode
  – Configured as STBY:
    - Low-power-mode command, disables selected rails. Both functions, MODE and STBY, can be combined
- **VSEL_SD/VSEL_DDR:**
  – Configured as VSEL_SD:
    - SD-card-IO-voltage select. Connected to SoC. Trigger a voltage change between 1.8 V and 3.3 V on LDO1 or LDO2. Polarity is configurable.
  – Configured as VSEL_DDR:
    - DDR-voltage selection. Hard-wired pull-up, pull-down or floating. Sets output voltage of Buck3 to 1.35 V / 1.2 V / 1.1 V.

TPS65219-Q1 pinout (tentative)

- **32-pins 0.5 mm pitch QFN (5 mm x 5 mm)**



AM62-Q1 Typical power tree using TPS65219-Q1 for Non-Functional Safety Applications

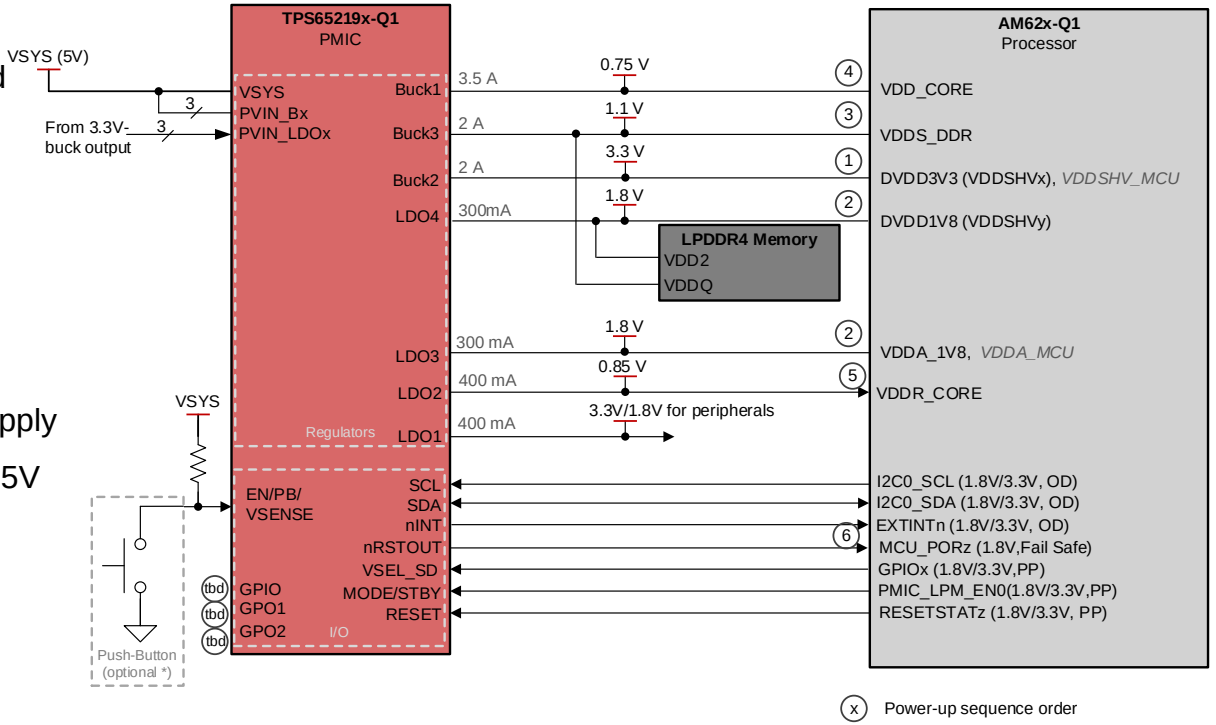
Texas Instruments

Disclaimer

- Note that this is only a very high level BOM. Use it only as a very generic guideline for the power tree.
- Power consumption on the different rails is subject to change as we get closer to the first silicon release
- This also applies on passives that are subject to adjustments as we get closer to the first silicon release
- Note also that some little passives are missing in the table, however these are much less relevant from price standpoint than the main passives

Fraser TPS65219-Q1 | TI optimized PMIC for AM62x-Q1 in Non-Functional Safety Applications

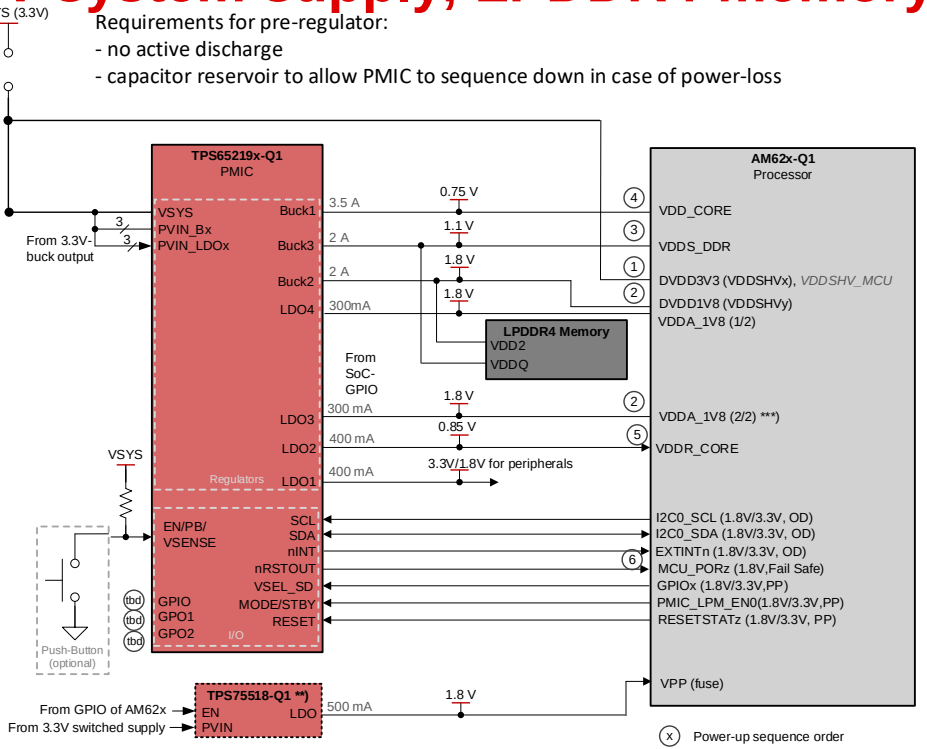
- Targeting **cost-optimized** designs
- Fully **programmable sequencing** and output voltages
- **Voltage monitoring** on all rails
- Up to **3.5A** for Core rails, supporting AM62x-Q1
- GPOs for external rails
- 4 LDOs to supply V_{DDR_CORE}, V_{DDA_1P8}, V_{DVDD_1P8} and dynamic SD-card-IO-supply
- Minimum output voltage support of 0.75V for V_{DD_CORE}
- High efficiency DC/DCs
- Small size (5x5 QFN, 0.5mm pitch)



Version 1.0

*) EN or PB require EEPROM options

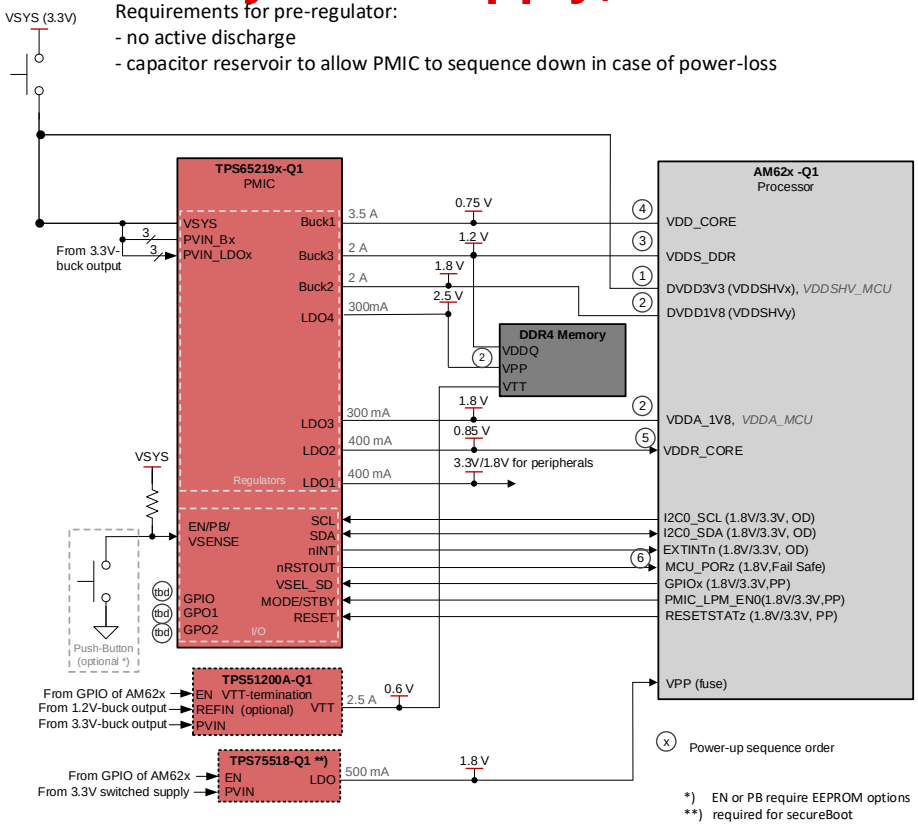
TI AM62x-Q1 - TPS65219-Q1 power solution block diagram 3.3V system supply, LPDDR4-memory



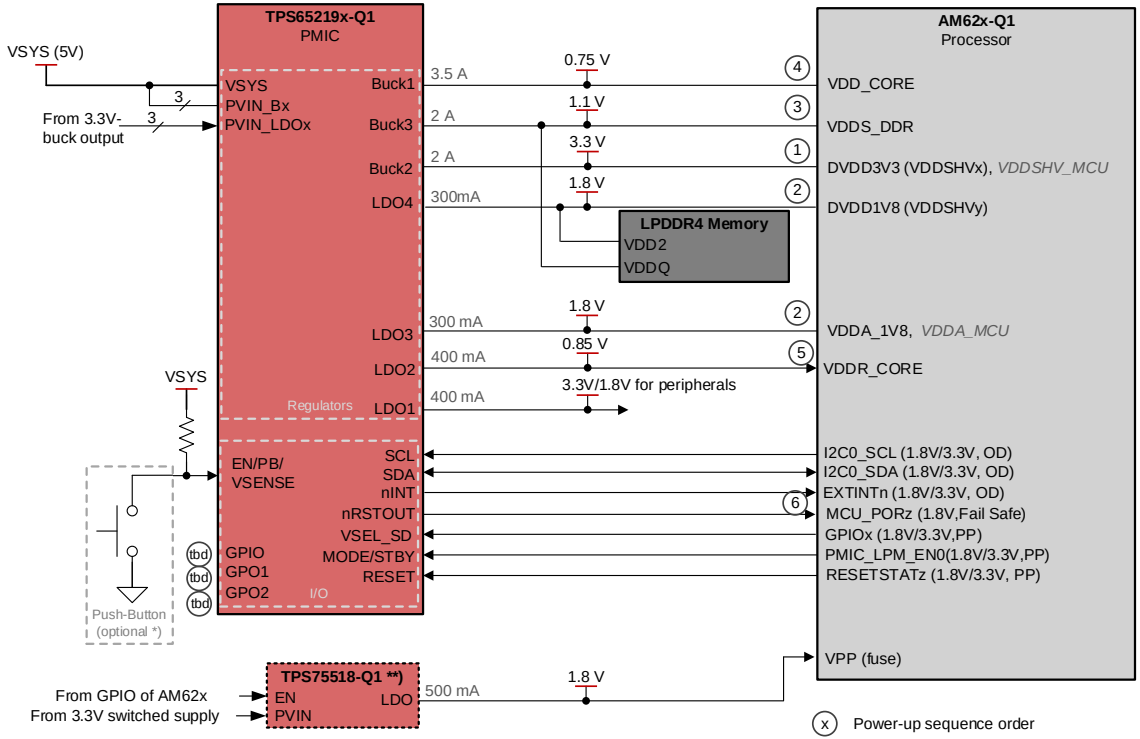
*) EN or PB require EEPROM options
**) required for secureBoot
***) alternatively, LDO3 can be used for peripherals

Version 1.0

TI AM62x-Q1 - TPS65219-Q1 power solution block diagram 3.3V system supply, DDR4-memory



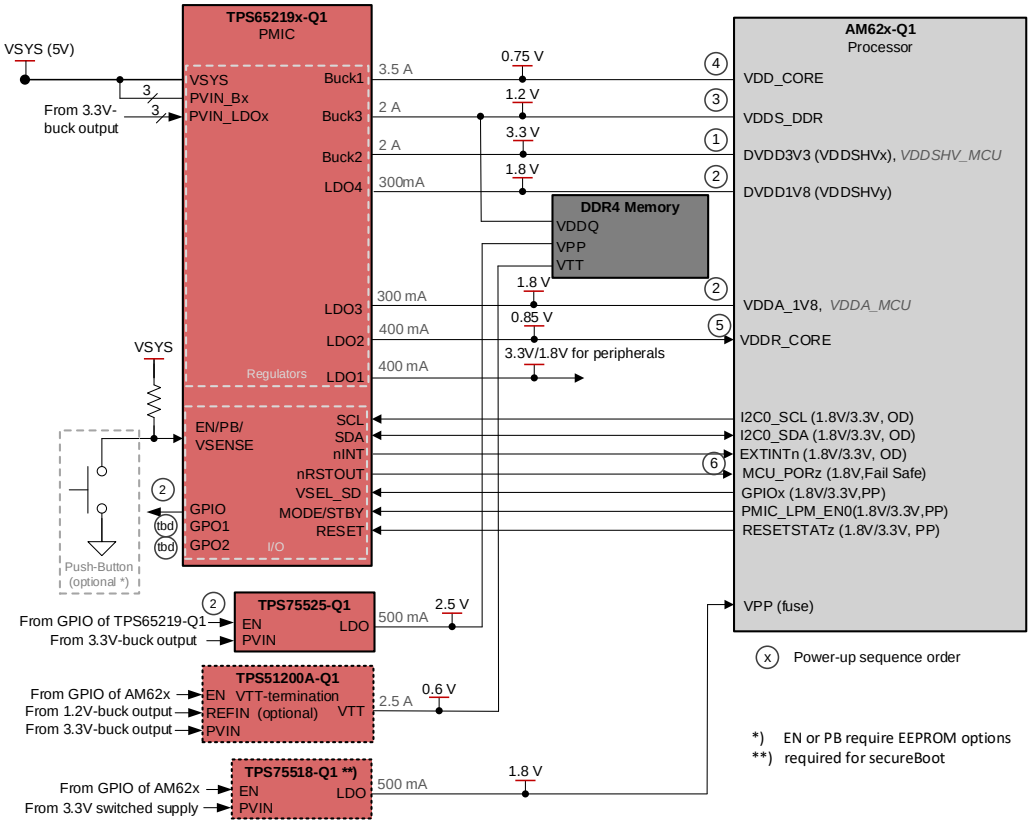
TI AM62x-Q1 - TPS65219-Q1 power solution block diagram 5V system supply, LPDDR4-memory



*) EN or PB require EEPROM options
**) required for secureBoot

Version 1.0

TI AM62x-Q1 - TPS65219-Q1 power solution block diagram
5V system supply, DDR4-memory



AM62x-Q1PowerSolution Size Estimation

Component type Automotive	QTY	Value	Orderable	Description	Size/unit [mm²]	Size (total) [mm²]
TPS65219-Q1 (5x5mm²)	1	N/A	tbd	PMIC	25	25
L1	1	470nH	NRS5020TR47NMGJV	0.47uH, +/-30%, Is~6.1A, 14.4mOhm, NonStandard, -40°C to 125°C, Ferrite, Shielded	24	24
L2/L3	2	470nH	NRS5020TR47NMGJV	0.47uH, +/-30%, Is~6.1A, 14.4mOhm, NonStandard, -40°C to 125°C, Ferrite, Shielded	24	48
Cin_DC/DC1..3	3	4.7uF	LMK212B7475KGHT	4.7uF, +/-10%, X7R, 10V, 0805, -55°C to +125°C, AEC-Q200, Multilayer Ceramic Cap	5	15
Cout _ DC/DC1..3	2	10uF *)	JMK212AB7106KGHT	10uF, +/-10%, X7R, 6.3V, 0805, -55°C to +125°C, AEC-Q200, Multilayer Ceramic Cap	5	10
Cout _ DC/DC1..3	2	33uF *)	CGA6P1X7S0J336M250AC	33µF, +/-20%, X7S, 6.3V, 1210, -55°C to 125°C, AEC-Q200, Ceramic Capacitor	8	16
LDO_Cin1..2	2	2.2uF	LMK212B7225KGHT	2.2uF, +/-10%, X7R, 10V, 0805, -55°C to +125°C, AEC-Q200, Multilayer Ceramic Cap	5	10
LDO_Cin34	1	4.7uF	LMK212B7475KGHT	4.7uF, +/-10%, X7R, 10V, 0805, -55°C to +125°C, AEC-Q200, Multilayer Ceramic Cap	5	5
LDO_Cout	4	2.2uF	LMK212B7225KGHT	2.2uF, +/-10%, X7R, 10V, 0805, -55°C to +125°C, AEC-Q200, Multilayer Ceramic Cap	5	20
Various resitors	5	N/A		0402	0.5	2.5
						148

*) 60uF min required to meet AM62-Q1-CORE-rail transient requirements in fixed frequency

Size includes PMIC and its main passives,
but no external ICs, their passives nor keepout/routing

AM62A-Q1
Typical power tree using TPS65219-Q1 for Non-Functional Safety Applications

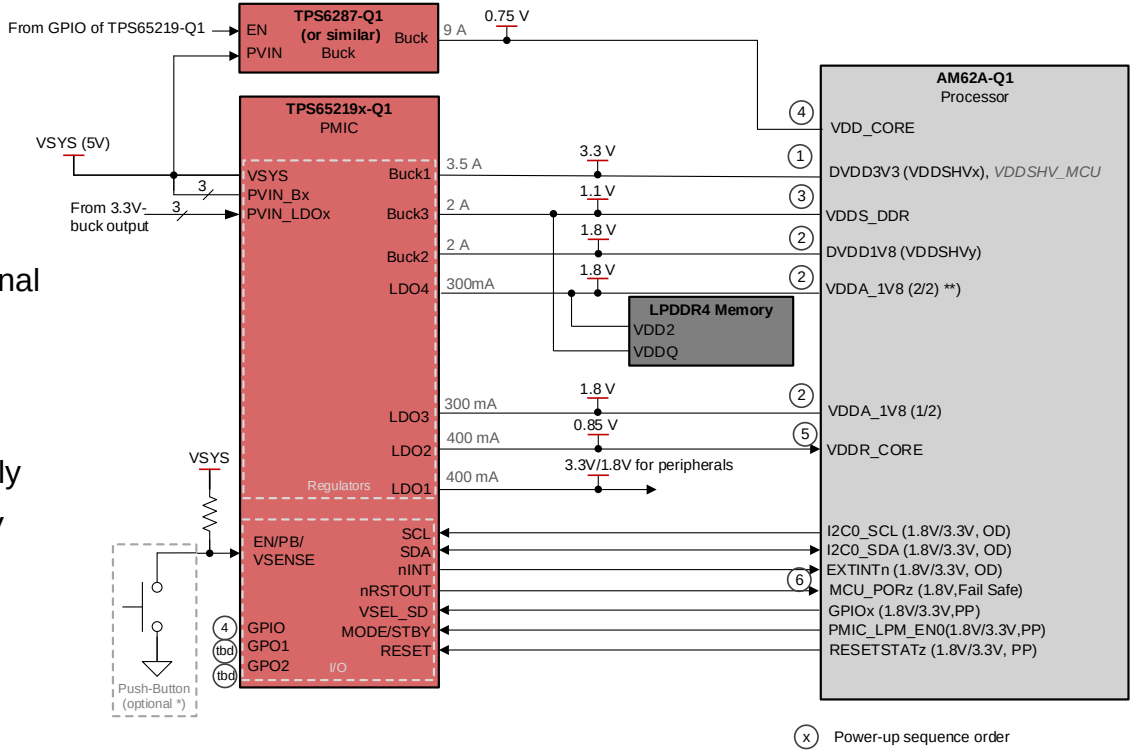
Texas Instruments

Disclaimer

- Note that this is only a very high level BOM. Use it only as a very generic guideline for the power tree.
- Power consumption on the different rails is subject to change as we get closer to the first silicon release
- This also applies on passives that are subject to adjustments as we get closer to the first silicon release
- Note also that some little passives are missing in the table, however these are much less relevant from price standpoint than the main passives

Fraser TPS65219-Q1 | TI optimized PMIC for AM62A-Q1

- Targeting **cost-optimized** designs
- Fully **programmable sequencing** and output voltages
- **Voltage monitoring** on all rails
- Up to **3.5A** for Core rails, supporting AM62x-Q1, AM62A-Q1 requires an external core supply
- GPOs for external rails
- 4 LDOs to supply V_{DDR_CORE}, V_{DDA_1P8}, V_{DVDD_1P8} and dynamic SD-card-IO-supply
- Minimum output voltage support of 0.75V for V_{DD_CORE}
- High efficiency DC/DCs
- Small size (5x5 QFN, 0.5mm pitch)



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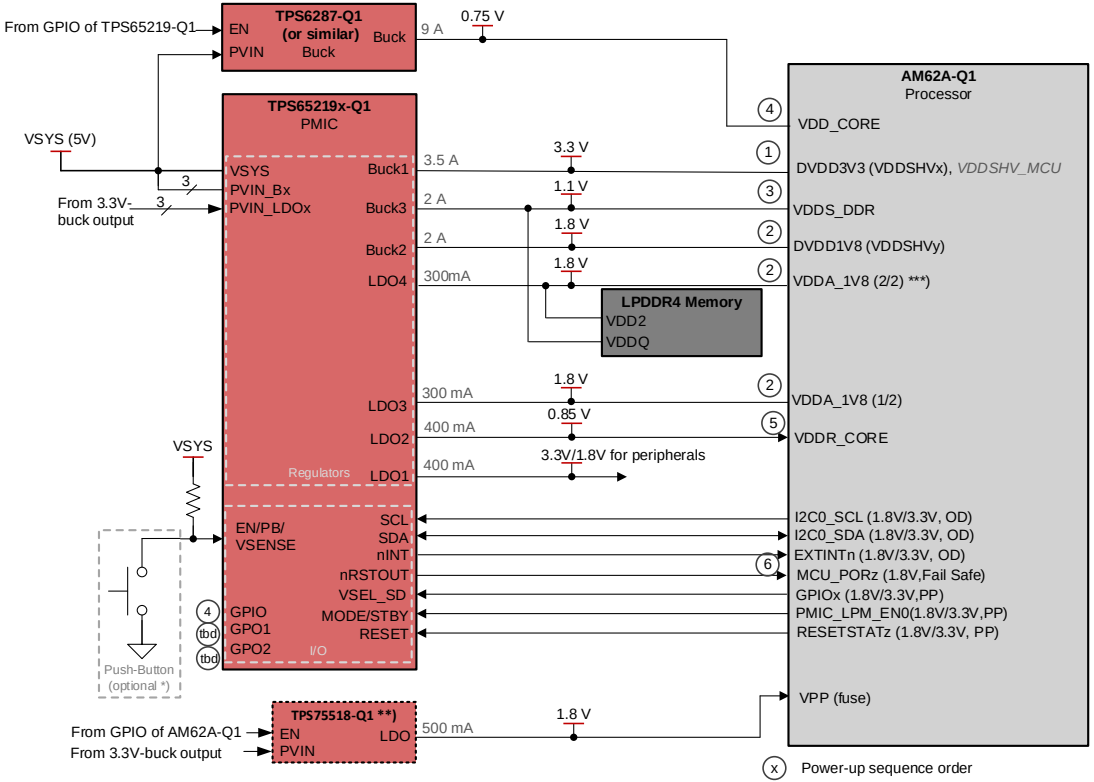
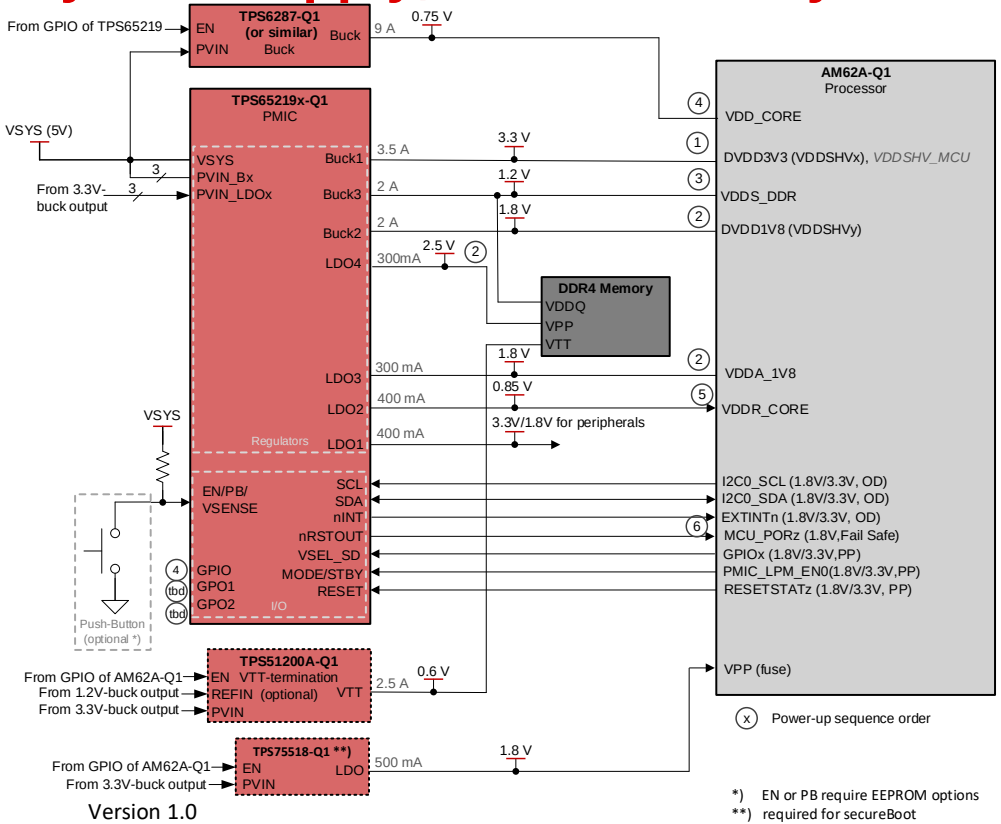
TI AM62A-Q1 - TPS65219-Q1 power solution block diagram
5V system supply, LPDDR4-memory



Version 1.0

*) EN or PB require EEPROM options
**) required for secureBoot
***) alternatively, LDO4 can be used for peripherals

TI AM62A-Q1 - TPS65219-Q1 power solution block diagram
5V system supply, DDR4-memory



Version 1.0

AM62A-Q1- PowerSolution Size Estimation (PMIC only)

Component type Automotive	QTY	Value	Orderable	Description	Size/unit [mm²]	Size (total) [mm²]
TPS65219-Q1 (5x5mm²)	1	N/A	tbd	PMIC	25	25
L1	1	470nH	NRS5020TR47NMGJV	0.47uH, +/-30%, Is~6.1A, 14.4mOhm, NonStandard, -40°C to 125°C, Ferrite, Shielded	24	24
L2/L3	2	470nH	NRS5020TR47NMGJV	0.47uH, +/-30%, Is~6.1A, 14.4mOhm, NonStandard, -40°C to 125°C, Ferrite, Shielded	24	48
Cin_DC/DC1..3	3	4.7uF	LMK212B7475KGHT	4.7uF, +/-10%, X7R, 10V, 0805, -55°C to +125°C, AEC-Q200, Multilayer Ceramic Cap	5	15
Cout _ DC/DC1..3	2	10uF *)	JMK212AB7106KGHT	10uF, +/-10%, X7R, 6.3V, 0805, -55°C to +125°C, AEC-Q200, Multilayer Ceramic Cap	5	10
Cout _ DC/DC1..3	2	33uF *)	CGA6P1X7S0J336M250AC	33µF, +/-20%, X7S, 6.3V, 1210, -55°C to 125°C, AEC-Q200, Ceramic Capacitor	8	16
LDO_Cin1..2	2	2.2uF	LMK212B7225KGHT	2.2uF, +/-10%, X7R, 10V, 0805, -55°C to +125°C, AEC-Q200, Multilayer Ceramic Cap	5	10
LDO_Cin34	1	4.7uF	LMK212B7475KGHT	4.7uF, +/-10%, X7R, 10V, 0805, -55°C to +125°C, AEC-Q200, Multilayer Ceramic Cap	5	5
LDO_Cout	4	2.2uF	LMK212B7225KGHT	2.2uF, +/-10%, X7R, 10V, 0805, -55°C to +125°C, AEC-Q200, Multilayer Ceramic Cap	5	20
Various resitors	5	N/A		0402	0.5	2.5
						148

*) 60uF min required to meet AM62-Q1-CORE-rail transient requirements in fixed frequency

Size includes PMIC and its main passives,
but no external ICs, their passives nor keepout/routing

Getting started

You can start evaluating this device leveraging the following:

Content type	Content title	Link to content or more details
Product folder	Product Folder	https://www.ti.com/product/TPS65219-Q1
PMIC portfolio	Multi channel IC's (PMICs) selection guide	https://www.ti.com/power-management/multi-channel-ics-pmic/overview.html
Development tool or evaluation kit	TPS65219EVM	https://www.ti.com/tool/TPS65219EVM

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For more information on the New Product Update series, calendar and archived recordings

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