Texas Instruments

Webinar

Rad-hard low-noise linear regulator for high-performance satellite sensing and communications systems

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Agenda

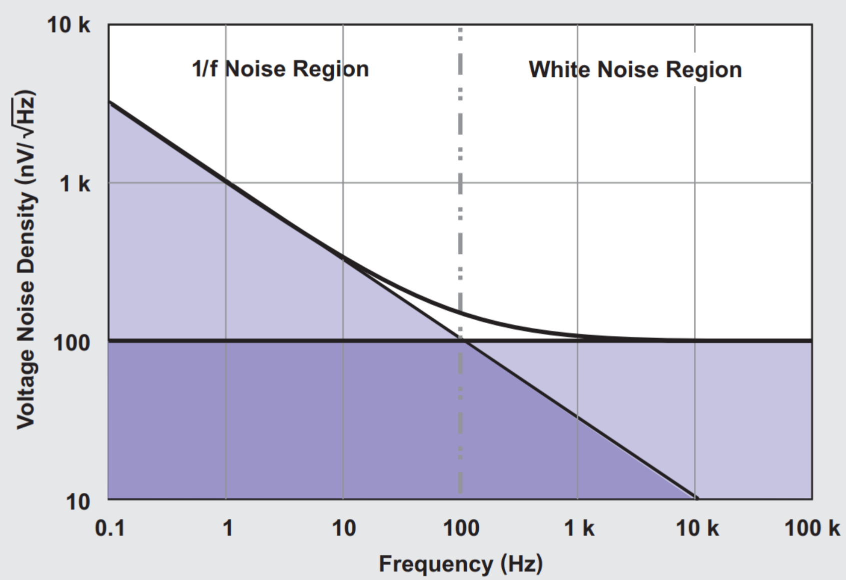
- Subsystems with low-noise power supply requirements
- Noise and PSRR basics
- Measuring noise & PSRR in low-noise power supplies
- TPS7H1111 introduction
- TPS7H1111 noise & PSRR
- TPS7H1111 final results

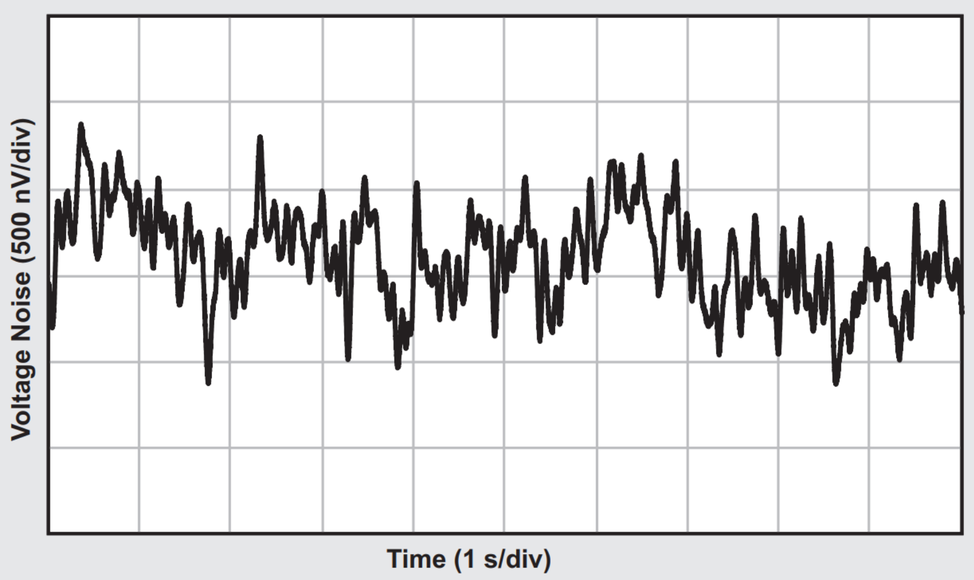
Subsystems with Low-Noise requirements

- As satellites process more data, signal processing requirements continue increasing
- Without careful power supply design, the power can become a limiting factor for:
  - Analog to digital converters (ADCs)
  - Digital to analog converters (DACs)
  - Imaging sensors
  - Clocking circuits
- A high-performance ADC is a key IC that may benefit from an ultra-low noise LDO
  - Noise can couple to an ADC both directly and through its clock mixing path
  - This coupling can reduce the SFDR (spurious free dynamic range) of the ADC

Noise & PSRR basics | Noise

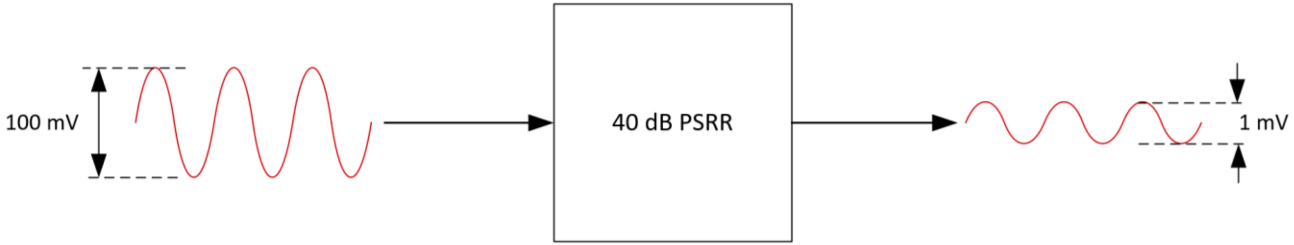
- All electrical devices create inherent noise
  - The most problematic noise to filter out is generally low frequency output noise (also referred to as 1/f noise or flicker noise)
  - Discrete filters would require large component values and consume valuable board space





Noise & PSRR basics | PSRR

- Linear regulators are often powered by switching regulators which inherently generate ripple voltage at the switching frequency and harmonics of higher frequency.
  - This input noise is attenuated by the Power Supply Rejection Ratio (PSRR) of the linear regulator before being passed to the linear regulator output.
  - $PSRR = 20 \times \log_{10} \frac{V_{IN}}{V_{OUT}}$



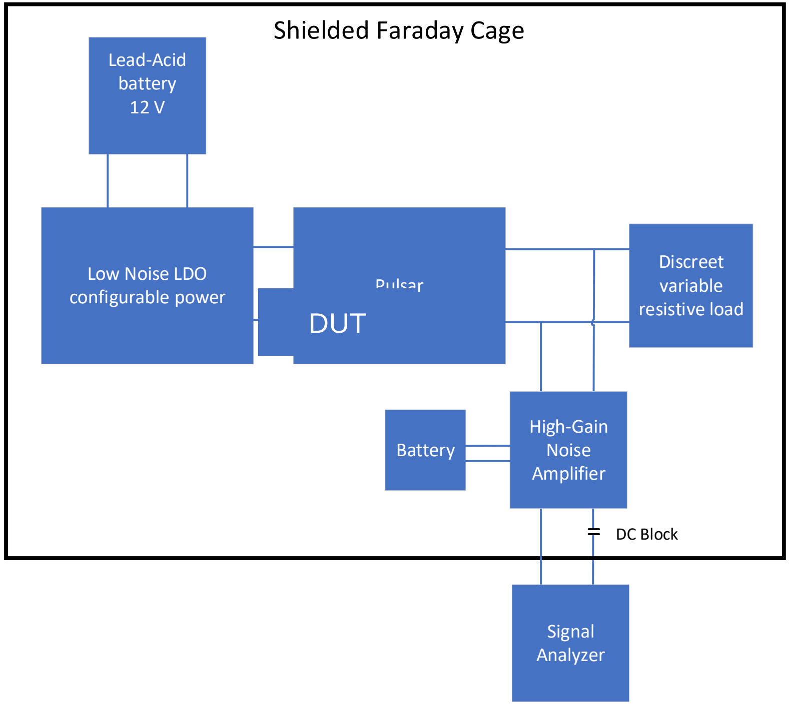
Example of 100 mV being attenuated by 40 dB

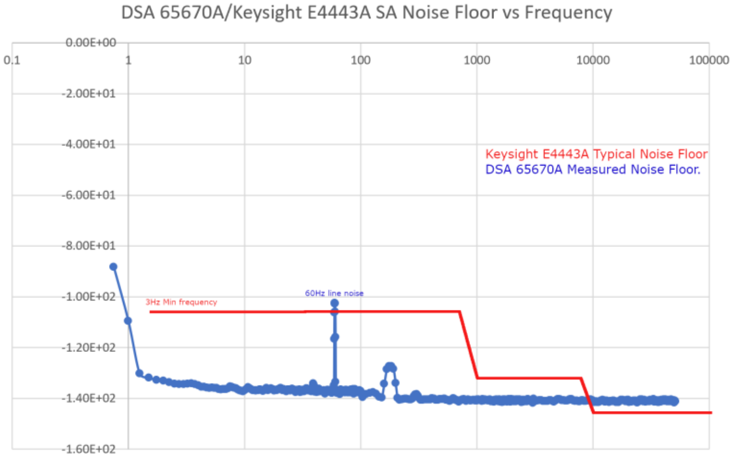
Measuring noise & PSRR | Noise

- Noise spectral density is obtained by sampling the random noise for a period of time
- External sources of noise must be removed which requires:
  - EMI shielding (Faraday cage)
  - Careful layout to minimize antennas or ground loops
  - Removing as much noise as possible from the input power supply
- Additional considerations:
  - Very large output AC signal capacitor to facilitate low frequency testing
  - Low noise, high gain pre-amplifier to gain up noise to a level that the signal analyzer can measure

Measuring noise & PSRR | Noise

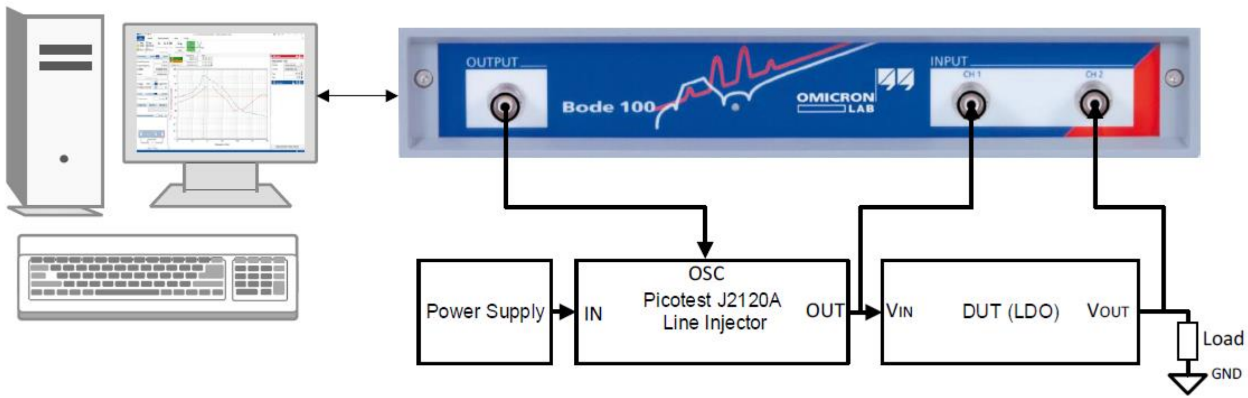
- Setup shown to right
- Signal analyzer options considered
  - HP DSA 35670A
  - Keysight E4443A





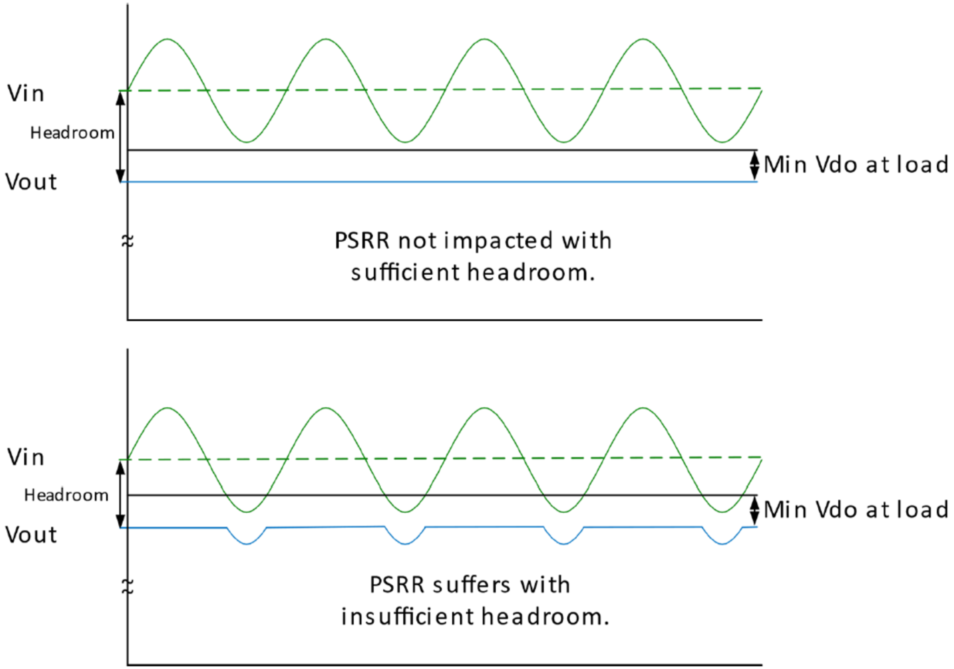
Measuring noise & PSRR | PSRR

- A voltage ripple is injected on VIN and the attenuated VOUT ripple is then measured
  - To properly drive VIN, the LDO’s input capacitance is removed
- An Omicron Bode 100 and Picotest J2120A can be utilized



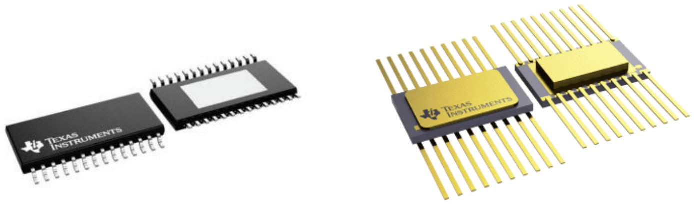
Measuring noise & PSRR | PSRR

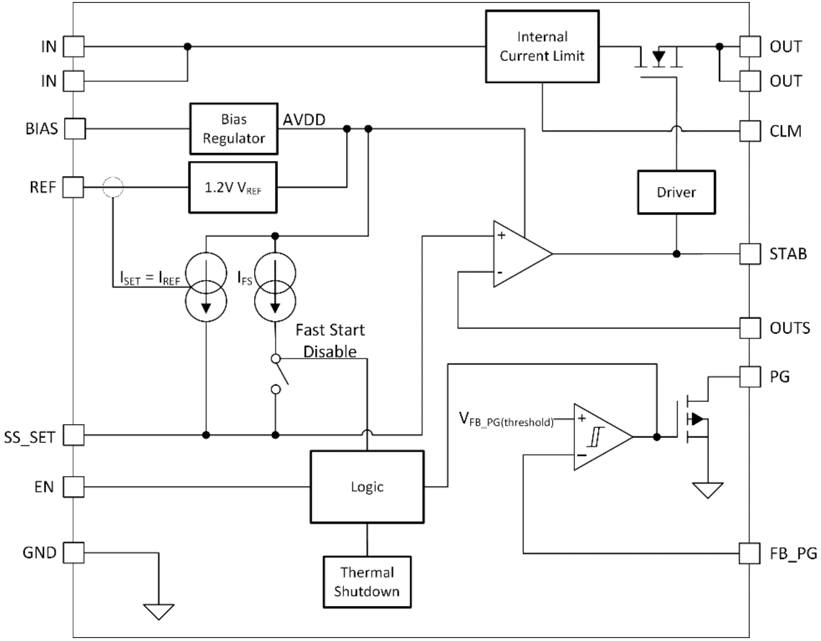
- Sufficient headroom is required for the test
- The injected signal needs to be large enough to be measured at the output but small enough to be considered small signal from the LDOs perspective



TPS7H1111 | Overview

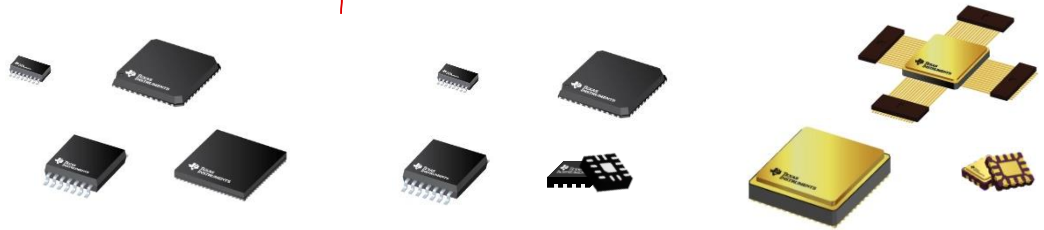
- Linear regulator with architecture optimized for low noise and high PSRR
- TID up to 100 krad(Si) and SEL/SEB/SEGR immune to 75 MeV-cm²/mg
- Electrical
  - Input voltage, V_{IN}: 0.85V to 7V
  - Bias supply, V_{BIAS}: 2.2V to 14V
  - Output voltage, V_{OUT}: 0.4V to 5.5V
  - Output current, I_{OUT}: 1.5A
  - Dropout voltage, V_{DO}: 450 mV (max) at 1.5 A
- Features
  - -1.3% to +1.2% accuracy across line, load, and temperature
  - Ability to parallel multiple devices
  - Configurable power good threshold (FB_PG)
  - Configurable current limit behavior (CLM)
  - Enable pin (EN)
  - Noise reduction and soft start pin (SS_SET)
  - Remote sense (OUTS)





TI Space product grades

Same radiation levels, same qualification, different package



Rad Tolerant Plastic	Rad Hard Plastic	Rad Hard Hermetic
TI Space EP	QML Class P	QML Class V

Pin-to-pin compatible, different radiation levels

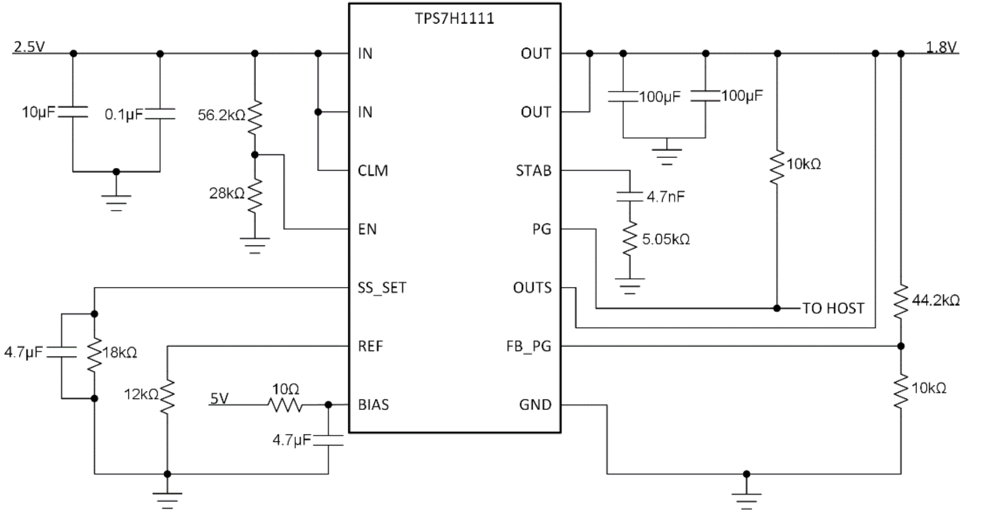
Packaging	Plastic	Plastic	Ceramic / Metal Can
Mil. Spec	VID	SMD	SMD
Burn- in	No	Yes	Yes
TID Char	**30 – 50 krad(Si)**	**< - - - - - - - - - - - - - - 50krad(Si) – 300 krad(Si) - - - - - - - - - - - - - >**	
TID RLAT	**20, 30, or 50 krad(Si)**	**< - - - - - - - - - - Non-RHA, 50, 100, or 300 krad(Si) - - - - - - - - - >**	
SEL	**43 MeV·cm²/mg**	**< - - - - - - - - - - - - - - ≥ 60 MeV·cm²/mg - - - - - - - - - - - - - - - - - - >**	

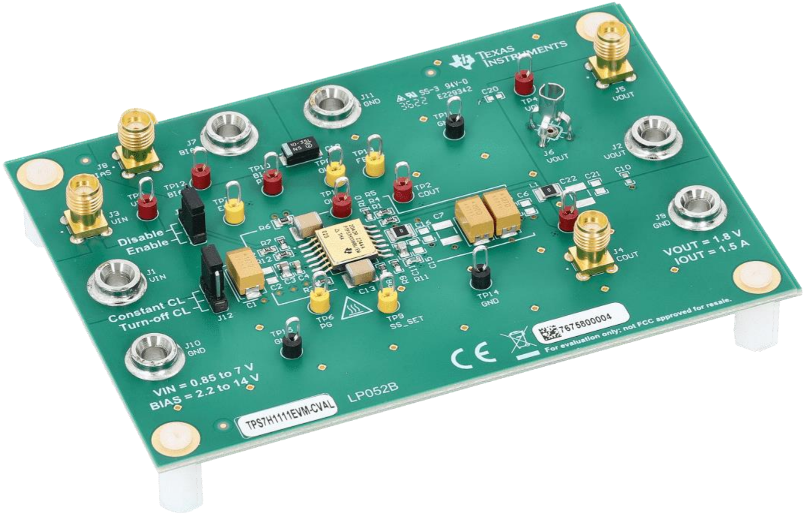
TPS7H1111-SEP

TPS7H1111-SP

TPS7H1111 noise & PSRR | Hardware overview

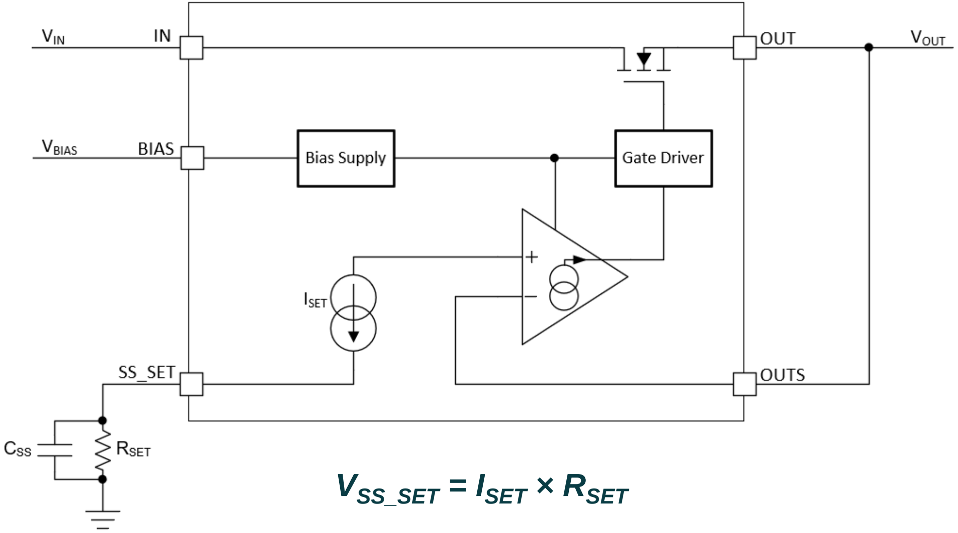
- Most measurements taken on TI evaluation board
- Focus on a golden configuration of 2.5V input, 1.8V output, with 5V bias supply





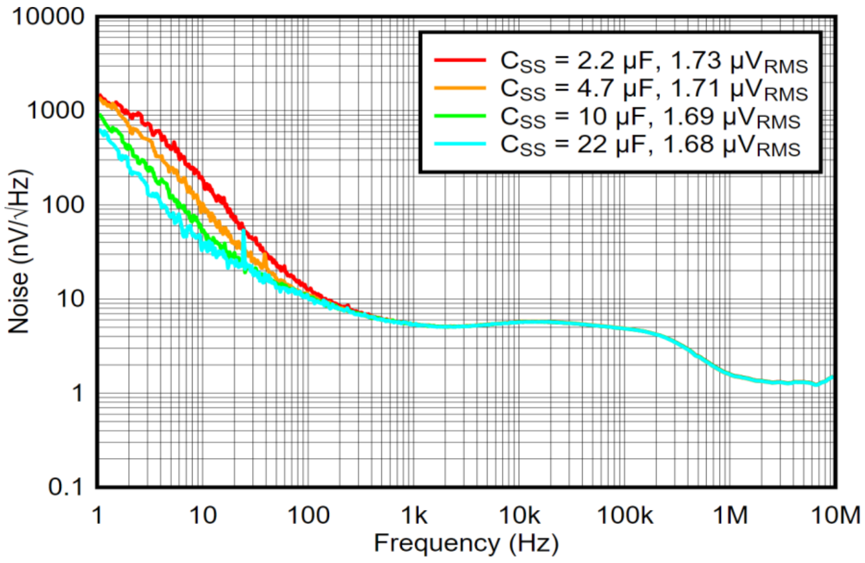
TPS7H1111 noise & PSRR | Noise optimization

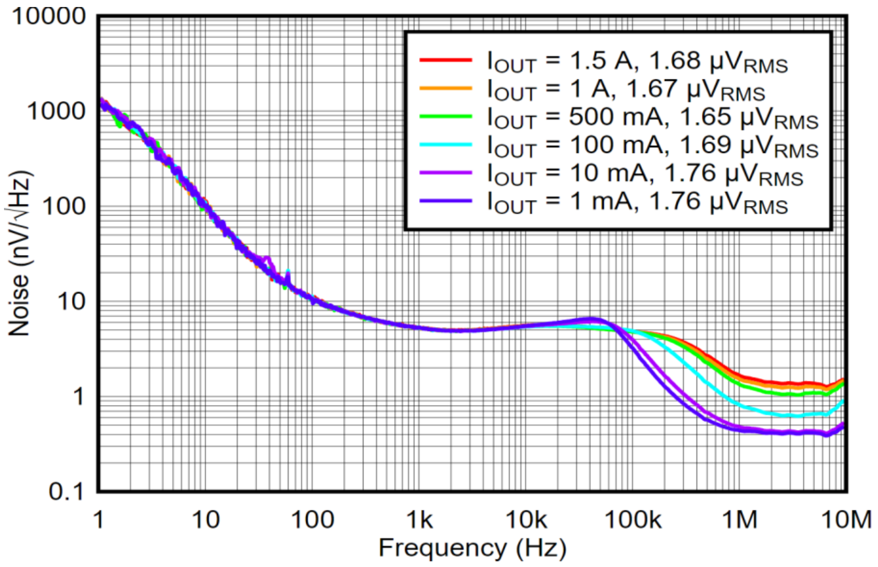
- A low-noise optimized, unity gain error amplifier is utilized to configure the output voltage
- A precision 100μA is sourced from the SS_SET pin
  - R_{SET} sets the output voltage
  - The desired output voltage is generated on SS_SET
  - The voltage on SS_SET will be replicated on the output
- Noise on SS_SET is not gained up by the resistor divider ratio (as in a traditional LDO)
- The SS_SET voltage is heavily filtered by C_{SS}
- The C_{SS} capacitor also enables a controllable soft start time



$$V_{SS\_SET} = I_{SET} \times R_{SET}$$

TPS7H1111 noise & PSRR | Noise results

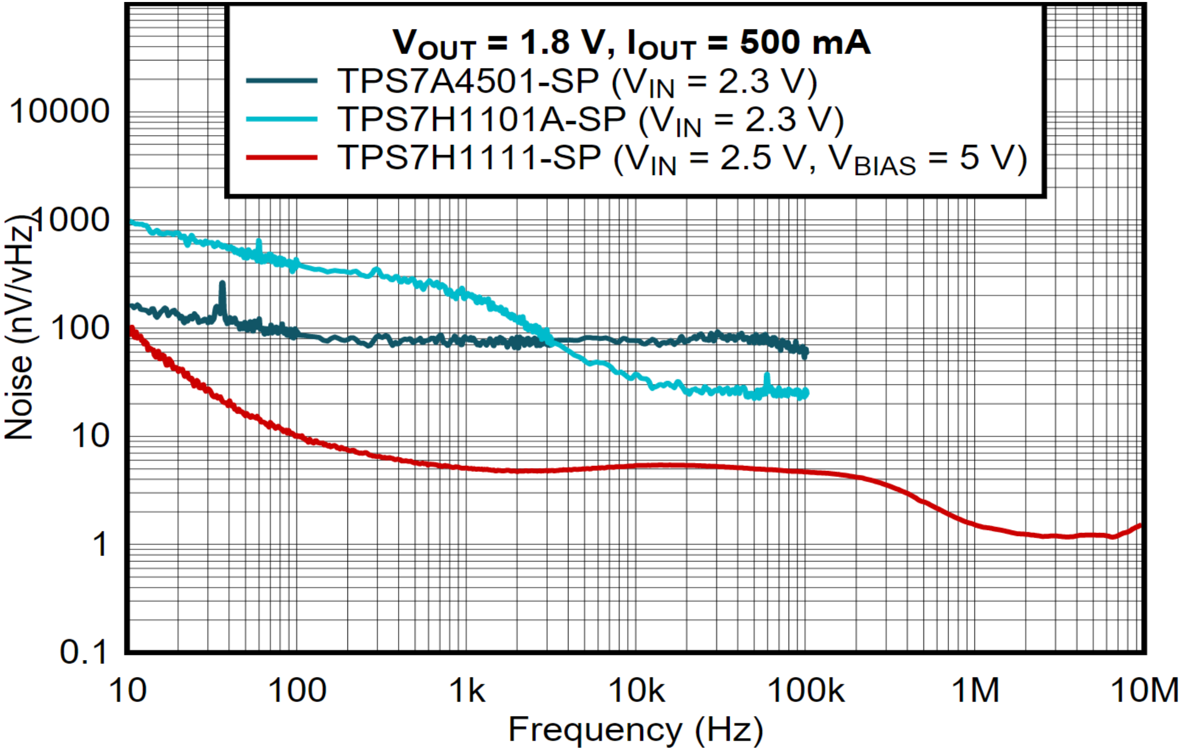




V_{IN} = 2.5V, V_{BIAS} = 5V, V_{OUT} = 1.8V

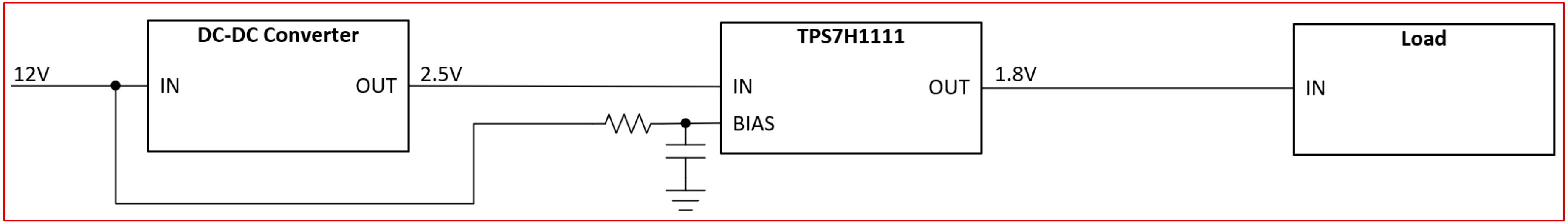
TPS7H1111 noise & PSRR | Noise comparison

Comparison to existing TI devices

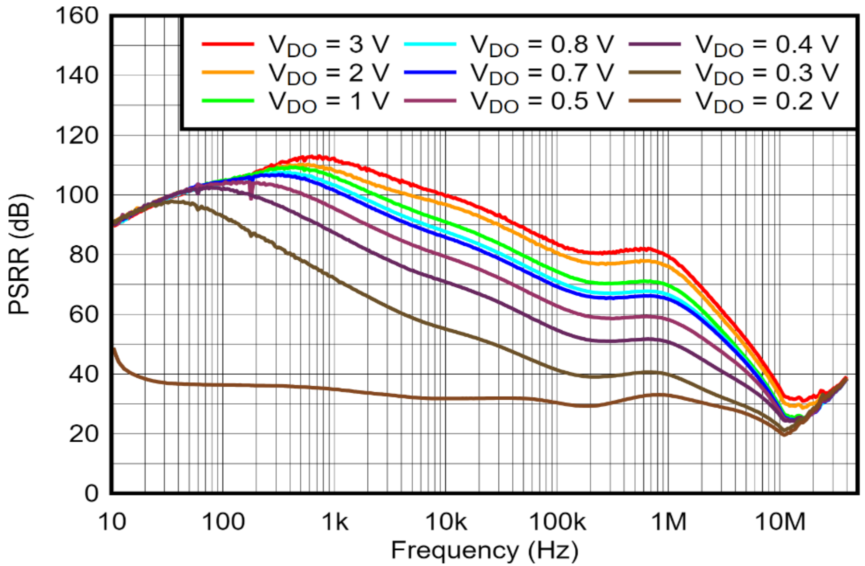


TPS7H1111 noise & PSRR | PSRR optimization

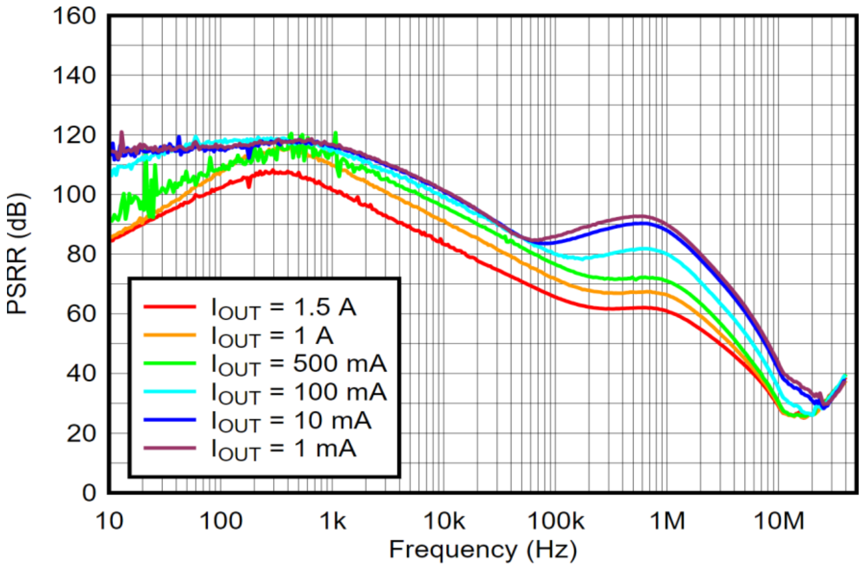
- High bandwidth error amplifier
  - Ability to maintain high gain through a wide frequency range attenuates input noise across a wide frequency
  - Must ensure stability across this bandwidth
- Pass element optimization
  - High self-gain required to maximize PSRR
  - An NMOS device has higher self-gain than a similar PMOS and therefore an NMOS was selected
  - Compared to a PMOS, an NMOS requires either a high dropout voltage requirement or a separate voltage greater than V_{OUT} to drive the NMOS gate
    - Charge pump could be utilized but this may introduce extra noise
    - Bias rail included, low current enables additional RC filtering to maximize overall PSRR



TPS7H1111 noise & PSRR | PSRR results



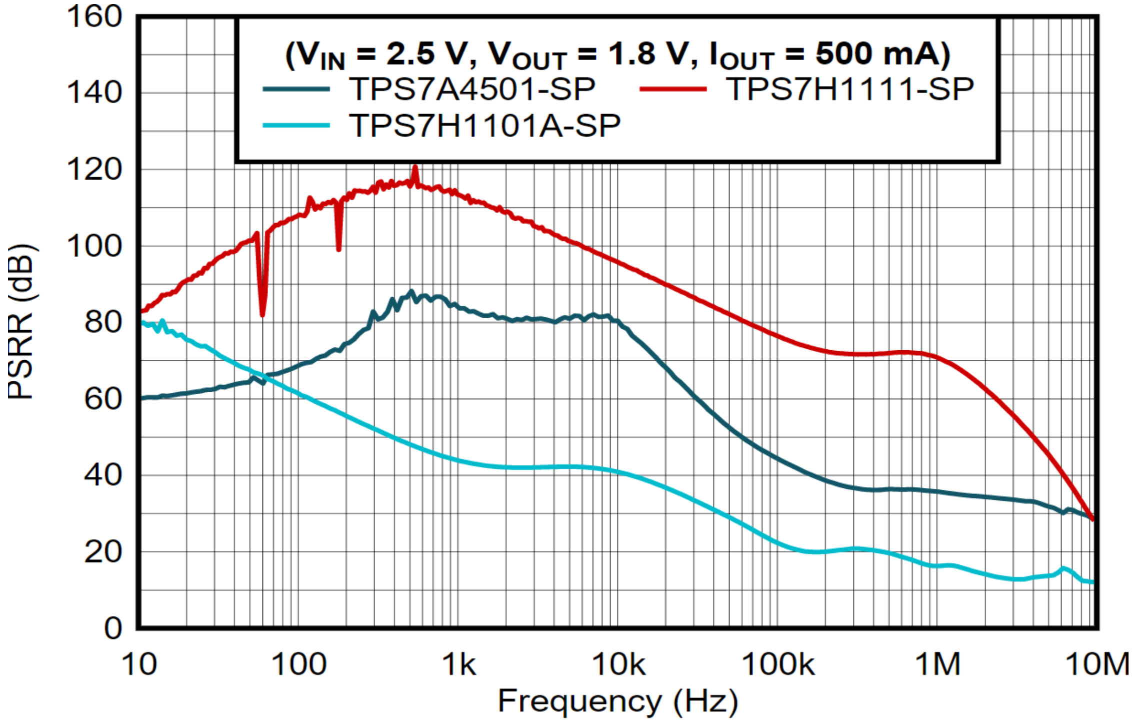
$V_{IN} = V_{OUT} + V_{DO}$, $V_{BIAS} = V_{OUT} + 1.6V$, $V_{OUT} = 1.8V$



$V_{IN} = 2.5V$, $V_{BIAS} = 5V$, $V_{OUT} = 1.8V$

TPS7H1111 noise & PSRR | PSRR comparison

Comparison to existing TI devices



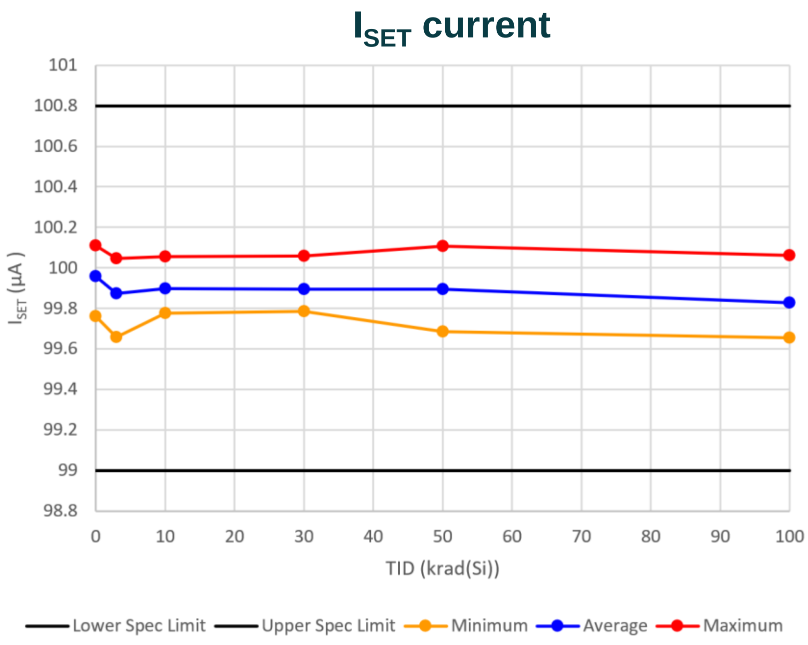
TPS7H1111 noise & PSRR | PSRR and noise

The TPS7H1111 offers many benefits while a discrete filter may be ineffective or impractical

Filter Type	Filter Values	Benefits	Tradeoffs
LC Filter with 5 kHz cutoff	10 µH and 100 µF	• Reduces high frequency ripple	• Affects control loop • Slower response to load transients • No 1/f noise filtering
LC Filter with 10 Hz cutoff	10mH and 25mF	• Reduces high frequency ripple • 1/f noise filtering	• Affects control loop • Slower response to load transients • Impractical size
TPS7H1111	N/A	• Reduces high frequency ripple • 1/f noise filtering • Improved transient performance	• Active component required

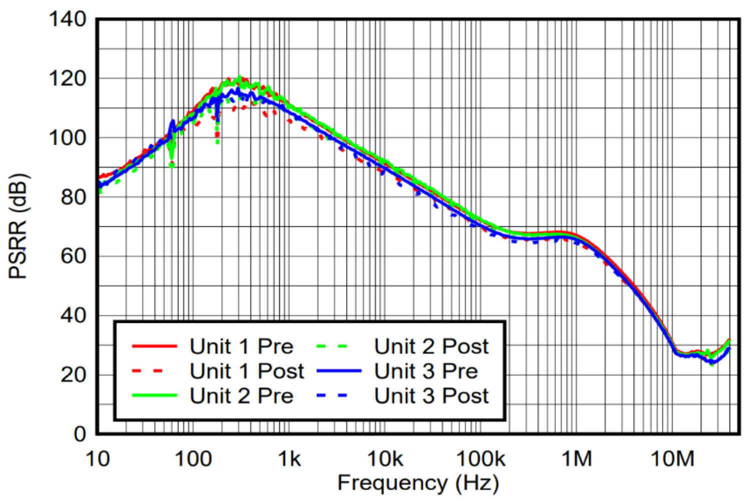
TPS7H1111 | TID overview

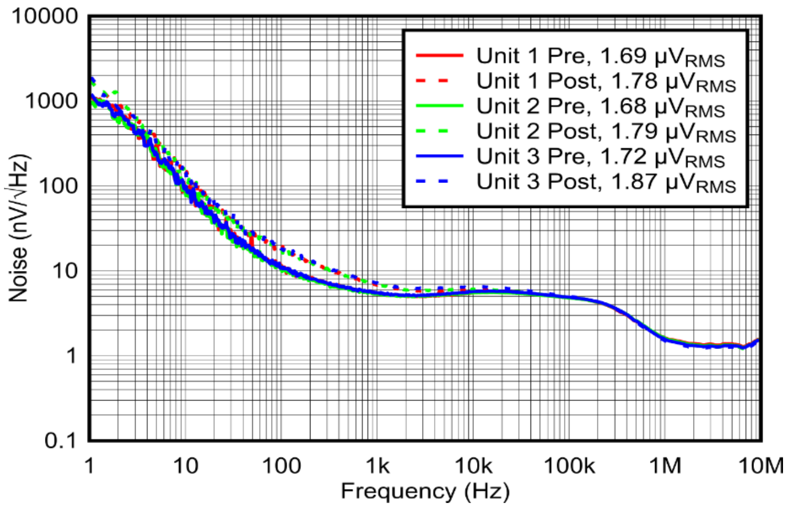
- The TPS7H1111 is designed and characterized to a TID of 100krad(Si).
  - Samples were irradiated then tested using the ATE (automated test equipment) program
- The TPS7H1111 is tested under both HDR and LDR conditions
  - HDR on biased and unbiased devices using TI's Co-60 gamma cell
  - LDR
    - The LBC7 process with annular NMOS has been demonstrated to be ELDRs free
    - An LDR characterization was performed to 100 krad(Si)



TPS7H1111 | TID for noise and PSRR

- Traditionally only ATE testing is performed post TID
- Additional post-TID noise and PSRR testing was done on an EVM for the TPS7H1111 due to the importance of the spec for this device
- Minimal change was observed





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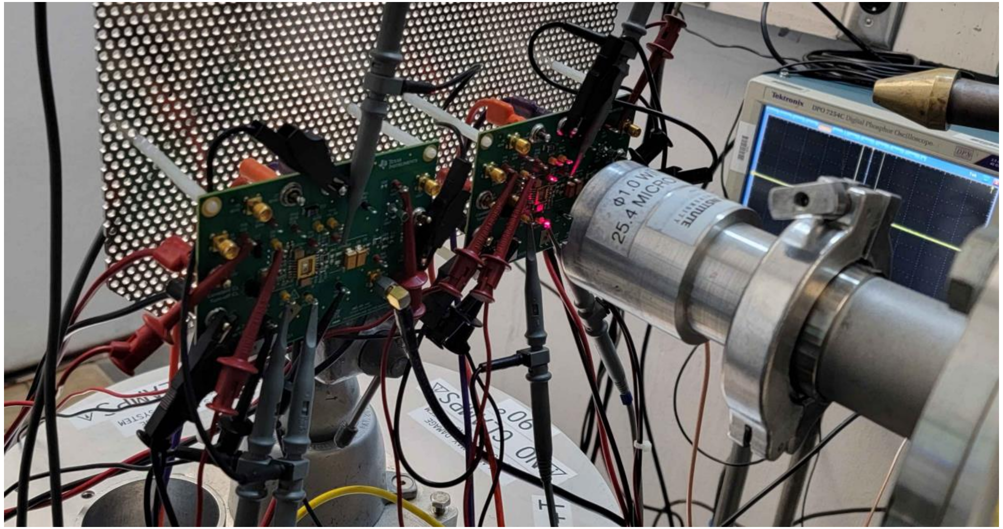
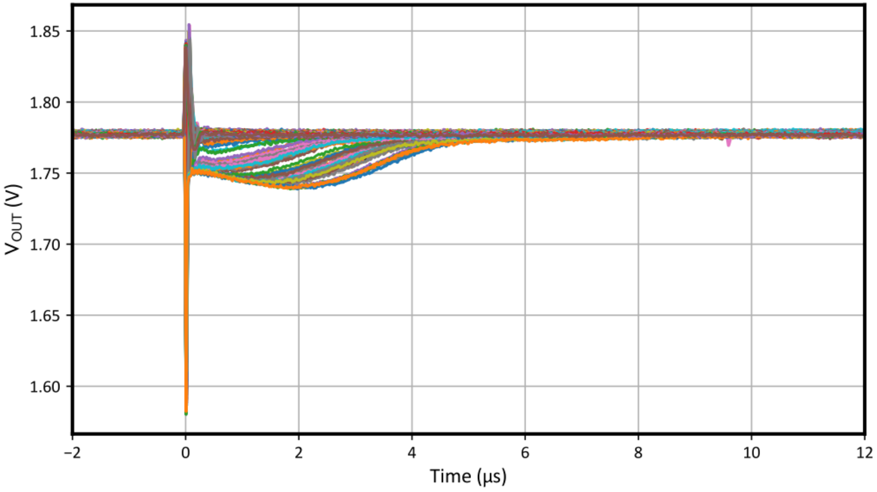
TPS7H1111 | SEE overview

- Tested at Texas A&M Cyclotron Institute's Radiation Effects Facility
- DSEE testing performed with V_{IN} = 7V and V_{BIAS} = 14V using ^{165}Ho
  - SEL testing was performed at a die temperature of approximately 125°C
  - SEB and SEGR testing was performed at a die temperature of approximately 25°C
  - SEB was tested with both the device enabled and with the device disabled.
- Four devices were tested for SEL and SEB/SEGR
  - No DSEE events were observed



TPS7H1111 | SEE – SETs

- SET testing performed with V_{IN} = 2.5V, V_{BIAS} = 5V, V_{OUT} = 1.8V, and I_{OUT} = 1.5A
  - Both ^{165}Ho and ^{109}Ag were utilized for an LET range of 48 to 75MeV×cm^2/mg
- The TPS7H1111 was found to have a very low SET cross section
  - The LET onset threshold in this configuration was found to be 60MeV×cm^2/mg
  - No SEFIs were recorded
- Event rate calculations were performed*
  - LEO (Low-Earth Orbit) MTBE of 1.51×10^6 years
  - GEO (Geosynchronous-Earth Orbit) MTBE of 5.09×10^5 years

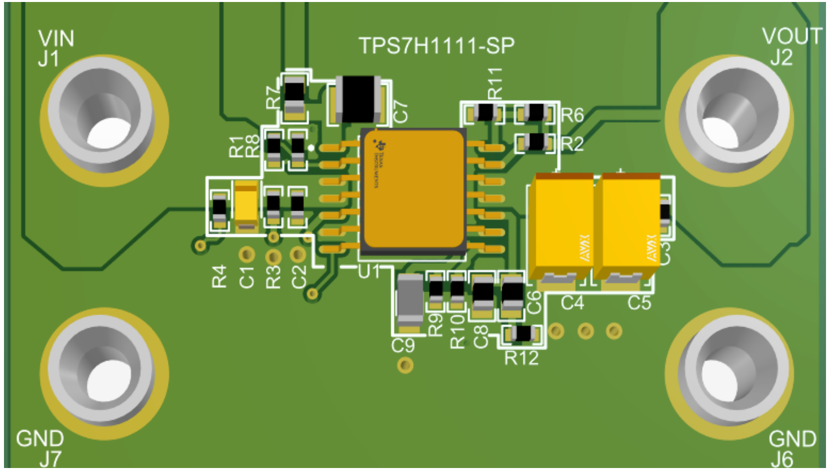


SETs detected for a single run (41 SET events with V_{OUT} transients ≥5%)

*Using CREME96 orbital integral flux estimations, 2.54 mm (100 mil) aluminum shielding, and "worst-week" solar activity

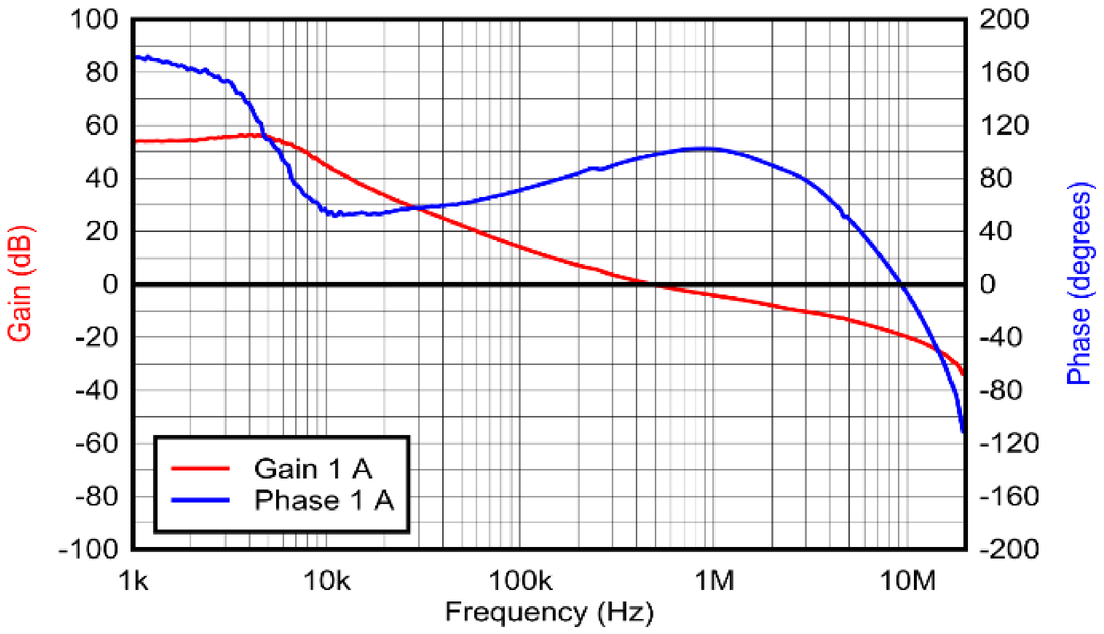
TPS7H1111 | Other benefits

- Excellent output voltage accuracy of –1.3% to 1.2%
  - Applies across –55°C to 125°C, a wide range of currents, input voltages, and output voltages
  - Simplifies powering circuits with tight voltage supply requirements
- Open drain power good pin with an adjustable power good threshold
  - Enables flexible sequencing options and voltage monitoring
- Configurable current limit for improved fault management
  - Turn-off current limit mode: The regulator turns off to prevent sustained high-power dissipation
  - Brick-wall current limit mode: The regulator maintains constant output current until fault is removed



TPS7H1111 | Stability

Bode plot from 2x100 µF AVX capacitors (TBME107K020LBLC9045)

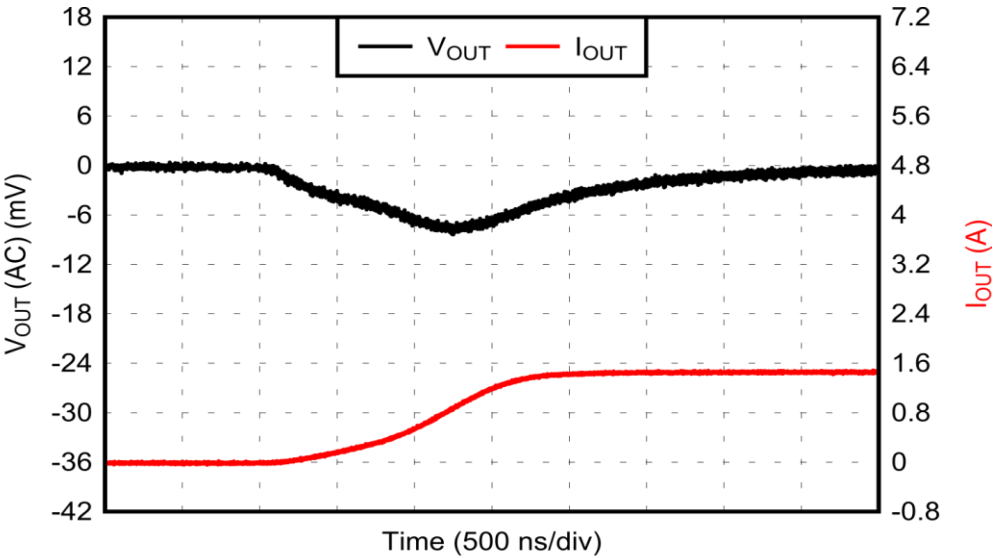


Load Current	Results	
	Phase Margin	***Gain Margin***
0A	83°	29dB
1A	98°	19dB
1.5A	99°	19dB

V_{IN} = 2.5V, V_{BIAS} = 5V, V_{OUT} = 1.8V

TPS7H1111 | Stability

- Demonstrated large signal stability with a fast load step
  - 1mA to 1.5A load step at a slew rate of 0.8A/µs.
- The output voltage falls appropriately 8mV which is 0.4% of the nominal output voltage.
- Smoothly recovers within approximately 3.5µs.



TPS7H1111 | Getting started

You can start evaluating this device leveraging the following:

Content type	Content title	Link to content or more details
Radiation Reports	TPS7H1111-SP Technical Documentation TPS7H1111-SEP Technical Documentation	https://www.ti.com/product/TPS7H1111-SP#tech-docs https://www.ti.com/product/TPS7H1111-SEP#tech-docs
EVM	TPS7H1111EVM-CVAL (Ceramic) TPS7H1111EVM (Plastic)	https://www.ti.com/tool/TPS7H1111EVM-CVAL https://www.ti.com/tool/TPS7H1111EVM
Simulation Model	TPS7H1111-SP PSpice Model	https://www.ti.com/product/TPS7H1111-SP#design-tools-simulation

References

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- https://www.ti.com/lit/an/slyt583/slyt583.pdf

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