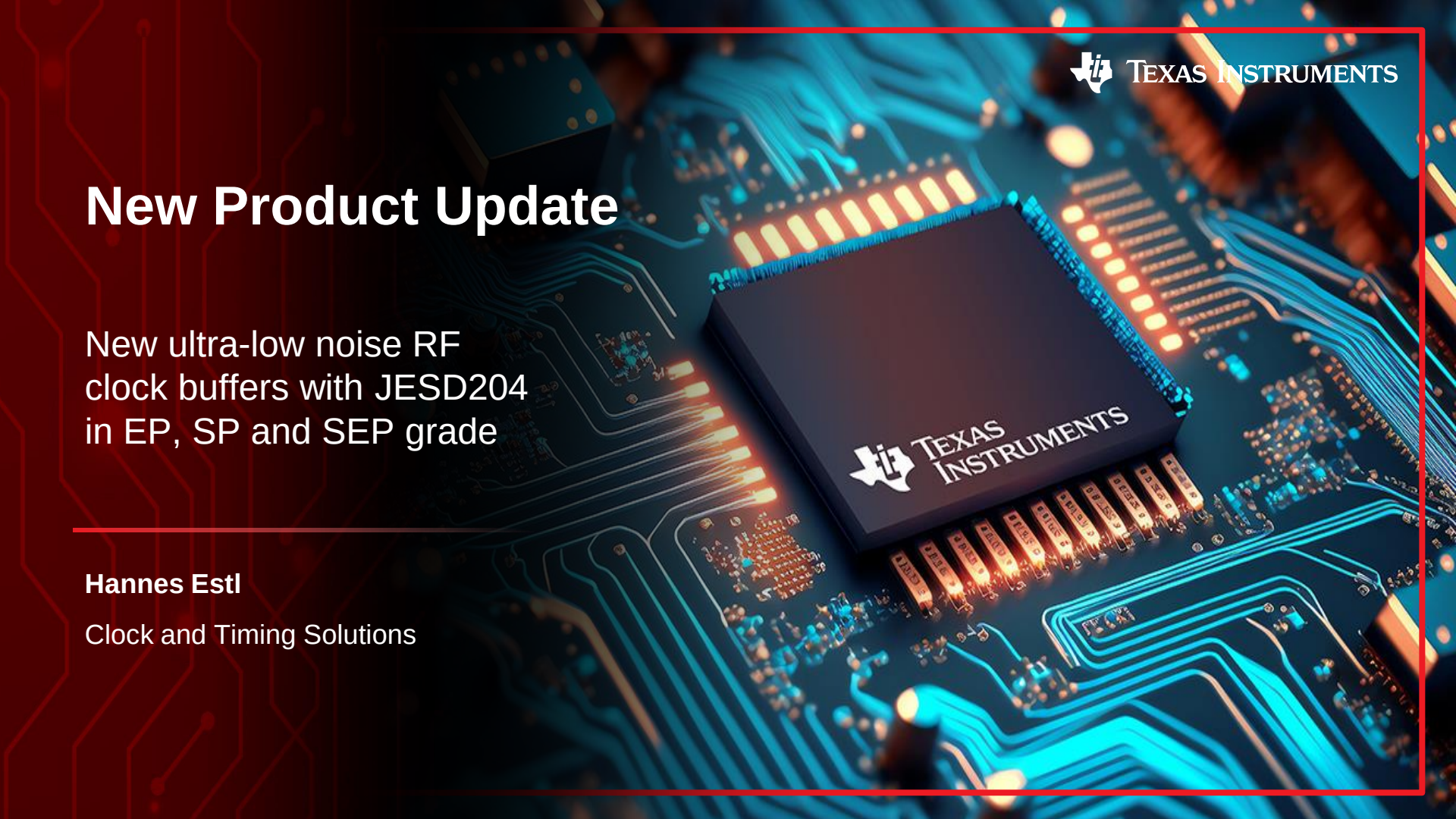
New Product Update

New ultra-low noise RF clock buffers with JESD204 in EP, SP and SEP grade



Hannes Estl

Clock and Timing Solutions

Agenda

- Portfolio overview and outlook
- RF clock distribution buffers up to 16GHz
- Simplified synchronization of data converters with JESD204
- The right solution for terrestrial and space applications

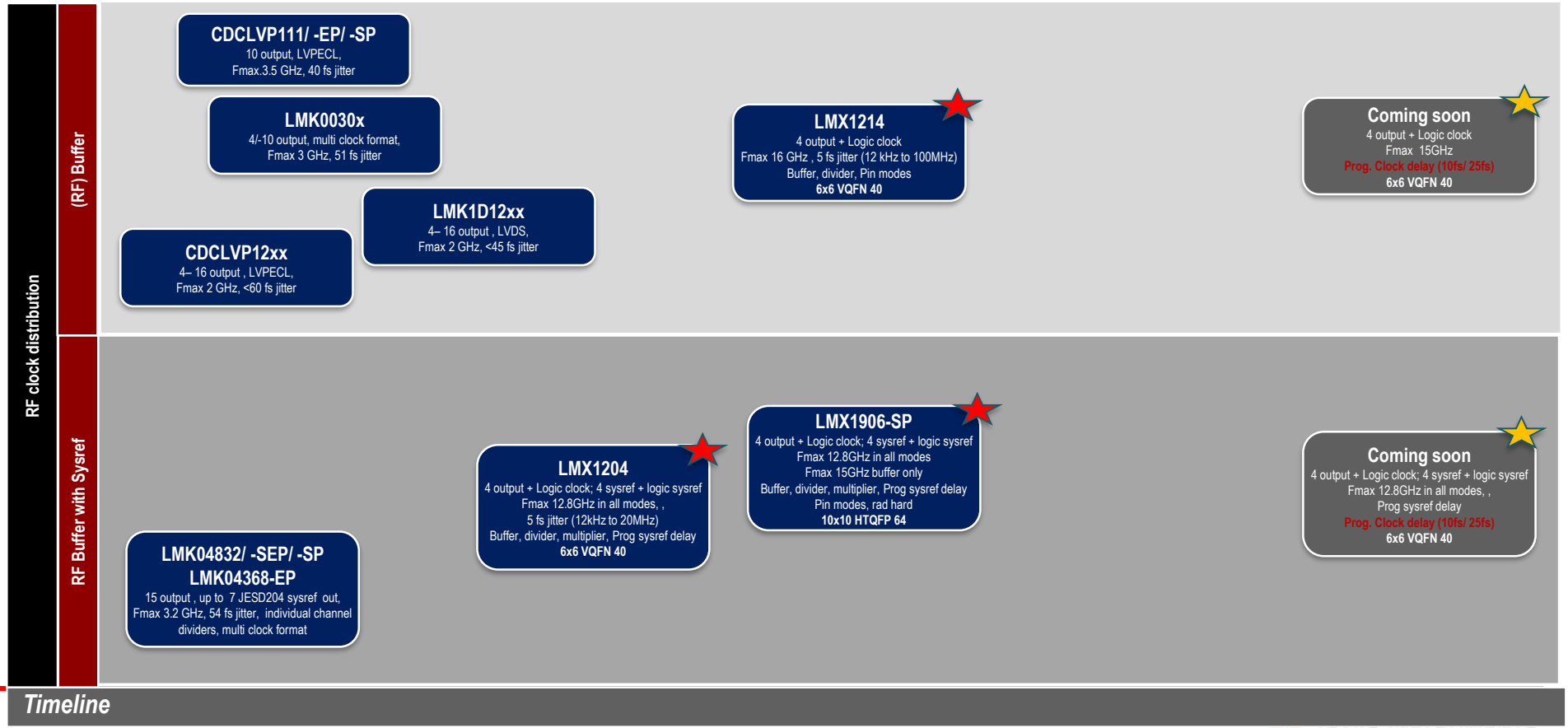
Please feel free to “chat.” We are available to answer any questions you have throughout this presentation.

RF clock distribution portfolio

(2 GHz and higher)

New family

Improved next gen



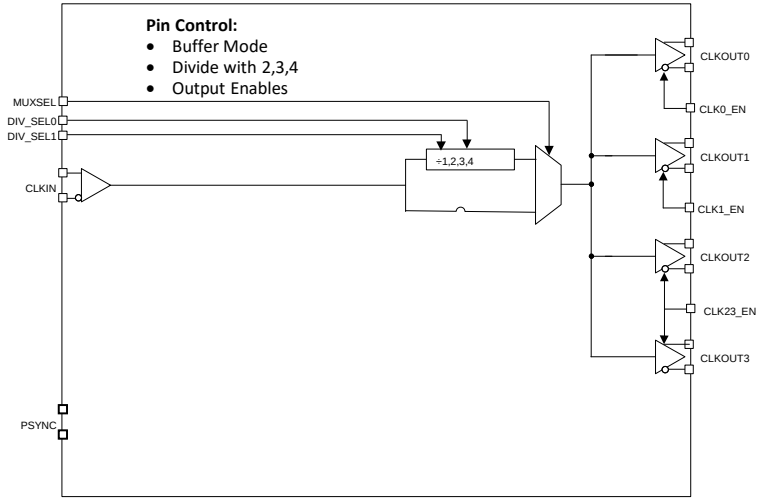
LMX1214 High-frequency buffer (pin mode, no serial interface needed)

Features

- **16 GHz** output frequency (L to Ku band)
  - 0 dBm at 18 GHz
  - 5 dBm at 10 GHz
- Low noise
  - Noise Floor of **-161 dBc/Hz** for 6 GHz Output
  - 26 fs jitter at 6 GHz (DC – 6 GHz integration)
  - **5 fs jitter** at 6 GHz (12 kHz to 100 MHz)
- **4 ps** typical skew (CLK0-CLK3)
- 1 ps typical propagation delay variation
- Multiple clocks with divide option
  - 4 high-frequency clock outputs
    - Supports buffer, divide by 2,3,4
- SYNC feature for all divide values
- **Pin Control** eliminates need for SPI
  - Can enable 0,1,2 or 3 outputs with pins (although CLK2 and CLK3 share OE pin)
  - Can select DIV 1,2,3,4
- 40-pin, 6x6 mm package

Target use-cases

- Aerospace & Defense, Test & Measurement, Communications
- High-channel count, phase-aligned, RF clocks 1GHz up to 18GHz



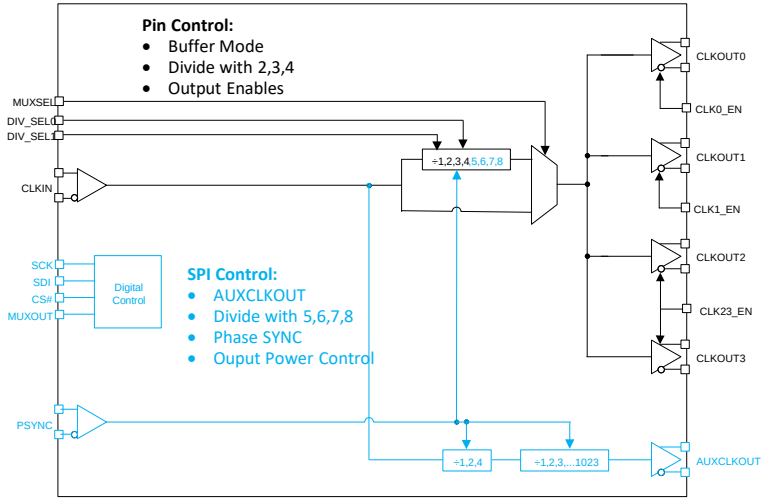
Value Proposition

- **High integration** reduces components & improve skew variation
- **Output power of each channel independent from input power**
- **Low noise floor and small additive jitter** minimize clock degradation of clock signal (A/D SNR, LO, ..)
- Covers L, S, C, X and Ku frequency bands

LMX1214 High-frequency buffer/divider (all features)

Features

- **16 GHz** output frequency (L to Ku band)
  - 0 dBm at 18 GHz
  - 5 dBm at 10 GHz
- Low Noise
  - Noise Floor of **-161 dBc/Hz** for 6 GHz output
  - 26 fs jitter at 6 GHz (DC – 6 GHz integration)
  - **5 fs jitter** at 6 GHz (12 kHz to 100 MHz)
- **4 ps** typical skew (CLK0-CLK3)
- 1 ps typical propagation delay variation
- Multiple clocks with divide option
  - 4 high-frequency clock outputs
    - Supports buffer, divide by 2,3,4,5,6,7,8
  - Auxiliary clock
    - 1/2/4 pre divider followed by 1,2,3,…1023 divider
  - Includes selectable buffer, divide by 2, 3, 4, 5, 6, 7 and 8
- SYNC feature for all divide values
- Pin Control eliminates need for SPI for many cases
  - Can enable 0,1,2 or 3 outputs with pins (although CLK2 and CLK3 share OE pin)
  - Can select DIV 1,2,3,4
- SPI support is for auxiliary clock, divides greater than 4 on main clocks, SYNC, and output power control (8 levels)
- 40-pin, 6x6 mm package



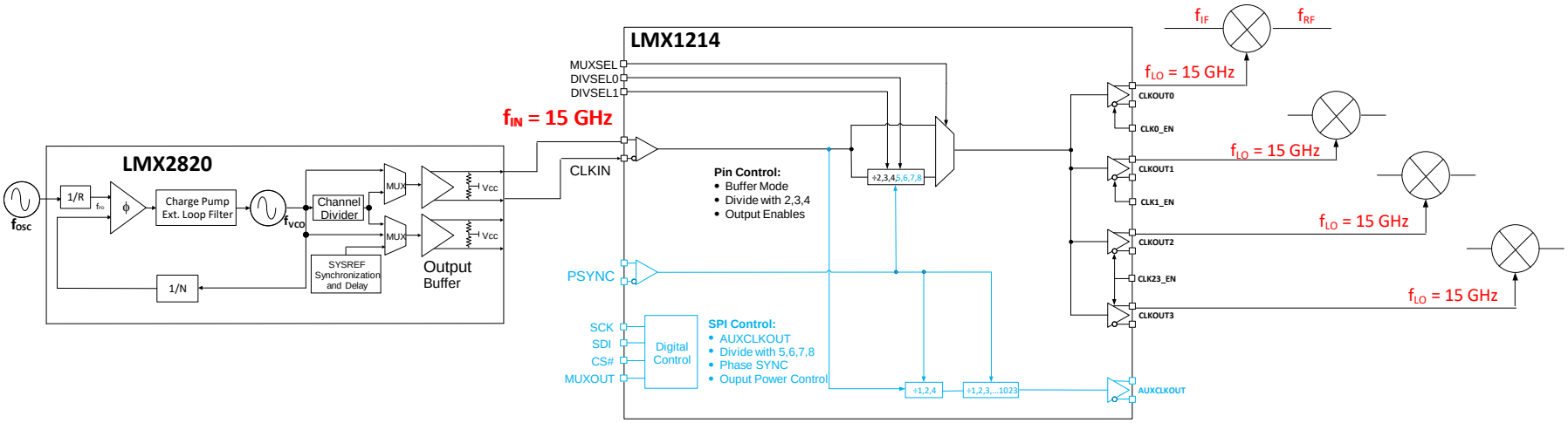
Additional Value Proposition (vs. LMX1214 pin mode)

- Provides additional clock out for FPGA, SoC, logic, …
- Clock divide 2-8

Target use-cases

- Aerospace & Defense, Test & Measurement, Communications
- High-channel count, phase-aligned, RF clocks 1GHz up to 18GHz

Simplified LO distribution using LMX1214

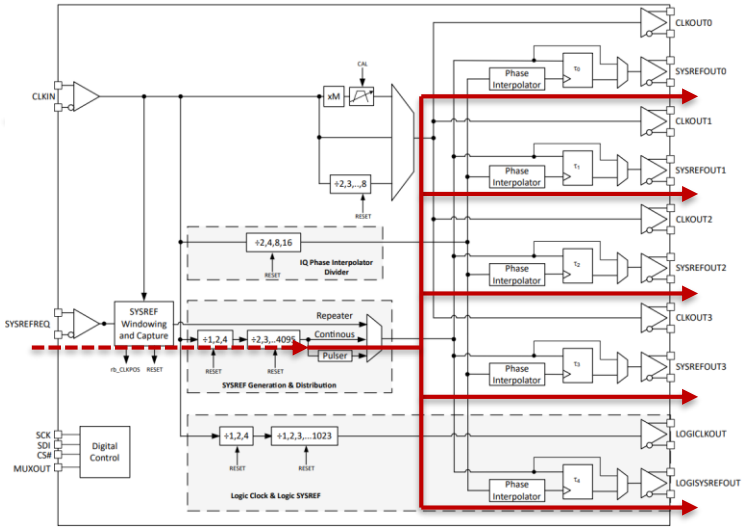


LMX1204 High frequency buffer/multiplier/divider with SYSREF

Features

- Up to **12.8 GHz** output frequency
  - **SYSREF** and SYNC features work up to **12.8 GHz** Input
- Noise Floor of **-161 dBc/Hz** for 6 GHz Output
- 4 high-frequency clock outputs
  - Includes selectable buffer, divide by 2…8
  - Multiply x2, x3, and x4 to 3.2 GHz to 6.4 GHz
- 1 FPGA clock output
  - Includes divides of 1,2,3,…1023
- SYSREF for all clock outputs
  - Individual delay adjustment (508 steps)
  - Supports both master and buffer mode
  - **SYSREF windowing**
- SYNC feature for all divide values
- 40-pin, 6 mm x 6 mm package

Mode	Output frequency	Noise floor @ 6.4 GHz
Buffer	0.3 – 12.8 GHz	-161 dBc/Hz
÷2, 3,…,8	0.15 – 6.4 GHz	-160.5 dBc/Hz
X2, X3, X4	3.2 – 6.4 GHz	-161.5 dBc/Hz



Value proposition

- High-integration reduces component count & improves skew variation
- Low Noise floor minimizes clock degradation of A/D SNR
- **Simplified synchronization of large numbers of Giga-sample data converters with JESD204**

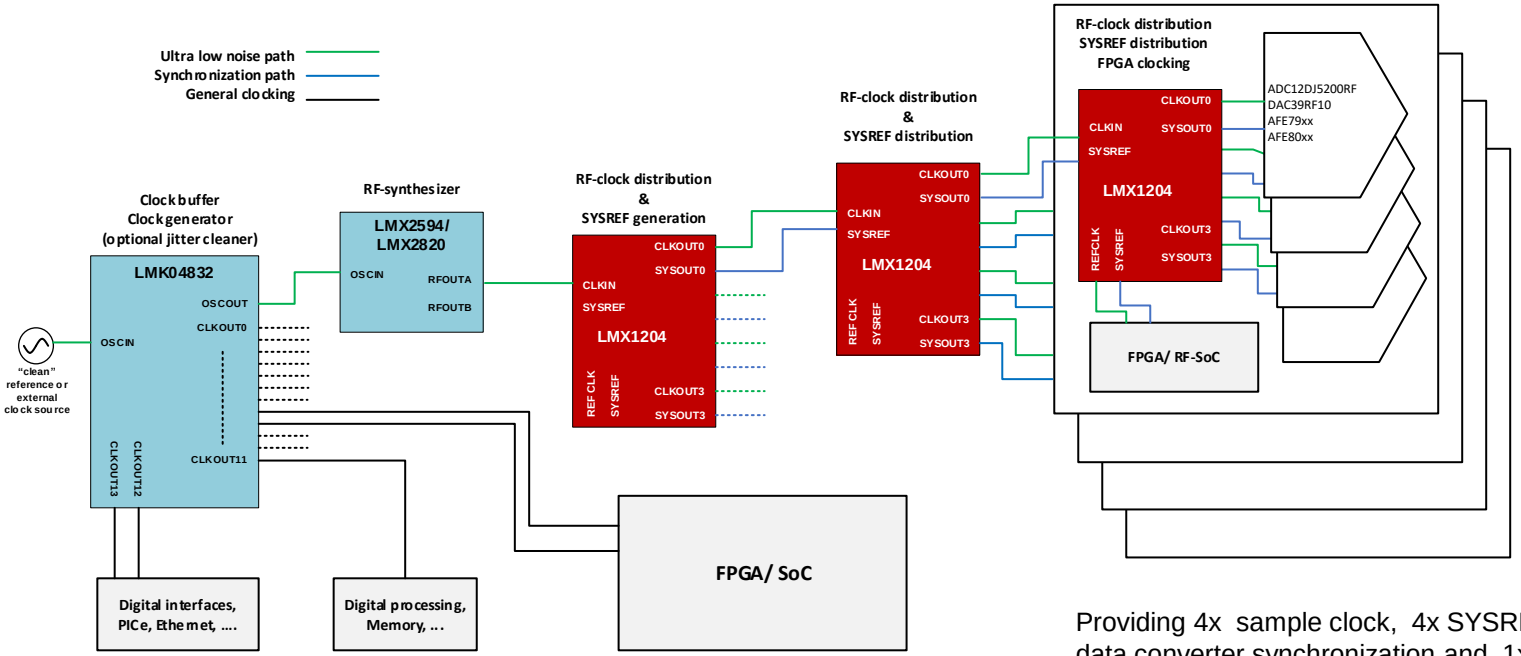
Target end equipment

- Aerospace & Defense, Test & Measurement, Communications
- Electronically scanned phased arrays for Radar and Communication

LMX1204 Optimized for high channel count RF data conversion

Clocks per level: 1 → 4 → 16 → 64 AFE

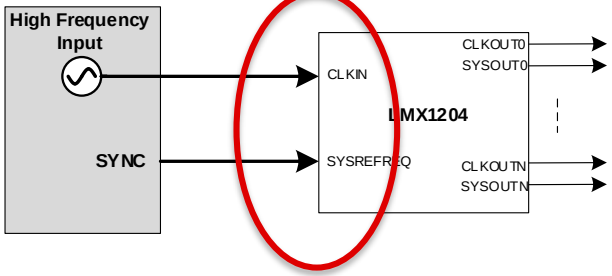
ICs per level: 1 IC + 4 ICs + 16 ICs

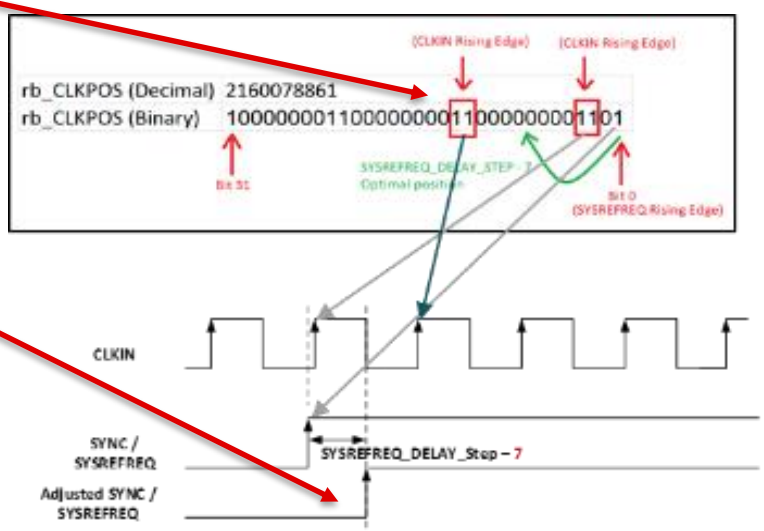


Providing 4x sample clock, 4x SYSREF for data converter synchronization and 1x FPGA clocking + SYSREF with a single IC

LMX1204 – SYSREF Windowing

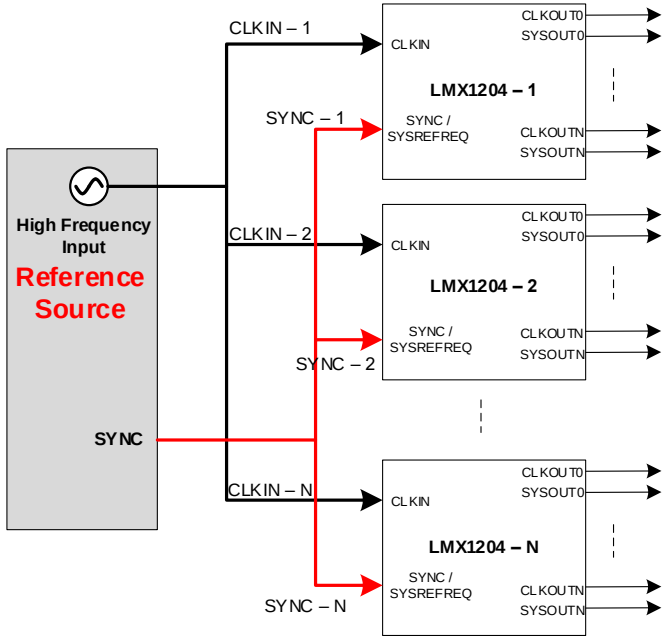
- In JESD architecture, SYSREF is used as SYNC input for data converter's internal sections reset (NCO, DDC, DUC, etc..). Hence the SYNC can be referred as SYSREF in this context
- SYSREF windowing used to calibrate the timing between the CLKin input and the SYSREF path in order to meet the setup/hold timing requirement
- It provides the timing samples of the SYSREFREQ rising edge (SYNC input) to the CLKIN rising edge
- To optimized the setup and hold time, the delay is provided in the SYSREFREQ input to keep near to the falling edge of the CLKIN then perform the SYNC

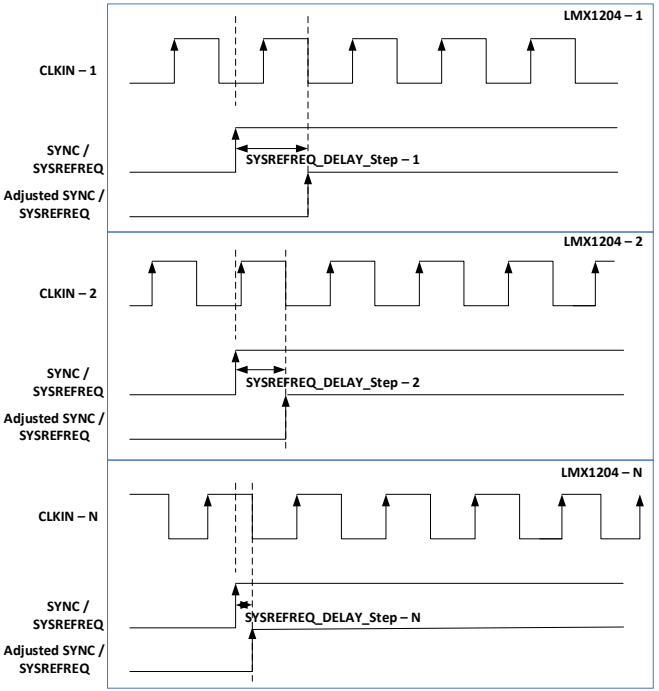




Multi-device SYSREF Windowing

- To perform the SYNC operation in multi-device LMX1204s, SYSREF windowing perform and using the individual CLKIN and SYSREFREQ rising edge location, the delay in provided and perform the synchronization.

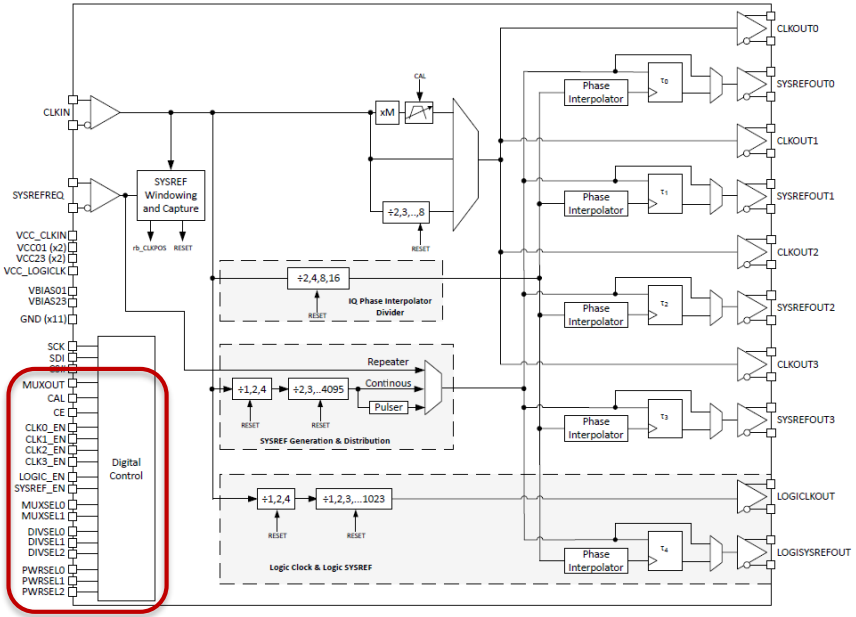




LMX1906-SP Rad-hard 15 GHz buffer/multiplier/divider with SYSREF and FPGA clock

Features

- **TID >= 100 krad(Si)**
- **Single Event Latch-up >= 120 MeV-cm²/mg**
- Ambient temperature range: **-55 ºC to 125 ºC**
- Up to **15 GHz** output frequency
  - **SYSREF** and SYNC features work with up to **12.8 GHz** input
- Noise Floor of **-158 dBc/Hz** for a 6 GHz output
- 4 high frequency clock outputs
  - Can be used as a buffer, divider (divide by 2, 3, 4, 5, 6, 7 or 8) or multiplier (x2, x3, x4)
- 1 LOGICLK Output for FPGA clocking
  - Includes divider values of 1, 2, 3, … up to 1023
- SYSREF paired with each clock output
  - Individual delay adjustment
  - Supports both master and repeater mode
- **SYSREF Windowing** optimizes setup and hold times of SYSREFREQ
- SYNC feature for all divide values
- **64-pin QFP Space high grade plastic** – smaller size & higher performance



Mode	Output Frequency	Noise Floor @ 6 GHz	Jitter (12k to 100M)
Buffer	0.3 – 15 GHz	-158 dBc/Hz	7 fs
÷ 2, 3, 4, 5, 6, 7, 8	0.15 – 7.5 GHz	-158 dBc/Hz	7 fs
x2	3.2 – 6.4 GHz	-158 dBc/Hz	17 fs
x3	3.2 – 6.4 GHz	-158 dBc/Hz	22 fs
x4	3.2 – 6.4 GHz	-158 dBc/Hz	27 fs

Value proposition

- High integration reduces components & improves skew variation
- Low noise floor minimizes clock degradation of data convertor SNR
- Radiation hardened IC design to meet mission targets
- Pin modes for easy device configuration without SPI – power, divider, mux selection and output EN

Texas Instruments

LMX1204/ 14 / LMX1906-SP / -SEP / -EP differences

Feature / Specifications	Conditions	LMX1214	LMX1204	LMX1906-SP	-SEP	-EP
Total ionizing dose (TID)	Radiation Test	Not applicable	Not applicable	100 krad	30 krad	Not applicable
Single event latch-up (SEL)				Up to 87 MeV-cm²/mg	Up to 43 MeV-cm²/mg	
Single event functional interrupt (SEFI)				Up to 87 MeV-cm²/mg	Up to 43 MeV-cm²/mg	
Operating Temperature (^{0}C)		-44 ºC to 85 ºC	-44 ºC to 85 ºC	-55 ºC to 125 ºC		
Noise Floor (6 GHz Normalized)	Buffer (bypass) Mode	-161 dBc/Hz	-161 dBc/Hz	-159 dBc/Hz		
	Divider Mode	-160.5 dBc/Hz	-160.5 dBc/Hz	-158.5 dBc/Hz		
	Multiplier Mode	Not applicable	-161.5	-169.5 dBc/Hz		
Output Frequency Range	Buffer Mode	0.3 – 18 GHz	0.3 – 12.8 GHz	0.3 – 15 GHz*		
	Divider Mode	0.15 – 6.4 GHz				
	Multiplier Mode	Not applicable	3.2 – 6.4 GHz			
Multiplier Output Values		Not applicable	x1,x2,x3,x4	x2,x3,x4		
Pin Mode Supported	Device configuration	Yes	No	Yes		
P and N output pins flipped	CLKOUT0/1 & SYSREFOUT0/1	CLKOUT0/1 & SYSREFOUT0/1 flipped	None	CLKOUT0/1 & SYSREFOUT0/1 P and N pins are flipped for simplifying routing		
SYSREF Supported	Input and Output	No	Yes			
SYNC & SYSREF Windowing Supported		No	Yes			
Logic clock & SYSREF default enable / disable		Disable		Enable		
Package		40 pins QFN (6 mm x 6 mm)		64 pins QFP (10 mm x 10 mm); pin-to-pin compatible		

* SYNC, divider, SYSREF and SYSREF windowing supported up to 12.8GHz frequency

Getting started

You can start evaluating this device leveraging the following:

Content type	Content title	Link to content or more details
Product folder	LMX1204	https://www.ti.com/product/LMX1204
Evaluation Module	LMX1204EVM	https://www.ti.com/tool/LMX1204EVM
Application Note	Getting the Most of Your Data Converter Clocking System Using LMX1204	https://www.ti.com/lit/an/snaa360
Application Note	LMX1204 Multiplier Clock Distribution Drives Large Phased-Array Systems	https://www.ti.com/lit/pdf/snaa366
Reference Design	TIDA-010259, Cascaded LMX1204 reference design	https://www.ti.com/tool/TIDA-010259
Product folder	LMX1214	https://www.ti.com/product/LMX1214
Evaluation Module	LMX1214EVM	https://www.ti.com/tool/LMX1214EVM
Product folder	LMX1906-SP	https://www.ti.com/product/LMX1906-SP
Evaluation Module	MX1906EVM-CVAL	https://www.ti.com/tool/LMX1906EVM-CVAL

Thank you

For more information please visit us at TI.com or directly at our RF PLL & Synthesizer product pages

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