Webinar

Power the Future: Selecting and Designing Power Components for AMD Versal™ AI Edge Series

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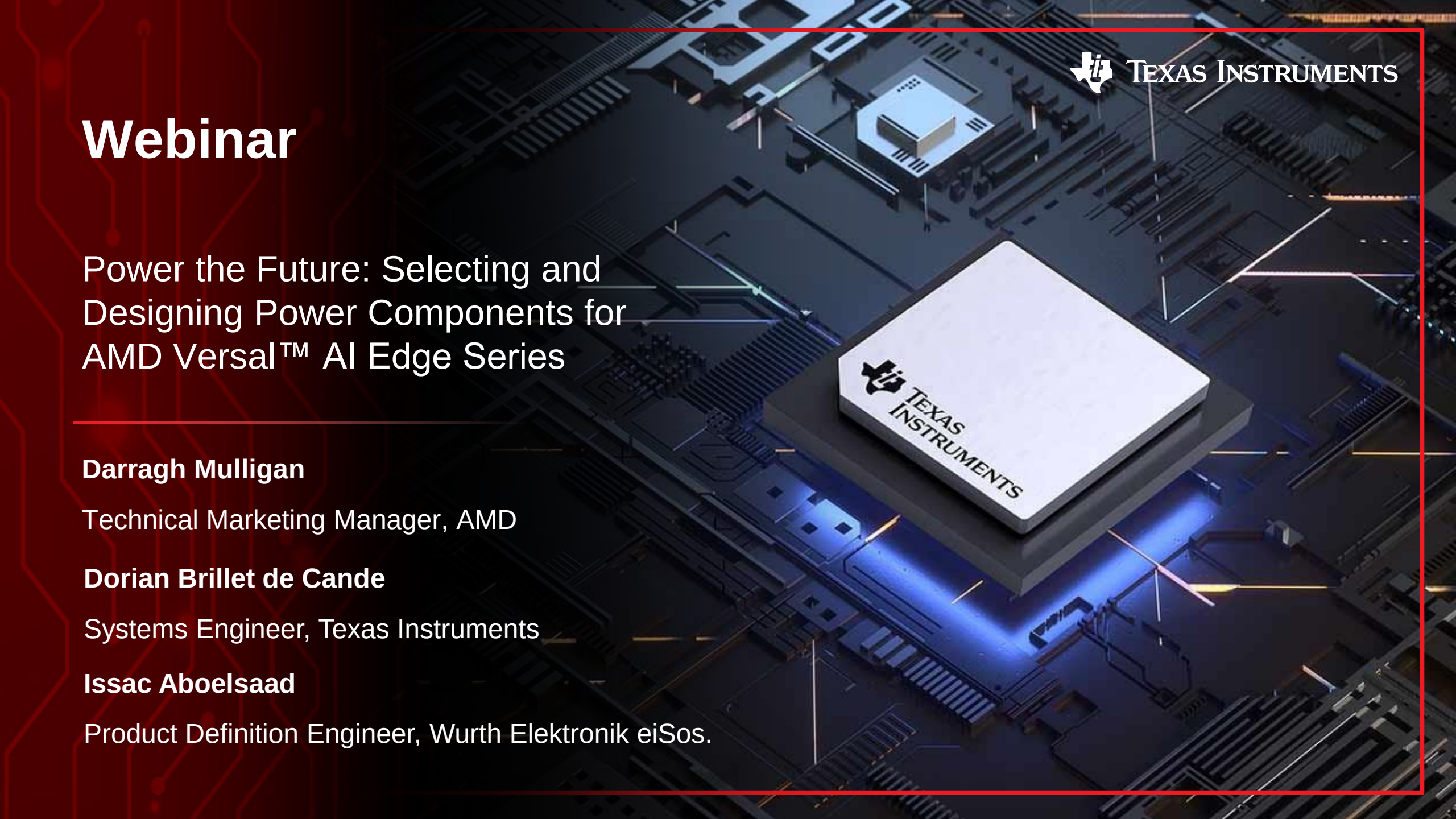


AMD VERSAL™ ARCHITECTURE POWER IMPROVEMENTS

Programmable Logic:

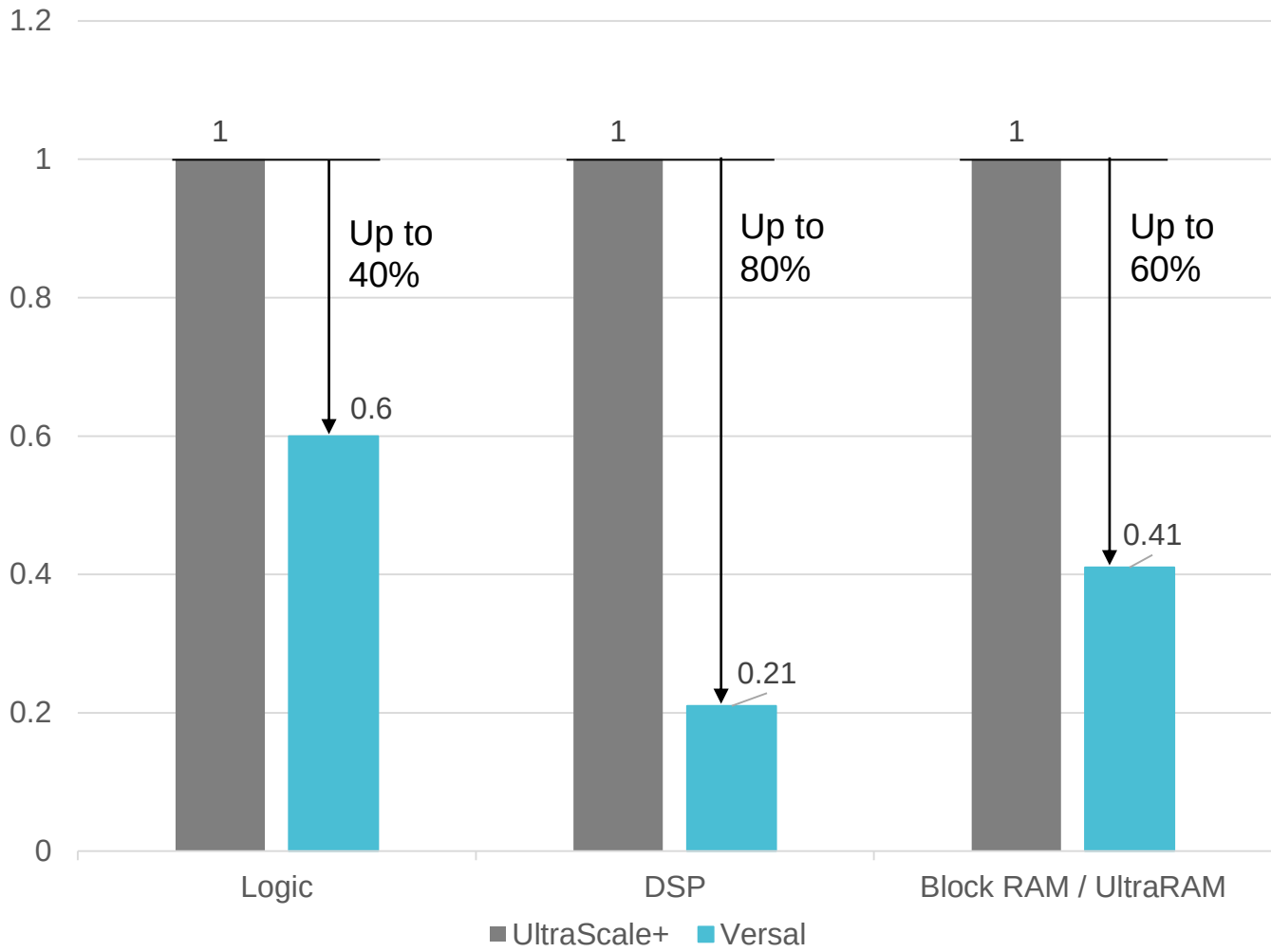
- Up to 40% lower power depending on LUT implementation: Logic, Distributed RAM, Shift Reg, or Register

DSP

- Up to 80% reduction for floating point operations: DSP58 vs. DSP48

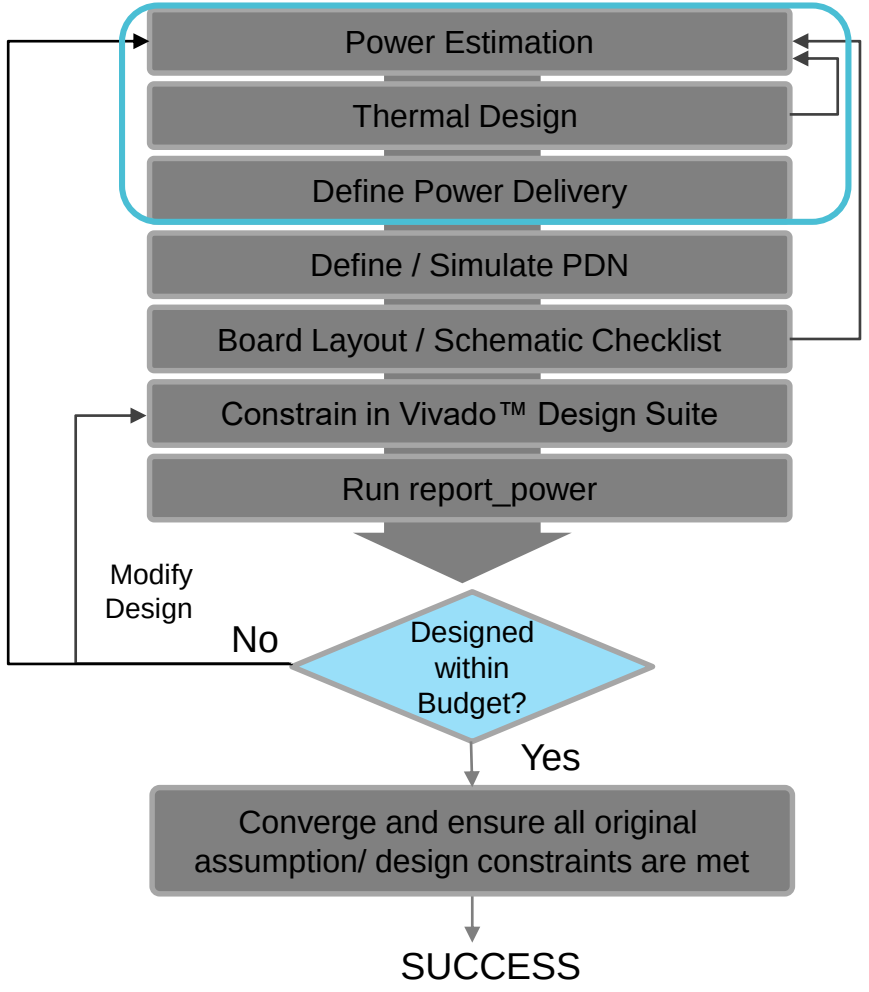
Block RAM / UltraRAM

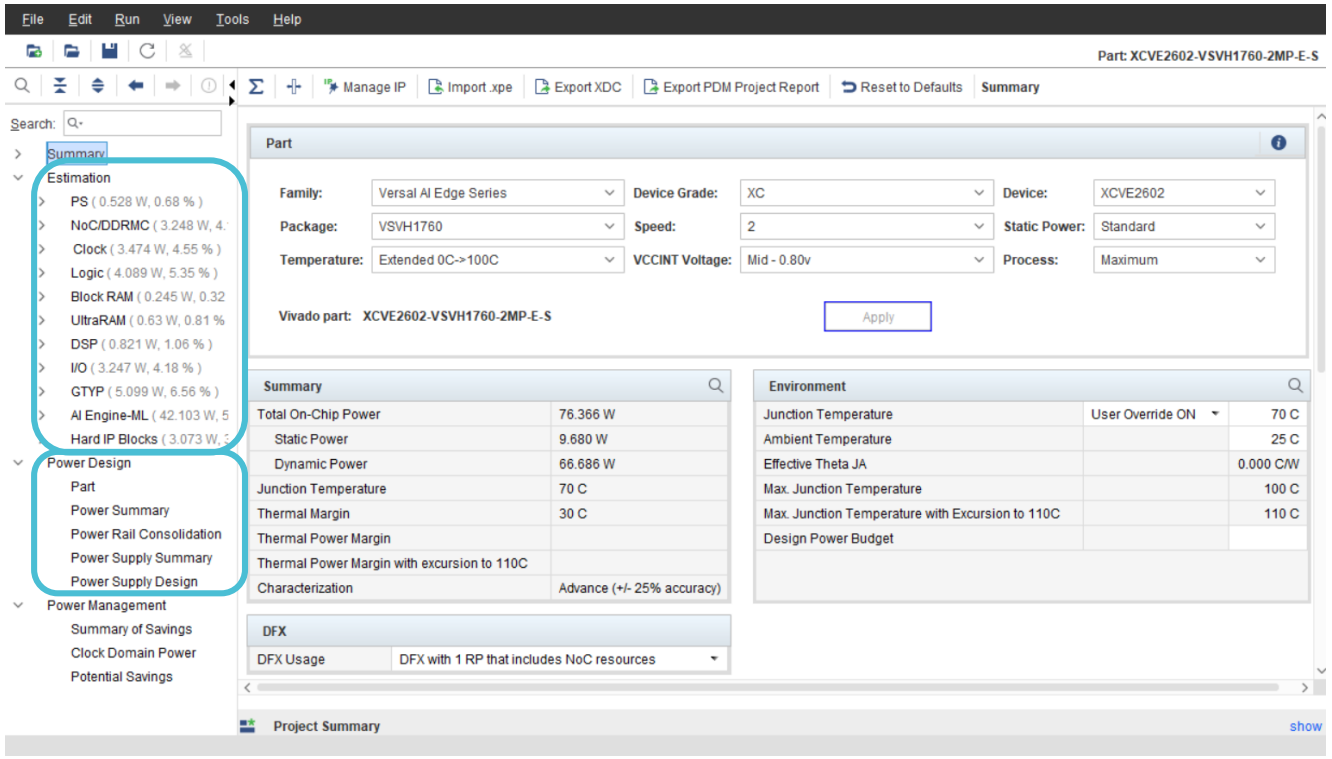
- Continued power reduction in AMD Versal™ adaptive SoCs compared to AMD UltraScale+™ FPGAs



See Endnotes VER-043

Versal™ Devices' Power Design Flow





Introduction to the Power Design Tab of PDM

Device Characteristics

- Summary of device details
  - Part number, speed & temperature grade, process information, packaging
  - Static, dynamic, and total device power
  - Export to .xml file
  - Import XPE files to PDM

Power Supply Design Table

- Individual rail characteristics by power domain
  - Rail names
  - Voltage tolerances
  - Static, dynamic, and power-up current requirements
  - Sequencing
  - Step load values

Power Rail Consolidations

- Full power management
  - Selected to allow for powering down of rails
- Minimum Rails
  - Reduces overall regulator count at the expense of power management
- Rail consolidation diagrams, power sequencing & tables

Part	
Family	Versal AI Edge Series
Device Grade	XC
Device	XCVE2602
Package	VSVH1760
Speed	2
Static Power	S
Temperature	E
VCCINT Voltage	MP
Process	Maximum

Power Summary	
Total	76.366 W
Static	9.680 W
Dynamic	66.686 W

ge	Min Voltage	Max Voltage	Step Load %	Static (A)	Dynamic (A)	Total (A)
0.800	0.775	0.825	33.00 %	0.022	0.000	0.022
1.500	1.455	1.545	33.00 %	0.833	0.014	0.846
0.800	0.775	0.825	33.00 %	0.347	0.000	0.347
0.800	0.775	0.825	33.00 %	0.036	0.000	0.036
0.800	0.775	0.825	25.00 %	2.071	0.008	2.080
0.800	0.775	0.825	33.00 %	0.011	0.000	0.011

Power Design Tab (Cont.)

Power Supply Design Table

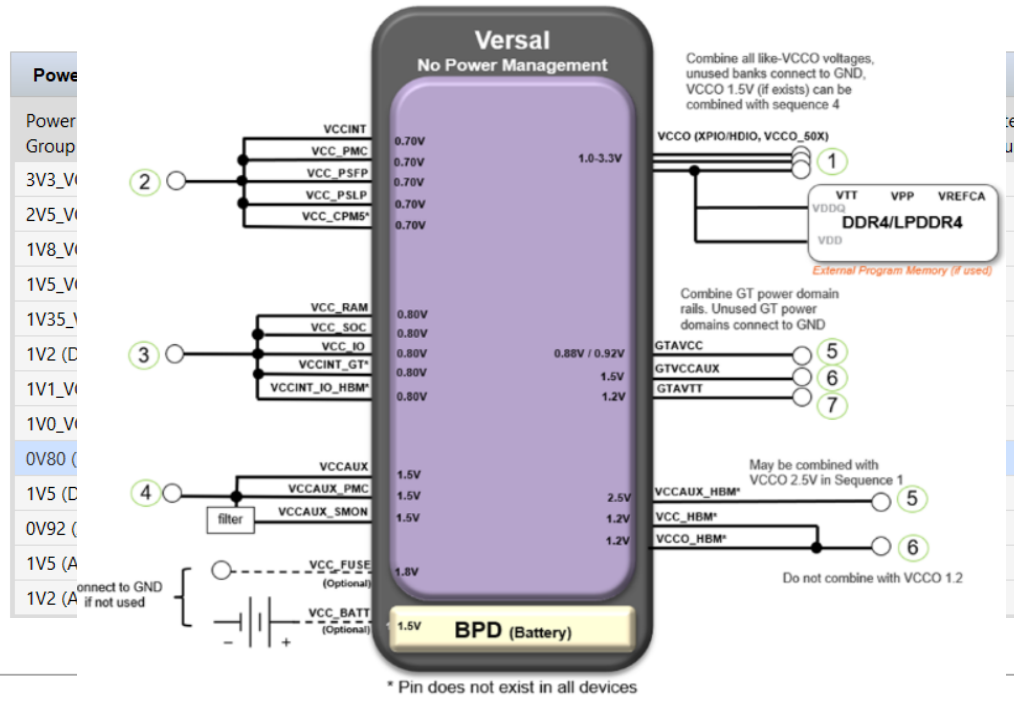
- Grouping of rails by group name
- Power sequence
- Combined power rail current requirements & tolerances
- Voltage regulator current capability entry

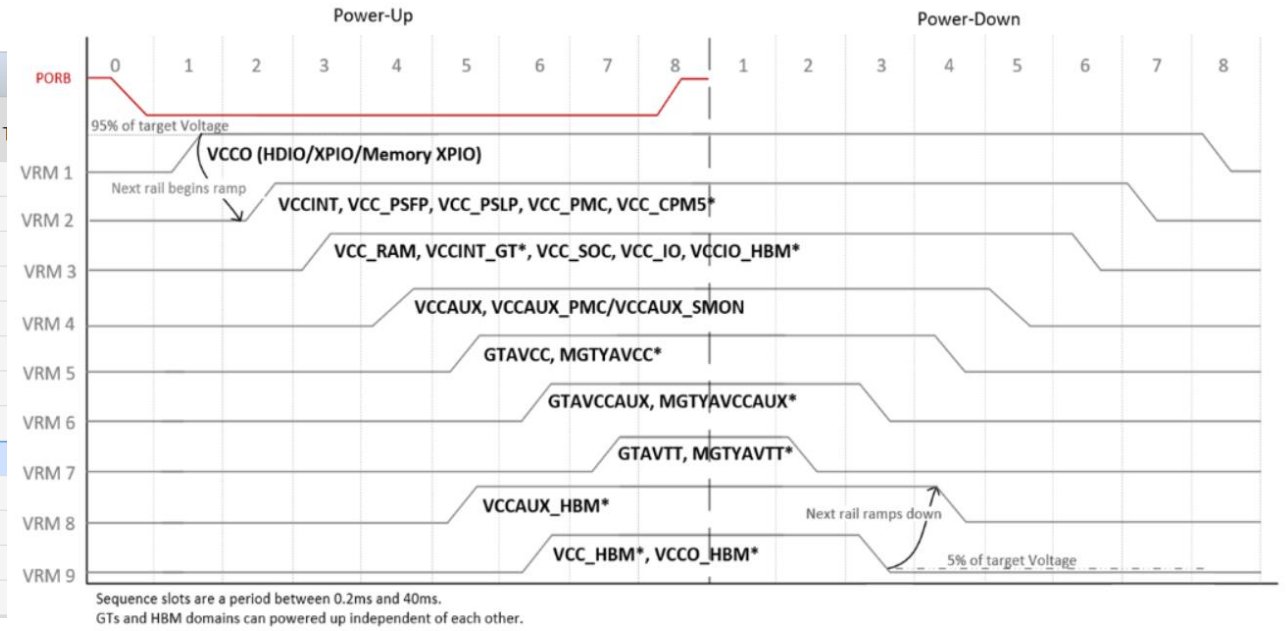
Decoupling Capacitor Details

- Dynamic decoupling recommendations
- XQ and XC temperature ranges
- Capacitor P/Ns, values, and placement techniques
- ESR, ESL information to aid alternative capacitor selection

Sequencing/Rail Diagrams

- Power-up & down sequencing by rail grouping
- Timing and ramping requirements
- POR_B pull down timings
- Conditions for next rail power up



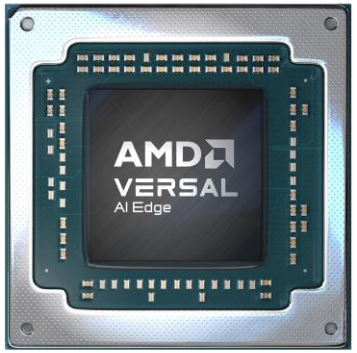


Summary

- Versal™ architecture's power improvements and new tools make power delivery more convenient
- Understanding the power design tab in PDM can ensure a successful power delivery design
- Download Power Design Manager from the AMD power delivery webpage www.amd.com/power

- Import designs from XPE to PDM if still using XPE
- Utilize the export .xml feature and submit your file to AMD's power delivery partners

- Example of Voltage regulator design for V_{CCINT}
- V_{CCINT} powers the programmable logic, AI Engines, and other internal blocks in Versal™ devices
- When using Minimum Rails consolidation, we combine V_{CCINT} with other like voltages
  - VCCINT, VCC_RAM, VCC_PSFP, VCC_PSLP, VCC_PMC
  - Power Supply Design table combines the current requirements of all rails



Endnotes

VER-043

Based on an AMD dynamic performance per watt comparison of the 7nm -2L Versal™ device architecture and the 16nm -2 Virtex UltraScale+ device architecture in February 2024, using the production-stage versions of the AMD Power Design Manager 2023.2. tool and XPE 2023.1.2 tool to measure the power per watt of the programmable logic, DSP Engines, Block RAM, UltraRAM, gigabit transceivers, and DDR memory controllers. Results may vary based on a variety of factors, including customer application design, implementation, and data inputs.

Introduction to Core Power Supply

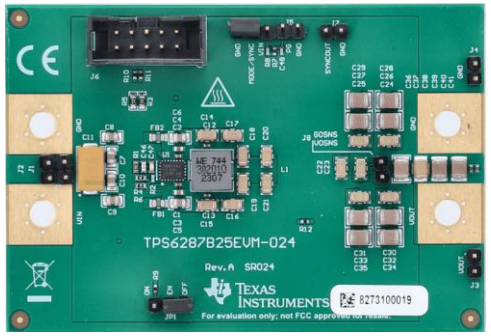
This webinar will help you

- Use AMD Power Design Manager tool and export data to start your power journey
- Choose the right TI part and Wuerth Elektronik inductor (passive) to maximise efficiency and minimize passive components in your high power density applications
- Use TI‘s WEBENCH® and RED EXPERT online tools to simulate the performance of your circuit

Some featured products

AMD *Versal™ AI Edge Series*

Texas Instruments TPS6287B25, 25-A Step-Down Converter



Wuerth Elektronik 74435030010 Series Ultra-Low Loss Shielded Power Inductors

AMD Texas Instruments WÜRTH ELEKTRONIK

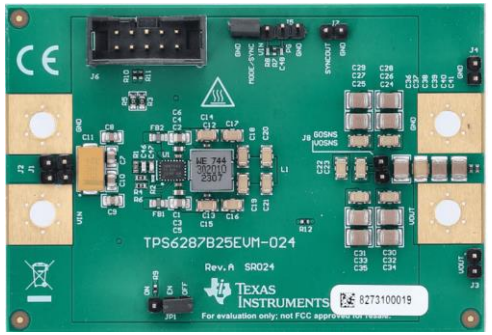
Agenda

- How to interpret AC + DC specification of a processor
- Maintaining a high voltage accuracy at DC and during load transients.
- Design Example using the latest VE2302 applications
- How to optimize the load transient performance

Some featured products

AMD *Versal*™ *AI Edge Series*

Texas Instruments TPS6287B25, 25-A Step-Down Converter



Wuerth Elektronik 74435030010 Series Ultra-Low Loss Shielded Power Inductors

Power Design Manager Output data for VE2302

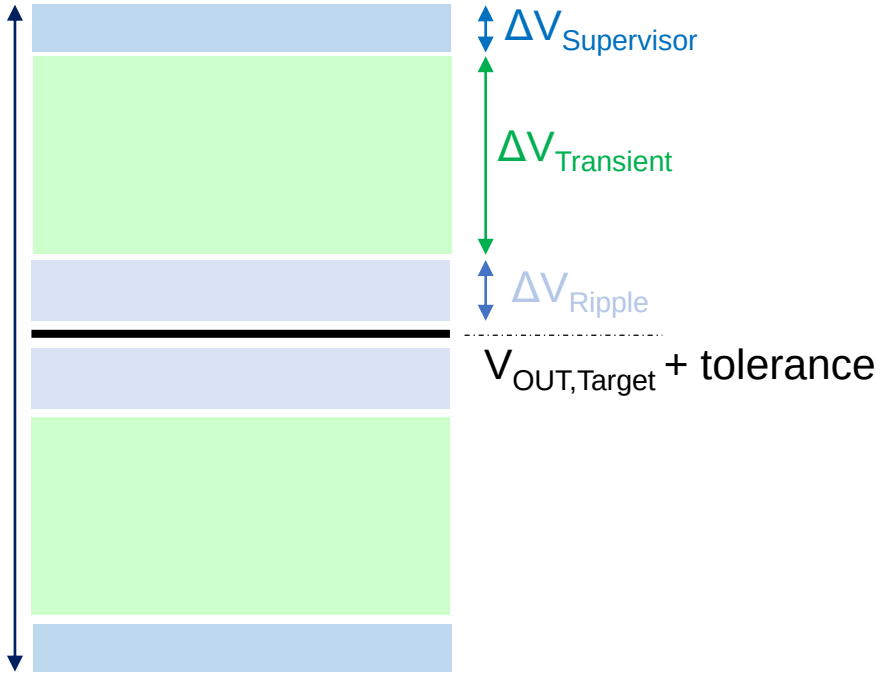
Rail Name	Voltage	DC Spec.	AC Spec.	Current	Step	Sequence #
VCCINT/VCC_PMC/VCC_PSFP/ VCCPSLP/VCC_RAM/VCC_SOC/ VCC_IO	0.8 V	±1%	±17mV	39 A	33%	2
VCCO	1.5 V	±1%	±5%	3 A	100%	1
VCCAUX/VCCAUX_PMC/ VCCAUX_SMON	1.5 V	±1%	10mVpp	1.1 A	100%	3
GTAVCC	0.88 V	±2%	10mVpp	0.7 A	70%	4
GTAVTT	1.2 V	±2%	10mVpp	1.3 A	70%	6
GTAVCCAUX	1.5 V	±2%	10mVpp	0.05 A	70%	5

$\Delta V_{OUT} = 34\text{mVpp}$

AC spec

Recommended

$C_{OUT} = 1065\ \mu\text{F}$



- Load Step Currents
- Min/Max Voltage Requirements
- Ripple Requirements
- Voltage for External Supervisor required?
- Max Current (DC and peak)
- DC accuracy (with remote sense)

Load transient is largest contributor to output voltage accuracy → drives output capacitance requirement

AMD Texas Instruments Würth Elektronik

TPS62 87Bx

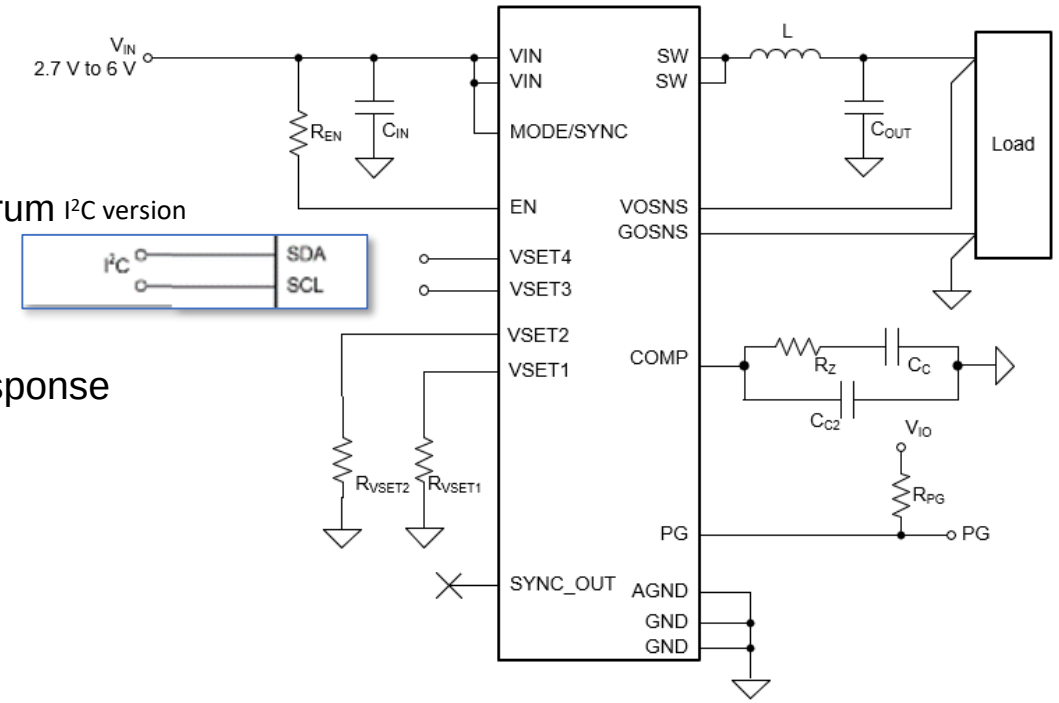
$6V_{IN}$, 10A to 25A Buck Converter with Remote Sense, Stackable

Features

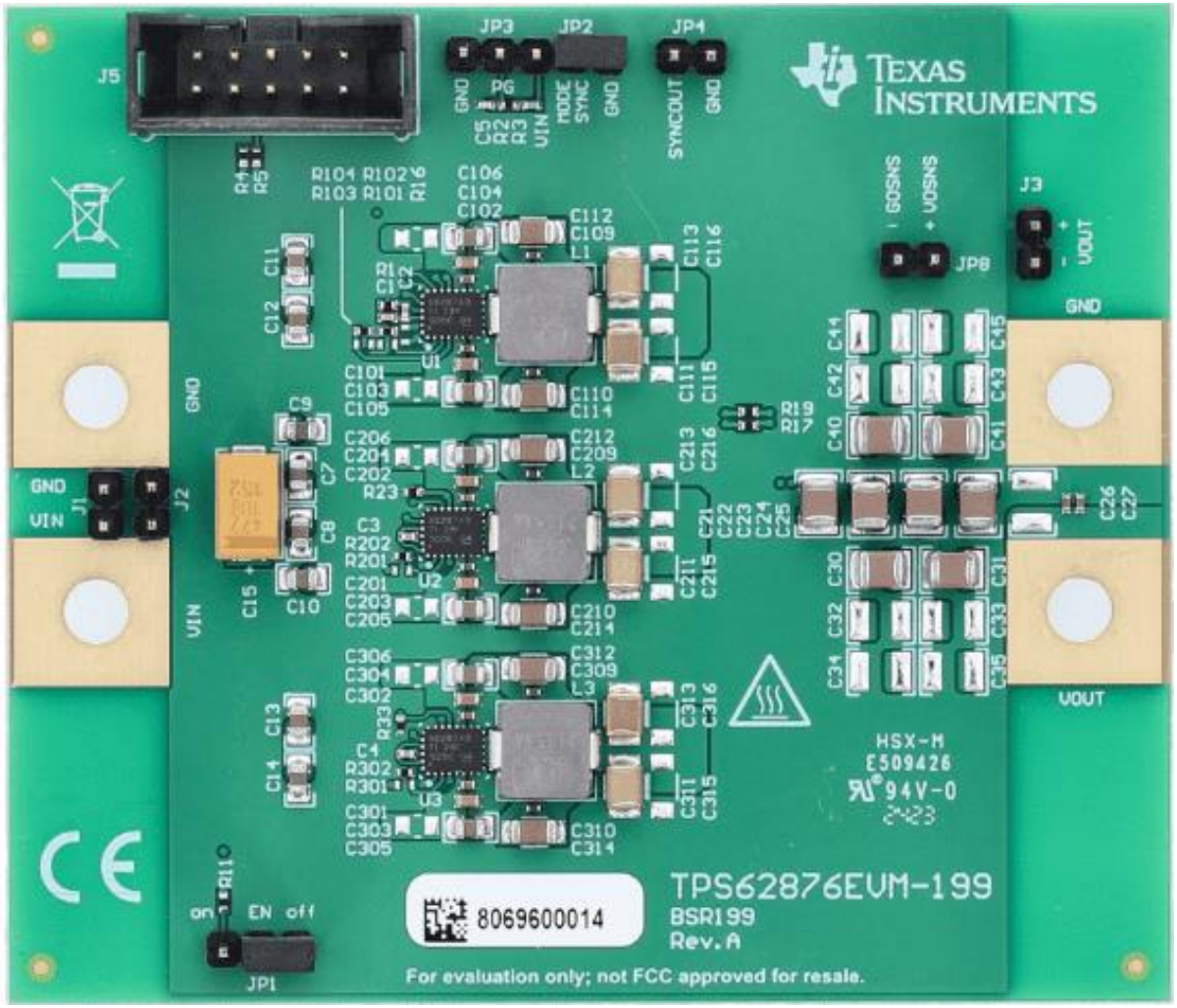
- 2.7V to 6.0V input voltage
- Low $R_{DS(ON)}$ Switches 2.6mΩ / 1.5mΩ
- Output voltage accuracy: ±0.8%
- Family with 10A, 15A, 20A, 25A (stackable to higher currents)
- **I²C version:** 2 x 16 V_{OUT} startup voltage options selectable:
  - Low output voltage range 0.4V – 0.775V in 25 mV steps
  - High output voltage range 0.8V – 1.55V in 50 mV steps
  - Dynamic Voltage Scaling in 1.25mV – 5mV steps
  - Temperature Warning, Voltage Monitoring, SoftStart, Spread Spectrum I²C version
- **V_{SET} version:** 64 selectable V_{OUT} options
  - 0.4V – 1.675V (in 25mV steps)
- Remote differential sense at load for high accuracy & fast transient response
- Droop compensation (optional)
- 1.5MHz switching frequency
- Forced-PWM or Automatic Power Save Mode
- Functional Safety Capable
- 3.05 x 4.05mm QFN

Benefits

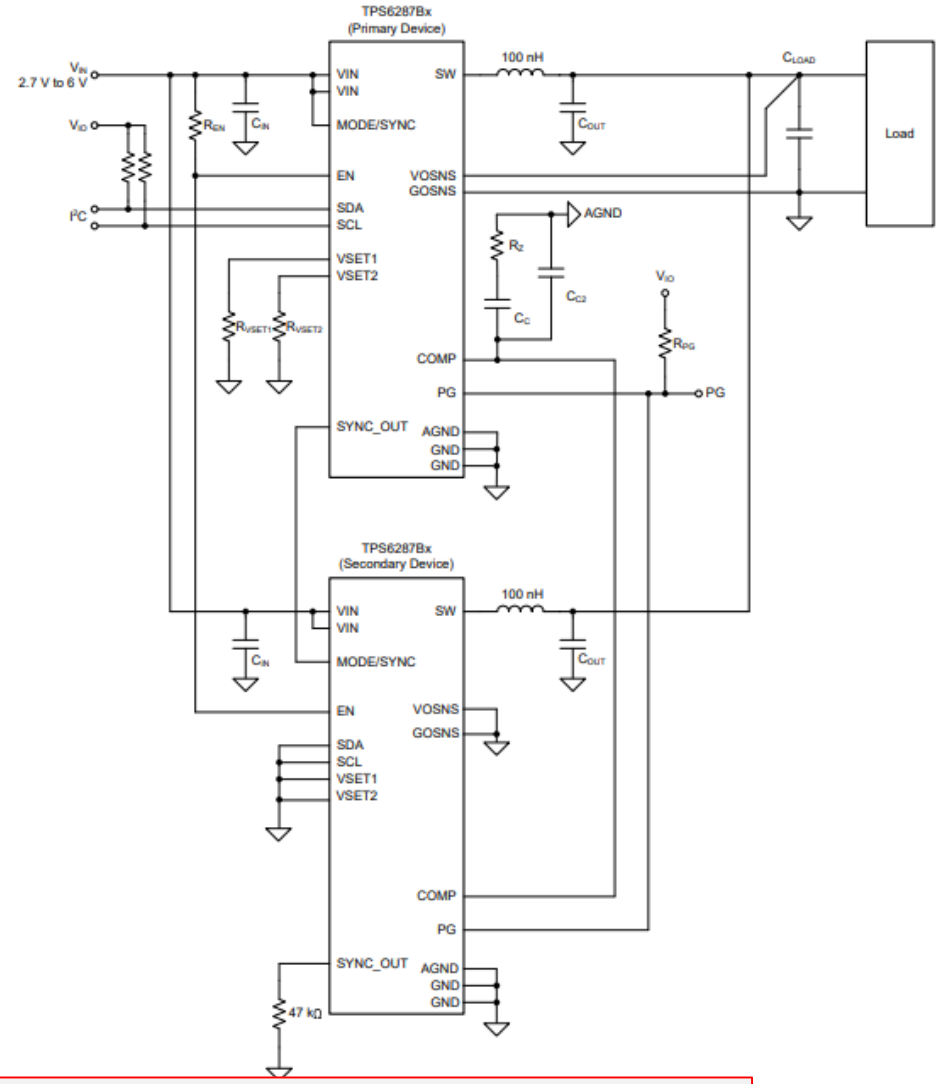
- High output current with small solution size
- Remote sense for Core supply
- Stackability to allow for smaller inductors and better heat distribution
- Dynamic adaptation to processor loads, adjustable output voltage



Output can be paralleled to support greater load currents



To optimize design
https://webench.ti.com/power-designer/



75 A EVM with 3x TPS62876-Q1

AMD Texas Instruments Würth Elektronik

WEBENCH Power Designer Inputs

Customize TPS6287B25LA0WRZV - 2.7V-6V to .75V @ 19.5A

Input: DC 4.5 V - 5.5 V Output: 0.8 V at 19.5 A Temp: 30 °C Change

SELECT | CUSTOMIZE | SIMULATE | EXPORT

Summary

Efficiency: 89.7%
BOM Cost: $4.17
Footprint: 267 mm²

CHANGE OPTIMIZATION

Configuration Options

Mode of Operation: FPWM

Custom Sync Frequency

Sync Frequency: 1.5 MHz (1.3 - 1.8)

Asynchronous Mode For Better Transi...

Output Voltage Range: 0b10: 0.4V to 1.675V

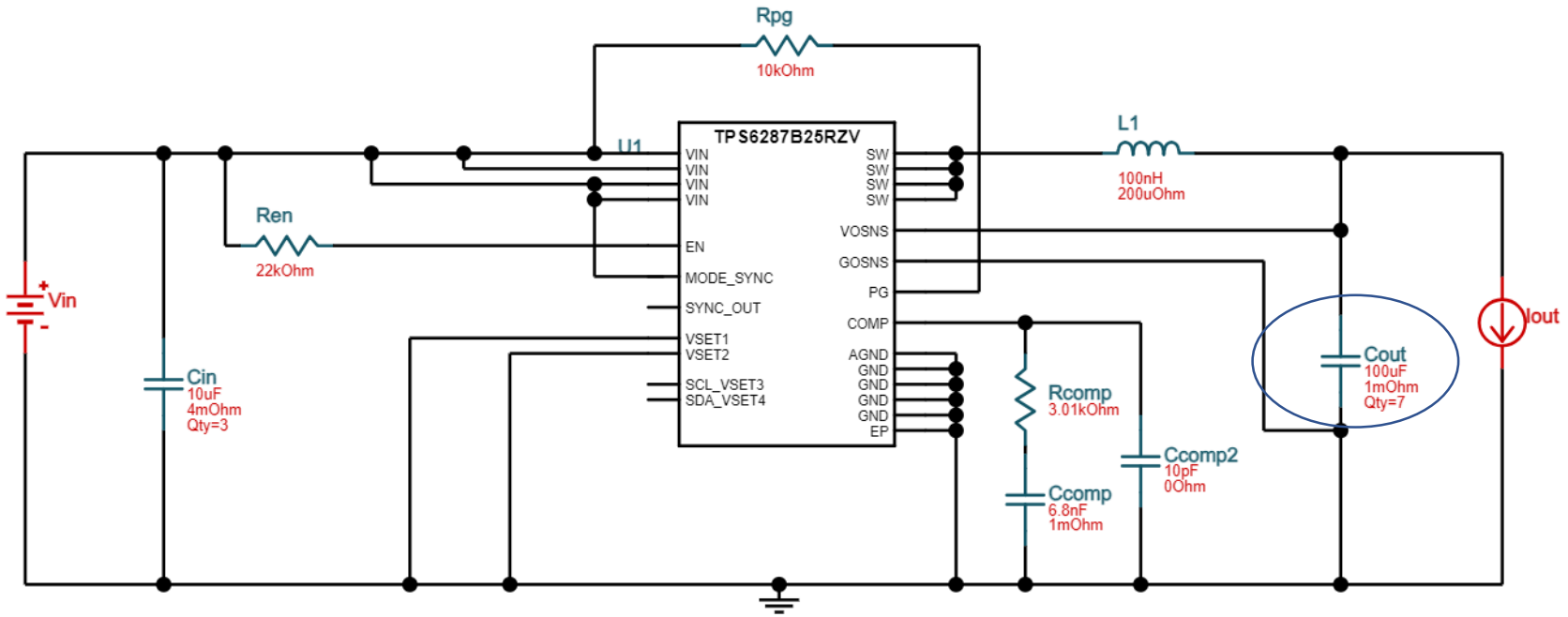
Default Output Voltage: Custom

Output Voltage Tolerance: 3 % (1 - 10)

REDESIGN

SCHEMATIC | BILL OF MATERIALS

Click a component to find out more information or select an alternate part.



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SELECT | CUSTOMIZE | SIMULATE | EXPORT

Summary

Efficiency: 89.7%
BOM Cost: $4.68
Footprint: 311 mm²

CHANGE OPTIMIZATION

Configuration Options

Mode of Operation: FPWM

Custom Sync Frequency

Sync Frequency: 1.5 MHz (1.3 - 1.8)

Asynchronous Mode For Better Transi...

Output Voltage Range: 0b10: 0.4V to 1.675V

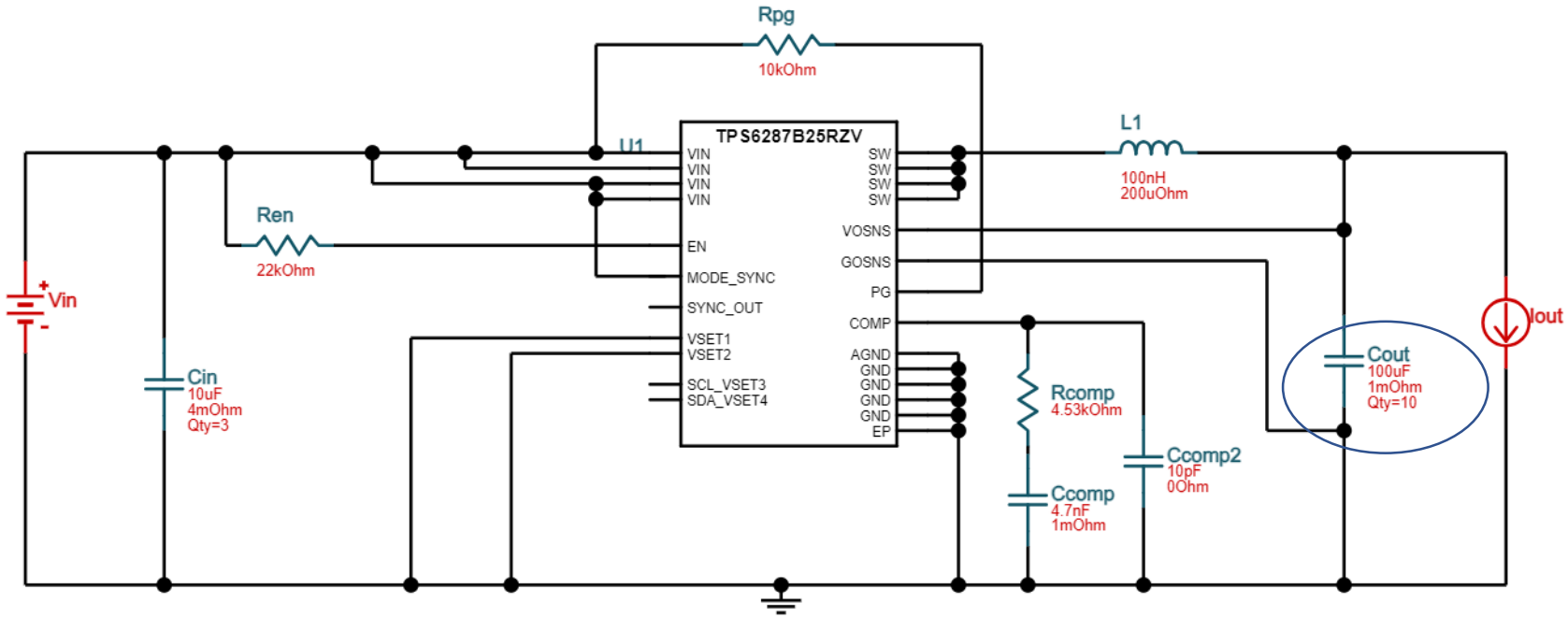
Default Output Voltage: Custom

Output Voltage Tolerance: 2 % (1 - 10)

REDESIGN

SCHEMATIC | BILL OF MATERIALS

Click a component to find out more information or select an alternate part.



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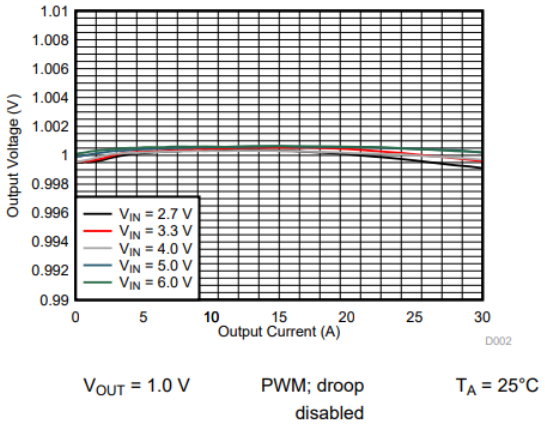
Load Transient : ~20% peak to peak improvement



V_{OUT} = 1.0 V PWM; droop disabled T_A = 25°C

Figure 9-12. Output Voltage Versus Output Current

Droop disabled

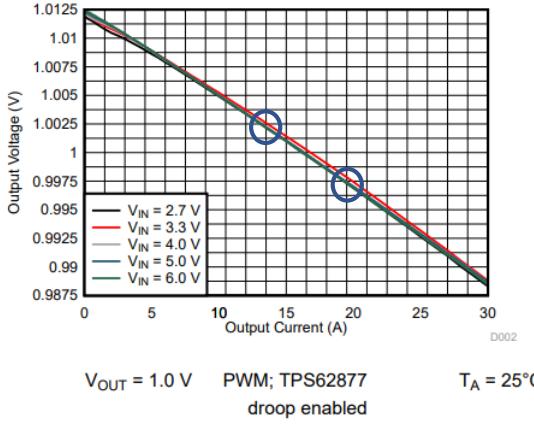
$$\Delta V_{OUT} = 34\ mVpp$$

AC+DC spec

$$C_{OUT} = 2*330+3*100+2*47+10+1\ \mu F$$

= 1065 uF

Recommended



V_{OUT} = 1.0 V PWM; TPS62877 droop enabled T_A = 25°C

Figure 9-13. Output Voltage Versus Output Current

Droop enabled

$\Delta V_{OUT} = 33.3mV\ peak\ to\ peak$

TI EVM

Load Step 26A↔39A

200A/us, Vout=0.80V

$\Delta V_{OUT} = 25.8mV\ peak\ to\ peak$

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Load Transient : ~-40% output capacitance reduction

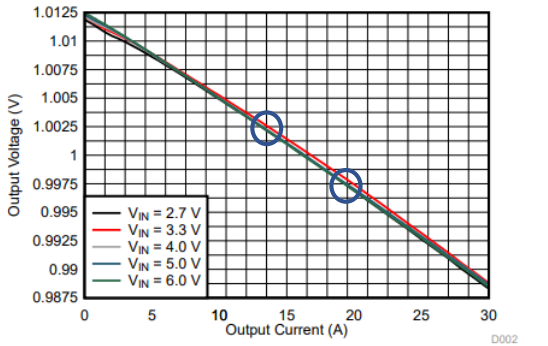
$\Delta V_{OUT} = 34\ mVpp$

AC+DC spec

C_{OUT} = 4*100+4*47

+10+1µF

= 599 uF Recommended



V_{OUT} = 1.0 V PWM; TPS62877 droop enabled T_A = 25°C

Figure 9-13. Output Voltage Versus Output Current

Droop enabled

<u>TI EVM</u>

<u>Load Step 26A↔39A</u>

<u>200A/us, Vout=0.80V</u>

$\Delta V_{OUT} = 30.7mV\ peak\ to\ peak$

WEBENCH Power Designer Inputs

Export Design Report

Customize TPS6287B25LA0WRZV - 4.5V-5.5V to .80V @ 19.5A

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REDESIGN

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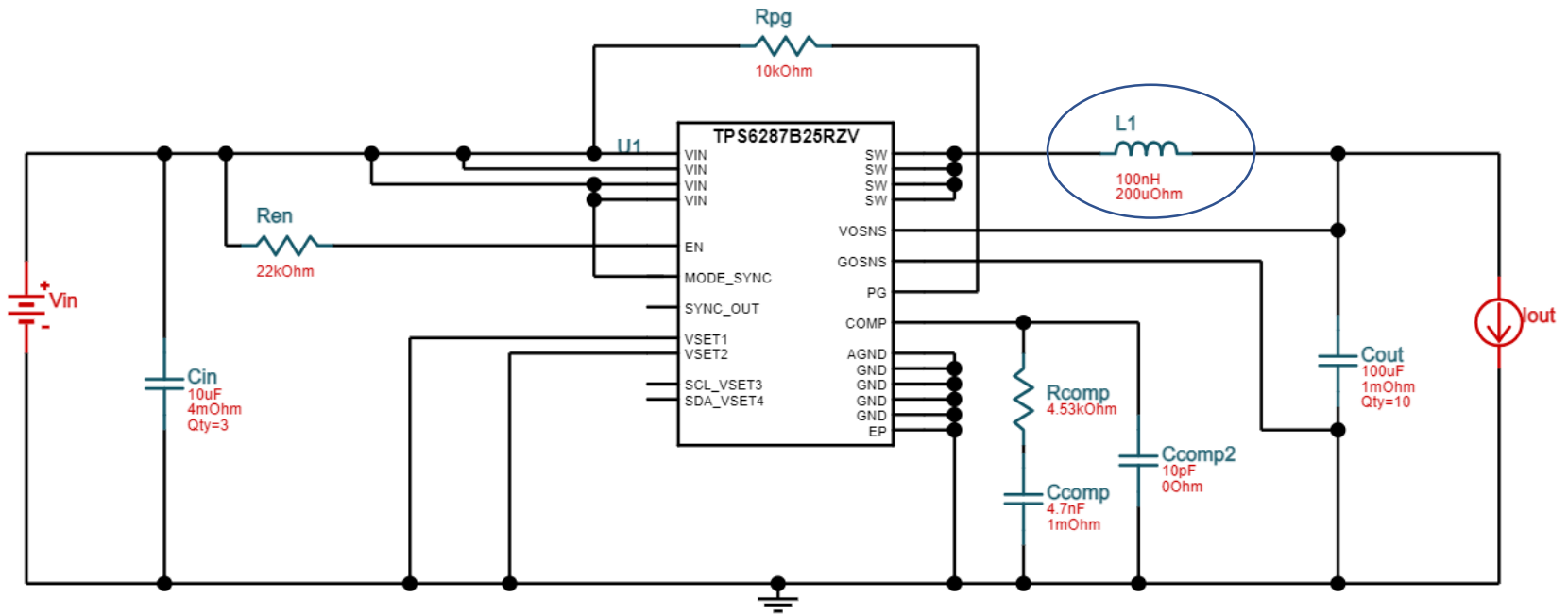

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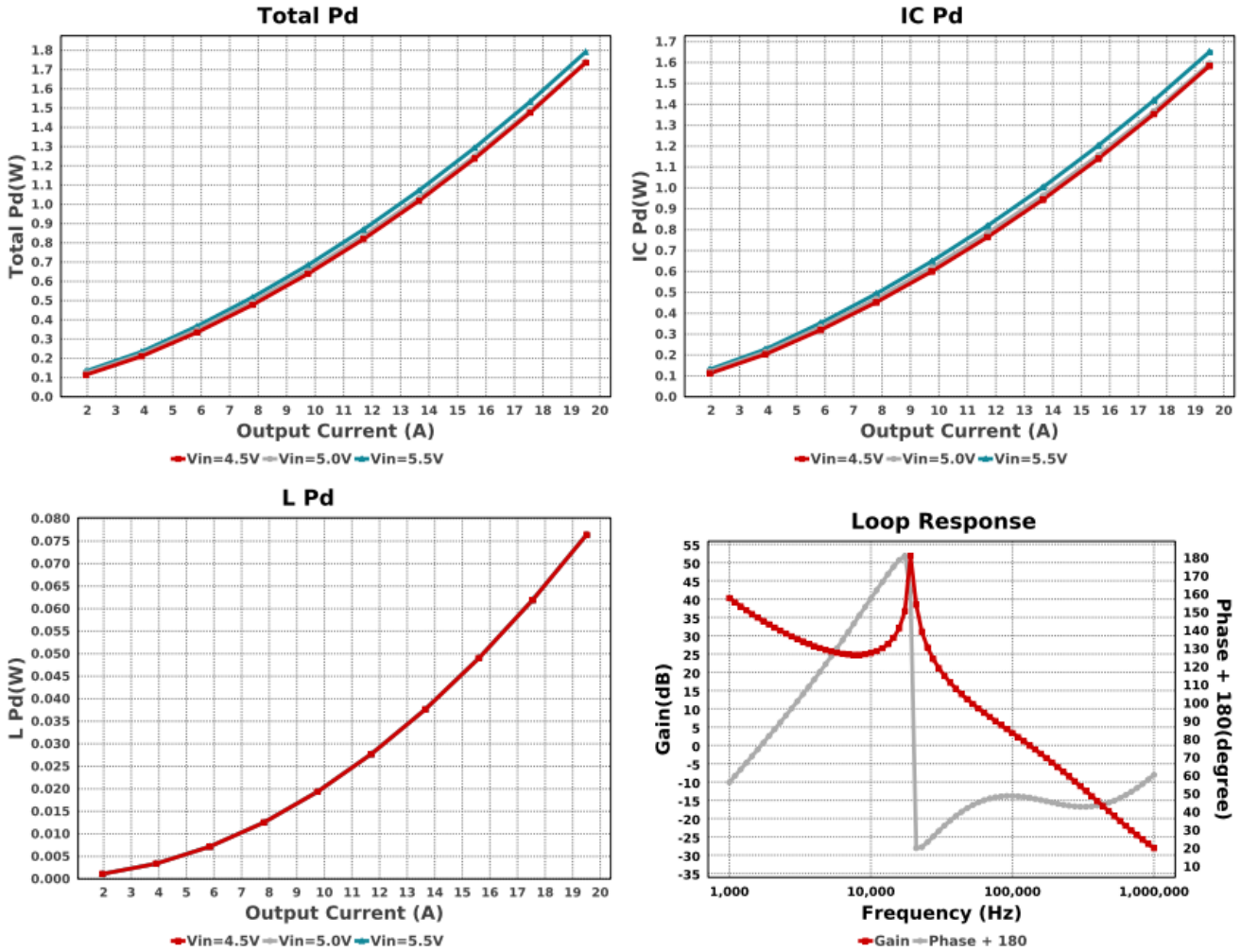
WEBENCH Power Designer Outputs

Design Report



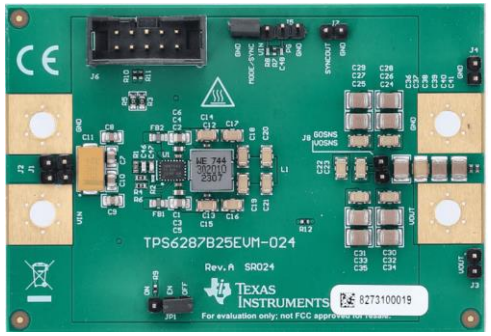
Summary

- The Main contributor for the use a large output capacitance bank is the load requirements of your processor
- Webench can help the bring up of your design by tuning your load transient requirements
- Stacking (paralleling), remote sense and tight DC accuracy are important for processor power
- Features such as Droop compensation can help improve your load transient performance and reduce your output capacitance up to 40%

Some featured products

AMD *Versal™ AI Edge Series*

Texas Instruments TPS6287B25, 25-A Step-Down Converter



Wuerth Elektronik
74435030010 Series Ultra-Low Loss Shielded Power Inductors

AMD TEXAS INSTRUMENTS WÜRTH ELEKTRONIK

Low entry access to electronics design with REDEXPERT®

Navigate by order code

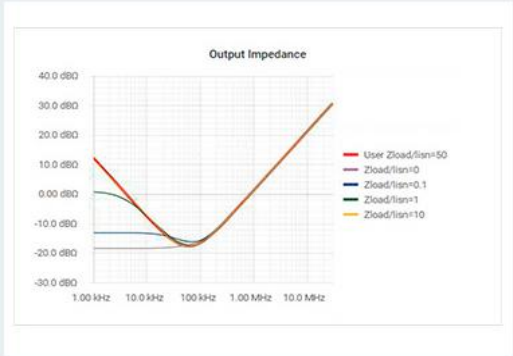
Enter at least first 4 characters

Design Tools

- EMI Filter Designer
- MagI³C Power Module Designer
- Resonance Tank Calculation for Wireless Power
- Filter Circuits
- DC/DC Converter
- Flyback Transformer
- AC/DC Converter
- Wireless Connectivity and Sensors

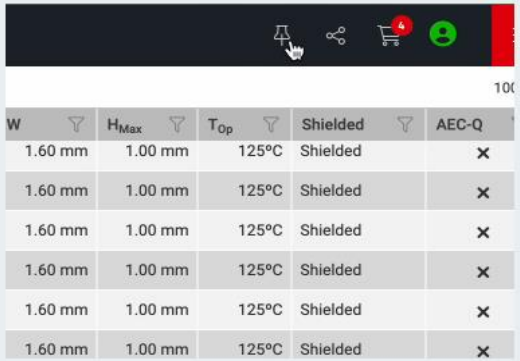
Product selection

- EMC Components
- Power Inductors and Magnetics
- MagI³C Power Products
- Signal & Communications
- Capacitors & Resistors
- Optoelectronics
- Quartz Crystals & Oscillators
- EMC Shielding & Grounding



Filter Designer shows the output impedance for many load impedances

Our EMI Filter Designer shows the output impedance for a variety of different load / LISN impedances from 0 up to 10 Ohms.



W	H_{Max}	T_{Op}	Shielded	AEC-Q
1.60 mm	1.00 mm	125°C	Shielded	✕
1.60 mm	1.00 mm	125°C	Shielded	✕
1.60 mm	1.00 mm	125°C	Shielded	✕
1.60 mm	1.00 mm	125°C	Shielded	✕
1.60 mm	1.00 mm	125°C	Shielded	✕
1.60 mm	1.00 mm	125°C	Shielded	✕

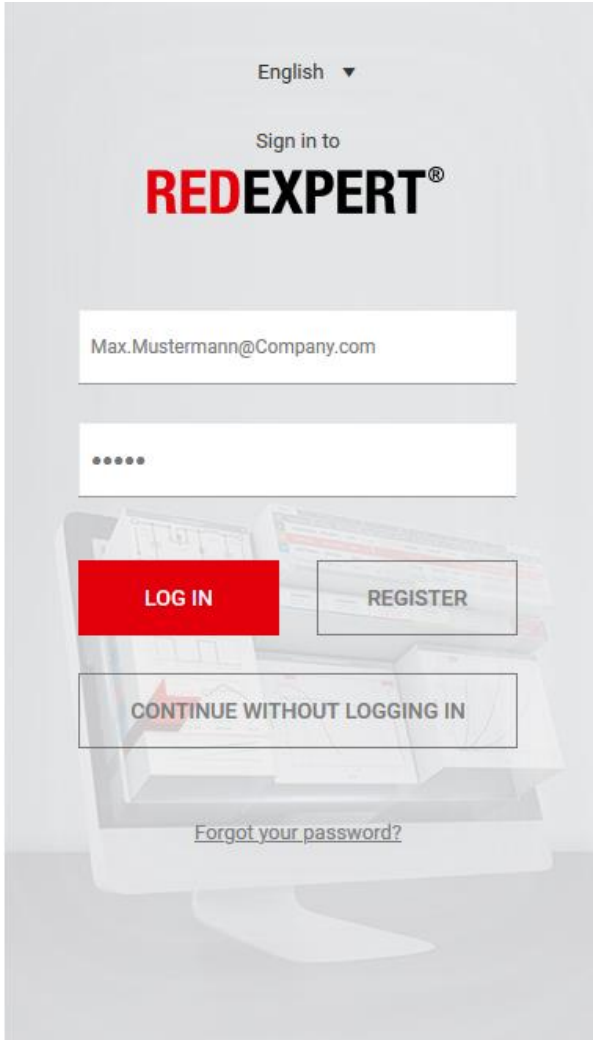
Bookmark the actual module

Add the actual module to your favorites (Login required), to have quick access directly on the REDEXPERT start page. Warning: It might save you time!

Register / Log In

Or continue without logging in

- Registration is not mandatory
- All basic functions are available without logging in
- Registration, use and enjoyment are totally **free of charge**
- A user account does have its perks:
  - Order free samples directly from the app
  - Using of sliders for advanced search queries

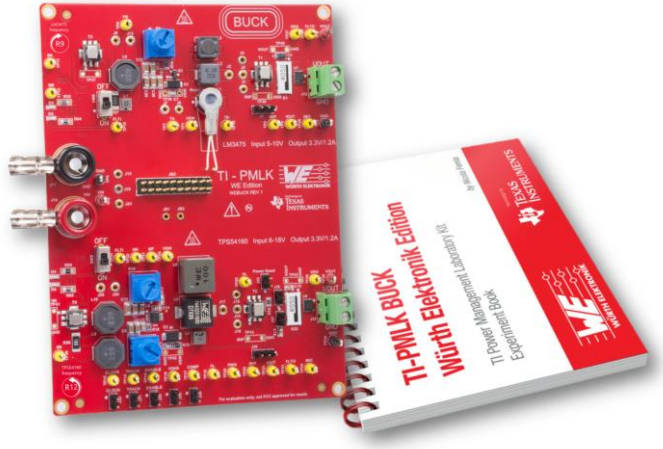


Privacy Concerns

Your personal information is stored according to GDPR rules

We need your contact information for the samples and offers only

Power Inductor Selection



https://www.we-online.com/en/components/products/DESIGNKIT_744732

Output Inductor Selection (LO)

To calculate the minimum value of the output inductor, use

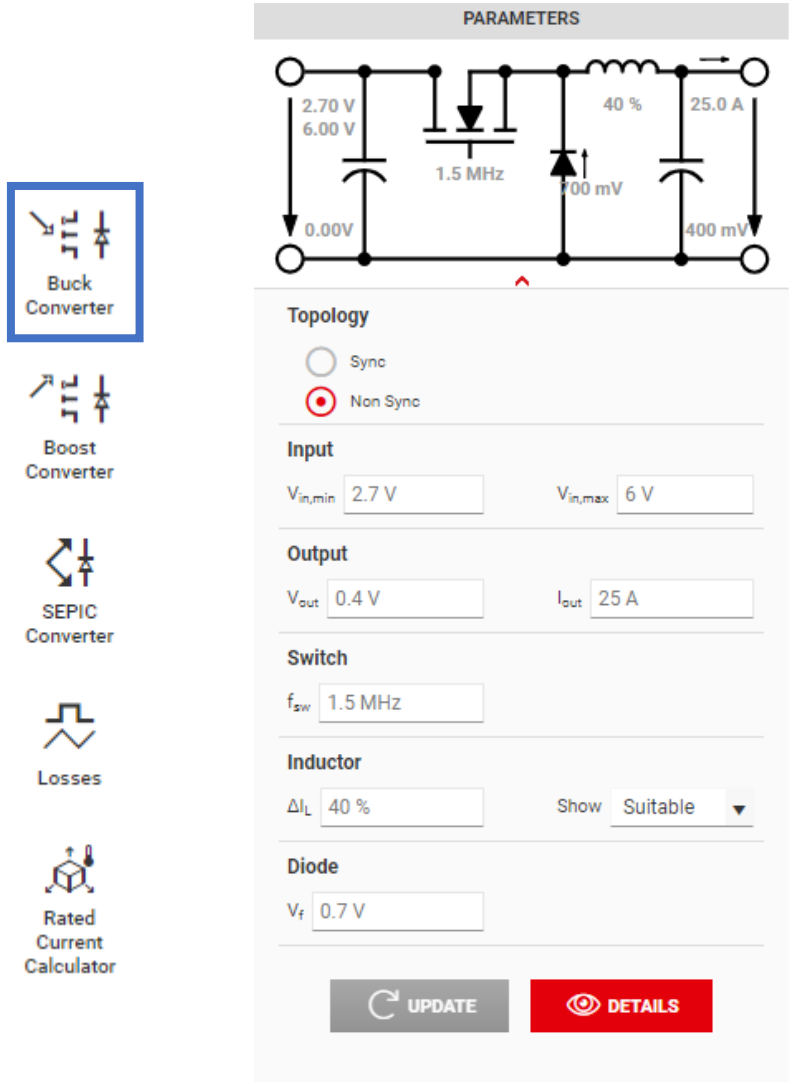
$$L_{O(min)} = \frac{V_{IN(max)} - V_{OUT}}{I_{OUT} \times K_{IND}} \times \frac{V_{OUT}}{V_{IN(max)} \times f_{sw}}$$

K_{IND} is a coefficient that represents the amount of inductor ripple current relative to the maximum output current

REDEXPERT

Power Inductor Selection

- With REDEXPERT you can select a power inductor based on you application
- It will need the following paramters of your SMPS:
  - Input / Output Voltage
  - Output Current
  - Switching Frequency
  - Ripple factor (in %)
  - Diode Voltage (Optional)



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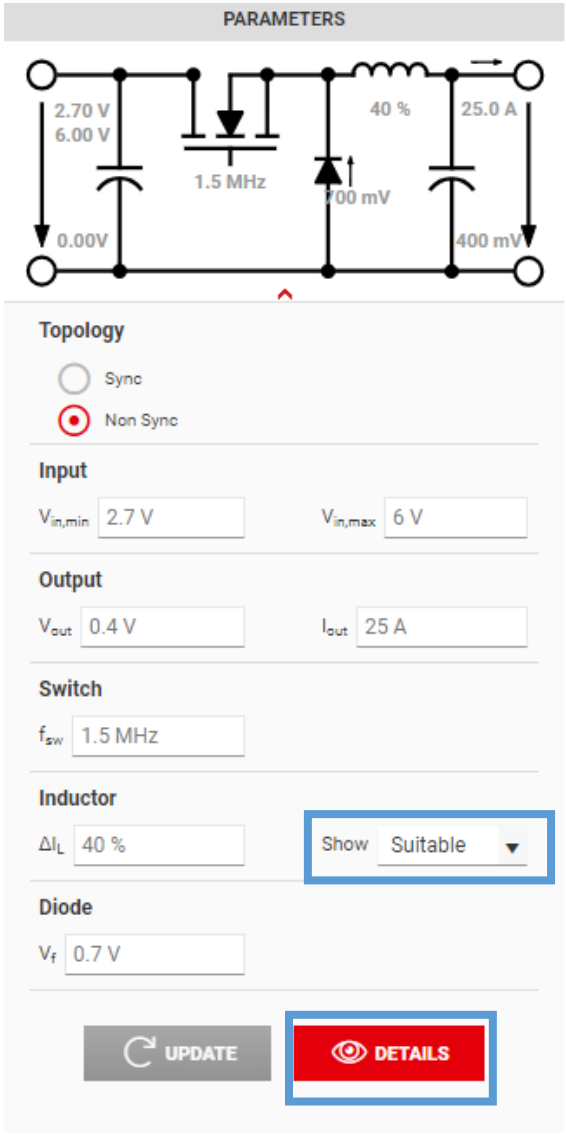
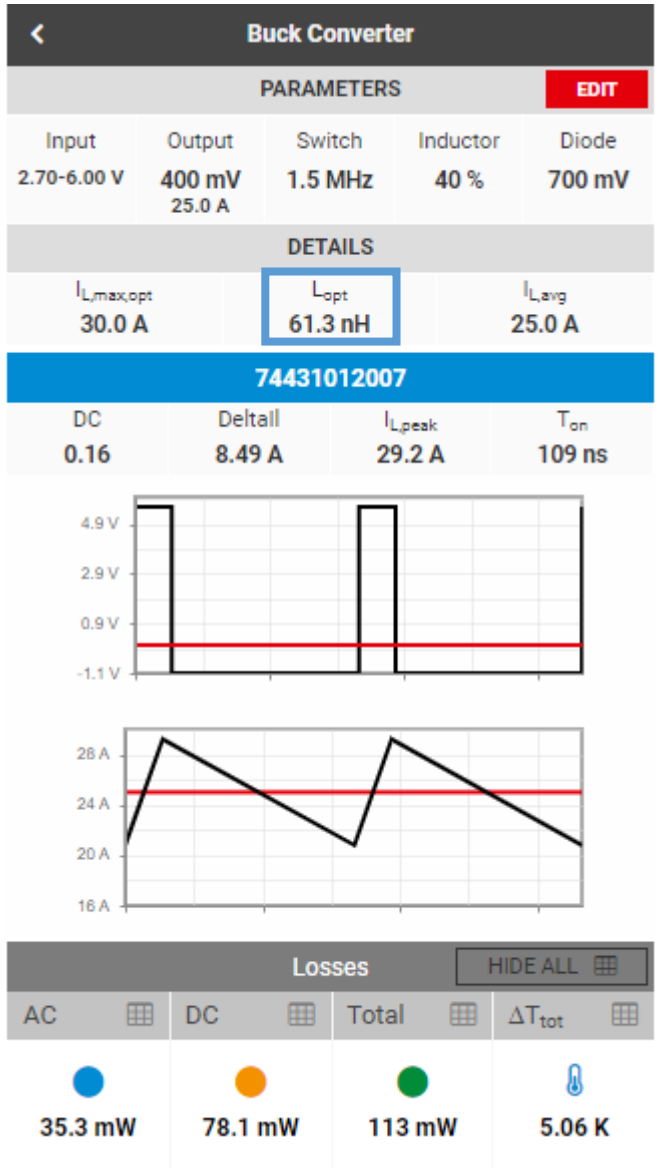
Power Inductor Selection

REDEXPERT will not only find all suitable inductors but will also calculate the expected losses and temperature rise with high accuracy

Suggestion: The „perfect“ inductance wont exist anyway, order a sample for one inductance value above and below your results





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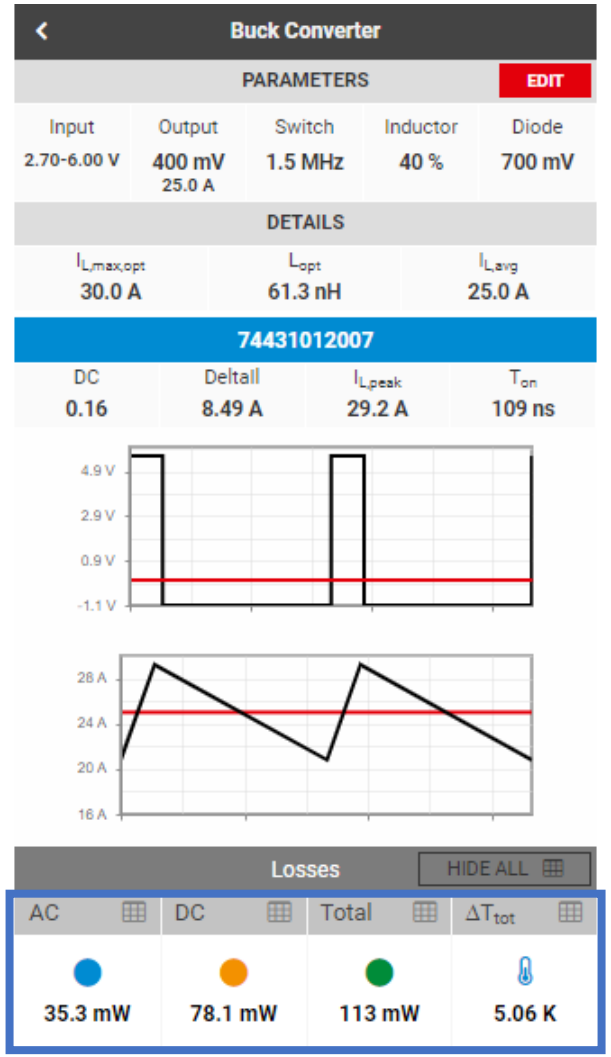
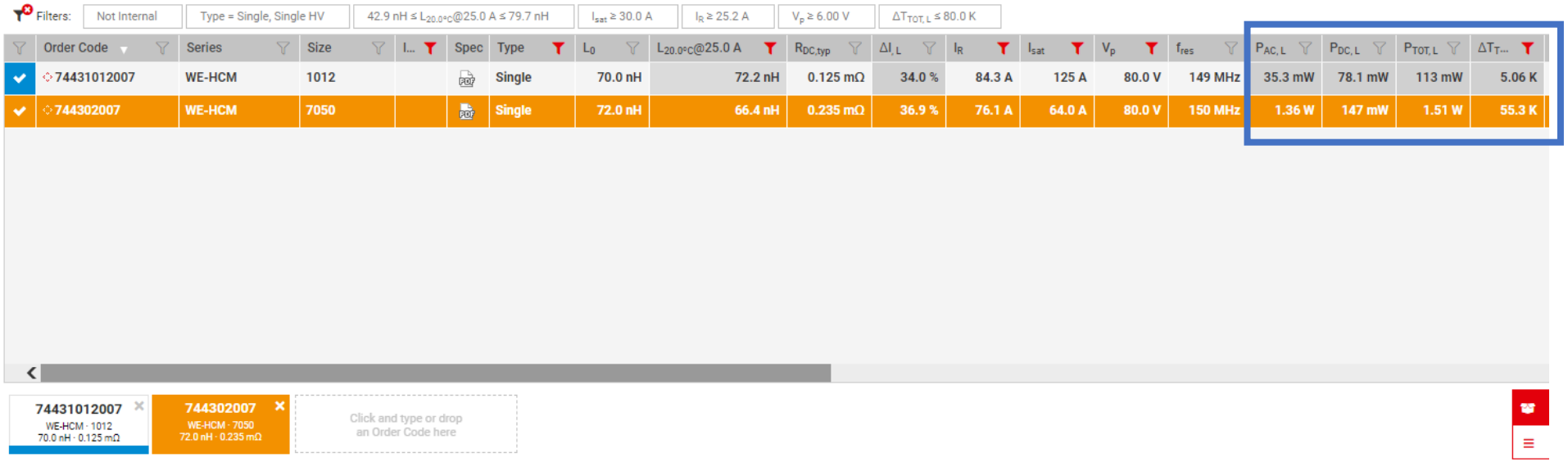
Power Inductor Selection

Losses





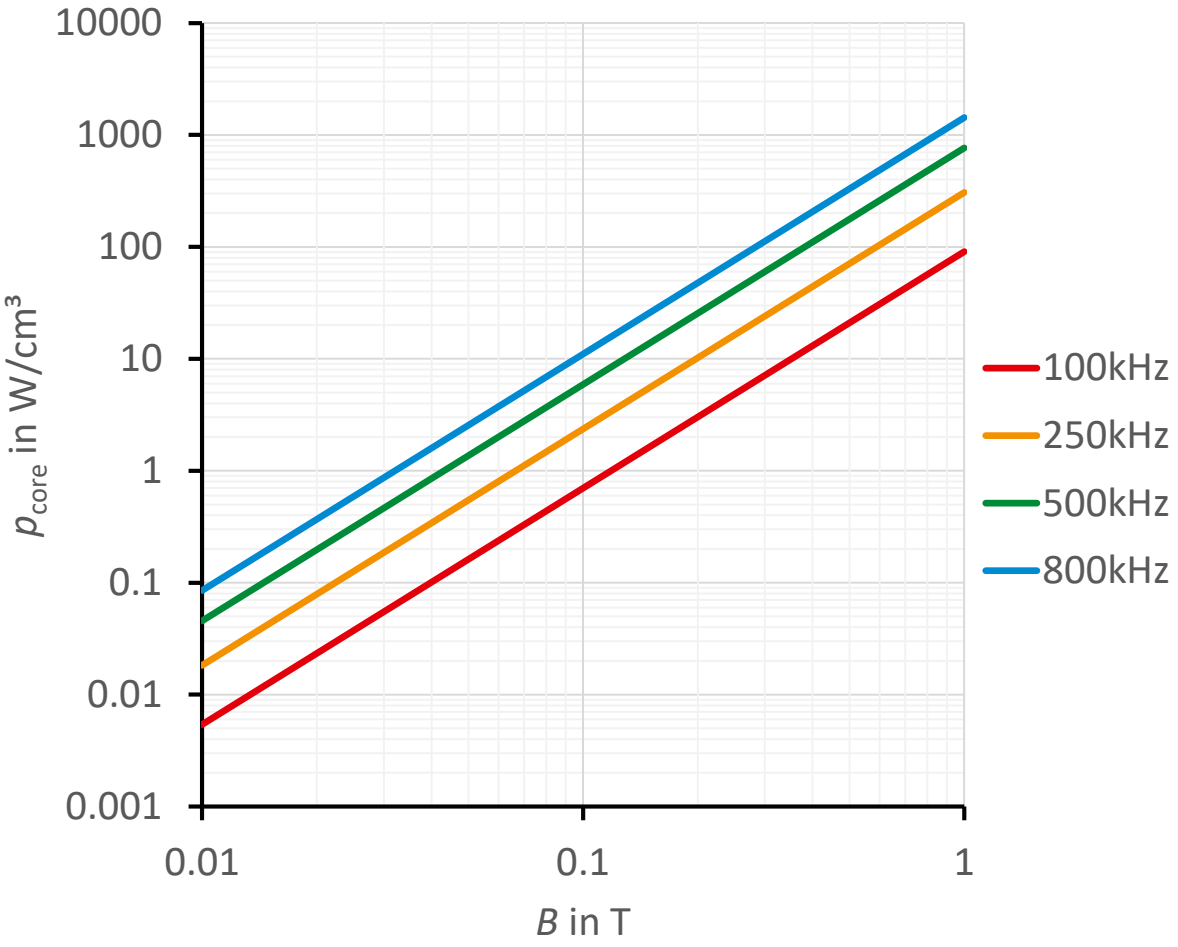
https://we-online.com/re/5qRQ42Zw

Core Losses (AC)

Steinmetz Method

- The Steinmetz Method is a formula to calculate the core losses
- It‘s based on empirical parameters, measured for toroidal core inductors
- $p_{core} = k * f^{a} * \hat{B}^{b}$

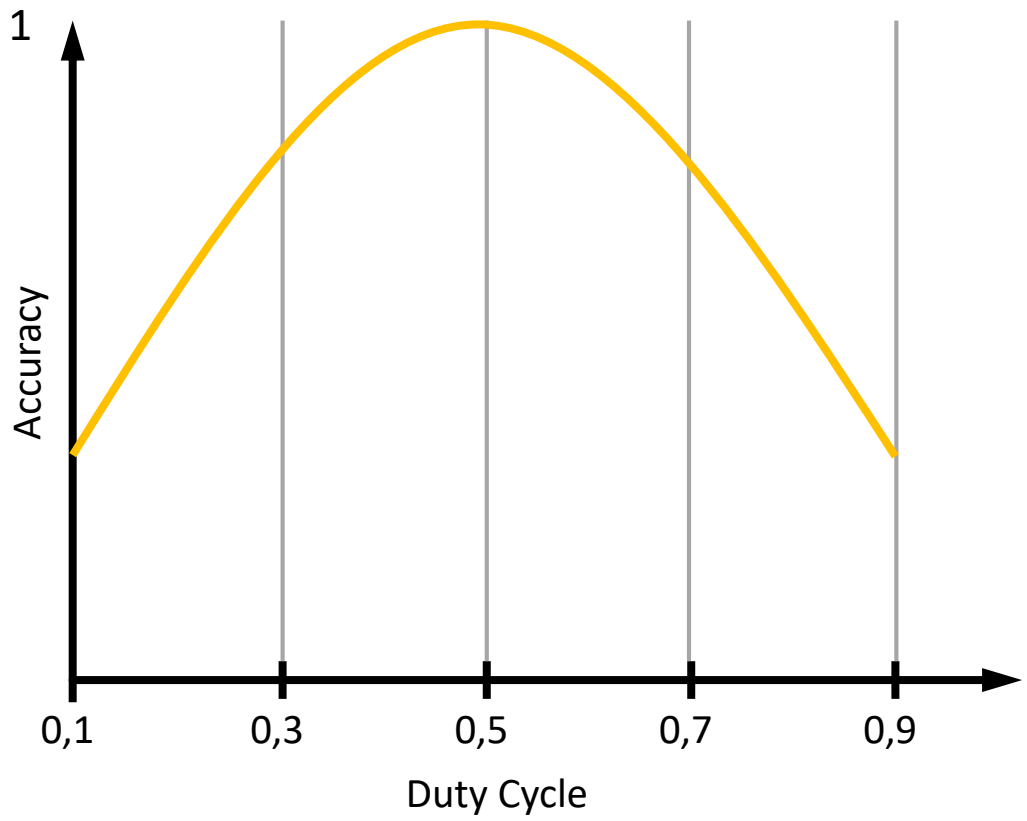
k = 7,62·10^{-14}
a = 1,325
b = 2,113



Core Losses (AC)

Steinmetz Method

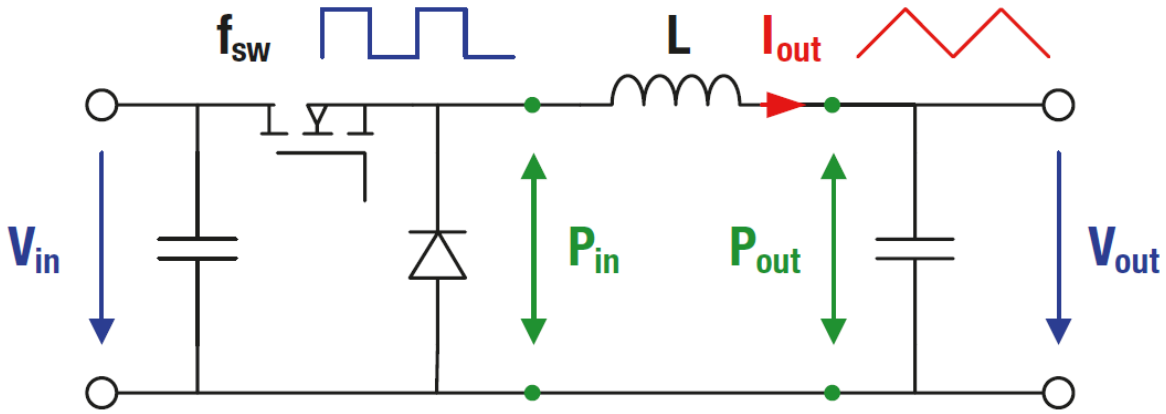
- Steinmetz Parameters are only conditionally valid for real power inductors
- The accuracy is okay for a duty Cycle of 50% but deteriorates quickly in both directions
- A modified Steinmetz Approach takes into account non-sinusoidal excitation of the core:
  - $p_{core} = k * {f_{eq}}^{a-1} * \hat{B}^b * f$
- Manufacturers have a different model to estimate core lesses

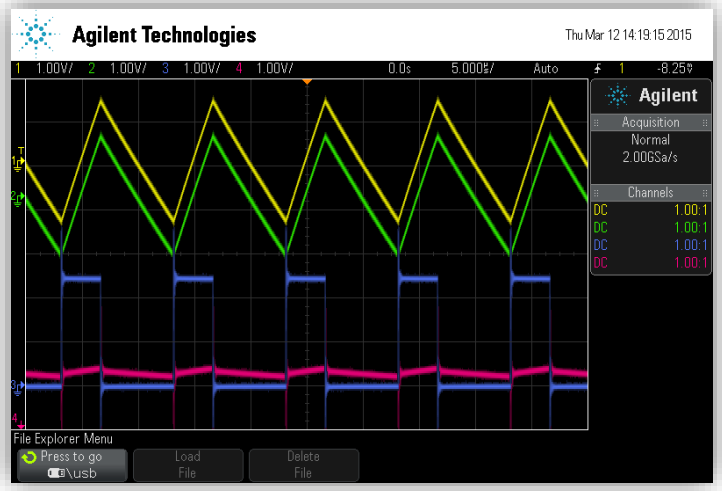


Inductor Losses

RedExpert:

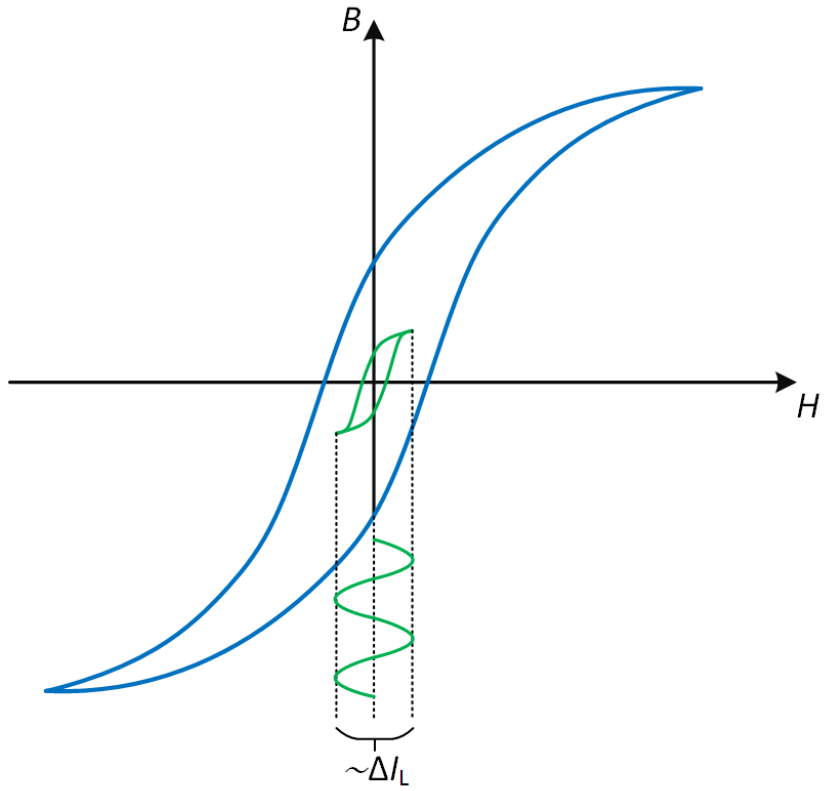
- Würth Elektronik uses specialized measurement equipment (Buck Converter + Class-D-Amplifier).
- A huge set of parameters is measured in an actual application like setting
- Losses can then be calculated quite easy
  - $P_L = P_{in} - P_{out}$
- Operating Point → **triangle** signal





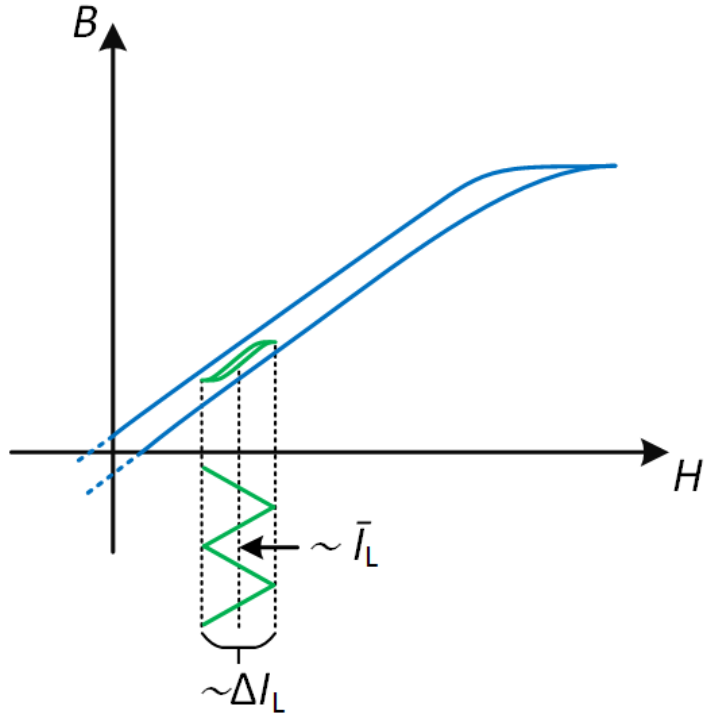
Inductor Losses

Comparison of Operating Point Conditions



Steinmetz

Sinusoidal Excitation, Core Losses only



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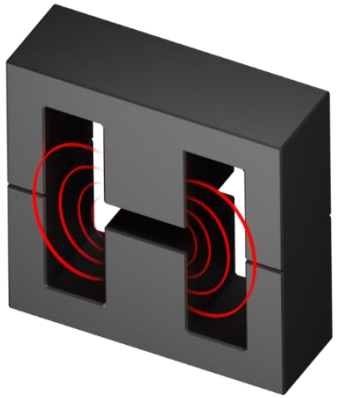
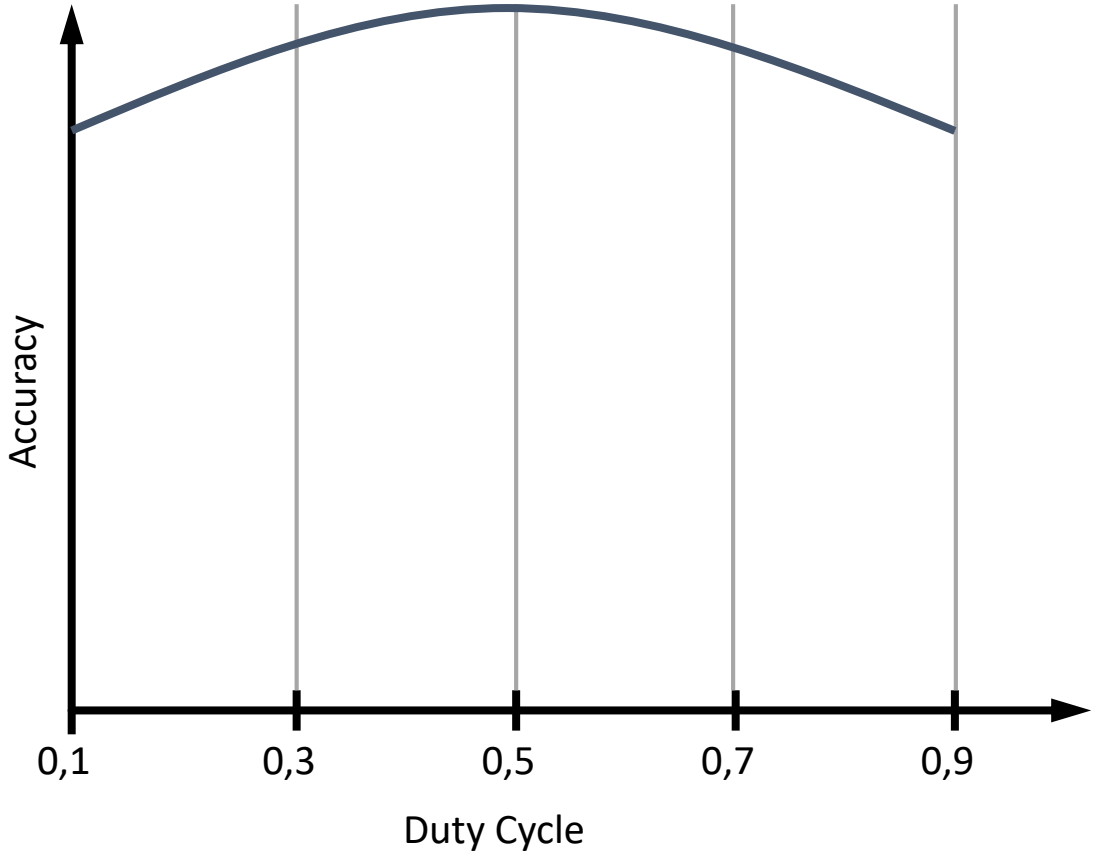
Real Operating Point, Total Losses

Inductor Losses

Accounting for

- Real Core geometry
- Stray field effects at the air gap
- Winding structure,
- Material composition,
- AC Losses in the wire





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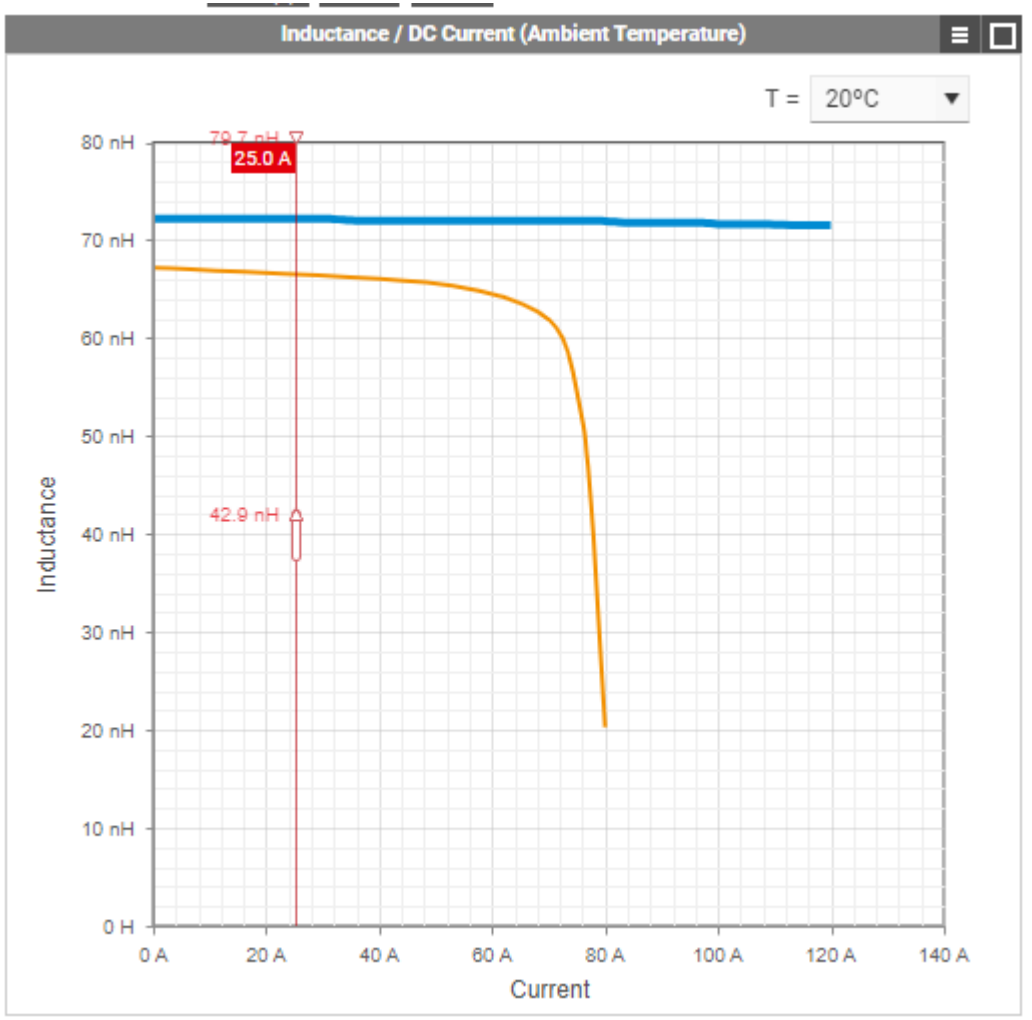
Beware the Saturation!

- RedExpert will rely on the rated inductance to calculate the ripple
- Inductance roll-off by saturation
- Saturation Roll_off is not standardized and can vary 10…35% percent between different Series
- Using the Slider, you can verify the actual inductance under operating conditions



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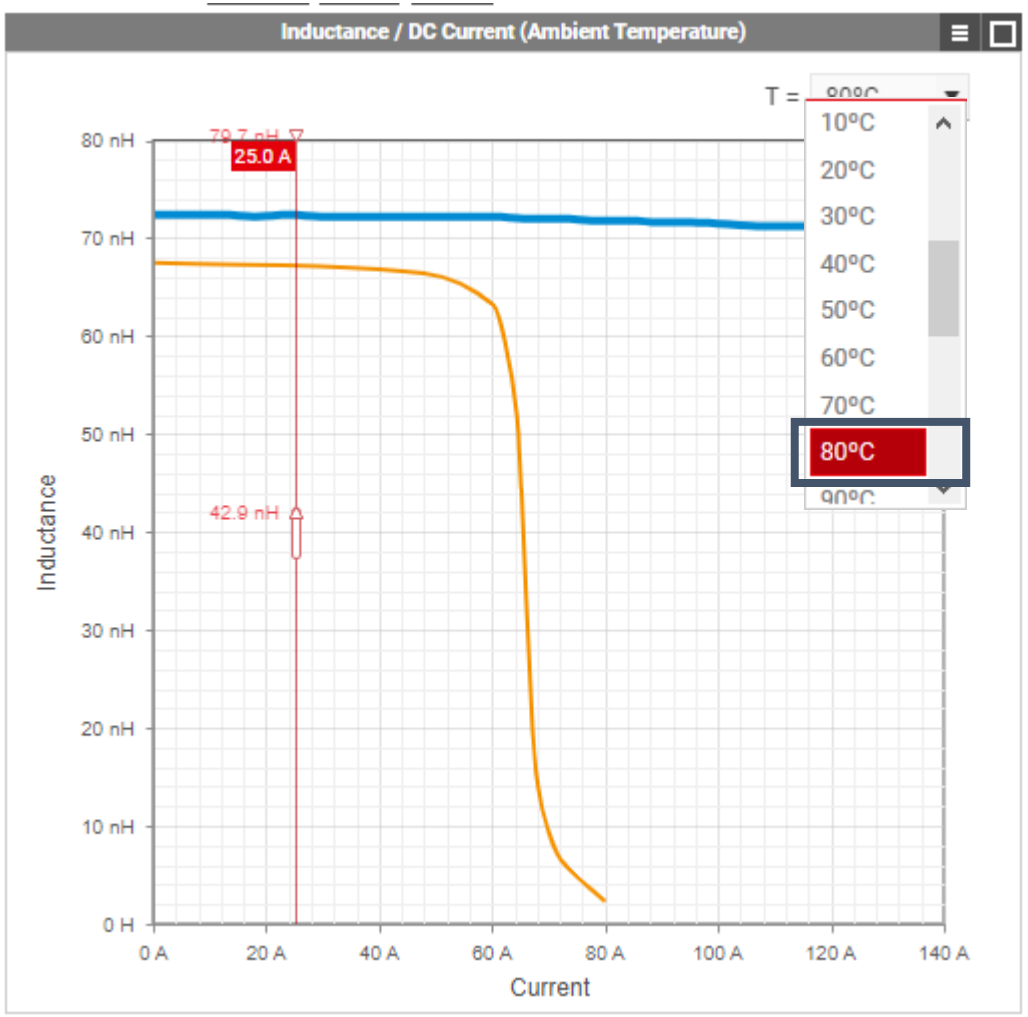
Saturation vs. Temperature



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Mind the Saturation!

- Datasheet!
- Power Inductors do have tolerances up to 30%
- Saturation effects and Tolerances have to be considered

Electrical Properties:

Properties		Test conditions	Value	Unit	Tol.
Inductance	L	100 kHz/ 100 mA	72	nH	±20%
Rated Inductance	L_R	100 kHz/ 10mA/ 30.0 A	71	nH	typ.
Rated Current	I_R	ΔT = 40 K	30	A	max.
Performance Rated Current [1)]	$I_{RP,40K}$	ΔT = 40 K	76.1	A	max.
Saturation Current @ 10%	$I_{SAT,\ 10\%}$	|ΔL/L| < 10 %	62	A	typ.
Saturation Current @ 30%	$I_{SAT,30\%}$	|ΔL/L| < 30 %	64	A	typ.
DC Resistance	R_{DC}	@ 20 °C	0.235	mΩ	±7%
Self Resonant Frequency	f_{res}		150	MHz	typ.

1) refer to IEC 62024-2-2020

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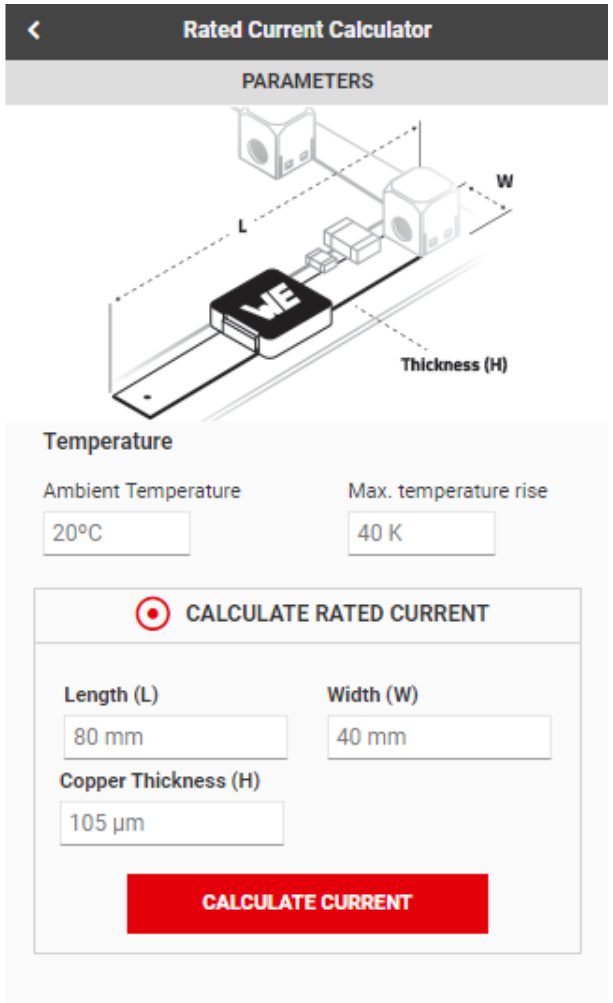
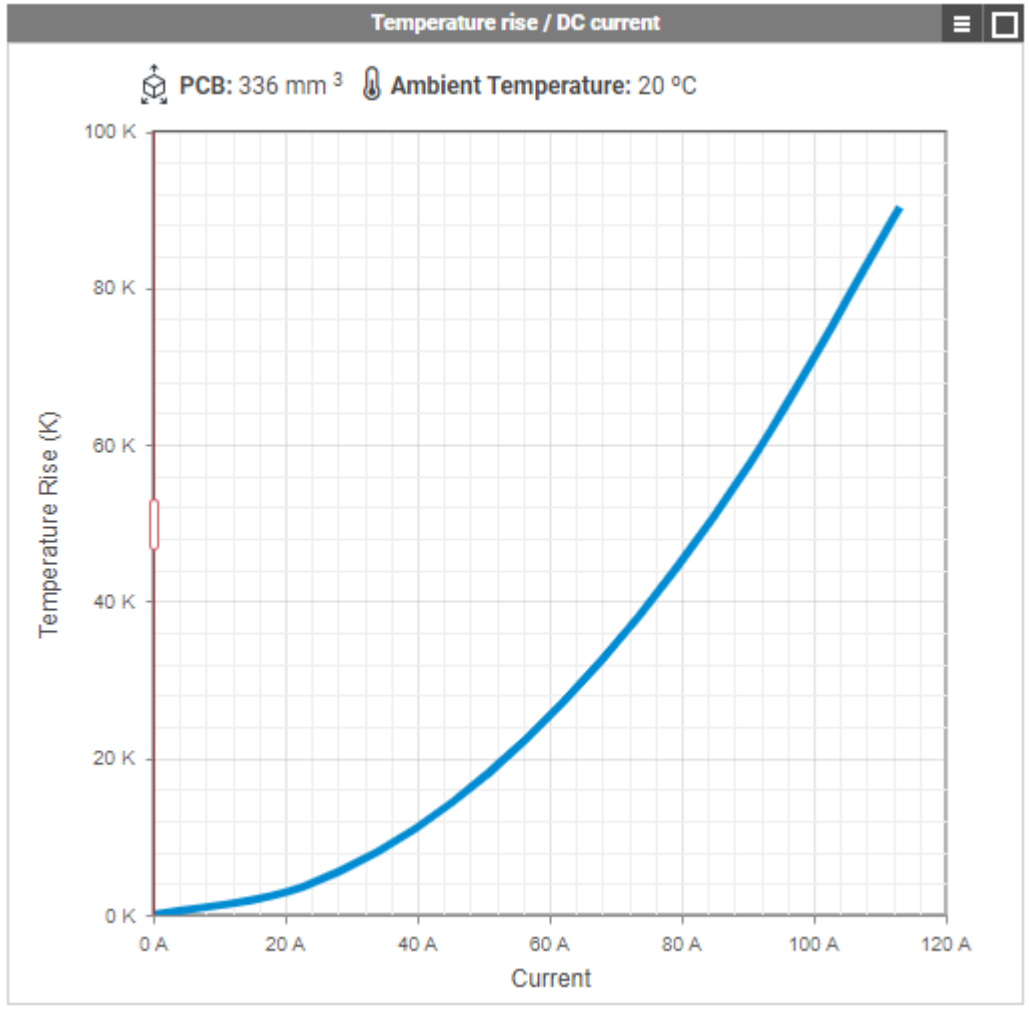
Rated current Calculator





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Filter Design

EMI Filter Designer for differential mode:

Use this application to design a discrete electronic EMI filter for conducted differential noise, for example from your DC-DC converter, and evaluate the realistic response based on real components.

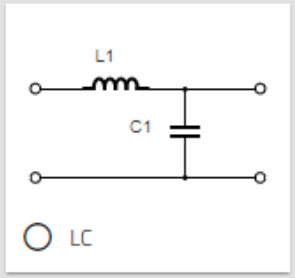
Project's Title:

Title
My EMI Filter project

Input parameters:

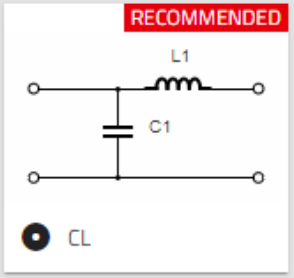
Operating voltage 12 V	Operating current 0.5 A
Load / LISN impedance 100 Ω	Noise source impedance 0.1 Ω
Cut-off frequency ☐ 100 kHz	ⓘ Cut-off frequency: 20 kHz
Attenuation ☑ 20 dB	at Frequency 200 kHz

Topology:

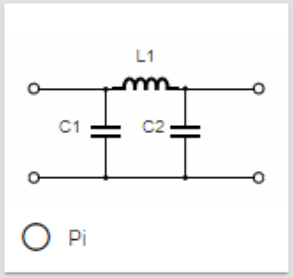


○ LC

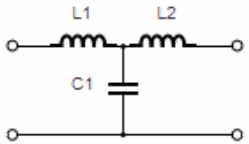
RECOMMENDED



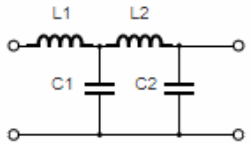
● CL



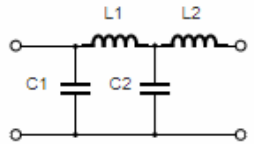
○ Pi



○ T-Filter



○ 4th-Order LC-LC



○ 4th-Order CL-CL

Advanced

- ☐ SMD components only
- ☐ Shielded inductors only
- ☐ High temperature (125°C)
- ☐ Shared input capacitor DC/DC converter — C1/C2 10 µF

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Q&A Session

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