2024 Embedded Seminar

Technical trends and solutions in industrial real-time control systems

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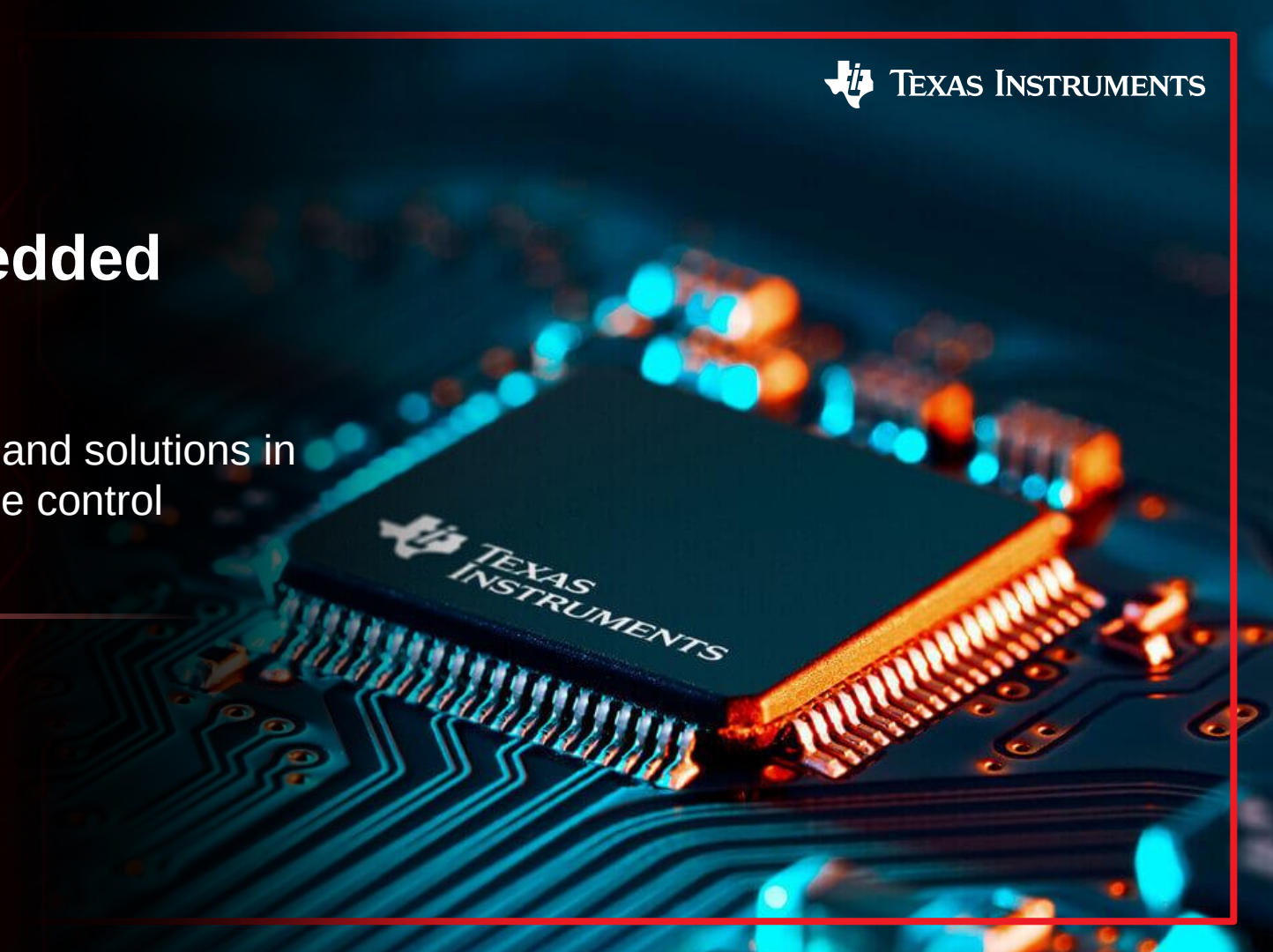
Applications Manager



Agenda

- AI data center and its impact on server power – newer topologies and algorithms
- Achieving high efficiency and power density through high performance computation
- Multi-level converters – complex Pulse-Width Modulation (PWM) enabled by Microcontroller
- Robotic trends – solutions for SPE, safety, EtherCAT, advanced encoders
- Enabling security

AI data center | impact on power consumption

- **AI-powered innovation supercharged**
  - AI applications demand cutting-edge GPUs with higher power needs.
- **Data center evaluation**
  - Data centers now require up to 100kW per rack to fuel AI workloads (vs. 15 – 30kW per rack in the past)
- **Introducing Modular Hardware System Common Redundant Power Supply (M-CRPS)**
  - Efficiency is everything
  - Maxmizing power density
  - Better transient response
- **Next-gen server power with new topologies and algorithms**

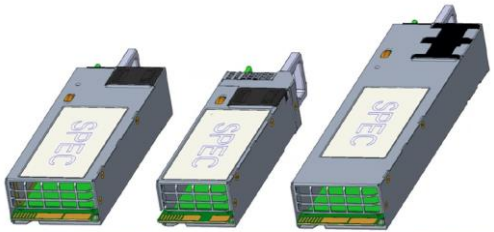
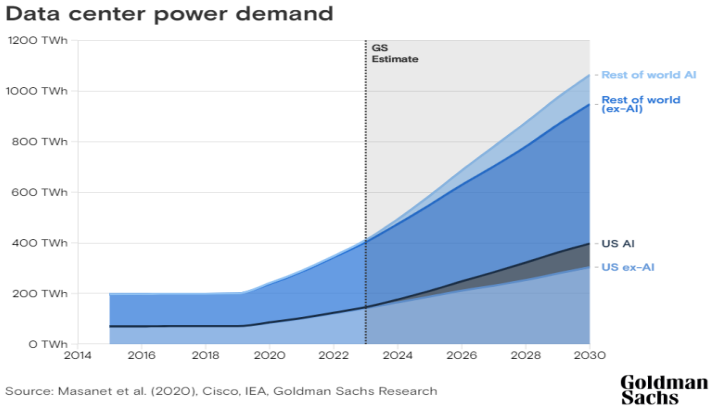


Figure 2-1 Form factors side by side (Front view), from left to right: 185mm by 73.5mm, 185mm by 60mm and 265mm by 73.5mm.

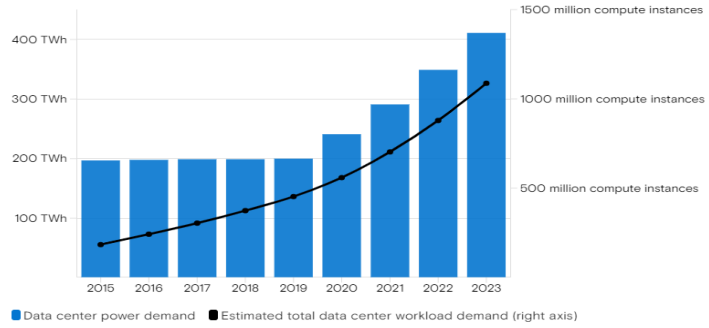
Source: Open Compute Project M-CRPS

Loading	100%	50%	20%	10%
Titanium η (>2.5kW)	94%	96%	94%	90%
Titanium η (≤2.5kW)	92%	96%	94%	90%



Source: Masanet et al. (2020), Cisco, IEA, Goldman Sachs Research

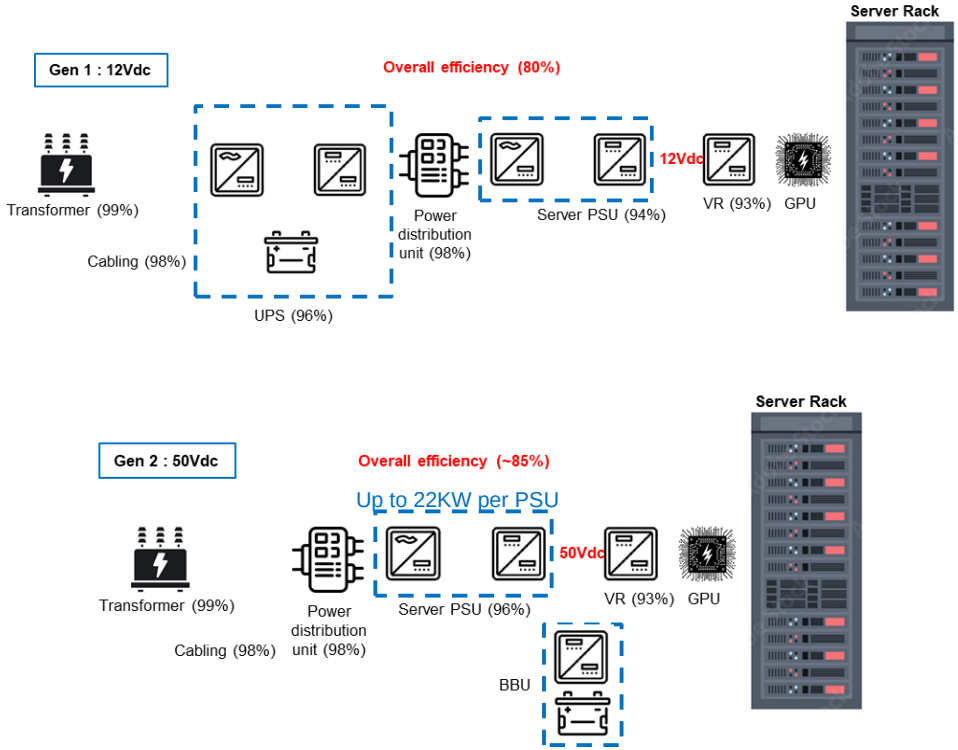
Goldman Sachs



Source: Masanet et al. (2020), Cisco, IEA, Goldman Sachs Research
The data center power demand for 2023 is an estimate.

Goldman Sachs

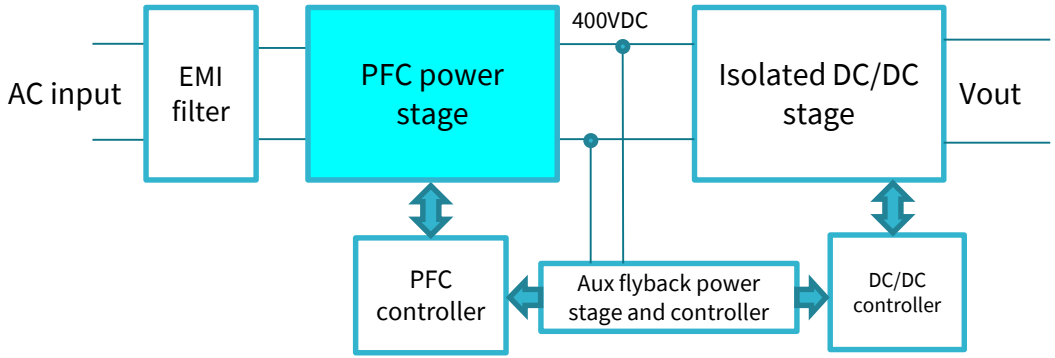
AI data center | power architecture



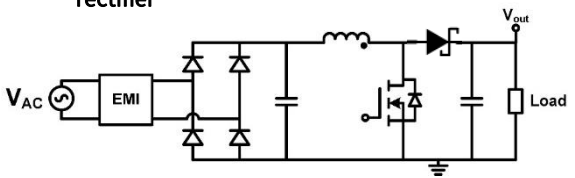
Gen 1 to Gen 2 evolution

- **12V DC bus to 48V DC bus**
  - Lower current in bus bar reducing conduction losses.
- **Power architecture change**
  - Removal of online UPS from system and replacement with digitally controlled battery backup unit (BBU)
  - 4 switch buck-boost with smooth transitioning across operating modes.
  - High transient response -> Peak current mode control algorithm.
  - BBU in light load operation -> Burst mode control
- **Topology innovation for higher efficiency, power density and transient response**
  - Transition / Triangular current / Continuous conduction mode PFC
  - Hybrid hysteresis controlled LLC/Interleaved
  - 3 phase LLC

Server power | PFC



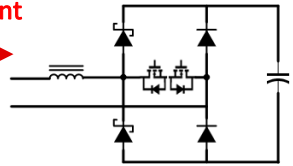
Classic boost PFC with diode bridge rectifier



η~98%

efficiency improvement

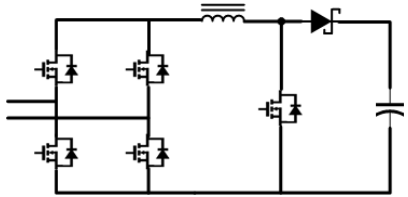
AC-switch PFC (or 'H-PFC')
Implementable with Si MOS



η~98.3%

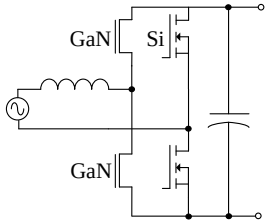
Higher efficiency improvement

Active "bridge rectifier" in classic boost PFC
Implementable with Si MOS **η~98.5%**



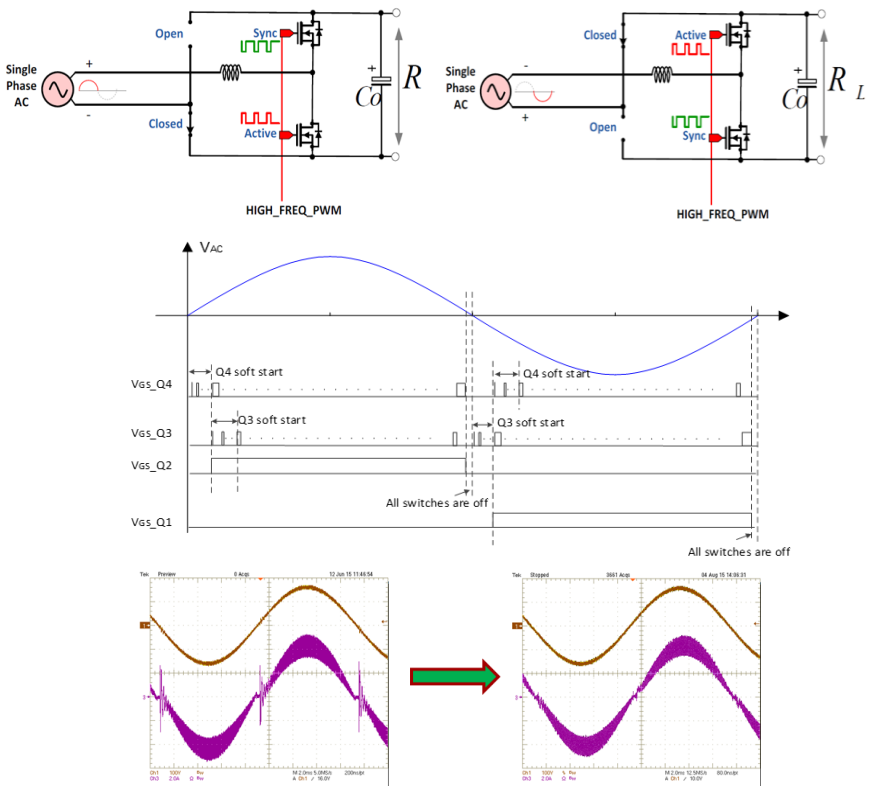
Highest efficiency improvement

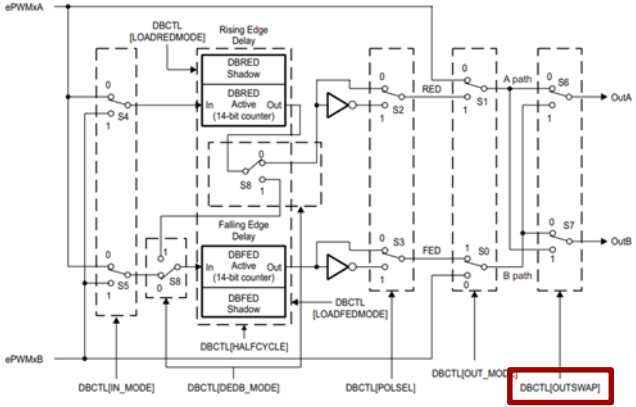
CCM Totem pole "bridgeless" PFC
Cannot be realized with Si MOS, WBG devices needed for fast FETs



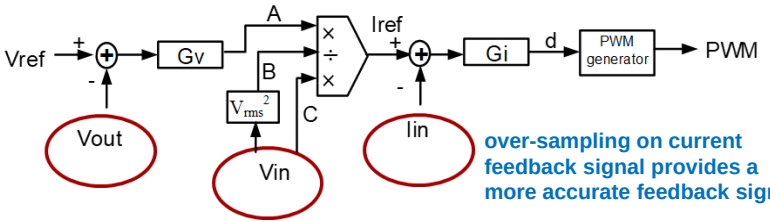
η~99%

Server power | Totem pole PFC digital control (CCM)





C2000 Advanced dead band sub module enables PWM changeover for active and Sync FET

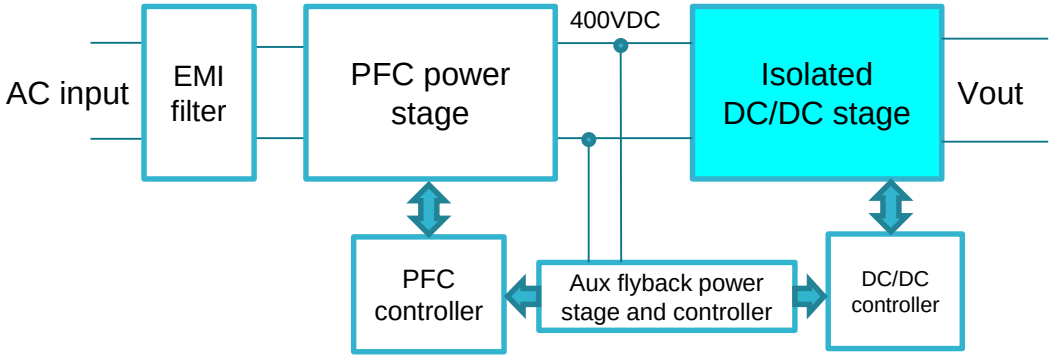


over-sampling on current feedback signal provides a more accurate feedback signal

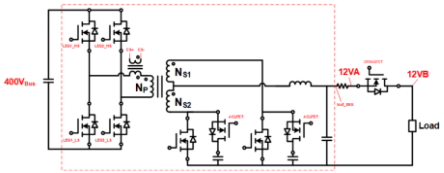
Optional digital filter to reduce noise

PMP23338 - 3.6kW single-phase totem-pole bridgeless PFC reference design with e-meter functionality

Server power | DC/DC



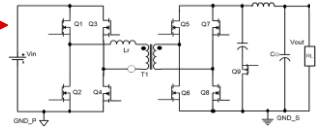
PSFB (with secondary doubler)



η~97.5%

Better transformer utilization and single clamp

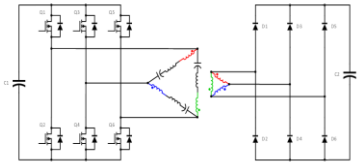
PSFB (with secondary full-bridge)



η~97.5%

High efficiency for higher power rating

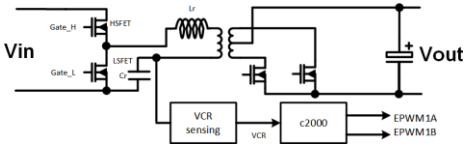
3 phase LLC



η~98%

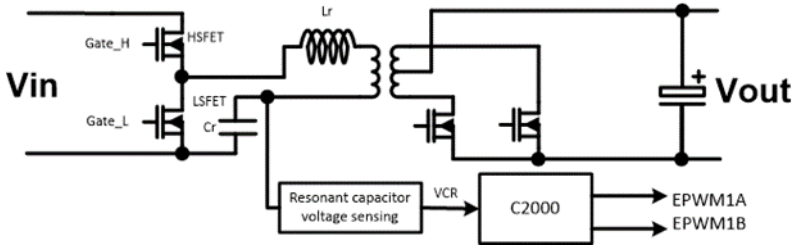
HHC - LLC η~98.5%

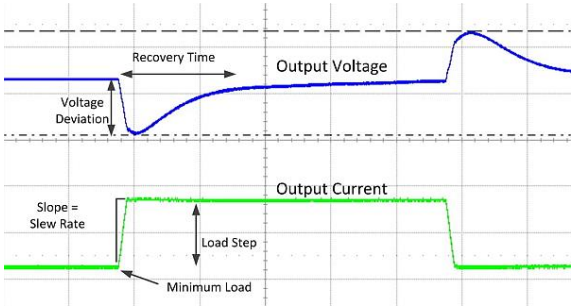
Higher efficiency improvement

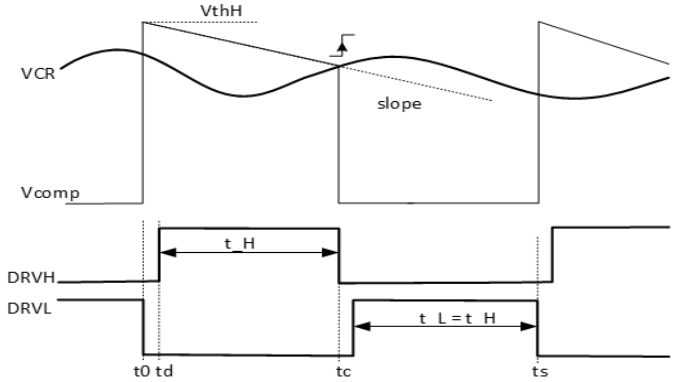


Server power | DC/DC HHC control

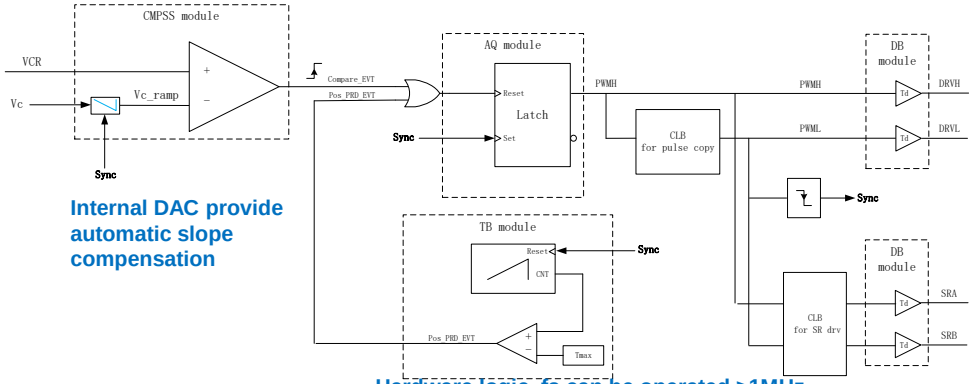
- **Higher load transient response** (CRPS – 0.5A/µs to M-CRPS – 2.5A/µs)
- VMC to current mode control techniques like HHC







PMP41081 – Single comparator (CLB for complementary PWM)
PMP41006 – Dual comparator (CLB only for SR)



Internal DAC provide automatic slope compensation

Hardware logic, fs can be operated >1MHz
CLB provide control flexibility of SR & PWM logic

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- Multi-level converters – complex Pulse-Width Modulation (PWM) enabled by Microcontroller
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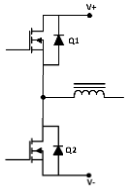
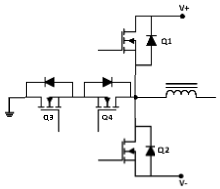
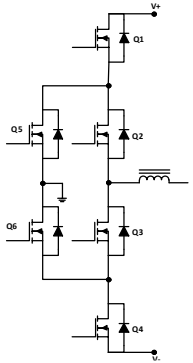
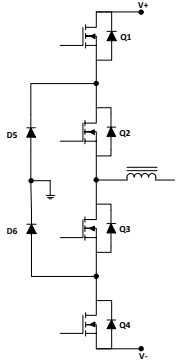
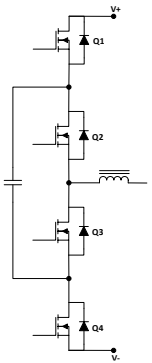
Inverter / PFC | multilevel topologies summary





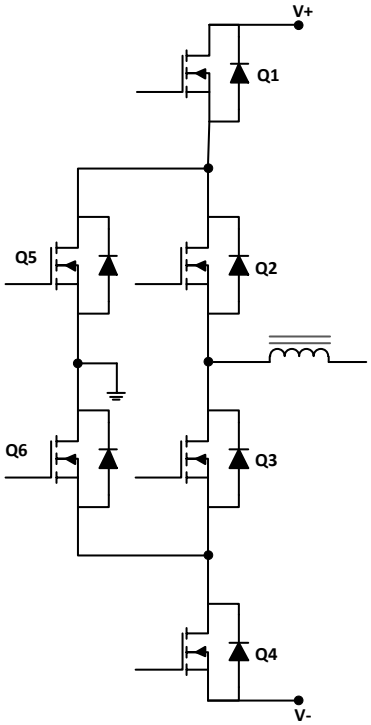






	2L TIDA-01606 in 2L	T-Type 3L TIDA-01606	ANPC TIDA-010210	NPC 3L derived from ANPC	FC3L Flying Capacitor 3L
Benefits	• Simple control scheme • 2 switches only • 2 PWM	• Easy control scheme • Q3/Q4 see ½ V_{DC} • Better EMI than 2L • $f_{RIPPLE} = f_{PWM}$	• Good efficiency • All switches see ½ V_{DC} • Better EMI than 2L • $f_{RIPPLE} = f_{PWM}$	• Lower cost than ANPC • All switches see ½ V_{DC} • Better EMI than 2L • $f_{RIPPLE} = f_{PWM}$ • 4 PWM	• Highest efficiency • Only 4 HF FETs (& 1Cap) • $f_{RIPPLE} = 2 \times f_{PWM}$ • Smallest magnetics • Lowest EMI
Challenges	• Q1/Q2 see full V_{DC} • High EMI for higher f_{PWM} • Passives are biggest	• Q1/Q2 see full V_{DC} • 4 PWM	• More complex control scheme • Shutdown sequencing critical • 6 PWM	• Lower efficiency than ANPC • More complex control • Shutdown sequencing critical	• Initial charging of flying capacitor • Shutdown sequencing critical

ANPC 3L | HV failure protection

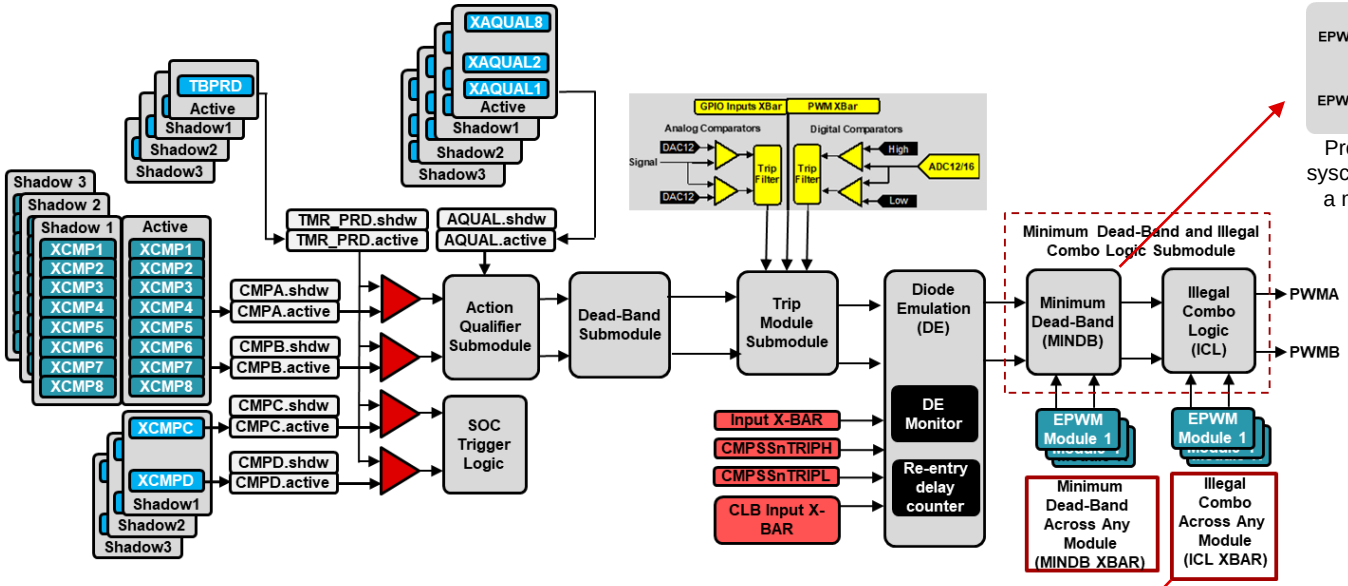


- Outer switches (Q1/Q4) to turn off before inner switches (Q2/Q3)
- Fault protection logic is required during normal operation at crossover and at all shutdown conditions
- Software algorithm causes too much delay to provide in-time protection
- Additionally, run-time implementation of the above in software imposes CPU bandwidth challenges in single MCU solution
- Use of external hardware circuits, like FPGA or CPLD increases system and development cost

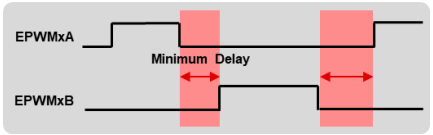
State \ FETs	Q1	Q2	Q3	Q4	Q5	Q6
Hazardous	1	0	0	0	0	0
	1	0	1	0	0	0
	0	0	0	1	0	0
	0	1	0	1	0	0
	1	0	0	1	0	0
Destructive	1	1	1	X	X	X
	1	1	X	1	X	X
	1	X	1	1	X	X
	X	1	1	1	X	X
	1	X	X	X	1	X
	X	X	X	1	X	1

Ref: APPLICATION NOTE UnitedSiC_AN0023 – March 2021, Revision 3

Advanced PWM module on C2000 & AM26x



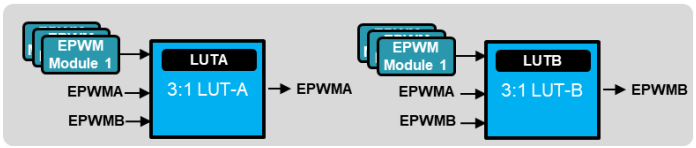
Minimum Dead-Band



Programmable delay (DelayA and Delay B in sysclk cycles) is added to ensure there is always a minimum amount of delay between outputs

Illegal Combo Logic

Based on the truth table, output of EPWMA/EPWMB are configured high or low



Input 1	Input2	Input3	Output
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

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Power conversion| high performance computing

Increased power semiconductor switching frequency

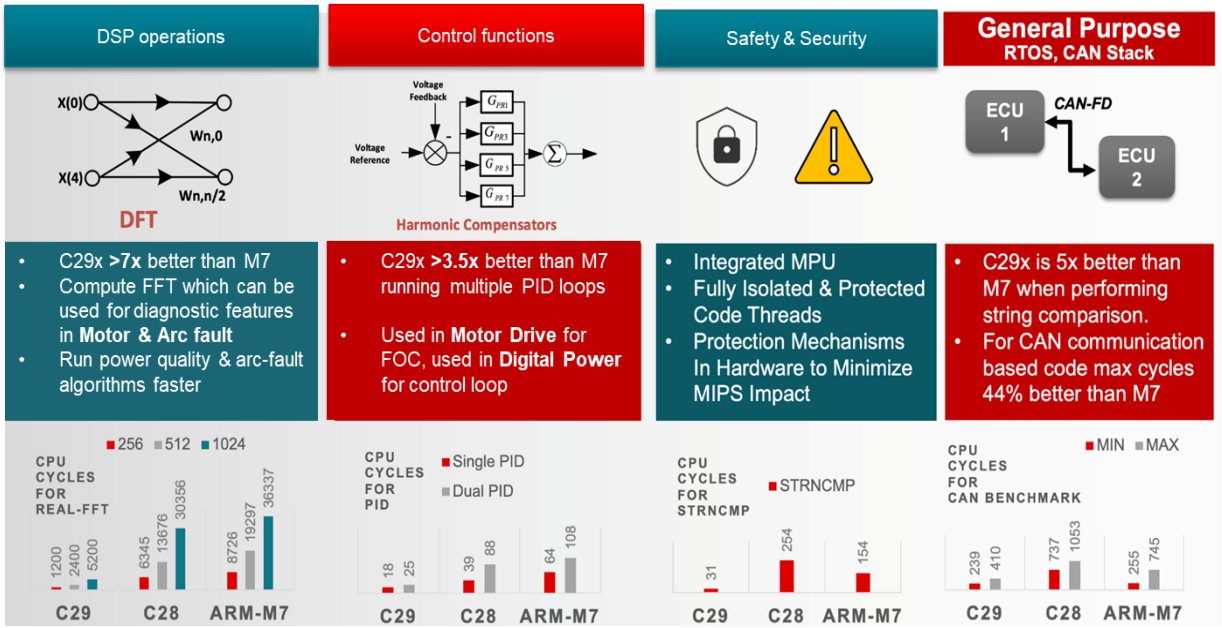
- Reduced LC filter component sizes – Compact system footprint and Lower cost.
- Enables use of ceramic capacitors instead of electrolytic – Better reliability and lifetime.
- Faster transient response – Better regulation to load and line parameter variations.

Increasing computation requirements

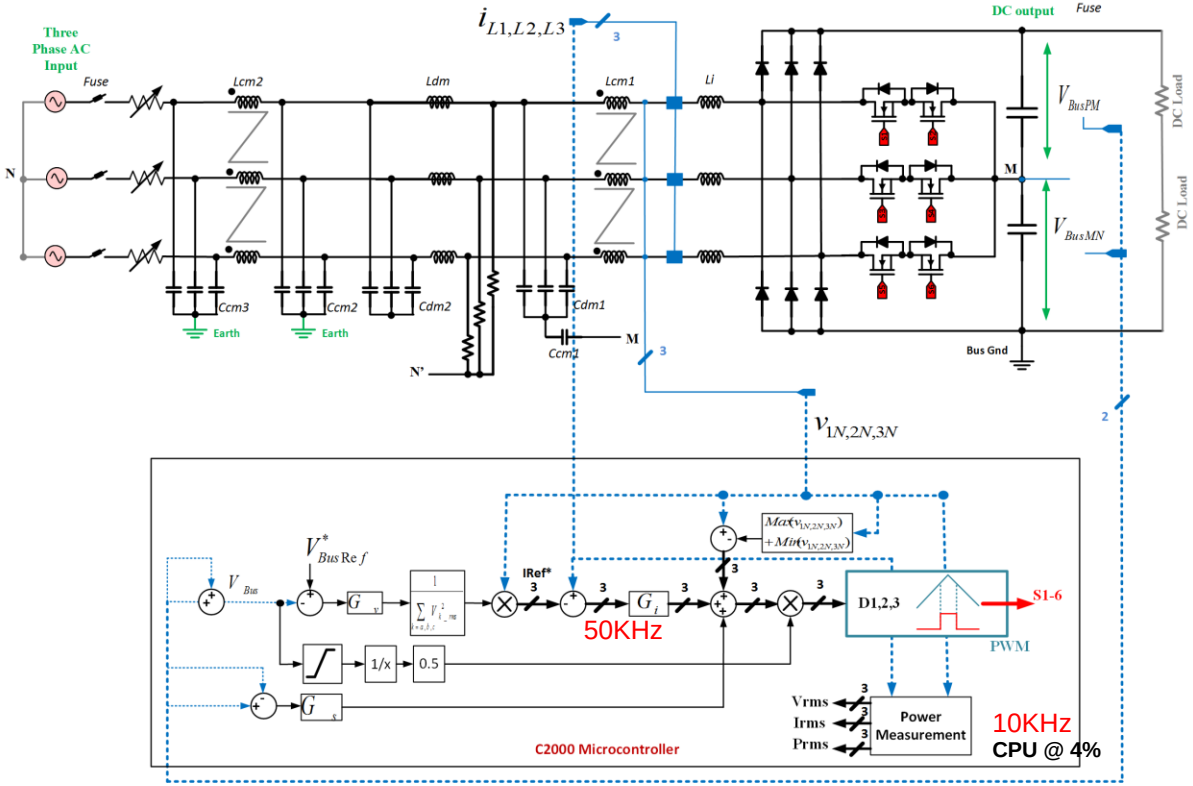
- Higher control loop frequency (500Khz)
- Advanced control algorithms
- Multiple power stages and communication all with one CPU.
- Meeting safety regulations from continuously evolving standards.
- Additional feature enhancements in existing products.

F29x | New gen DSP meet increased compute need

- Can Execute 1 to 8 Instructions In Parallel (up to 8x higher throughput per cycle vs C28)
- Multiple Parallel Functional Units (2x comparators, 2x logical, 3x adders, 2x multipliers,...)
- Specialized Operations Targeting Real-Time Control (Trigonometric, Multi-Phase Vector Translation)
- New Operations To Minimize Discontinuities & Accelerate Decision Making Code (if-then-else, switch)
- Can Perform 8/16/32/64-bit Dual Reads & Writes In A Single Cycle (6x higher throughput vs C28)
- All Registers Save/Restored automatically On Real-Time Interrupt In 10 Cycles (vs 40 cycles for C28)
- Hardware Interrupt Prioritization Requires No Software Overhead (on C28 it is managed by Software)



F29x | Vienna rectifier benchmark example



CPU Utilization	F2837xD / 200MHz	F29 / 200MHz
"*control ISR*" @ **50 kHz** • Compensators, ADC and PWM drivers, SFRA • Feedforward Elements in the control loop • Frequency response analyzer (Optional)	CPU @ 20%	CPU @ 10% (estimated)
	• Max achievable control loop frequency **300KHz**	• Max achievable control loop frequency **600KHz (estimated)**

- SineAnalyzer and Datalog

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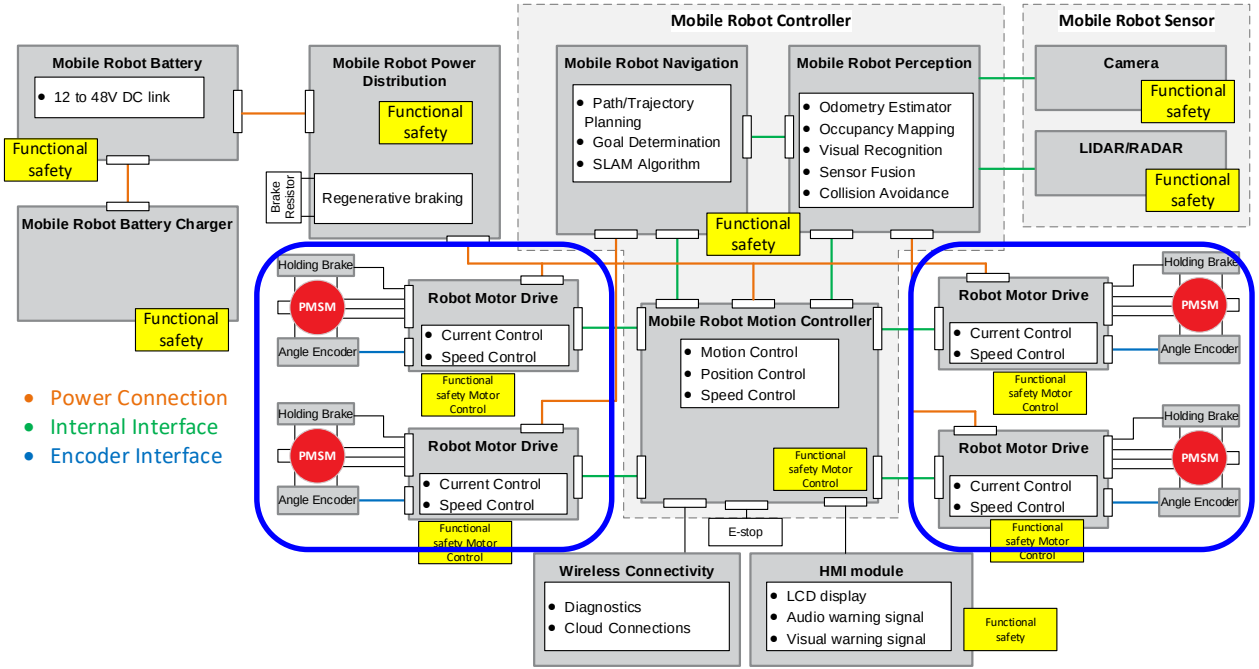
Motor control | trend for robotics

- **AGV/AMR**
  - Multi-axis motor control with one MCU
  - One MCU drive 2-4 motors
- **Humanoid Robot**
  - Up to 8 motors in hand assembly
  - Requires very small form factor
  - One MCU for multiple motors
  - Higher efficiency requirement for body temperature limit
- **Collaborative Robotics (Cobot)**
  - Small form-factor MCU with safety and multi-protocol support
  - < 9x9 mm package required to fit into O / C shape PCB on motor assembly end



TMS320F28P650DK

C2000™ 32-bit MCU, 2x C28x+CLA CPU, Lock Step, 1.28-MB flash, 16-b ADC, HRPWM, EtherCAT, CAN-FD, AES

AM2634

Quad-core Arm® Cortex®-R5F MCU up to 400 MHz with real-time control and security

Robotics | trend for functional safety

Complex safety landscape

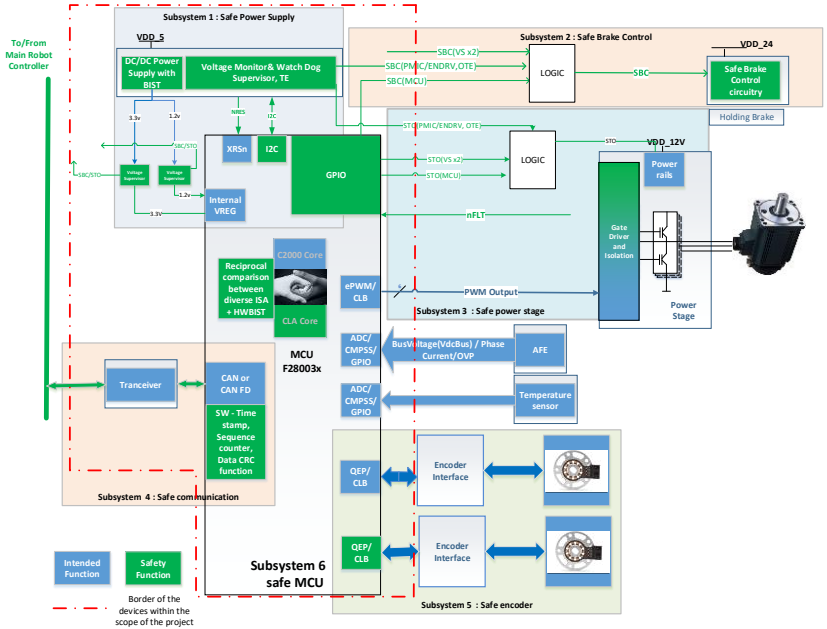
- AGV/AMR in warehouse: ISO 3691-4
- Industrial robot / Cobot: ISO 10218
- Customer needs to understand their system level safety structure

Trend: higher and higher requirement on functional safety

- Safety on system level needs to build to a reasonable level with price / safety balance
- Increasing complexity and capability in MCU driving state of art safety solution to be more and more complex

TI doing system level safety argumentation

- TI offers certified safety concept for systems up to CAT 3 and PLd with TUV SUD
- Help customer on how to take TI MCU and documentation to get safety assessment



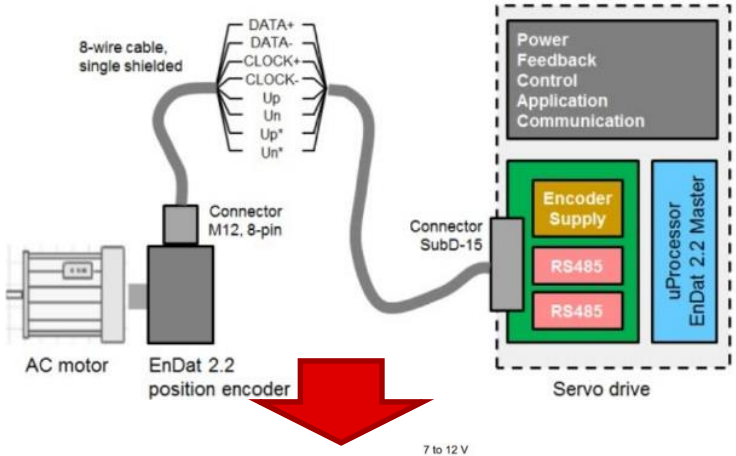
https://www.ti.com/lit/wp/sprad98/sprad98.pdf

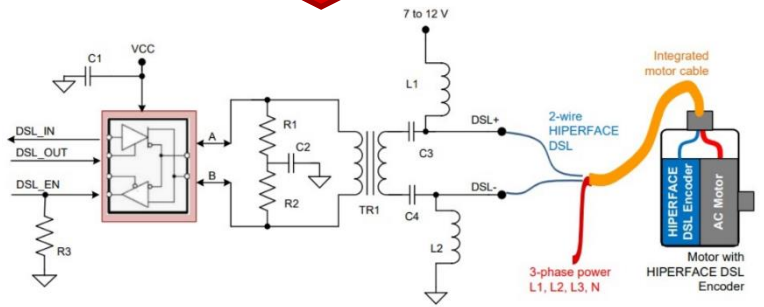
Motor control | trend for absolute encoder

- **Higher data rate**
  - More features in Encoder and need to send more data - beyond position (vibration (AI), temperature, torque, etc.)
  - Higher bandwidth and lower latency / jitter requirement
- **Less cabling**
  - Enables 2 cable encoder interface with power & data on 1 twisted pair
  - 100BASE-T1L, Hiperface DSL, EnDat 3.0, BiSS Line
- **Added safety**
  - Allows built-in redundancy with 2 encoder data on one interface
  - Functional safety: black-channel communication

Device	Technology	Encoders supported	
AM26X	PRU – ICSS / QEP	• T Format • Nikon / A Format • BiSS- C • SSI • QEP	• EnDAT 2.1/2.2/3.0 • Hiperface DSL • BiSS-Line
C2000	CLB / QEP		• EnDAT 2.1/2.2

Technical White Paper: “Safe Torque Off – A Functional Safety Concept Using AM64x With HIPERFACE DSL®” available under NDA. Concept certified by TUV SUD on 6-Dec-2021

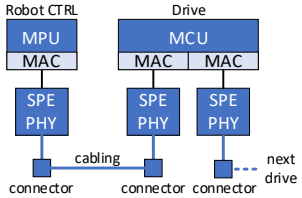




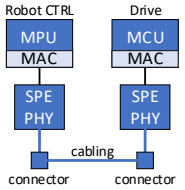
CLB – Configurable logic block
ICSS – Industrial communication sub system
PRU – Programmable real time unit

Single twisted pair Ether-CAT in Servo / Robot and AMR/AGV

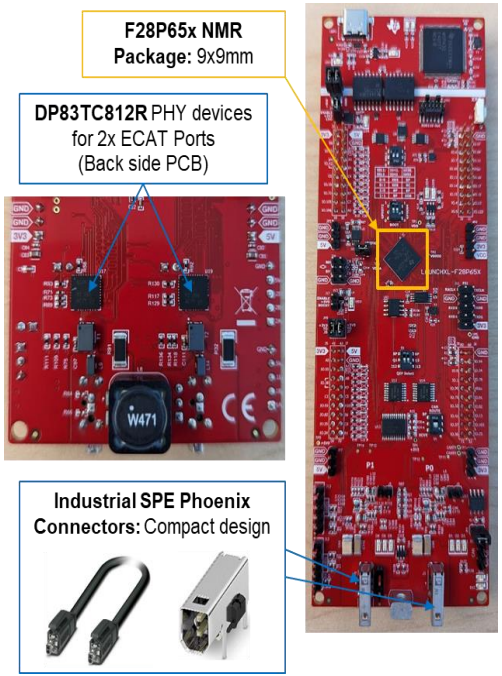
- Higher bandwidth requirement
  - Added functional safety
  - Lower latency / jitter
- No Royalty / higher speed (CAN FD → SPE)
- 100Mbps is sweat spot today
- EtherCAT P supplies power and communication in a single hybrid cable
- Ether CAT over single twisted pair
- EtherCAT G -> ICSS-G can support 1000Mbps Ether CAT)
- ICSS on AM261x and EtherCAT IP in F28P65x



Daisy chain



Point to point



Agenda

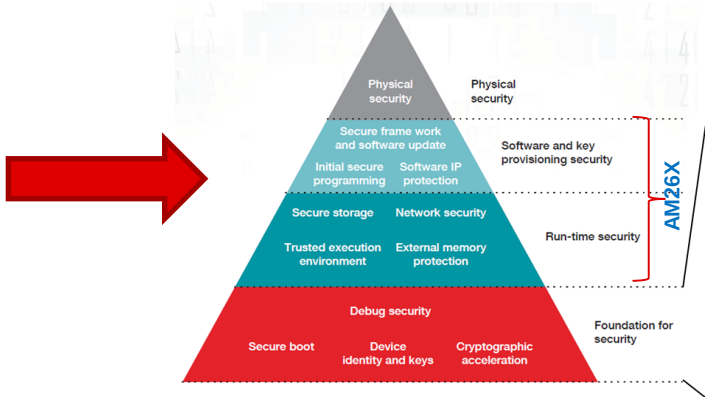
- AI data centers and its impact on server power –newer topologies and algorithms
- Multi-level converters – enabling complex PWM through Microcontroller
- Achieving High efficiency, high power density through high performance compute
- Robotic trends – Solutions for SPE, Safety, Ether CAT, Advanced encoders
- Enabling security

Security requirement | trend

- Risk of cyberattacks
- Lose of customer firmware IP.
- New standards to be followed – example is European Cyber resilience act (CRA)

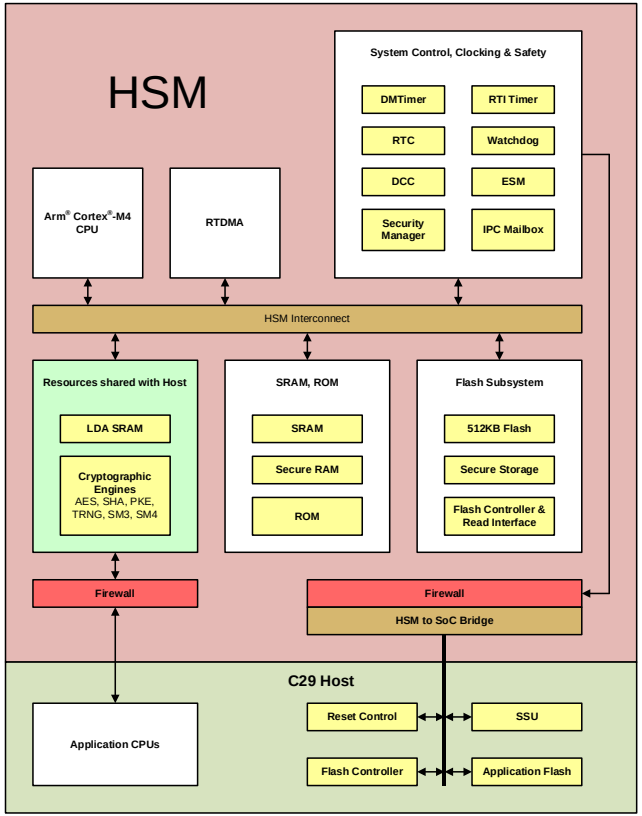
Industrial products are now requiring

- Secure boot.
- Debug security.
- Secure firmware update.
- Authentication of genuine firmware.
- Encryption/decryption of communication.
- Hardware protection against side channel attached.
- Advance algorithms(post-quantum cryptography) for protection against quantum computers.
- Security accelerators to reduce the computation time for security features.



Enabler	Feature	AM26x	F29x
Cryptography Acceleration	AES : 128,192, 256	✓	✓
	SHA2-224, 256	✓	✓
	SHA2: 384, 512	✓	✓
	True RNG	✓	✓
	DRBG	✓	✓
	PKA: RSA 2048 acceleration	✓	✓
	PKA: RSA 4096 acceleration	✓	✓
	PKA: ECC acceleration	✓	✓
	DMA support for cryptographic engines	✓	✓
Device ID and Keys	Device Public ID via ROM API	✓	✓
	Booting keys (MPK/SMPK, KEK, MEK/SMEK)	OTP	Secure Flash
	General OTP bits and other OTP (MSV, SWRV)	✓	✓
Secure Boot	Customer programs own keys	✓	✓
	RSA 2048-based		✓
	RSA 4096-based	✓	✓
	ECDSA (NIST Curve)		✓
	Authenticated boot	✓	✓
	Encrypted boot	✓	✓
	Model ID check	✓	✓
	Anti-roll back check	✓	✓
Debug Security	SW-controlled JTAG access	✓	✓
	Permanent disable JTAG via efuse	✓	✓
	Security-aware debugging	✓	✓

F29x HSM | Hardware Security Manager



- EVITA-Full compliant HSM with dedicated CPU, RAM, ROM and Flash memory
- Two 256KB Flash banks with FOTA (A/B swap) support and rollback control/anti-rollback protection
- Secure storage of keys, certificates and user secrets
- Secure factory provisioning of keys and code
- Secure boot support for Root-of-Trust
- Secure debug with challenge-response authentication
- Device lifecycle management
- Cryptographic accelerators – AES, RSA, ECC, SHA-2, TRNG, SMx
- Protection against DPA and fault injection attacks
- IPC communication with C29 host CPUs

Thank you!

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