High-Performance Analog Products

Analog Applications Journal

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Introduction

The *Analog Applications Journal* is a digest of technical analog articles published quarterly by Texas Instruments. Written with design engineers, engineering managers, system designers and technicians in mind, these "how-to" articles offer a basic understanding of how TI analog products can be used to solve various design issues and requirements. Readers will find tutorial information as well as practical engineering designs and detailed mathematical solutions as they apply to the following product categories:

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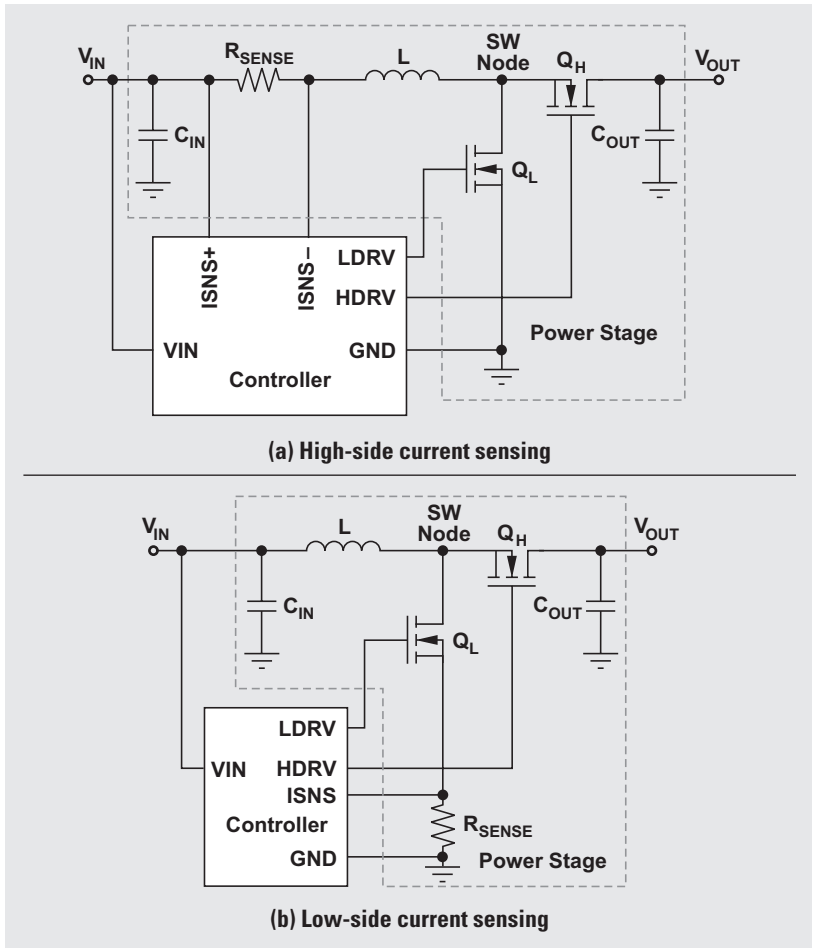
Split-rail approaches extend boost-converter input-voltage ranges

By Haifeng Fan
Systems Engineer

Introduction

Wide-input-range DC/DC controllers usually have built-in undervoltage lockout (UVLO) circuits to prevent the converters from misoperating when the input voltage is below the UVLO threshold. However, the UVLO circuit might also cause undesirable shutdown in the event of a load transient or a supercapacitor discharge in applications where input voltage is above the UVLO threshold at start-up but later may drop below this threshold. In addition, these controllers normally cannot be used in applications where the input voltage is always under the UVLO threshold. This article presents several split-rail approaches to extend boost-converter input-voltage ranges, enabling the use of these controllers with input voltage lower than their UVLO thresholds. Design examples along with test results are provided to validate these approaches.

Figure 1. Boost converters in single-rail configuration



Minimum input voltage of a boost converter

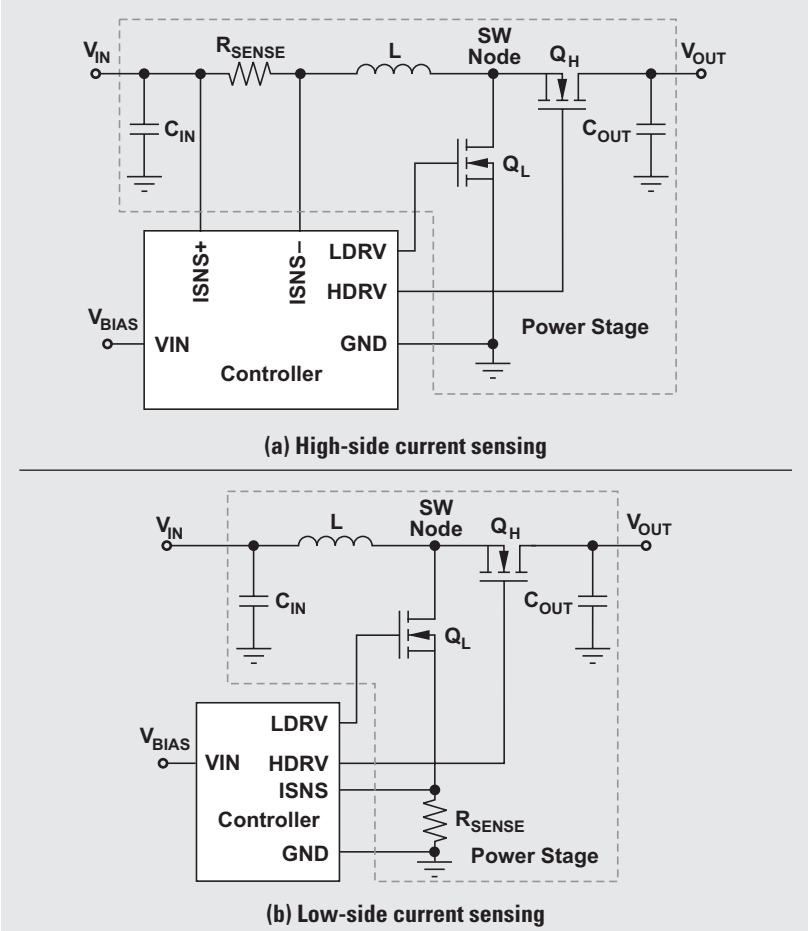
Figure 1 shows typical boost converters with a single input supply (V_{IN}) that provides the input voltage to the power stage and the bias voltage to the controller. The minimum bias voltage to the controller at the V_{IN} pin is set by the controller's input UVLO threshold. To guarantee functionality of boost converters with high-side current sensing (Figure 1a), the minimum input voltage to the power stage is defined by the minimum common-mode voltage of the current-sense comparator. This is because the input voltage is also connected with the non-inverting input of the current-sense comparator. The minimum common-mode voltage of the current-sense comparator often is less than the controller's input UVLO threshold. For the boost converter with low-side current sensing (Figure 1b), the input voltage to the power stage is not directly connected to the current-sense comparator. Therefore, it is not required to match the minimum common-mode voltage. Consequently, in the single-rail configuration where the input voltage to the power stage and the bias voltage to the controller are tied together, the controller's input UVLO threshold imposes a constraint on how low the input voltage to the boost power stage can go.

As shown in Figure 2, the input supply to the boost converter can be split into two rails: the power-stage input rail (V_{IN}) and the controller's bias input rail (V_{BIAS}). In the split-rail configuration, although V_{BIAS} is still required to be above the controller's UVLO threshold to turn on the controller, V_{IN} can go below the UVLO threshold. Since V_{BIAS} needs to supply only a very small amount of power, it can be generated by a charge pump or even share another voltage rail already existing in the system. As a result, the voltage range of the power rail (V_{IN}) can be extended.

This article will discuss several approaches to implementing the split-rail configuration. The TPS43061 synchronous boost controller from Texas Instruments (TI) will be used to elaborate on the split-rail concept and to validate the presented approaches. This boost controller has a high-side current-sense comparator and an internal input UVLO circuit at the bias-supply input (V_{IN}) pin.

Figure 3 shows the turn-off waveforms of the boost converter in the single-rail configuration shown in Figure 1a. The converter stops switching once V_{IN} falls below 3.9 V, which is the controller's UVLO turn-off threshold. The boost converter can be turned on only when V_{IN} rises above the UVLO turn-on threshold of 4.1 V.

Figure 2. Boost converters in split-rail configuration



Extending input-voltage range after start-up

In some applications with only one input supply, the input-supply voltage is greater than the controller's UVLO turn-on threshold at start-up. However, it might fall below the input UVLO threshold afterwards, leading to undesired shutdown. For example, in power systems using a photovoltaic panel combined with a supercapacitor as an input supply, the input voltage may drop below the controller's UVLO turn-off threshold due to discharge. Another example is a power system powered by a USB power cable where the voltage drops significantly during a load transient, resulting in an unexpected system shutdown.

Figure 3. Turn-off waveforms of boost converter in single-rail configuration

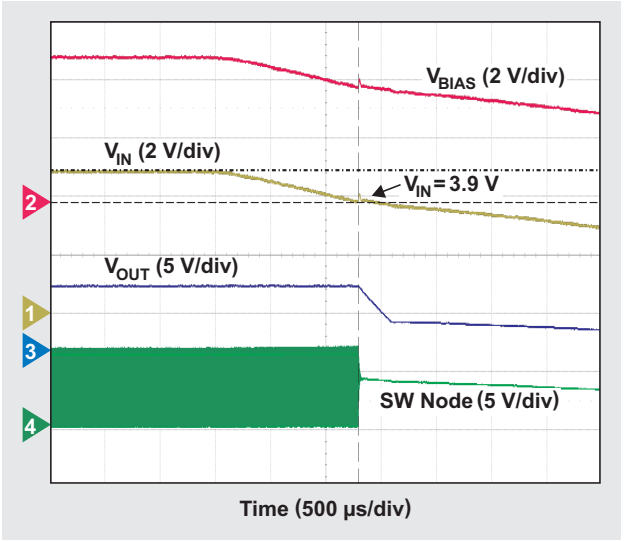
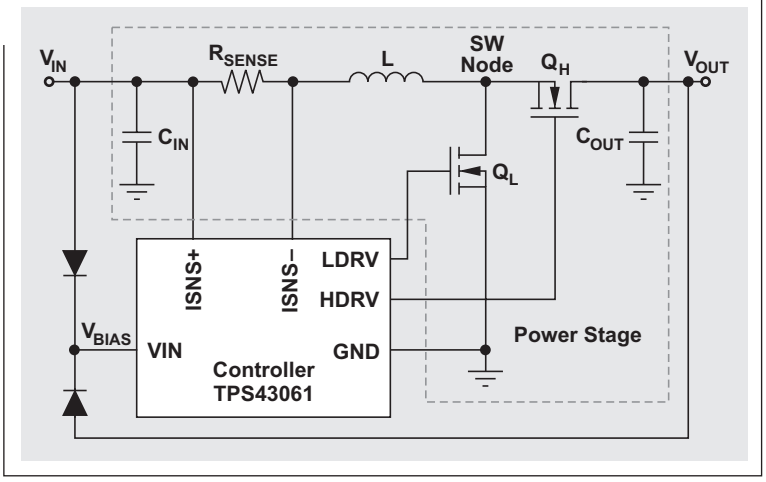


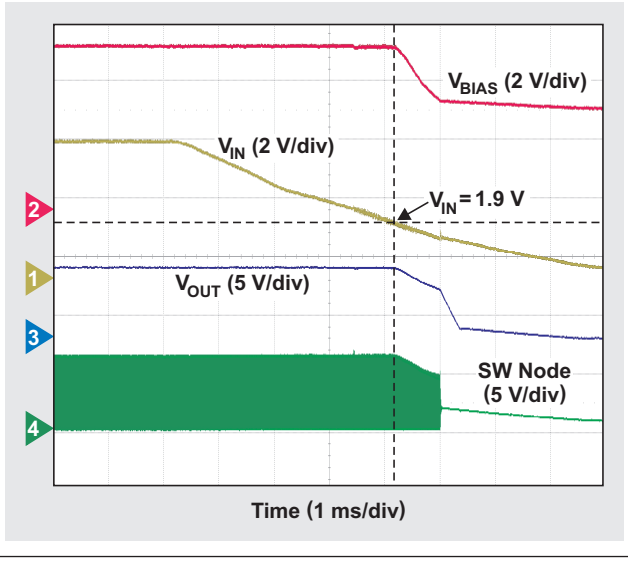
Figure 4. Split-rail approach feeding V_{OUT} back as bias supply



For these applications, if V_{OUT} is within the V_{BIAS} specification range, which is always higher than the UVLO turn-on threshold, V_{OUT} can be fed back as the bias supply (V_{BIAS}) via a diode (Figure 4). After start-up, V_{BIAS} is clamped to V_{OUT} rather than V_{IN} and stays above the UVLO threshold even if V_{IN} drops below this threshold. The boost converter can maintain normal operation as long as V_{IN} can meet the current-sense comparator's requirement for the minimum common-mode voltage.

Figure 5 shows the turn-off waveforms of the boost converter shown in Figure 4, where V_{OUT} is set as 6 V and fed back as the bias supply. With diode's forward voltage drop neglected, the bias-supply voltage (V_{BIAS}) is clamped to V_{OUT} rather than V_{IN} when V_{OUT} is higher than V_{IN} after start-up. Hence, V_{BIAS} stays above the 3.9-V UVLO turn-off threshold to avoid the undesired turn-off when V_{IN} falls below 3.9 V. V_{OUT} stays within regulation until V_{IN} falls below the minimum common-mode voltage of the current-sense comparator, in this example 1.9 V. This means that the minimum input voltage (V_{IN}) has been extended from 3.9 V to 1.9 V after start-up.

Figure 5. Turn-off waveforms of configuration shown in Figure 4

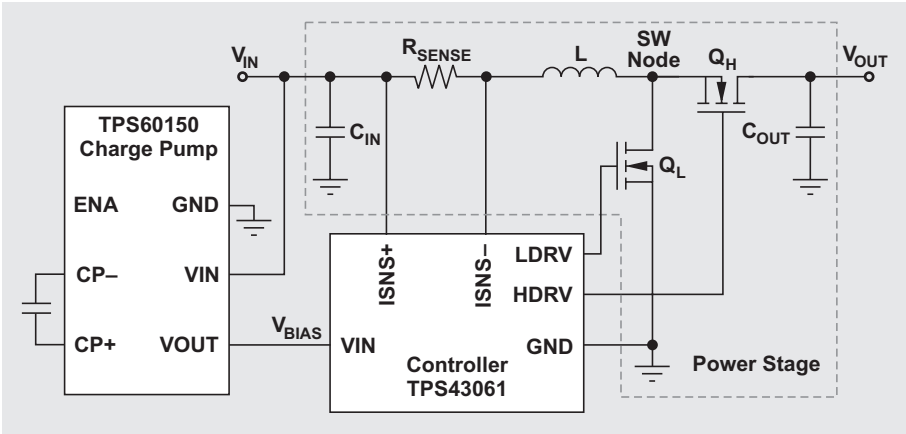


Extending the start-up input-voltage range

Lithium-Ion (Li-Ion) batteries are widely used in smartphones, tablet PCs, and other handheld devices. The voltage of a single-cell Li-Ion battery rated at 3.6 V usually ranges from 2.7 V to 4.2 V due to discharge and charge. This is lower than the UVLO threshold of some wide-input-range boost controllers, even before start-up. For these applications, neither a single-rail scheme nor a split-rail approach feeding V_{OUT} back as the bias supply works. A separate bias supply different from the battery input is needed.

Fortunately, a bias supply needs to supply only very low power. If there is another supply rail above the UVLO turn-on threshold already available in the system, it can be connected to V_{BIAS} while connecting the power rail (V_{IN})

Figure 6. Split-rail approach using charge pump to produce bias voltage

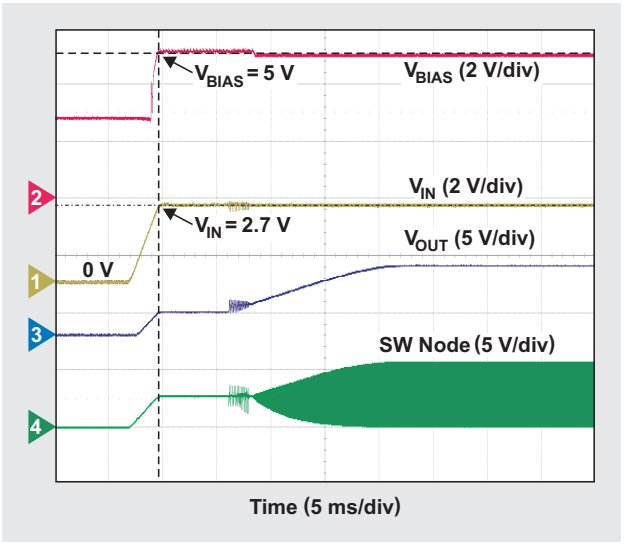


to the battery (Figure 2). If not, a charge pump can be added for a bias supply (Figure 6).

In this example, from the 2.7 V to 4.2 V of battery input, TI's TPS60150 charge pump produces a regulated 5-V supply, which is higher than the UVLO turn-on threshold of the TPS43061 controller, so it can be used as the bias supply. Using a charge pump with the split-rail approach, the boost converter can start up and operate with a single input supply that is lower than the boost controller's UVLO turn-on threshold .

Figure 7 shows the start-up waveforms of the boost converter shown in Figure 6. The converter can start up and operate with a single 2.7 V of supply since V_{BIAS} is regulated at 5 V, although V_{IN} is only 2.7 V. By using this split-rail approach, the boost converter's minimum operating input voltage is extended from 4.1 V to 2.7 V.

Figure 7. Start-up waveforms of configuration shown in Figure 6



Conclusion

Two inputs are usually required for a boost converter to operate: the input supply to the power stage and the bias supply to the controller. The controller's UVLO threshold sets the low limit of the bias supply. It also places a constraint on the input supply to the power stage, if these two rails are connected to share one input supply. Split-rail approaches separate the power rail from the bias supply rail to eliminate the constraint on the minimum operating voltage of the power rail. This extends the input-voltage range of boost converters.

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Low-cost flyback solutions for 10-mW standby power

By Adnaan Lokhandwala
Product Manager

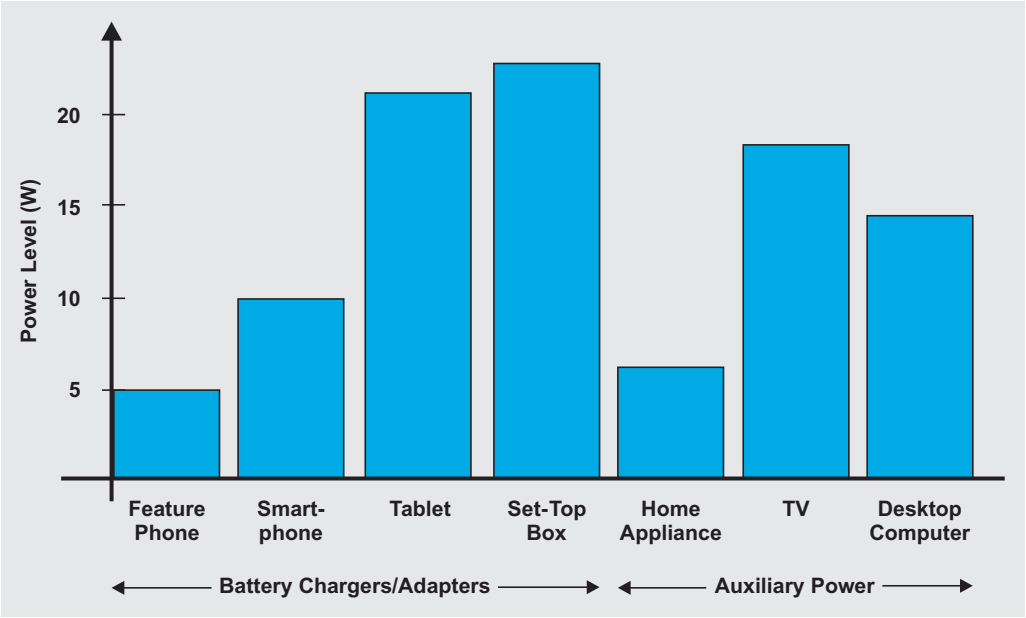
For low-power AC/DC conversion, flyback topology remains the preferred choice due to its simplicity and low cost. Using a small number of external components, this topology can provide one or more outputs for a very wide input-voltage range. It is used in isolated and non-isolated forms to cover a broad range of applications, such as battery chargers in smartphones and tablets; auxiliary power supplies in TVs, desktop computers, and home appliances; AC adapters for portable computing, set-top boxes, and networking; and many more. Figure 1 shows the typical power levels in some of these applications. The widespread applicability and use of the flyback topology in high-volume consumer markets (estimated 2012 worldwide shipments for the markets shown in Figure 1 alone exceeded a few billion units) make it a perfect candidate for optimizing every possible performance specification, such as cost, efficiency, and standby power.

In most applications, flyback converters are stand-alone external power supplies in wall chargers/adapters. In some cases they are powering either a portion of larger equipment or providing standby power to maintain system functions like the user display and remote control when the equipment is not performing its primary function. In all cases, the standby-power consumption of the flyback converter is being heavily scrutinized to minimize the overall power drain when it seems the converter is doing nothing. For example, a flyback power supply used in an AC wall charger may have a mass-production specification of less than 30 mW. If the actual supply consumes only 10 mW of standby power, the 20-mW difference can allow a higher margin for leaky circuit components such as input filters, capacitors, and bias components, reducing overall solution cost. Similarly, a flyback converter with low standby-power consumption can allow more system functions to be active in standby mode while keeping the end equipment's total power consumption to a minimum.

The push towards green power

There is an array of initiatives and directives in the power industry addressing efficiency and standby power that vary by end equipment, power level, and governing authority. In the U.S., these include the California Energy Commission and the Environmental Protection Agency's ENERGY STAR®,[1] and in Europe, the European Union's Standby Initiative, to name a few. After a quick glance at many of these energy-conservation initiatives, it is clear that they all have a common theme—driving minimal power loss at light loads and no-load/standby. Many

Figure 1. Typical power levels for AC/DC flyback-converter designs



regions in the world are also introducing mandatory and voluntary limits for standby-power consumption and light-load operating efficiency of external power supplies.

In the U.S., the California Energy Commission adopted for its own state a battery-charging efficiency standard that became effective in February 2013. Additionally, the U.S. Department of Energy is finalizing a draft that will affect current regulations for power-supply efficiency worldwide. Similarly, the Joint Research Centre of the European Commission (EC) published the final draft of Version 5 of its Code of Conduct on Energy Efficiency of External Power Supplies in October 2013. These new voluntary specifications, which propose tightening of active-mode efficiency and no-load power consumption, are tougher to meet than the mandatory specifications of the EC's current Ecodesign Directive.

To ensure that the external supply is efficient in the idle and standby modes of some applications, the EC has added an additional efficiency requirement at 10% load beyond the four-point active-mode average-efficiency requirement. The EC also has added an additional classification for mobile handheld battery-driven external supplies of less than 8 W that must limit no-load power consumption to less than 75 mW starting in 2014. Finally, the EC's Ecodesign Directive for energy-related products, Lot 6, Tier 2 took effect in January 2013. This part of the directive limits total system standby-power consumption of household and office equipment to less than 0.5 W.

Less than 10 mW of standby-power consumption

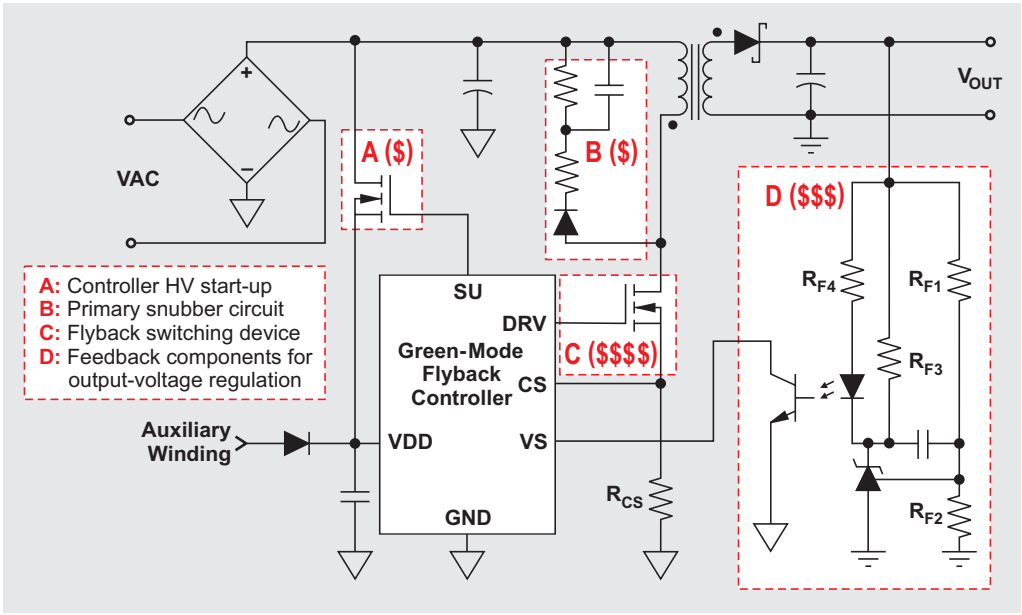
The typical architecture for an isolated flyback converter that consumes less than 10 mW of standby power is shown in Figure 2. Four key elements (labeled A through D) in a flyback that contribute most to its standby-power loss are shown along with their relative cost. Traditionally, this type of converter compares its output voltage with a secondary-side reference. An optoisolator is used to transfer an error signal across the isolation barrier.

There are two fundamental issues with this approach. First, a low-cost reference like the widely used TL431 shunt regulator from Texas Instruments (TI) needs a minimum cathode bias current (~1 mA) independent of converter loading under all conditions. Second, the standard optocoupler configuration is such that it consumes the most current under no-load conditions. Note that in order to achieve standby-power consumption of less than 10 mW, a more expensive reference such as TI's TLV431 shunt regulator with very low bias current may need to be used for feedback control.

One way to address these issues is to use a constant-voltage, constant-current (CVCC) controller with primary-side regulation, such as TI's UCC28710. This type of controller can simplify and improve performance in AC/DC designs. The UCC28710 regulates the flyback output voltage and output current within 5% accuracy without optocoupler feedback. It also processes information from the primary power switch and transformer auxiliary winding for precise output CVCC control.

To reduce its no-load consumption, the controller enters smart sleep modes as the converter load decreases and the controller reduces its average current consumption down to 95 µA. The control algorithm modulates the converter's switching frequency and the primary current's peak amplitude while maintaining MOSFET valley switching for high conversion efficiency across line and load. Finally, thanks to high-voltage IC technology, the external HV start-up

Figure 2. Conventional AC/DC flyback consumes less than 10 mW of standby power



MOSFET is also integrated into the controller to further reduce component count and simplify the solution (Figure 3a).

The choice of a flyback converter switch is very application-specific and performance-driven. In some situations, a bipolar junction transistor (BJT) can be a better choice than a MOSFET. Fundamentally, BJTs cost less than power MOSFETs because their fabrication involves a simpler process with fewer layers, particularly for high-voltage (≥700-V) and low-power applications. BJTs with very high voltage (>900 V) are economical options today, making BJT-based designs attractive in off-line power supplies for the industrial market and in regions with widely varying AC utility voltages.

Converters with BJTs can have lower manufacturing cost because they normally have less di/dt and dV/dt switching stress, EMI compliance is easier with no Y capacitor, no common-mode choke is required, and transformer construction is simpler. Also, due to slow di/dt at turn-off, some energy in the transformer's leakage inductance can be dissipated at the BJT turn-off transition, potentially eliminating snubber circuits in some designs. On the flip side, BJTs suffer from higher switching losses, are limited to designs with lower switching frequencies, and require a complex drive scheme.

A highly integrated solution for driving a BJT is shown in Figure 3b. The UCC28720 controller incorporates a driver that dynamically adjusts the base-current amplitude based on the converter load. This ensures that the BJT always operates in optimal switching conditions with minimal switching and conduction losses even for higher-power AC/DC designs.

Figure 3. Simplified flyback schematics

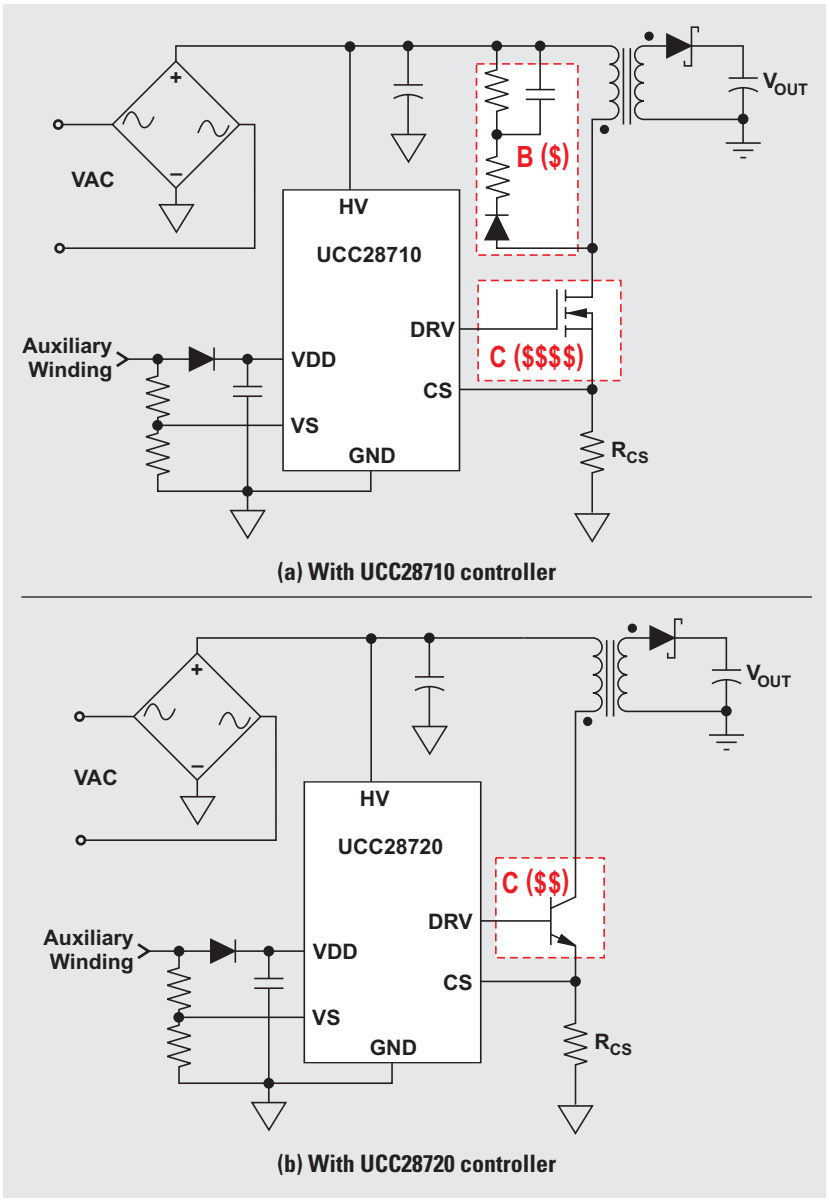
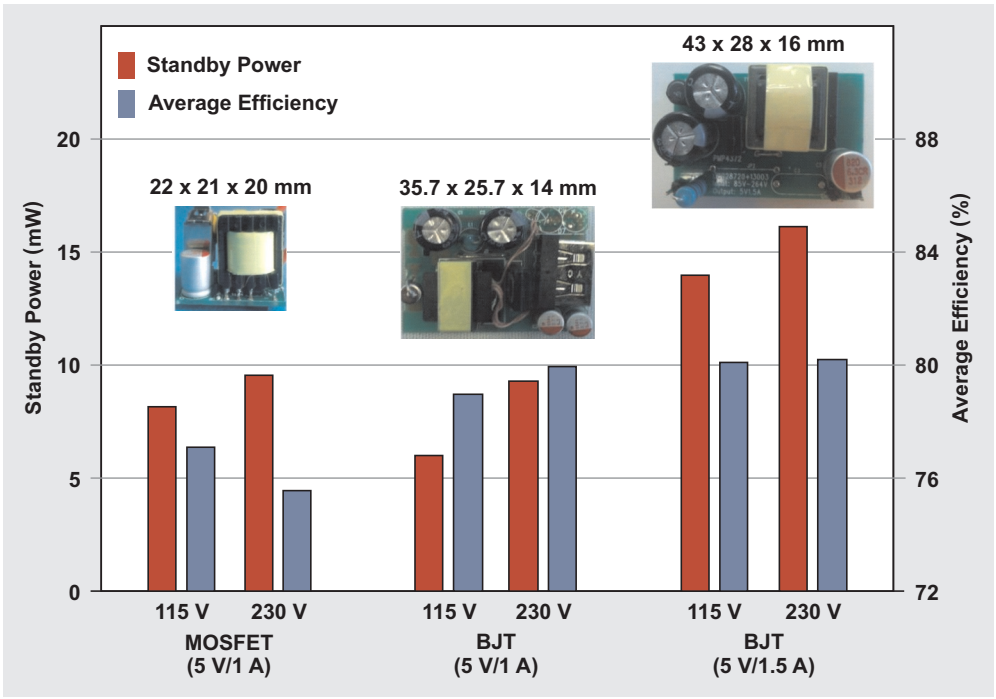


Figure 4. Summary of test data for AC/DC flyback designs with UCC287xx controllers



Two 5-V/1-A USB chargers were designed to illustrate some of the preceding points. Their test data are summarized in Figure 4. Note that the controllers enable ultralow standby-power consumption of less than 10 mW. Optimized modulation and drive schemes also facilitate achieving high average efficiency to meet the most stringent worldwide regulations. References 2 and 3 provide links to full test data and a bill of materials for these designs. Test data for a higher-power 5-V/1.5-A design is included in Figure 4 to illustrate that this BJT-based solution can provide an average efficiency of 80+%.[4]

Conclusion

The simplicity and cost-effectiveness of the flyback topology have made it the preferred choice for the many low-power AC/DC designs powering consumer electronics. Power-supply designers are continuously challenged to achieve the same performance at lower cost or improved performance at the same cost. This article has touched on a few of these performance aspects and how th e cost of the power-supply solution can be addressed with the smart choice of a power-efficient controller. The UCC28710 and UCC28720 members of TI's 700-V flyback-controller family enable cost-optimal designs with best-in-class standby power and efficiency for compliance with current and future industry standards.

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Accurately measuring efficiency of ultralow-I_Q devices

By Chris Glaser
Applications Engineer

Introduction

While almost every power-supply engineer intimately knows and understands the lab setup for measuring efficiency, there are many important nuances that must be considered when measuring the efficiency of a device with ultralow quiescent current (I_Q). For a device that consumes less than 1 µA, the circuit's currents are very small and difficult to measure. These measurements may equate to calculated light-load efficiencies that are far lower than what is shown in the datasheet graphs and lower than what would be seen in the real application. This article reviews the basics of measuring efficiency, discusses common mistakes in measuring the light-load efficiency of ultralow-I_Q devices, and demonstrates how to overcome them in order to get accurate efficiency measurements.

Basics of measuring efficiency

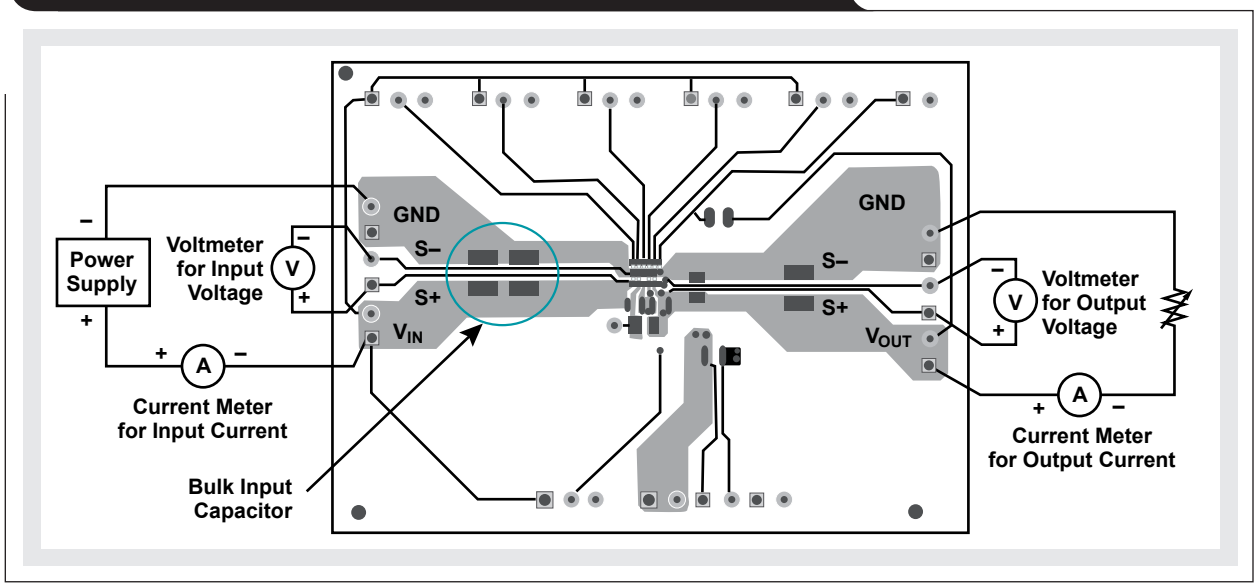
Reference 1 details the best setup to accurately measure a device's efficiency with a power-save or pulse-frequency-modulation (PFM) mode. This reference provides an excellent background to the topics covered in this article and should be read first. Generally, and especially in this article, efficiency is defined as

$$\eta\,(\text{efficiency}) = \frac{\text{Power}_{OUT}}{\text{Power}_{IN}} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times I_{IN}}.$$

The following summarizes two key points made in Reference 1. The first is that any power-save mode draws relatively large bursts of current from the input supply. These bursts are an AC current from the input. Devices that always operate in continuous-conduction or pulse-width-modulation (PWM) mode draw DC currents from the input supply. Unlike the DC current drawn in PWM mode, the power-save mode's bursts of current create an incorrect RMS-current reading in the input-current meter. Therefore, the proper test setup for measuring efficiency in power-save mode includes sufficient input capacitance after the input-current meter to smooth out the AC currents drawn by the PFM mode in order to present a DC current to the current meter.

The second key point in Reference 1 regards the placement of the voltmeters relative to the current meters. It is critical in both PFM and PWM modes not to include the voltage drops across the current meters in the efficiency calculations. Therefore, each voltmeter should be connected to the input and output voltages on the PCB, ideally at the S+/S– header on most evaluation modules (EVMs). This places the input-current meter out of the circuit and the output-current meter as part of the load. These placements are shown in Figure 1 with the recommended setup for measuring PFM-mode efficiency with the best accuracy.

Figure 1. Recommended setup for measuring PFM-mode efficiency



Setup issues in measuring efficiency of an ultralow-I_Q device

Devices with an ultralow I_Q have special considerations for their efficiency-measurement setup. For simplicity, ultralow I_Q can be approximated as less than roughly 10 µA of I_Q. Below this level, the input current drawn by one or both voltmeters, as well as the leakage current of the additional input capacitor, can substantially affect the measured input current and thus the calculated light-load efficiency. Note that if higher-leakage equipment is used, these concerns also would be relevant for higher-I_Q devices. Reference 2 explains I_Q in detail.

Input resistance of the input voltmeter

In the test setup in Figure 1, the two voltmeters have some finite input resistance. For example, the standard handheld, battery-powered Fluke digital multimeter (DMM) has an input resistance of around 10 MΩ. While this certainly seems very large and unlikely to affect the efficiency measurement, calculating how much current it draws when it measures a very common 3.6-V input voltage can be revealing. In this case, when 3.6 V is applied to the DMM's terminals (across its resistance), 0.36 µA of current flows into the meter. This is effectively 360 nA of leakage current that is drawn directly from the input voltage applied to the device and flows through the input-current meter. Just attaching the input voltmeter to the circuit increases the input current by 360 nA. If the measured device has a 20-µA I_Q, then this 360 nA is less than 2% of the input current and is not very significant. But, if a step-down converter like the Texas Instruments (TI) TPS62740 with its 360-nA I_Q is being tested, then this extra current drawn by the voltmeter could be up to half of the input current. This results in quite a large difference in efficiency.

Extra load current through the output voltmeter

A voltmeter connected on the output behaves in the same way. It draws some extra (leakage) current not measured as part of the load's current. This leakage current is not included in the numerator in the efficiency calculation. The output voltmeter creates an extra load, which draws an extra (and measured) input current. With this extra unmeasured load current creating an increased input current, the measured efficiency is lower than the actual efficiency.

High leakage current of the extra input capacitor

Finally, the additional input capacitor used to smooth out the input current might have a sufficiently high leakage to draw substantial current from the input. For example, some high-capacitance capacitors have maximum leakage currents in the hundreds of microamperes. This leakage may change over time, so it should be checked before any efficiency testing. This extra current, if too high, is sure to throw off the efficiency calculations.

Solutions to measurement-setup issues

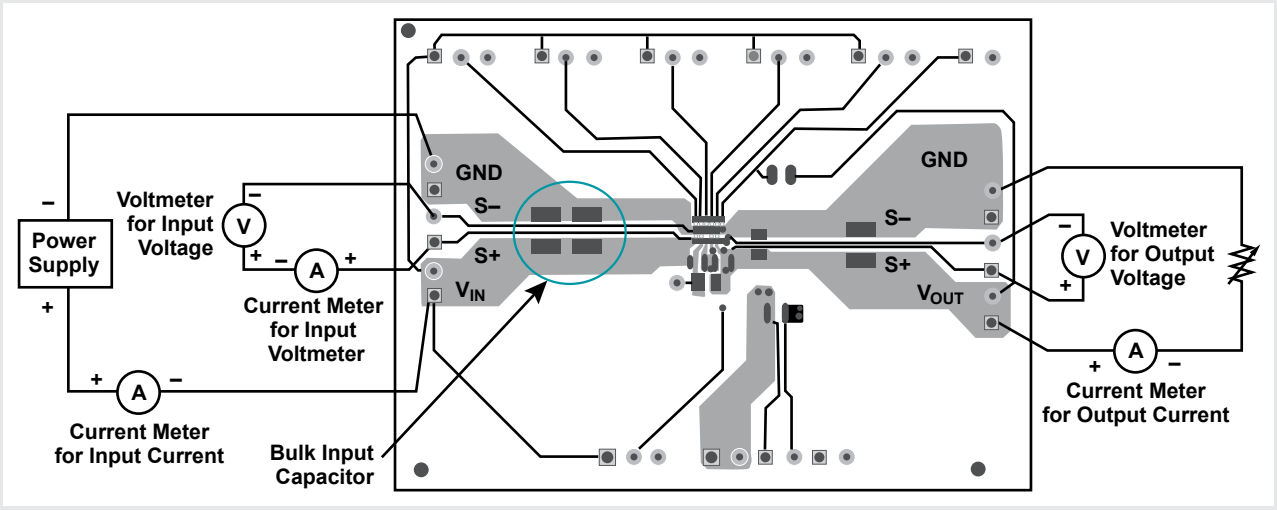
There are easy solutions to the three measurement-setup issues just described. The most important point, however, is simply to be aware that the setup used to take efficiency data can cause inaccuracies in the efficiency data collected. This is especially true at light loads, where the currents are very small and difficult to measure.

Overcoming the effects of the input voltmeter's input resistance

There are three methods of accounting for current leakage through the input voltmeter: (1) disconnecting the voltmeter, (2) connecting it in a different location, or (3) compensating for the current into it. The first and simplest method is to record the input voltage with the voltmeter connected as usual and then disconnect the voltmeter from the input terminals before recording the input current. This accurately measures the input voltage without increasing the input current. Minimal measurement inaccuracy is introduced by this method. What is not advisable is to read the input voltage from the display on the input supply (which typically is not calibrated) and use this value for the efficiency calculations. Rather, a high-quality, high-resolution voltmeter should be used to measure the input voltage at the EVM. This overcomes small voltage drops in wires and cabling between the input supply and the EVM.

The second method of accounting for the leakage current is to connect the input voltmeter in a different location. Specifically, the voltmeter's positive lead can be connected to the input-current meter's positive side, while the voltmeter's ground lead remains connected to the same location as before (the S– header on the EVM). In this way, the input voltmeter does not draw any measured current and so does not affect the calculated efficiency. The downside of this method is that the voltage drop across the input-current meter is not accounted for. At very light loads, however, such a drop is usually insignificant. To minimize this inaccuracy at heavier loads, the input voltmeter can be moved to its original location (after the input-current meter) once the measured input current is about 100 times greater than the leakage current into the voltmeter. This allows for a simple setup where the input voltmeter remains connected throughout testing and inaccurate measurement is minimized.

Figure 2. Efficiency-measurement setup to compensate for leakage into the input voltmeter



The third method of accounting for the leakage current into the input voltmeter is to measure the current through it with an additional current meter (Figure 2). The current through this new current meter is subtracted from the measured input current. The result is used to compute the efficiency. This is the most accurate way of accounting for the leakage current into the input voltmeter. The computed efficiency is highly accurate because the input voltmeter remains connected where it should be throughout the entire testing. Furthermore, assuming that the input voltage is not varied considerably throughout testing, the leakage current also remains fairly constant. This fact allows for a single measurement of the leakage current to be made at a given input voltage and for this value to be used for all data points in the efficiency testing. In other words, it is not necessary to record the data of this extra multimeter for all measurement points.

Overcoming the extra load current through the output voltmeter

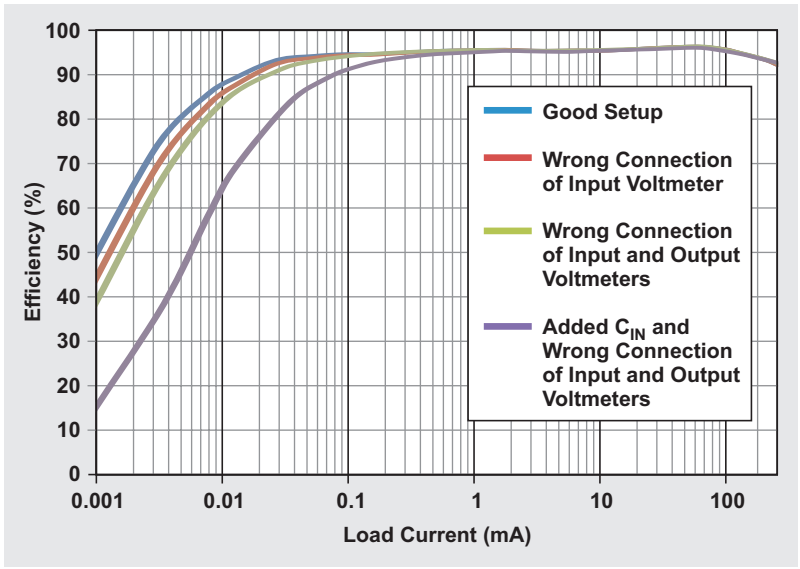
The leakage current into the output voltmeter can be accounted for in the same three ways as for the input voltmeter. The first method (disconnecting the output voltmeter) can be used in exactly the same way—connecting the voltmeter as usual, reading the output voltage, then disconnecting it and reading the input current. The second method (connecting the voltmeter in a different location) is slightly different for the output voltage. In this method, the output voltmeter should be connected after the output current meter so that its current sums with the load's current to give the total output current. Once the load current is about 100 times greater than the leakage current into the output voltmeter, the voltmeter can be moved back to its usual location on the S+/S– header. The third method (compensating for the current drawn by the voltmeter) can be used in the same way as for the input voltmeter. Note that for this method the load current used to graph the efficiency data should be the sum of the current into the load and the leakage current into the output voltmeter. Not accounting for this may slightly shift the efficiency graph on the load-current axis.

Of course, the best way to eliminate errors from leakage currents into the voltmeters is to use voltmeters with extremely low leakage currents. For example, the efficiency data in the TPS62740 datasheet[3] was taken with Agilent 34410A multimeters. Their 10-GΩ input-resistance setting was used for the voltage measurements, producing a negligible amount of leakage current with no effect on the calculated efficiency.

Minimizing leakage current from the extra input capacitor

Finally, the leakage of the input capacitor is best mitigated by choosing a proper bulk input capacitor. X5R or X7R dielectric ceramic capacitors and their inherent low-leakage currents are recommended for measuring ultralow-power efficiency, as the ceramic technology used in these capacitors produces the lowest leakage currents. If the voltage is too high for a ceramic capacitor, then a low-leakage-current polymer or tantalum capacitor should be used. It is important to consult the datasheet of the chosen capacitor to determine if its leakage might cause measurement errors. It is also important to measure the leakage current of the exact capacitor used in the efficiency testing.

Figure 3. Efficiency comparison of different test setups



Test results of efficiency-measurement setups

Figure 3 compares the measured efficiency of several different test setups that used the TPS62740EVM-186 evaluation module.[4] A proper test setup with a 100-µF ceramic bulk input capacitor was used, with compensation for the leakage current into the input and output voltmeters. This bulk input capacitance was sufficient to produce accurate results, as was evidenced by a DC input current. If longer wires from the input supply with their larger impedance had been used instead, the input-current shape might have changed to be more sinusoidal. This would have produced an inaccurate input-current reading and shows that more bulk input capacitance would have been required for an accurate measurement.

Figure 3 also shows the test results of three improper test setups: the input voltmeter's leakage not accounted for, the output voltmeter's leakage not accounted for, and an extra input capacitor with about 5 µA of leakage. For the three improper test setups, the wrong configurations build on one another; they are additive. The wrong connection of input voltmeter used the correct input capacitor as well as the correct output voltmeter. The wrong connection of input and output voltmeters used the correct input capacitor. The setup using the leaky input capacitor also used the wrong connection for the input and output voltmeters. As expected, less accurate efficiency measurements were obtained with worse test setups.

Other considerations in measuring efficiency

With an understanding of the impact that measurement setups have on measuring an ultralow-I_Q device's efficiency, there are two final considerations that deserve a mention: the remote-sense lines on the input supply, and the use of external or internal feedback resistors. Though less commonly seen, each of these has an impact on efficiency.

An input-power supply with remote-sense capability is sometimes used in efficiency-measurement test setups to provide a regulated input voltage as the load and voltage drop across the input-current meter change. However, just like the input voltmeter, these remote-sense lines draw current. In many instances, this current is relatively large—sometimes in the hundreds of microamperes. Needless to say, such high currents drawn by the test setup certainly affect the calculated efficiency and produce erroneous results. Therefore, for best results, the remote-sense lines of the input supply should be connected *before*, not after, the input-current meter.

A final consideration in measuring the efficiency of ultralow-I_Q devices is whether to use external or internal feedback resistors to set the output voltage. Most power supplies use two external resistors between the output voltage, FB pin, and ground to set the output voltage. This gives the user full flexibility to set the output voltage at any desired point. However, with external resistors and the highly sensitive external FB pin come more susceptibility

to noise. Any external noise seen at the FB pin is gained up, resulting in an incorrect output voltage. To avoid this, the two feedback resistors typically should have between 1 and 10 µA of current flowing in them to keep them robust against external noise sources. Since this current is not flowing to the load, it should be considered a loss that results in decreased efficiency.

To keep efficiency high, the FB pin and two resistors should be located inside the power supply to remove them from the variable and noisy external environment. In this way, a large resistance with minimal current flow is used for the feedback resistors, and efficiency is not significantly lowered. While internal feedback resistors fix the output voltage inside the power supply and prevent the user from having every possible output voltage available, a step-down converter like the TPS62740 overcomes this limitation. It has four digital input pins that allow the user to choose from among the most common output voltages ranging from 1.8 V to 3.3 V. As well, many other TI TPS62xxx devices internally set the output voltage to be either completely fixed (as in the TPS62091) or adjustable via I^2C (as in the TPS62360). These low-I_Q devices are preferred because they do not lower the efficiency with external resistors but still allow sufficient user configurability.

Conclusion

Accurately measuring the efficiency of ultralow-I_Q devices is difficult because the currents in the circuit are very small. The basic efficiency-measurement test setup must be slightly altered to achieve accurate measurement results that reflect the capability of the real circuit in the final application. Accounting for and/or eliminating the various leakage currents in the measurement equipment is the key to an accurate measurement.

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When is the JESD204B interface the right choice?

By Sureena Gupta
Worldwide Analog Marketing

Introduction

Anyone involved in high-speed data-capture designs that use an FPGA has probably heard the buzzword for the new JEDEC standard: JESD204B. Recently a lot of engineers have contacted Texas Instruments requesting information on the JESD204B interface, including how it works with an FPGA and how it will make their designs easier to execute. So what is the JESD204B interface all about? This article discusses the evolution of the JESD204B standard and what it means to a systems design engineer.

What led to the JESD204B standard?

About ten years ago, designers of high-speed data converters switched from using the traditional single-ended CMOS interface to using a differential LVDS interface because the latter enabled higher data rates. (The CMOS interface is limited to about 200 Mbps.) The LVDS interface also improved noise coupling on signal lines and power supplies. The drawback of this interface was higher power consumption at lower sampling speeds. This gave the CMOS interface a reason for existence, and it is still being used today.

But with the evolution of analog-to-digital converters (ADCs) requiring faster sampling rates and higher channel density, the industry was demanding a faster, more power-efficient digital interface than parallel LVDS. In order to overcome this challenge, a true serial interface called JESD204 was developed and approved by JEDEC in April 2006. The JESD204 interface is defined as a single-lane, high-speed serial link connecting single or multiple data converters to a digital logic device with data rates of up to 3.125 Gbps. It needs a common frame clock sent to the converter and the FPGA to synchronize the frames.

Supporting only one lane and one serial link, JESD204 was soon viewed as not quite as useful as initially hoped, so in April 2008 the standard was revised to JESD204A. JESD204A extended support for multiple aligned lanes and multipoint links, but the maximum speed was still limited to 3.125 Gbps. This drove the development in July 2011 of JESD204B, which promises to address several different system-design challenges. Besides drastically increasing the supported data rates from 3.125 Gbps to 12.5 Gbps, it also greatly simplifies multichannel synchronization by adding the deterministic latency feature.

What is the JESD204B standard?

JESD204B supports interface speeds of up to 12.5 Gbps, uses a device clock instead of the previously used frame clock, and has three different subclasses. Subclass 0 is backward-compatible with JESD204A except with higher speeds, and it does not support deterministic latency. Furthermore, the SYNC signal has special timing requirements for error reporting (Figure 1). Subclass 1 uses synchronization signal SYSREF to initiate and align the local multiframe clocks across devices (Figure 2). This

Figure 1. JESD204B Subclass 0 interface

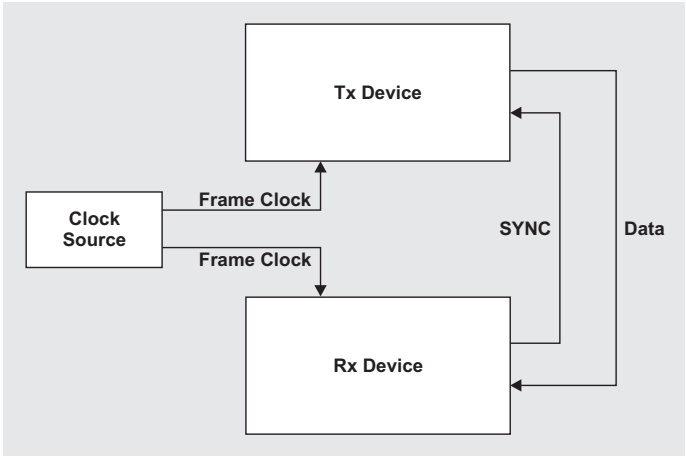
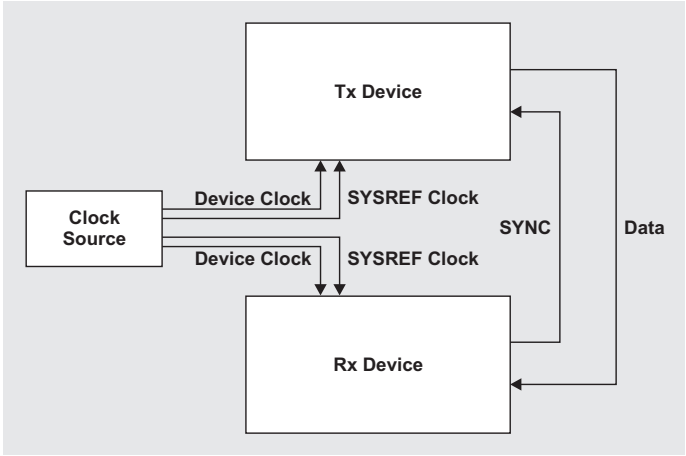


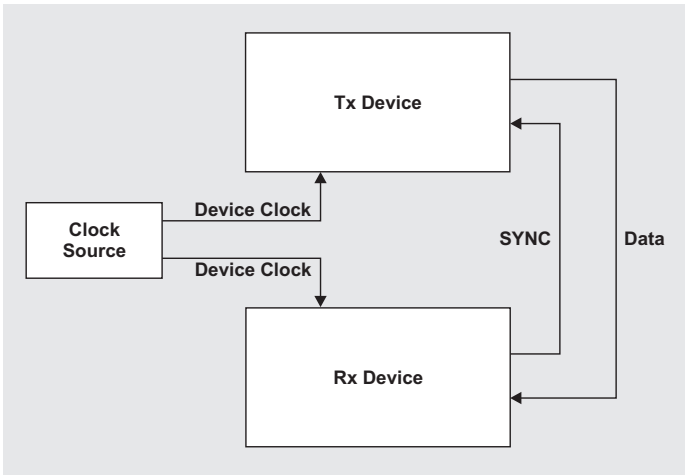
Figure 2. JESD204B Subclass 1 interface



synchronizes data transmission and achieves a known, deterministic latency across the digital link. Subclass 2 uses the SYNC signal for that same purpose (Figure 3). Due to SYNC timing constraints, Subclass 2 typically is employed for data rates lower than 500 MSPS. For speeds higher than 500 MSPS, Subclass 1 with an external SYSREF clock is commonly preferred.

JESD204B-compliant receivers are outfitted with an elastic buffer that is used to compensate for skew across serializer/deserializer (SerDes) lanes, which simplifies board layout. This elastic buffer stores the data until the data from the slowest lane arrives. It then releases the data from all lanes simultaneously for digital processing. This skew management is possible because the data clock is embedded in the serial data stream.

Figure 3. JESD204B Subclass 2 interface



Why care about the JESD204B interface?

Since JESD204B-compliant data converters serialize and transmit output data at a much higher rate than with previous interfaces, the number of pins required on the data converters as well as on processors or FPGAs is drastically reduced, translating to smaller package sizes and lower cost. However, the biggest benefits from the reduced pin count may be a much simpler layout on the printed circuit board (PCB) and easier routing because there are much fewer lanes on the board.

Layout and routing are further simplified by the reduced need for skew management, which is made possible by the data clock now being embedded in the data stream and the presence of the elastic buffer in the receiver. Hence, the need for trace squiggles to match lengths is eliminated. The JESD204B standard also allows longer transmission distances. Relaxed skew requirements enable logic devices to be placed much farther from data converters to avoid any impact on sensitive analog parts.

Additionally, the JESD204B interface is adaptable to different resolutions of data converters. This removes the need for physical redesign of transceiver/receiver (Tx/Rx) boards (logic devices) for future ADCs and digital-to-analog converters (DACs).

Does this mean the end for the LVDS interface?

The CMOS interface provides lower power consumption for data converters with lower data rates, while the JESD204B interface offers a few benefits over the traditional LVDS interface. So does the LVDS interface have any chance of survival?

The simple answer is yes. While the JESD204B standard has simplified multichannel synchronization by using deterministic latency, there are applications that require minimal latency (and, in an ideal world, no latency). These applications (for example, aerospace applications like radar) need an immediate response to an action or detection. Any possible delay must be minimized. For these applications, the LVDS interface should be considered, since the JESD204B-compliant data converter's delay in serializing the data is omitted.

Conclusion

This article has discussed the evolution of the JEDEC JESD204B standard and has explained the many benefits of using this type of interface, including faster data rates, simplified PCB layout, smaller package sizes, and lower cost. It is hoped that the reader now understands the JESD204B-based system a little better.

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CAN bus, Ethernet, or FPD-Link: Which is best for automotive communications?

By Mark Sauerwald
Applications Engineer

Introduction

In 1915 Ford Motor Company introduced electric lights and an electric horn to its Model T automobile. Since then, the dependence on electrical and electronic systems in automobiles has been steadily increasing. The initial systems tended to be local and independent. For example, a switch that controlled the headlights was connected directly to the battery. Today, however, these systems are all interconnected. When a car's headlights are turned on, the dashboard lighting, mirrors, and other systems may all adjust to the new conditions. For this to work properly, the various different systems must communicate with one another. As the automobile has evolved, so have the networks used within it to make this communication possible. As autonomously driven vehicles continue to be developed, there will be an even greater demand for data transport within the vehicle and between vehicles. This article examines three automotive communications standards—the controller area network (CAN) bus, Ethernet, and Flat Panel Display Link (FPD-Link)—and explores which interface best suits which system.

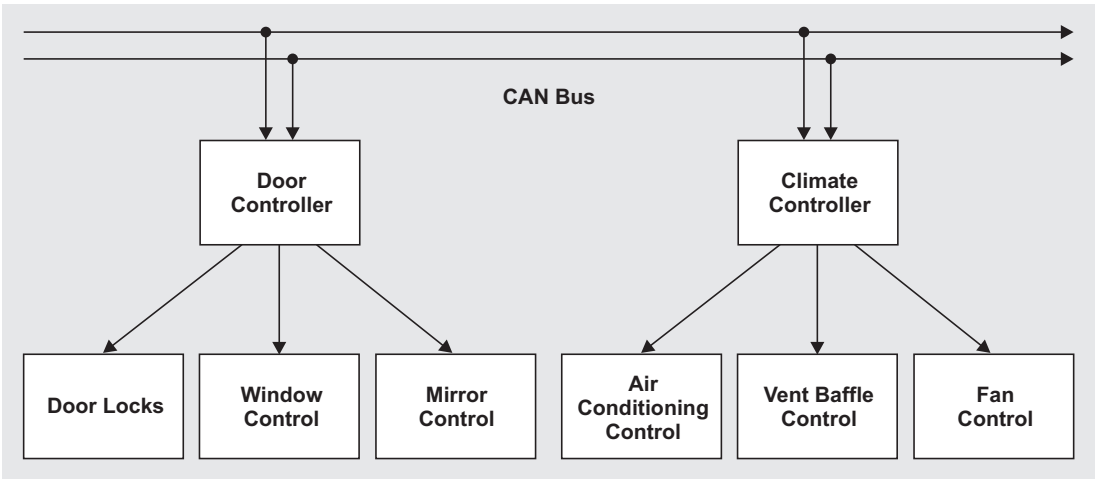
CAN bus

The CAN bus was initially developed by Robert Bosch GmbH in the 1980s. Today it is supported by several manufacturers of integrated circuits and subsystems and is used in all modern automobiles. The CAN bus allows different controllers or processors on the bus to communicate with one another via messages that are passed on the bus. There is a method for prioritization so that lower-priority messages do not interfere with higher-priority messages. The CAN bus operates at speeds of less than 1 Mbps, and message lengths (CAN frames) are typically 50 to 100 bits in length.

Since a CAN bus can be shared by many different controllers, it is generally not very good for sending messages that might require updates more than approximately 100 times per second. Ideally it is suited for relaying much slower status updates from sensors to the engine-control unit. This includes applications such as communication about other mechanical systems (transmission, braking, cruise control, power steering, windows, door locks, and others) where the amount of data is limited and the bandwidths involved tend to be relatively low.

Further reducing the overall transmission speed is the fact that automotive systems have become more complicated, with more sensors and processors being added to the network. Figure 1 shows a CAN bus being used for both door- and climate-control functions. Since each of these is a low-bandwidth application, there is little concern about one interfering with the other. However, if the same bus is also handling a higher-bandwidth, more critical function

Figure 1. Portion of a CAN-bus implementation



such as engine control, the priorities of door and climate control need to be set low enough so that these functions do not interfere with engine control.

The net result is that the CAN bus is well suited as a communications network between the mechanical sensors and systems within a car, but it is not readily extended to the higher-bandwidth requirements of applications such as entertainment systems or sensors for cameras or radar.

Ethernet

Ethernet is one of the most common high-speed interfaces found in homes and offices, and there are some automobiles where Ethernet is being used to transport a variety of high-speed data. Like the CAN bus, Ethernet is a packetized system, where information is transferred in packets between nodes on various parts of the network. Also like the CAN bus, Ethernet is bidirectional, and the speed possible on any individual link decreases as the number of nodes on the system increases. Still, Ethernet can transport data over a link 100 times faster than a CAN bus.

Ethernet is good for midbandwidth communications in applications such as navigation systems and control. It can be used in much the same way as a CAN bus while providing much more bandwidth. Ethernet would be an ideal choice to replace the CAN bus, but since Ethernet's cost per node is higher, it probably will not replace but rather will augment the CAN bus.

Some cars today are using Ethernet for data-intensive requirements such as backup cameras and entertainment systems. Of particular interest in automotive applications is the DP83848Q-Q1 from Texas Instruments (TI). This is an Ethernet PHY, screened to AEC-Q100 grade 2, and includes a loopback test mode for facilitating system diagnostics.

To transport video over an Ethernet network, even if there is only one video channel being transported, the video must be compressed at its source, then decompressed at the destination to avoid exceeding Ethernet bandwidth limitations. For an application such as a backup camera, this implies that there needs to be a relatively high-power processor in the camera to compress the image sufficiently to get it into the Ethernet network. This in turn means that the camera will be physically larger and more expensive and will have higher power dissipation than a solution that doesn't require much image processing. Another disadvantage of this solution is that video compression and decompression add latency to the link.

If the same Ethernet network is shared by several cameras or other video sources in the car, there is a trade-off between the amount of compression (and corresponding video quality) and the number of video channels that can be supported. This limitation could be mitigated by setting up multiple networks within the car in a hierarchical configuration. There might be one network that deals only with engine control and diagnostics, a second network that handles backseat entertainment and the audio system, and another network that handles driver-assist functions such as vision-enhancement cameras. In the end, Ethernet provides greater capacity than the CAN bus, at the expense of greater complexity, but still struggles to handle the highest-bandwidth applications such as video.

FPD-Link

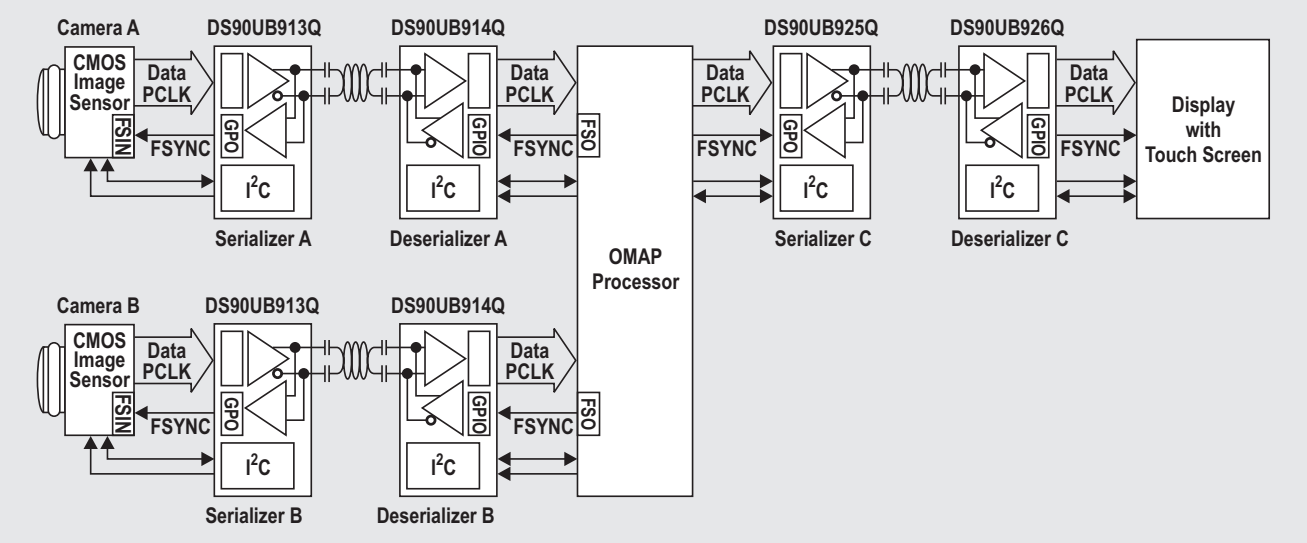
FPD-Link is a technology developed for point-to-point transport of high-bandwidth data. It has one forward channel with a very high speed of several gigabits per second and a low-speed back channel. The back channel can be used to transport an I^2C bus at 400 kbps or it can control GPIO lines at rates of up to 1 Mbps. FPD-Link was developed to transport video data within the car. For example, it can be used to send uncompressed video to a video display while the back channel sends information from a touch panel on the display screen back to the processor generating the video. The physical layer for FPD-Link is either a twisted-pair or coaxial cable. The wiring is dedicated, so if FPD-Link is used for a backup camera, one cable goes from the backup camera to a processor, and a second cable goes from the processor to the display in the cabin.

The big advantage of using FPD-Link in this application is that both the camera and the display can be much simpler circuits, since compression and decompression are not required. Additionally, since the links are dedicated, the image quality of one video system is independent of what else is going on in the vehicle. The back channel can be used to configure a camera, operate a zoom lens, or send touch-screen information back to a controller without interrupting video flow on the forward channel.

For autonomously driven vehicles, another important factor will be the amount of latency in the link. The processing required to compress and decompress an image adds to this latency. For an application such as backseat entertainment, a delay between reading the data from a DVD and its display on the screen is not important. However, if the image being transported is from a camera looking for pedestrians in the path of the vehicle, latency may have dire consequences.

FPD-Link is perfect for critical links where high bandwidth and low latency are the most important factors. Additionally, with the ability to support a back channel and power over a single twisted-pair or coaxial connection,

Figure 2. Using FPD-Link to connect dual cameras and display



wiring can be simplified. Figure 2 shows an OMAP™ video processor connected to two different cameras, and a display with a single twisted-pair cable going to each peripheral. This twisted-pair cable supports camera video data and touch-screen/camera-setup data. It can also provide power for the display or camera. Since each link is dedicated to one peripheral, there is no risk of interference between the signals from the two cameras.

Conclusion

So which interface is best for automotive communications? They all are—but each for its own purpose. The CAN bus reigns supreme for low-speed control applications where cost is a driving factor. When bandwidth requirements move up, Ethernet can step in as an enhanced interface to support moderate bandwidth requirements. When the highest bandwidth and lowest-latency link are required, such as for a surround-view camera system providing input to an autonomous vehicle pilot, then FPD-Link is ready to meet the challenge.

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New-generation ESD-protection devices need no V_{CC} connection

By Roger Liang
High Volume Linear

Introduction

As digital and analog ICs grow increasingly sensitive to electrostatic-discharge (ESD) damage due to their shrinking process nodes, discrete ESD-protection diodes have become necessary to guarantee sufficient system-level ESD protection. In the past, the V_{CC} connection was added to diodes to reduce their junction capacitance. With the advent of new diode technology, this is no longer required. This article explains the V_{CC} connection's necessity in the past and the advantages of not having to use it in the present.

ESD is the release of built-up static electricity when two objects of different electric potential come into contact. For example, on a dry winter day, up to 20 kV of ESD can build up simply from packing a printed cuircuit board (PCB) into a foam-lined box. To ensure that electronic end equipment is immune to everyday ESD events, discrete diodes with more robust ESD ratings than the standard 2-kV human-body model (HBM) are often required. The ESD rating of discrete diodes is directly proportional to the area of the diode's p-n junction; however, the bigger the junction, the larger is the parasitic capacitance. In order not to compromise a diode's ESD rating, adding a V_{CC} connection is one IC design technique that effectively decreases the diode's parasitic capacitance, but at the risk of damaging any other device connected to V_{CC}. However, recent improvements in process technologies have allowed diode designers to remove the V_{CC} connection while still guaranteeing a high ESD rating with low capacitance.

Diode characteristics

A diode is the most basic semiconductor device. It is made from a p-type and an n-type junction and has two terminals: an anode at the p-type end and a cathode at the n-type end (Figure 1). When a large enough voltage is applied from the cathode to the anode (reverse biasing), the diode enters its breakdown region and, in theory, can conduct an infinite amount of current at zero resistance. A voltage applied in the other direction (forward biasing) causes the diode to enter its forward-conducting region. Figure 2 shows the IV curve of a basic diode with the anode grounded and voltage swept across the cathode. While there are many types of diodes made for different applications, the topic under discussion is ultrafast-response diodes made for ESD-protection applications. These diodes can respond to a high ESD voltage very quickly and clamp thousands of volts to just tens of volts in a matter of nanoseconds by shunting the ESD current to ground.

There are two contributing factors to a diode's parasitic capacitance: junction capacitance (due to charge variation in the depletion layer) and diffusion capacitance (due to excess carriers in the quasi-neutral region). Junction capacitance dominates in the reverse-biased region, which is the

Figure 1. Construction of a diode

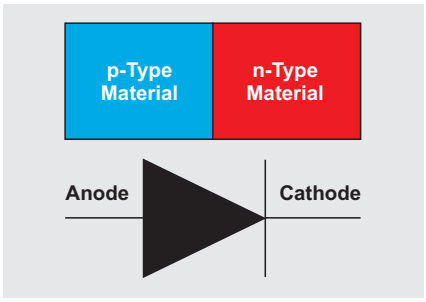
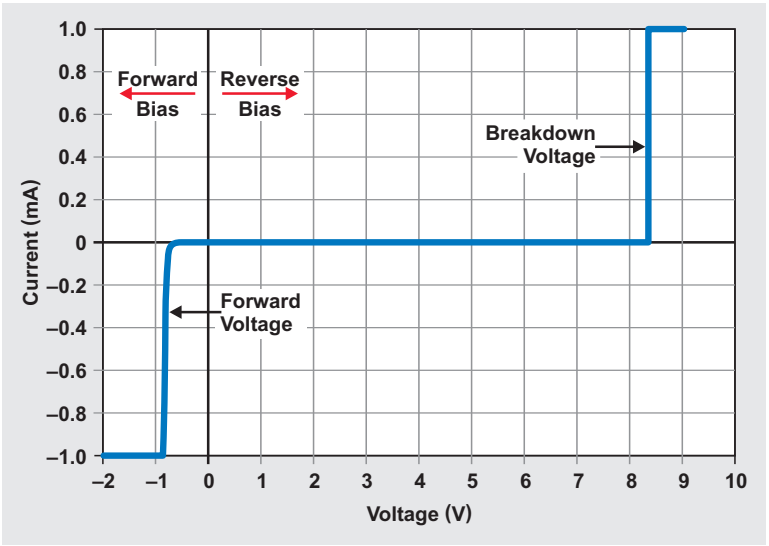


Figure 2. Diode IV curve



usual application region for ESD diodes. The junction capacitance of a diode is characterized by

$$C_j(V) = A\sqrt{\frac{\varepsilon_{Si} q}{2}\left(\frac{N_A N_D}{N_A + N_D}\right)}\left(\frac{1}{\sqrt{\varphi_0 - V_A}}\right),$$

with the following definitions:

A is the area of the junction.
ε_{Si} is the dielectric constant of silicon.
q is one coulomb charge.
N_A is the acceptor doping concentration.
N_D is the donor doping concentration.
ϕ_0 is the built-in voltage of the junction.
V_A is the bias voltage applied on the junction.

On the application level, the more V_A is applied, the lower the junction capacitance will be (Figure 3). This is the reason why older diode technology required a V_{CC} bias in order to adjust V_A and bring down the parasitic capacitance. Having a V_{CC} connection also allows a systems engineer to add a large capacitor at the V_{CC} node (Figure 4), which serves as a charge reservoir to absorb some extra ESD energy, thus increasing ESD protection incrementally.

Figure 3. TPD4E001 capacitance versus bias voltage

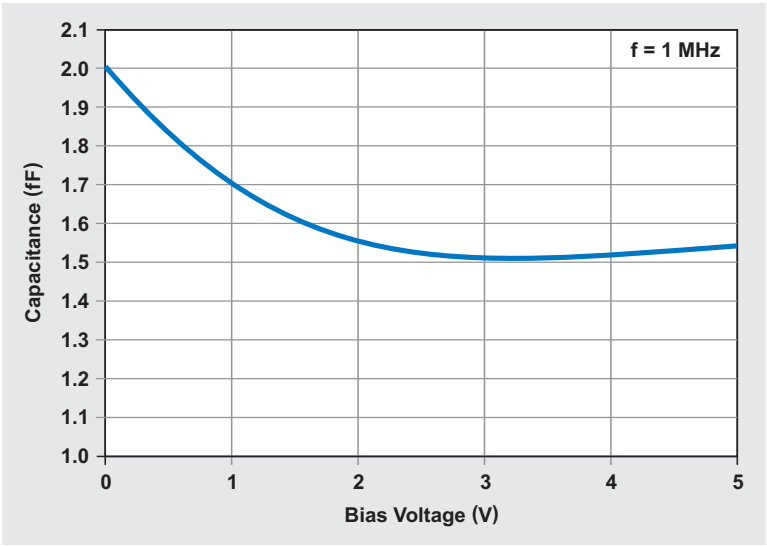


Figure 4. Older diode technology with V_{CC} connection

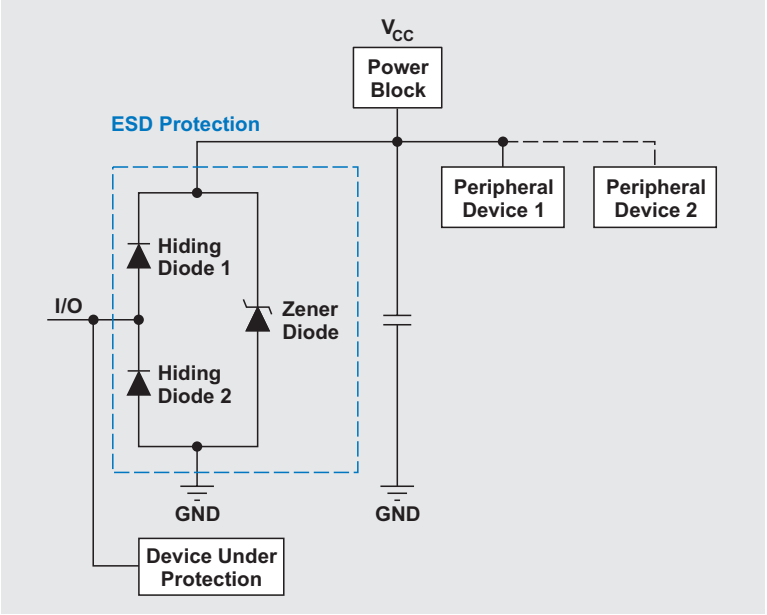


Figure 5. Discharge path of positive ESD strike

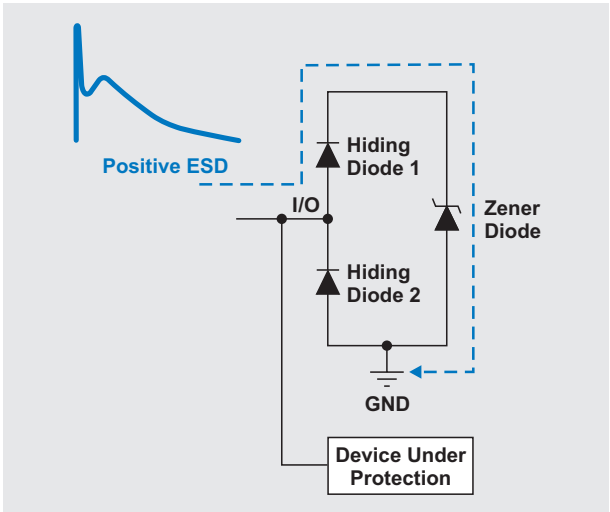
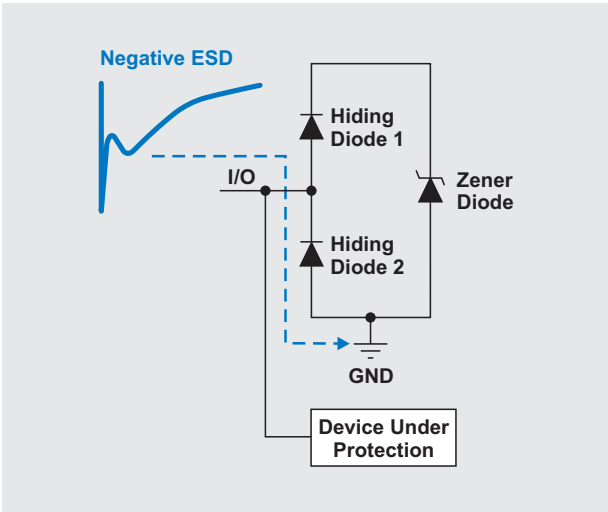


Figure 6. Discharge path of negative ESD strike



Using high-speed diodes for ESD protection

To design a low-capacitance diode structure with a high ESD rating, a three-diode approach often is used (see Figures 5 and 6), for three reasons:

1. A diode can withstand much more current in the forward-conducting region than in the reverse-breakdown region.
2. Hiding Diode 1 with the Zener diode protects against positive ESD strikes.
3. Hiding Diode 2 protects against negative ESD strikes.

Two smaller *hiding* diodes are connected in series with a larger Zener diode because the hiding diodes' smaller capacitance effectively hides the Zener diode's large capacitance due to the series structure. During a positive ESD event, Hiding Diode 1 enters its forward-conducting region. The Zener diode enters its reverse-breakdown region, creating a path for ESD current to be shunted to ground without entering the device under protection. The size of the larger Zener diode allows it to withstand the large amount of current flow in its breakdown region. During a negative ESD event, Hiding Diode 2 enters its forward-conducting region and channels ESD energy directly to ground. During either event, the hiding diodes can handle the large amount of ESD current flow because they never break down and enter only the forward-conducting region.

Advantages of not using a V_{CC} connection

Diode-fabrication technology has made great improvements over the past few years that have enabled a lower junction capacitance without sacrificing a high ESD rating. These improvements are:

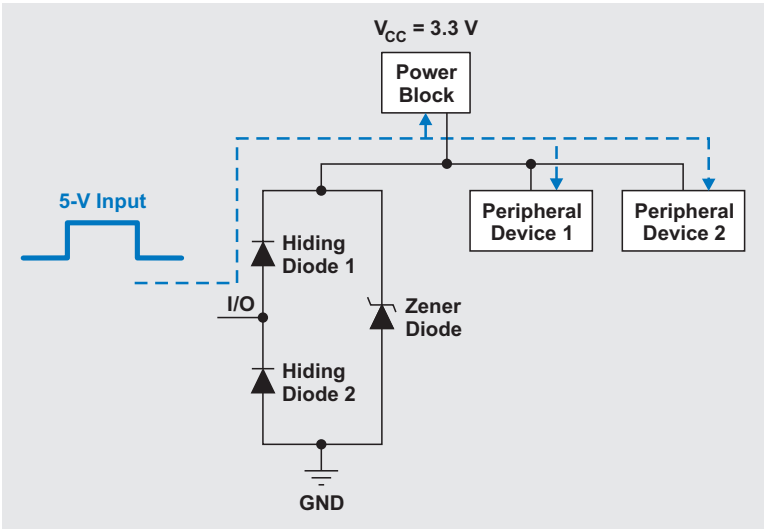
- Moving away from a lateral diode structure to a vertical diode structure
- Increased unit area ESD performance
- Less N_A and N_D doping to reach the same forward and breakdown voltages

These improvements mean a V_{CC} connection is no longer required to bring down the junction capacitance to support high-speed interfaces. Having no V_{CC} connection gives the systems engineer the following three advantages.

1. No current leakage into internal power supply

If a higher-voltage input signal is connected to the ESD diode I/O with a lower V_{CC} level, signal current could leak through Hiding Diode 1 into the V_{CC} and other devices connected on that node (Figure 7). This could damage either

Figure 7. Leakage path from I/O to V_{CC}



the power supply or any device connected to it. If V_{CC} is not connected to the ESD diode, there is no such worry.

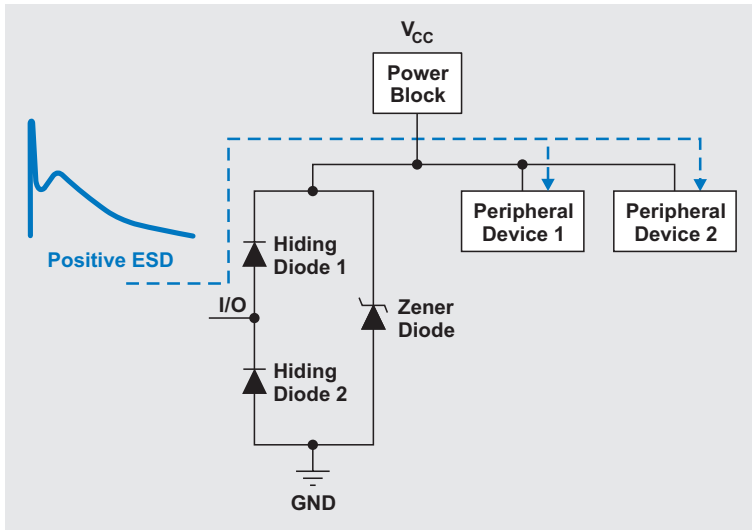
2. No ESD damage to internal power supply

During a positive ESD strike, V_{CC} is along the ESD current's discharge path and experiences a voltage level that is one V_F (~0.5 to 0.7 V) drop below the clamping voltage at the I/O. Although the power supply is very robust against ESD due to the shunt capacitor, this raised voltage level could very likely damage any device powered by the V_{CC} (Figure 8). Again, if V_{CC} is not connected to the ESD diode, there is no such worry.

3. No external capacitor necessary

ESD-diode process development at Texas Instruments (TI) is focusing on strengthening the overall p-n structure so it can withstand more ESD voltage. With TI's new generation of ESD-protection diodes rated as high as 30 kV, an extra capacitor can improve the overall ESD rating only marginally. Using one will generally reach a point of diminishing returns. Not having a capacitor reduces the bill of materials count, saves on cost, and allows more PCB space for other critical devices.

Figure 8. Positive ESD strike can damage V_{CC}



Examples of TI's new-generation ESD-protection devices

TI's TPD2E2U06 ESD-protection device is a noteworthy example of the improvements made in diode technology. Unlike its predecessor, the TPD2E001 does not require a V_{CC} connection but maintains the same capacitance, clamps to a lower voltage, and increases the ESD rating threefold. (See Table 1.) Other similar ESD-protection devices from TI include the TPD4E1U06, TPD4E1U06, and TPD4E05U06.

Table 1. Specifications of TPD2E001 versus TPD2E2U06

SPECIFICATIONS	TPD2E001	TPD2E2U06
V_{CC} connection	Recommended	Not required
Contact ESD (kV)	±8	±25
Air ESD (kV)	±15	±30
C_{IN} (pF)*	1.5	1.5
Clamping voltage (V)**	12	9.5

* Capacitance measured at f = 1 MHz, V_{BIAS} = 2.5 V.
** Clamping voltage measured using TLP curve at 1 A, 100-ns pulse width.

Conclusion

ESD-protection diodes that don't require a V_{CC} connection bring many advantages to the table. No capacitor is needed on the V_{CC} pin to boost the ESD rating; this reduces component count, simplifies layout, and lowers placement cost. Having no V_{CC} connection also guarantees no leakage into the power supply and no ESD damage to any internal nodes that otherwise would be connected to the power supply via V_{CC}.

Related Web sites

Interface:
www.ti.com/interface-aaj

www.ti.com/tpd2e001-aaj
www.ti.com/tpd2e2u06-aaj
www.ti.com/tpd4e001-aaj
www.ti.com/tpd4e05u06-aaj
www.ti.com/tpd4e1u06-aaj

For more information about TI's new-generation ESD-protection devices:
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