

TPS544B20 / TPS544C20

Quick Reference Guide

For more information:
www.ti.com/product/TPS544B20
www.ti.com/product/TPS544C20



The SWIFT™ 20-A TPS544B20 and 30-A TPS544C20

non-isolated DC/DC integrated FET converters feature high-frequency operation and fast transient performance in a small 5mm x 7mm package. The PMBus interface offers converter configuration as well as monitoring of key parameters including output voltage, current and an option for external temperature. This quick reference guide is intended to provide key information that is useful during the design, development and support processes. More information is available at: www.ti.com/pmbus

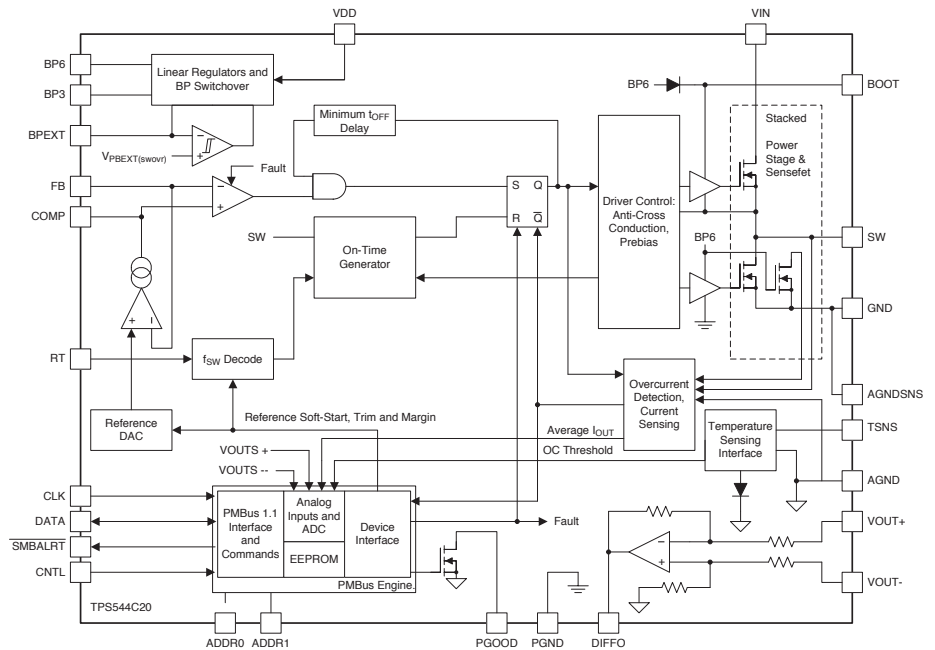
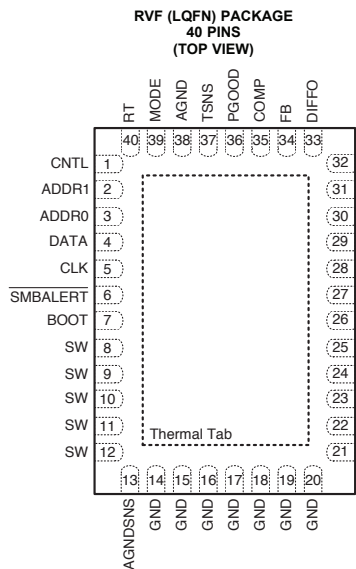


Table 2. Fault Protection Summary

FAULT	VDD UV	UV	OV	HSOC	LSOC	OT	TSD (OTFI)
FAULT CAUSES	1) Input undervoltage 2) Loss of input	1) Output overcurrent 2) Low-side short 3) FB short high	1) Pre-biased output 2) High-side short 3) FB short to GND	1) High-side short 2) Output short to GND	1) Low-side short 2) Output overcurrent	High board temperature	High device temperature due to ambient or power dissipation
MONITORING SIGNAL	Voltage on VDD pin	Voltage on FB pin	Voltage on FB pin	Voltage drop across high-side MOSFET	Sensed current in low-side MOSFET	Voltage on TSNS pin	Temperature on internal sensor
HIGH-SIDE MOSFET	Latch off	Latch off	Latch off	Turns off on cycle-by-cycle basis, incrementing OC counter; latch off when counter overflows	Tripping increments OC counter; latch off when counter overflows	Latch off	Latch off
LOW-SIDE MOSFET	Latch off	Latch off	Latch on until VOUT returns to within PG window	Latch off when counter overflows	Latch off when counter overflows	Latch off	Latch off
HICCUP	No	Yes ⁽¹⁾	No ⁽²⁾	Yes ⁽¹⁾	Yes ⁽¹⁾	Hiccup after temperature below reset threshold	Hiccup after temperature below reset threshold
DURING SOFT-START	Enabled	Disabled	Enabled	Enabled	Enabled during or after SS once LDRV pulse width first exceeds CSA sampling period	Enabled	Enabled
AFTER SOFT-START	Enabled	Enabled	Enabled	Enabled	Enabled	Enabled	Enabled

(1) If the device is configured to restart continuously, triggering the fault causes a hiccup.
 (2) Hiccup is not triggered if the device can bring the output voltage back to regulation. Hiccup remains enabled if the output reaches the UV limit following an OV event

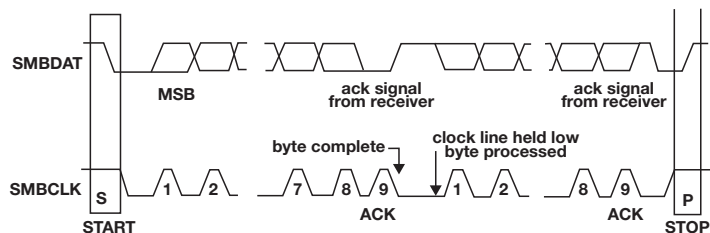
Table 1. Required RT Resistors

NOMINAL FREQUENCY (kHz)	1% RESISTOR VALUE (kΩ)
250	10.0
300	17.8
400	27.4
500	38.3
650	56.2
750	86.6
850	133
1000	205

Table 3. Required Address Resistors

DIGIT	1% RESISTOR VALUE (kΩ)
0	10.0
1	17.8
2	27.4
3	38.3
4	56.2
5	86.6
6	133
7	205

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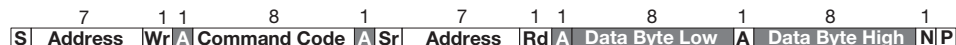
Data Transfer diagram.



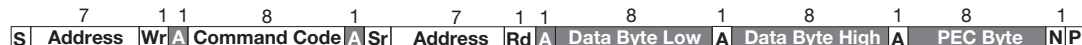
Write Word Protocol.



Write Word Protocol with PEC.



Read Word Protocol.



Read Word Protocol with PEC.

PMBus Command List		Green = read/write								Red = Read only					Shade = NVM Backup				S = sign bit			
HEX	COMMAND NAME	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	Default	LSB Unit	Min	Max	
01	OPERATION	-	-	-	-	-	-	-	-	ON	x			Margin		x	x	00h	-	-	-	
02	ON_OFF_CONFIG	-	-	-	-	-	-	-	-	x	x	x	pu	cmd	cpr	pol	cpa	16h	-	-	-	
03	CLEAR_FAULTS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	
10	WRITE_PROTECT	-	-	-	-	-	-	-	-	b7	b6	b5	x	x	x	x	x	00h	-	-	-	
15	STORE_USER_ALL	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	
16	RESTORE_USER_ALL	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	
19	CAPABILITY	-	-	-	-	-	-	-	-	PEC	SPD	ALRT			Reserved			80h	-	-	-	
20	VOUT_MODE	-	-	-	-	-	-	-	-			Mode			Exponent			17h	-	-	-	
35	VIN_ON ¹			Exponent														F011h	0.25 V	4.25 V	16V	
36	VIN_OFF ¹			Exponent														F010h	0.25 V	4 V	15.75 V	
39	IOUT_CAL_OFFSET			Exponent														E000h	62.5 mA	-4 A	3.94 A	
46	IOUT_OC_FAULT_LIMIT (C20) ²			Exponent														F84Eh	0.5 A	5 A	36 A	
46	IOUT_OC_FAULT_LIMIT (B20) ²			Exponent														F834h			24 A	
47	IOUT_OC_FAULT_RESPONSE	-	-	-	-	-	-	-	-	x	x		RS		x	x	x	3Fh	-	-	-	
4A	IOUT_OC_WARN_LIMIT (C20) ²			Exponent														F833h	0.5 A	4 A	30 A	
4A	IOUT_OC_WARN_LIMIT (B20) ²			Exponent														F828h			20 A	
4F	OT_FAULT_LIMIT ³			Exponent														0096h	1 C	120 C	165 C	
51	OT_WARN_LIMIT ³			Exponent														007Dh	1 C	100 C	140 C	
61	TON_RISE			Exponent														E02Bh	62.5 us	600 us	9 ms	
78	STATUS_BYTE	-	-	-	-	-	-	-	-	x	OFF	OV	OC	VIUV	TMP	CML	NA	-	-	-	-	
79	STATUS_WORD	VF	IF	x	MFR	PGD	x	x	x	x	OFF	OV	OC	VIUV	TMP	CML	NA	-	-	-	-	
7A	STATUS_VOUT	-	-	-	-	-	-	-	-	OVF	x	x	UVF	x	x	x	x	-	-	-	-	
7B	STATUS_IOUT	-	-	-	-	-	-	-	-	OCF	x	OCW	x	x	x	x	x	-	-	-	-	
7D	STATUS_TEMPERATURE	-	-	-	-	-	-	-	-	OTF	OTW	x	x	x	x	x	x	-	-	-	-	
7E	STATUS_CML	-	-	-	-	-	-	-	-	IVC	IVD	PEC	MF	x	x	OTH	x	-	-	-	-	
80	STATUS_MFR_SPECIFIC	-	-	-	-	-	-	-	-	OTFI	x	x	IVAD	x	x	x	x	-	-	-	-	
8B	READ_VOUT																	-	2 ⁻⁹ V	0 V	5.8 V	
8C	READ_IOUT																	-	62.5 mA	0 A	40 A	
8E	READ_TEMPERATURE_2			Exponent														-	1 C	-40C	165C	
98	PMBUS_REVISION	-	-	-	-	-	-	-	-	0	0	0	1	0	0	0	1	11h	-	-	-	
D0	MS_00 (SCRATCH)	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	00h	-	-	-	
D4	MS_04 (VREF_TRIM)	S																0000h	2 ⁻⁹ V	-120 mV	60 mV	
D5	MS_05 (STEP_VREF_MARGIN_HIGH)																	001Eh	2 ⁻⁹ V	0	60 mV	
D6	MS_06 (STEP_VREF_MARGIN_LOW)	S																FFE2h	2 ⁻⁹ V	-120 mV	0	
D7	MS_07 (PCT_VOUT_FAULT_PG_LIMIT)	-	-	-	-	-	-	-	-	x	x	x	x	x	x		PCT	00h	-	-	-	
D8	MS_08 (SEQUENCE_TON_TOFF_DELAY)	-	-	-	-	-	-	-	-					TON_DELAY	x	TOFF_DELAY	x	00h	TON_RISE	0	7	
E5	MS_21 (OPTIONS)	x	x	x	x	x	x	x	x	x	x	x	x	x	x	ADC	x	x	0004h	-	-	-
E7	MS_23 (MASK_SMBALERT)	OTFI	PRTC	SMBT	IVC	IVD	PEC	MEM	ARA	OTF	OTW	OCF	OCW	OVF	UVF	PGD	VIUV	0100h	-	-	-	
FC	MS_44 (DEVICE_CODE) C20	Device Identifier Code											Revision Code				0153h	-	-	-		
	MS_44 (DEVICE_CODE) B20	Device Identifier Code											Revision Code				0143h	-	-	-		

¹: VIN_ON must be > VIN_OFF ²: OCF must be > OCW ³: OTF must be > OTW

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