Understanding Operational Amplifier Limitations and Long-Term Stability

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SLYW037

Summary of topics

Section 1: Op amp input topologies

- Common mode limits

Section 2: Causes of op amp output phase inversion

- Bipolar vs. JFET input effects caused by exceeding the Vcm

Section 3: Op amp output topologies

- Output swing limits

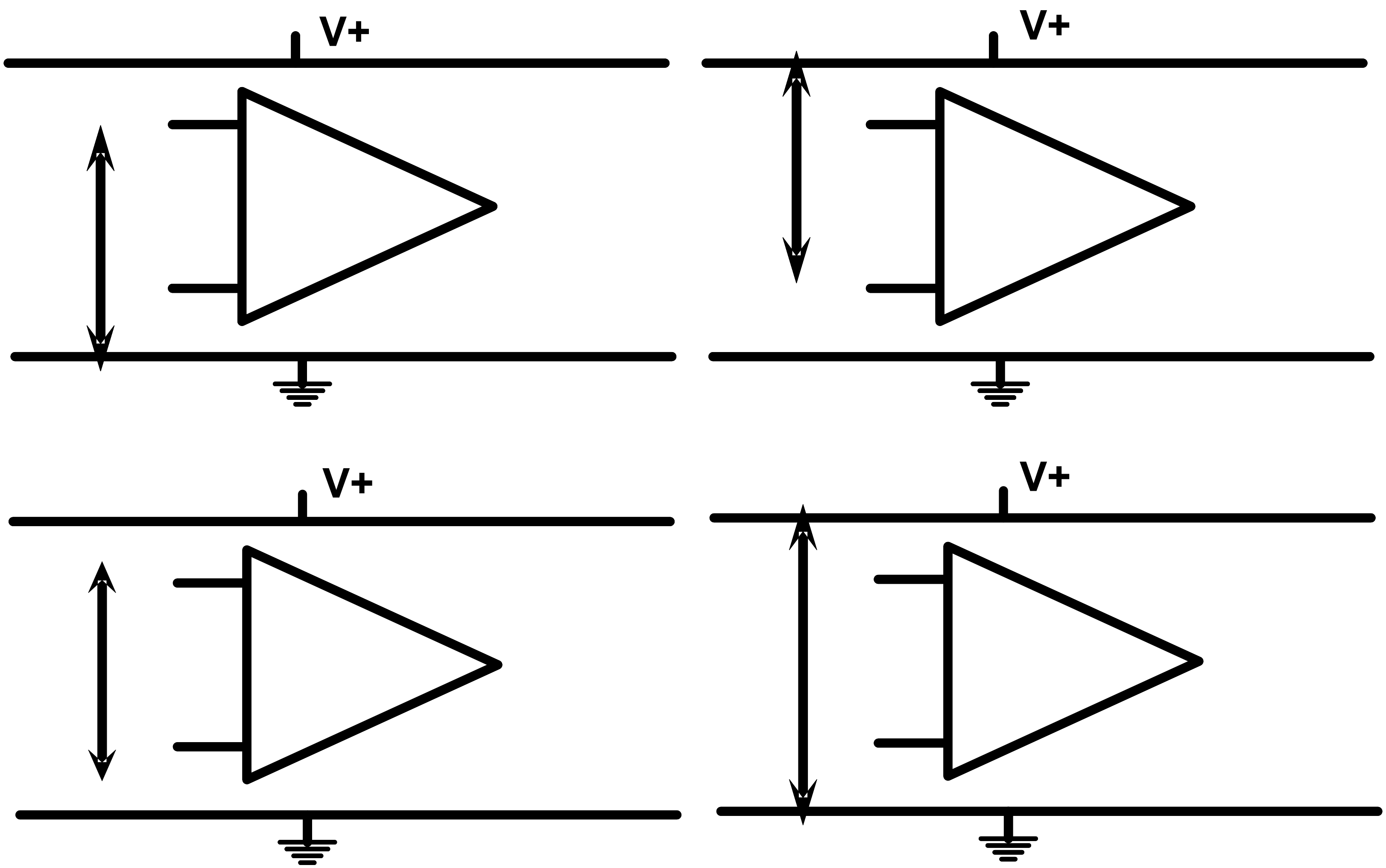
Section 4: Long-term stability spec

- For specs centered around a fixed value
- For parameters specified as an absolute value

Section 1

INPUT STAGE CONSIDERATIONS

Real world Vcm input range

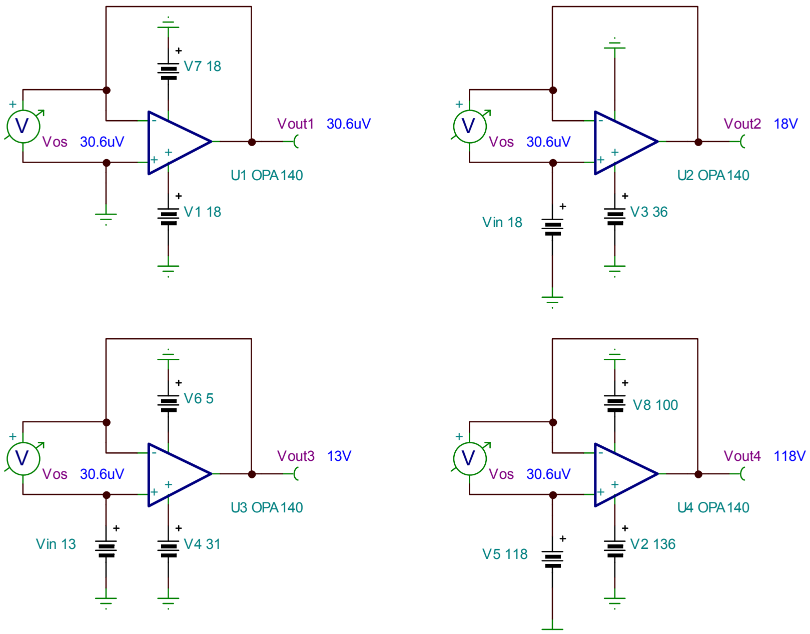


Op amp operation vs supply voltage

Each amplifier has 36V supplies!

The common mode in each case is the supply midpoint.

All amps can act as “single supply”

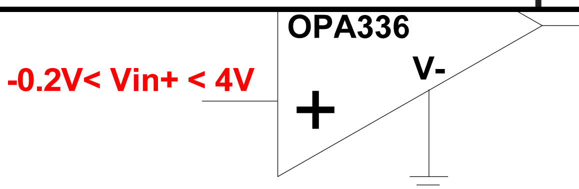


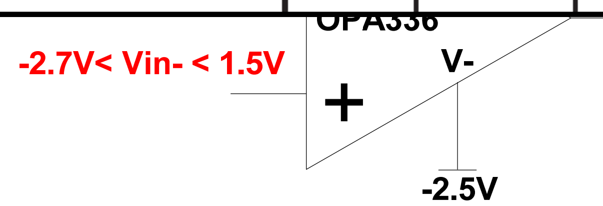
Note: A single-supply optimized op amp is not the same as a single supply op amp.

TEXAS INSTRUMENTS

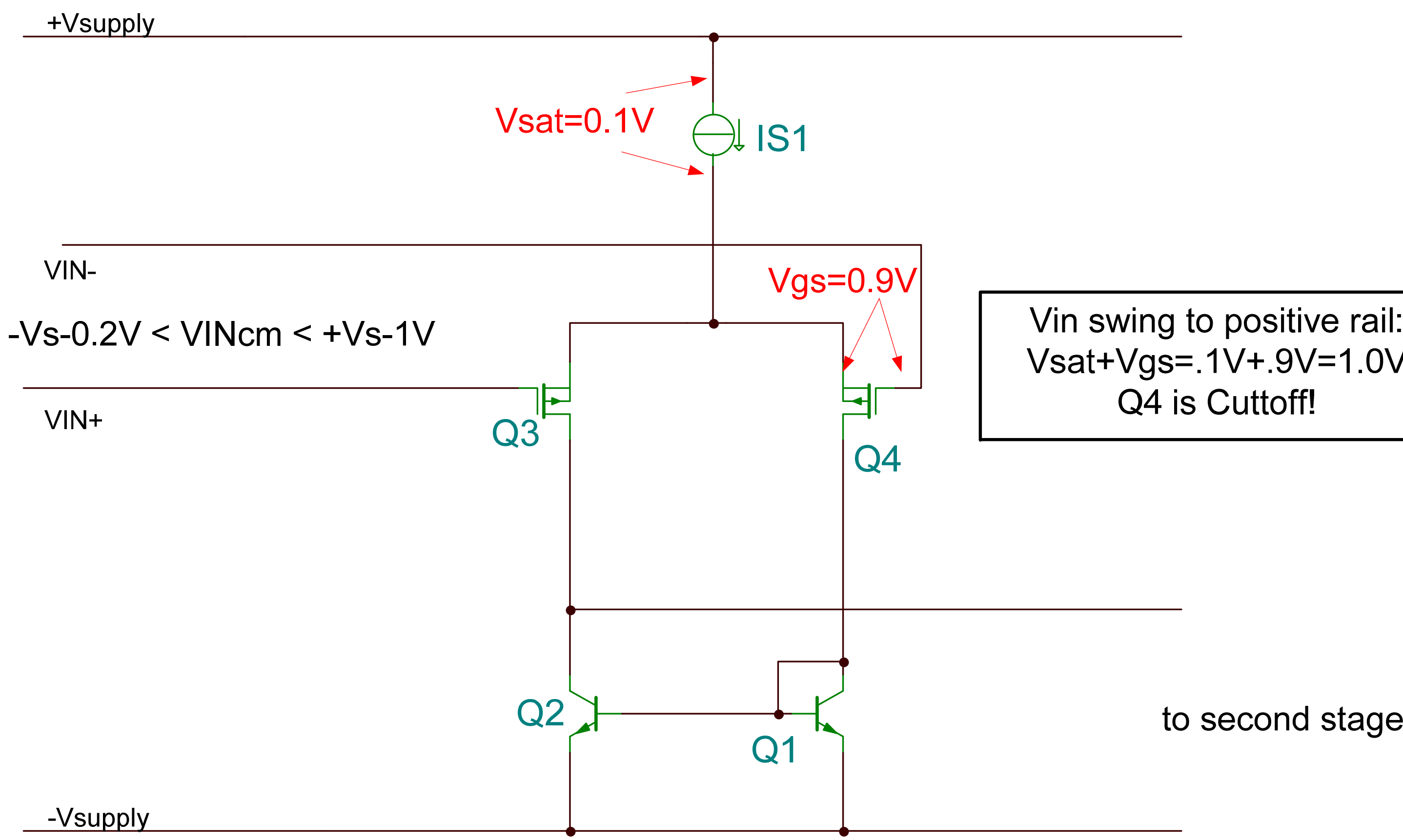
MOSFET simple input (Vcm to negative rail)

PARAMETER		CONDITION	OPA336N, U OPA2336E, P, U		
			MIN	TYP(1)	MAX
INPUT VOLTAGE RANGE					
Common-Mode Voltage Range	V_{CM}		–0.2		(V+) –1
Common-Mode Rejection Ratio	CMRR	$-0.2V < V_{CM} < (V+) -1V$	80	90	
Over Temperature		$-0.2V < V_{CM} < (V+) -1V$	**76**		



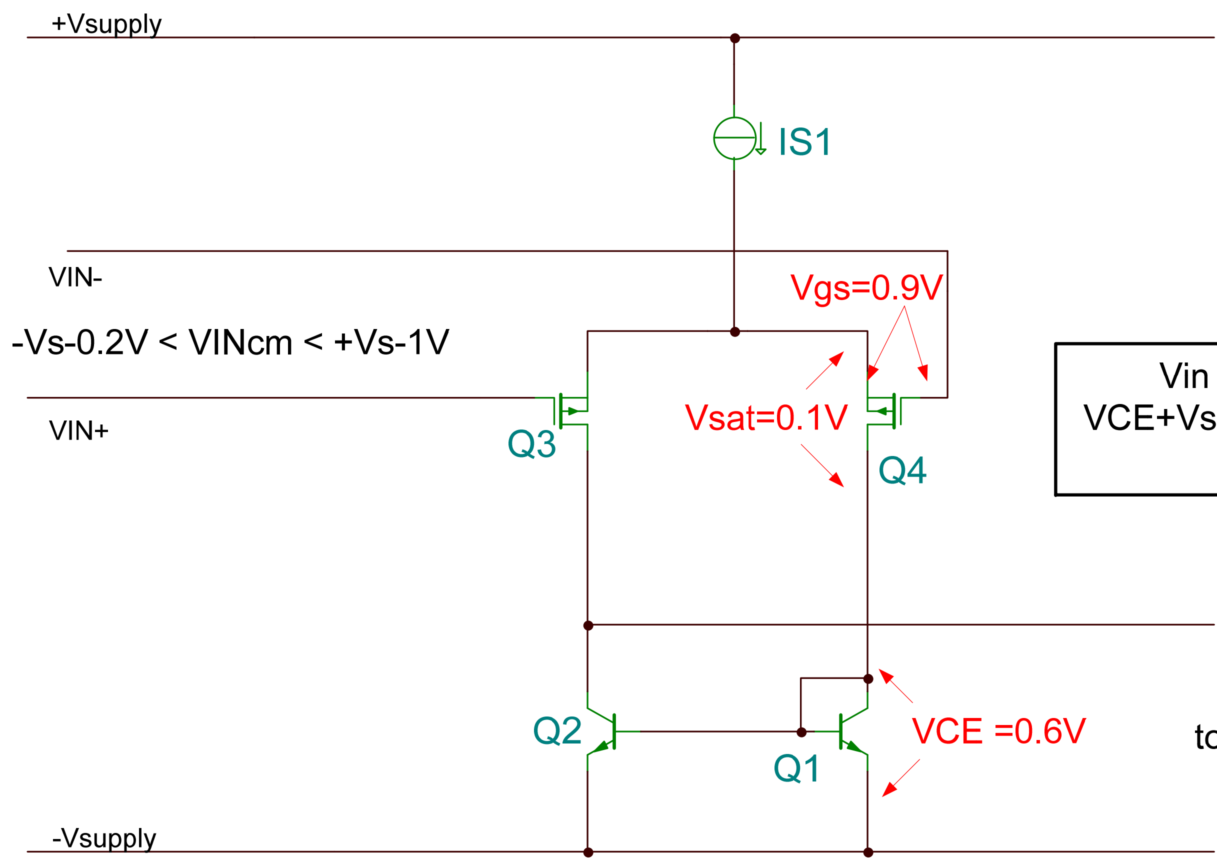


Simplified schematic of OPA336 input stage (swing to positive rail)



Vin swing to positive rail:
Vsat+Vgs=.1V+.9V=1.0V
Q4 is Cuttoff!

Simplified schematic of OPA336 input stage (swing to negative rail)

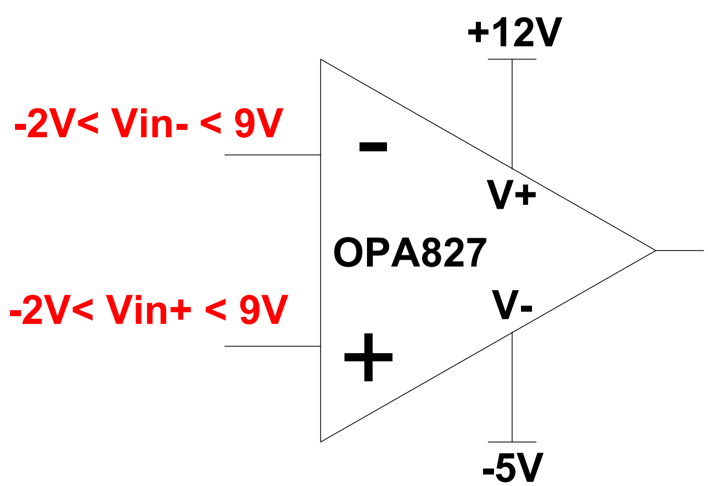


Vin swing to negative rail:
VCE+Vsat-Vgs=.6V+.1V-.9V=-0.2V
Q4 is saturated!

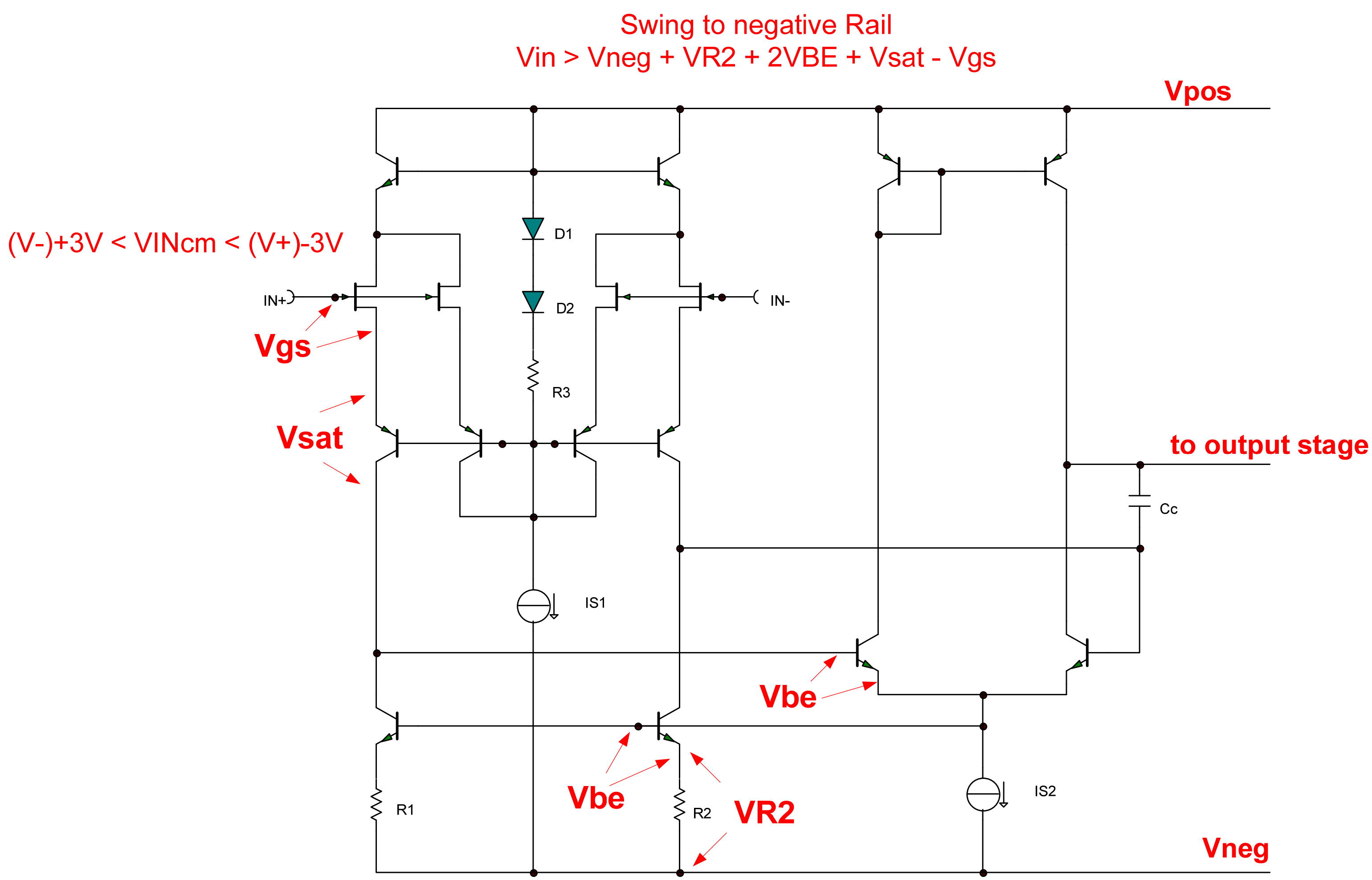
to second stage

Typical bipolar or JFET input (not rail-to-rail)

PARAMETER		CONDITIONS	STANDARD GRADE OPA827AI MIN	TYP	MAX
INPUT VOLTAGE RANGE					
Common-Mode Voltage Range	V_{CM}		(V−)+3		(V+)−3
Common-Mode Rejection Ratio	CMRR	$(V-)+3V \le V_{CM} \le (V+)-3V$, $V_S < 10V$	104	114	
		$(V-)+3V \le V_{CM} \le (V+)-3V$, $V_S \ge 10V$	114	126	
Over Temperature		$\mathbf{(V-)+3V \le V_{CM} \le (V+)-3V}$, $\mathbf{V_S < 10V}$	**100**		
		$\mathbf{(V-)+3V \le V_{CM} \le (V+)-3V}$, $\mathbf{V_S \ge 10V}$	**110**		

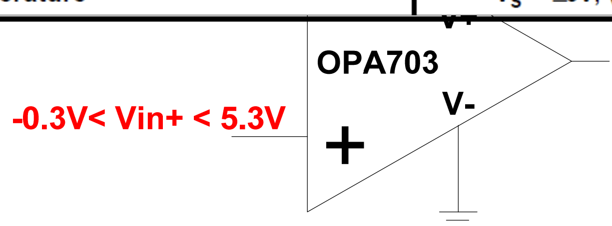


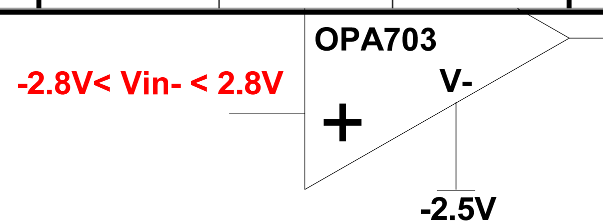
Simplified schematic of OPA827 input stage (swing to negative rail)



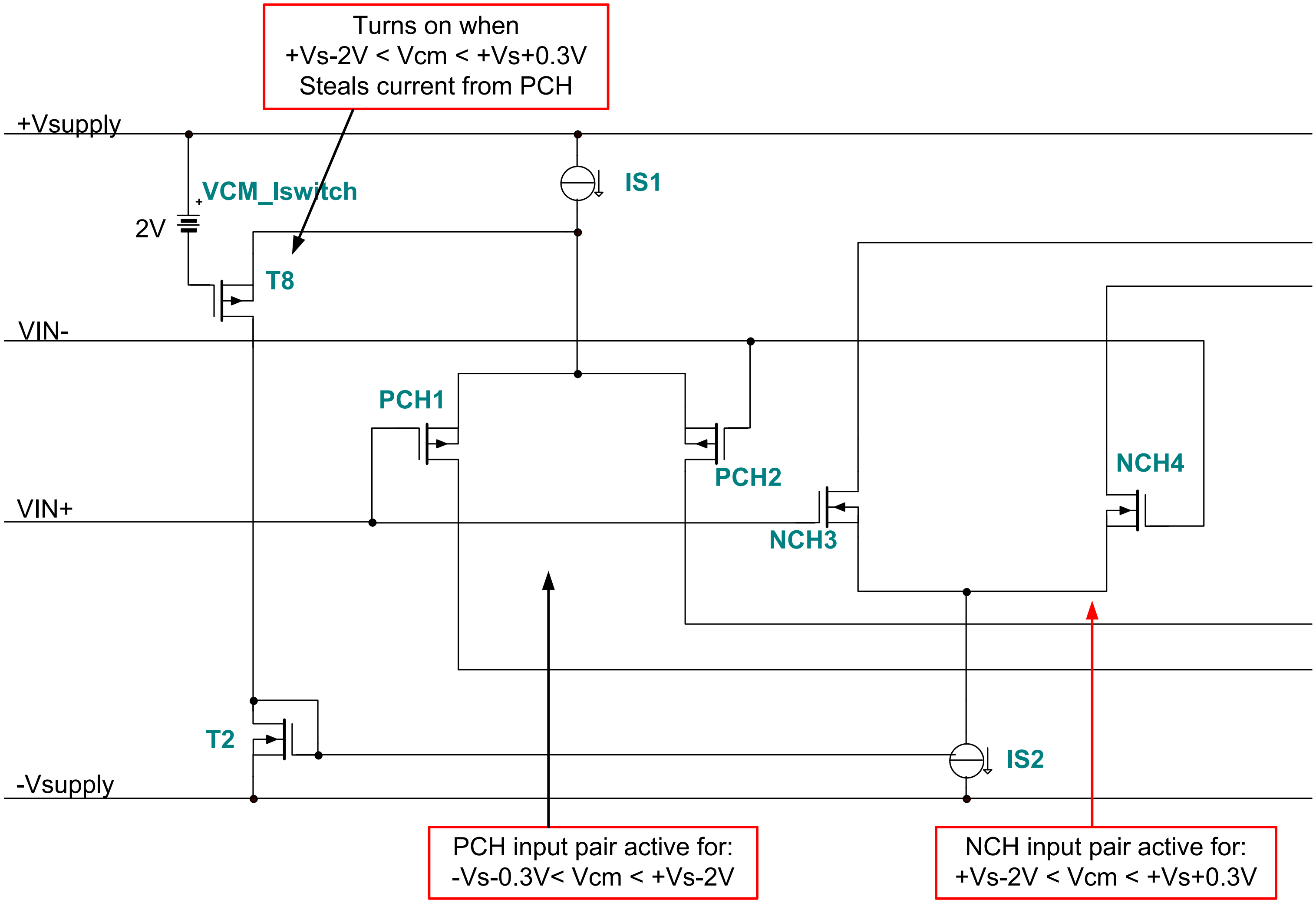
MOSFET complementary N-P-FET (rail-to-rail)

PARAMETER		CONDITION	OPA703NA, UA, PA OPA2703EA, UA, PA OPA4703EA, UA MIN	TYP	MAX	UNITS
INPUT VOLTAGE RANGE						
Common-Mode Voltage Range	V_{CM}		(V–) – 0.3		(V+) + 0.3	V
Common-Mode Rejection Ratio	CMRR	$V_S = \pm5V$, (V–) – 0.3V < V_{CM} < (V+) + 0.3V	70	90		dB
over Temperature		**$V_S = \pm5V$, (V–) < V_{CM} < (V+)**	**68**			**dB**
		$V_S = \pm5V$, (V–) – 0.3V < V_{CM} < (V+) – 2V	80	96		dB
over Temperature		**$V_S = \pm5V$, (V–) < V_{CM} < (V+) – 2V**	**74**			**dB**

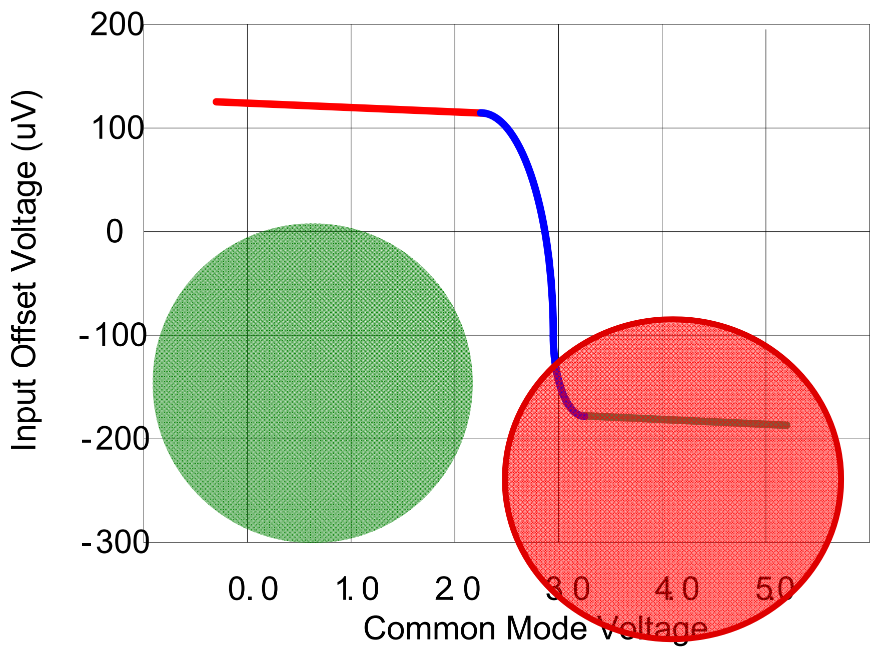


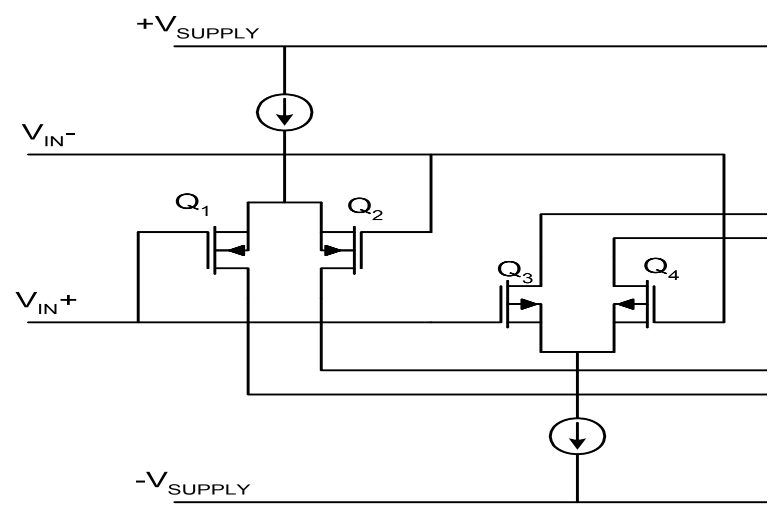


Simplified schematic of OPA703 input stage



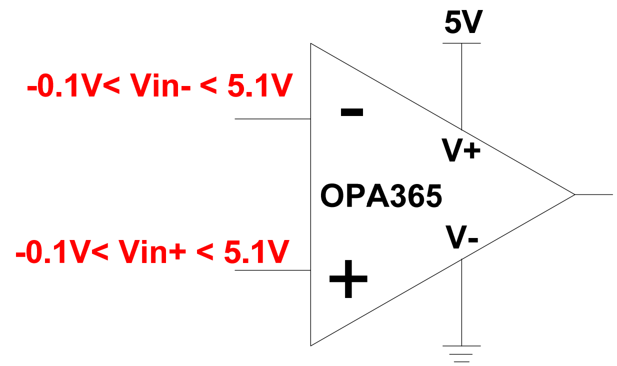
OPA703 complementary CMOS (rail-to-rail)

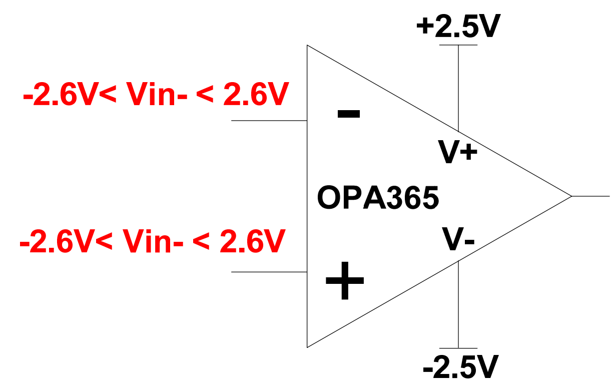




MOSFET charge pump (rail-to-rail)

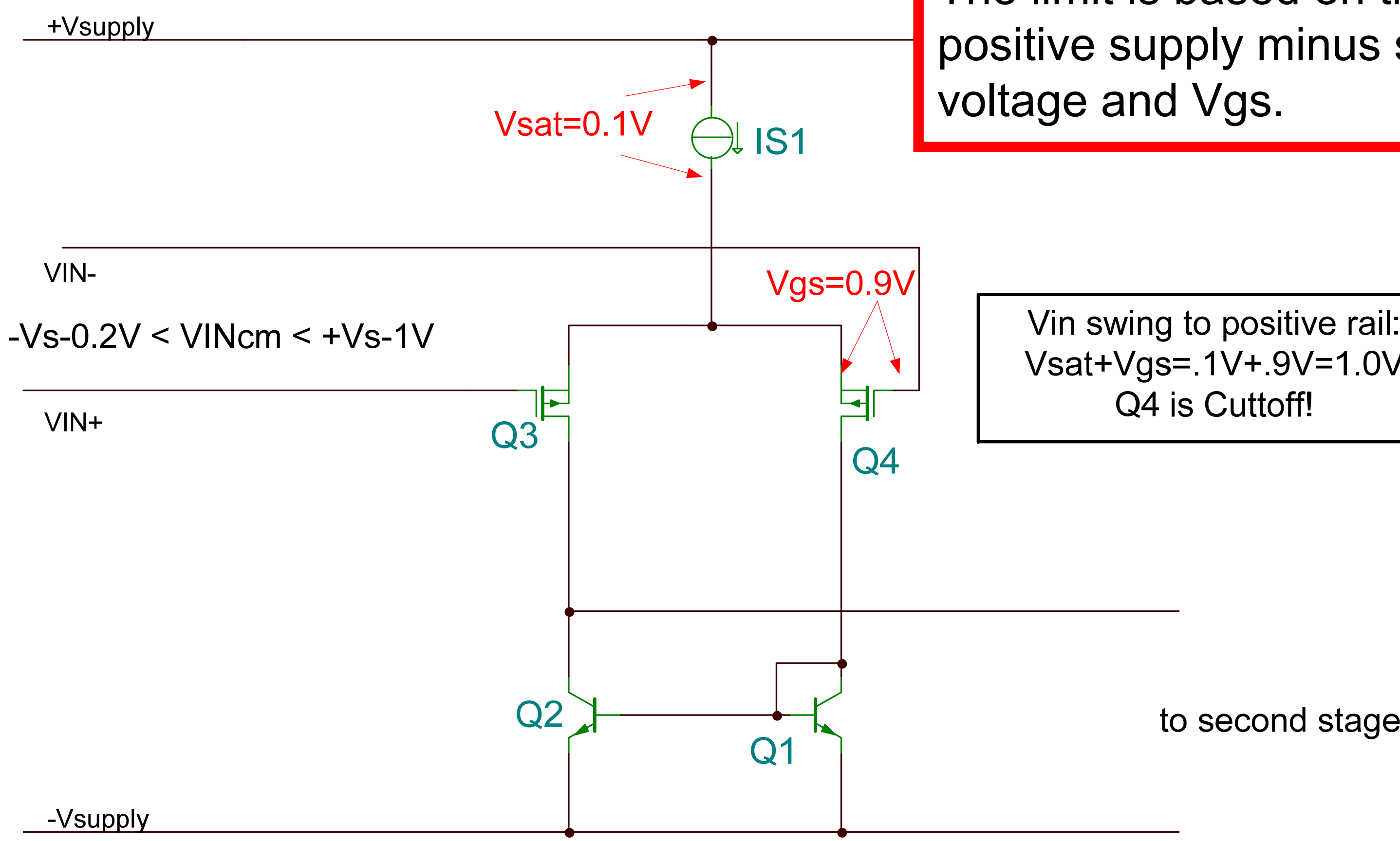
PARAMETER		TEST CONDITIONS	OPAx365 MIN	TYP	MAX	UNIT
INPUT VOLTAGE RANGE						
Common-Mode Voltage Range	V_{CM}		(V−) − 0.1		(V+) + 0.1	V
Common-Mode Rejection Ratio	**CMRR**	**(V−) − 0.1V ≤ V_{CM} ≤ (V+) + 0.1V**	**100**	**120**		**dB**





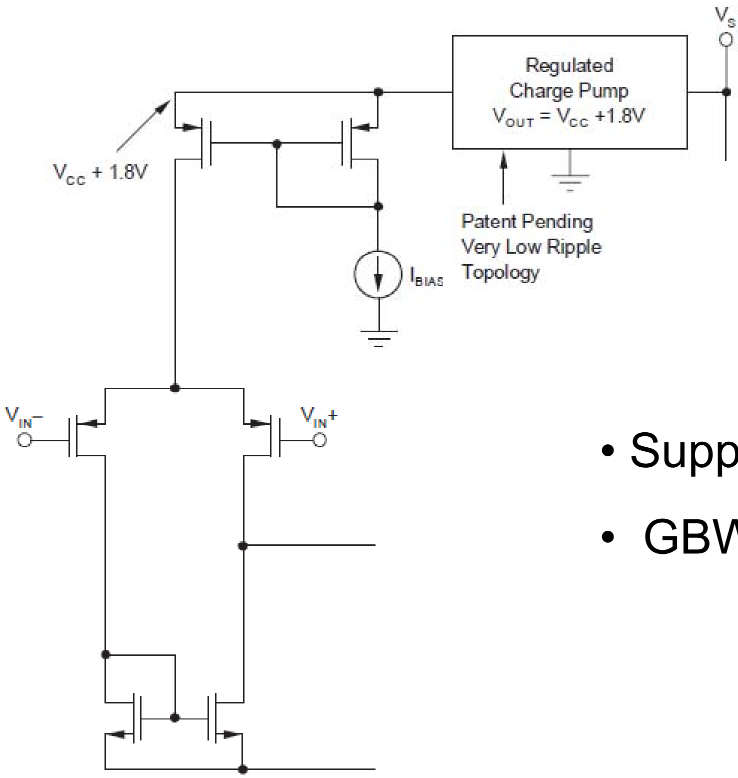
Remember from earlier in the presentation…

The limit is based on the positive supply minus saturation voltage and Vgs.



Vin swing to positive rail:
Vsat+Vgs=.1V+.9V=1.0V
Q4 is Cuttoff!

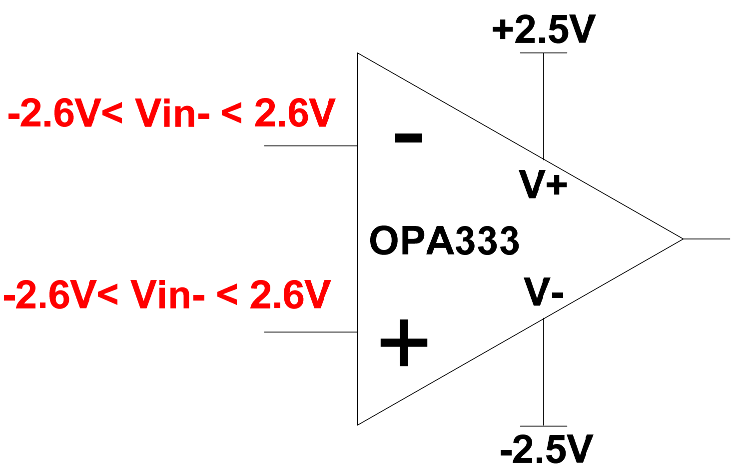
MOSFET charge pump OPA363 (rail-to-rail)

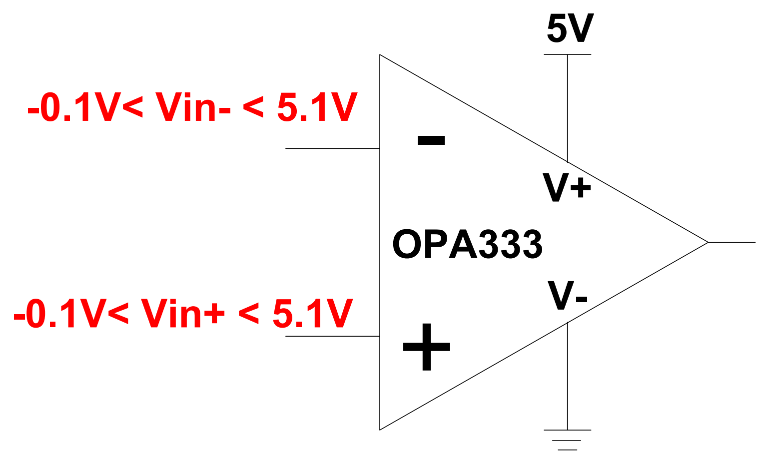


- Supplies a small current to input
- GBW = 50MHz, charge pump freq =10MHz

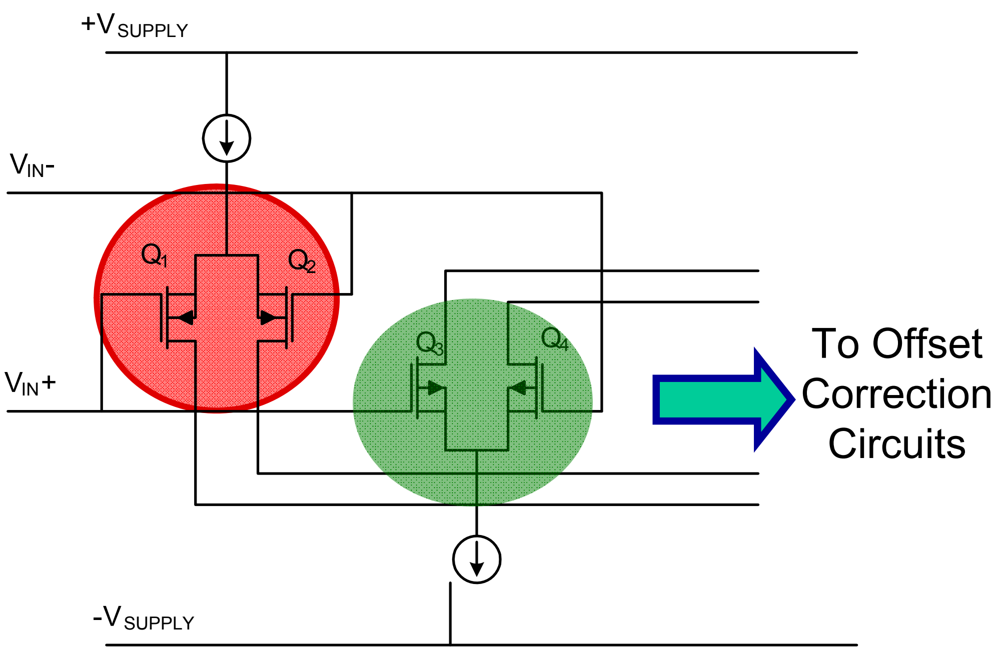
MOSFET zero drift (rail-to-rail)

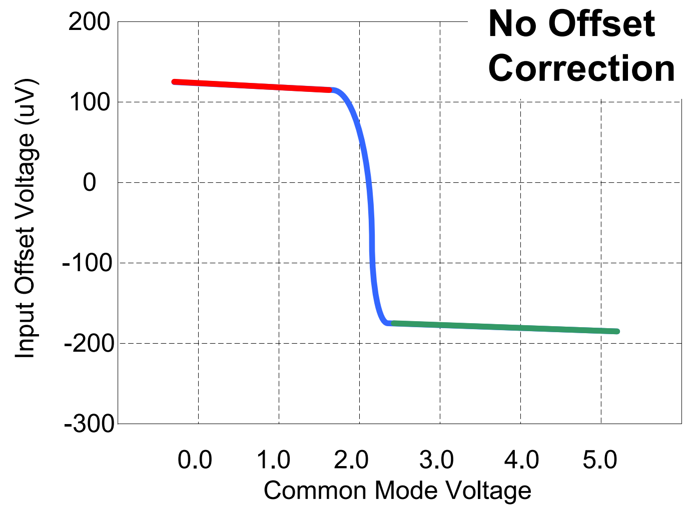
PARAMETER		TEST CONDITIONS	OPA333, OPA2333 MIN	TYP	MAX	UNIT
INPUT VOLTAGE RANGE						
Common-Mode Voltage Range	V_{CM}		(V–) – 0.1		(V+) + 0.1	V
Common-Mode Rejection Ratio	**CMRR**	**(V–) – 0.1V < V_{CM} < (V+) + 0.1V**	**106**	**130**		**dB**

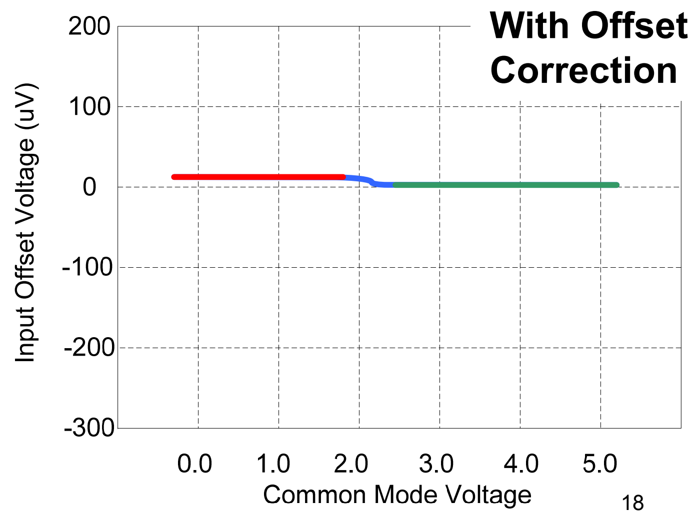




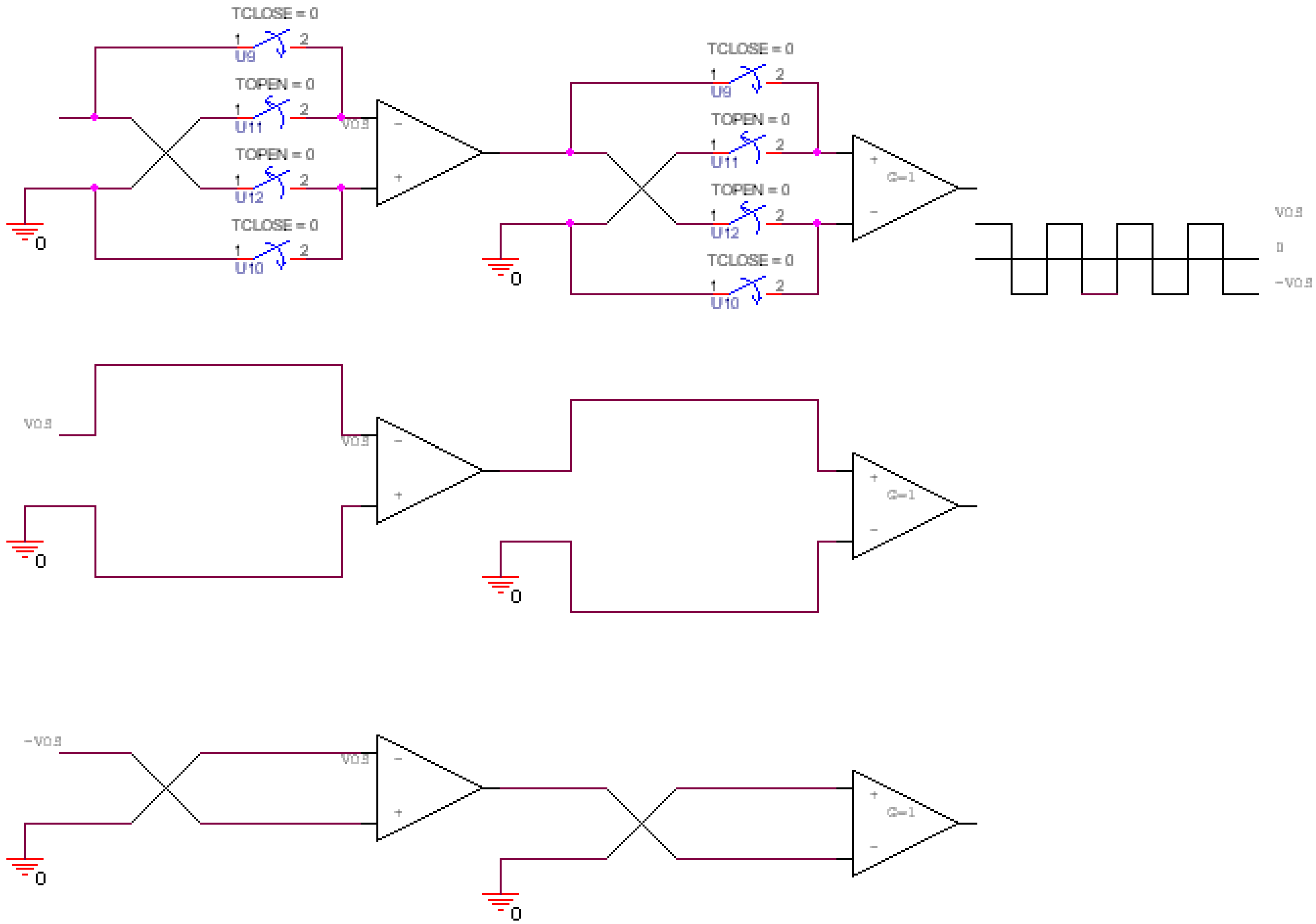
MOSFET zero drift (rail-to-rail)



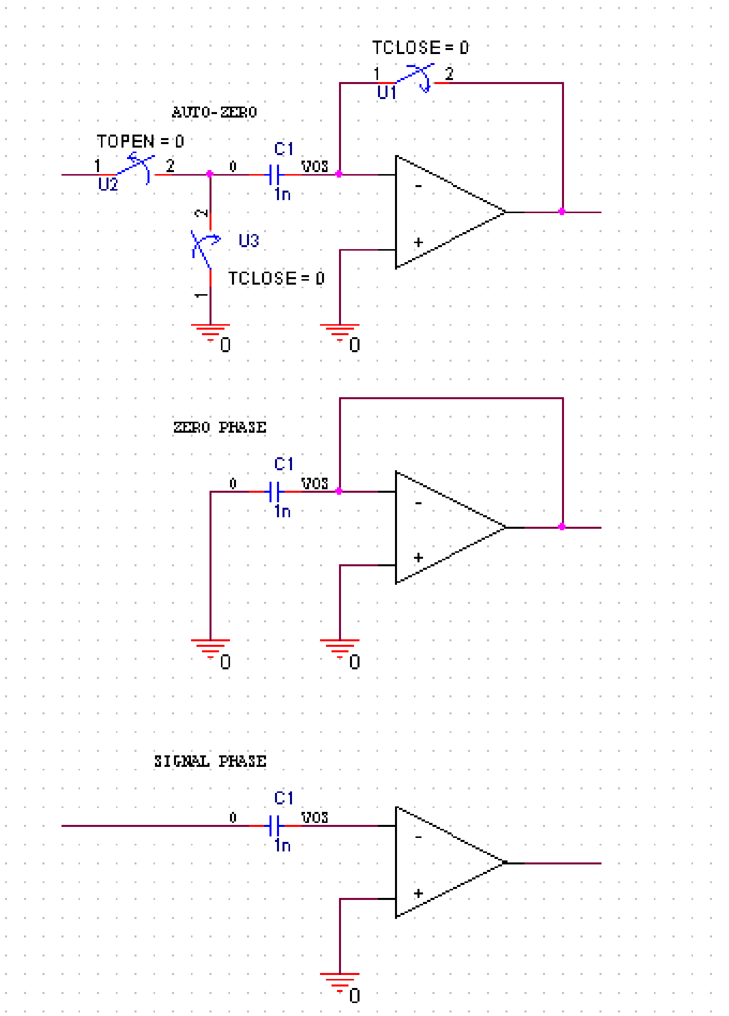




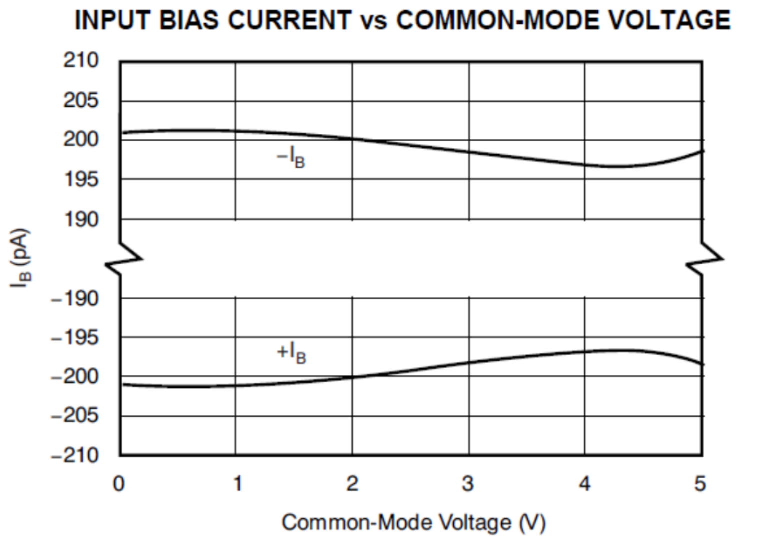
Zero-drift chopper topology



Zero-drift auto-zero topology



Input bias current in chopper op amps



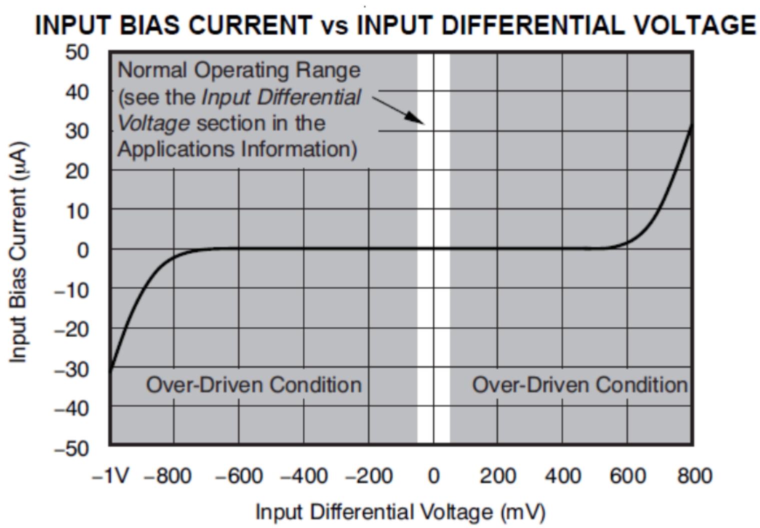


Figure 17.

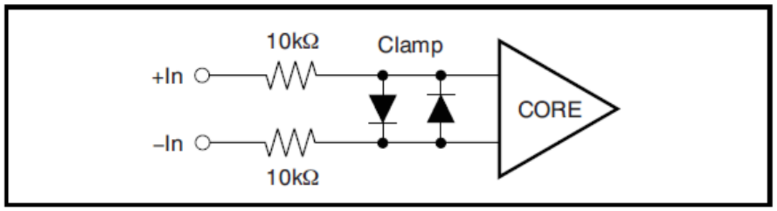


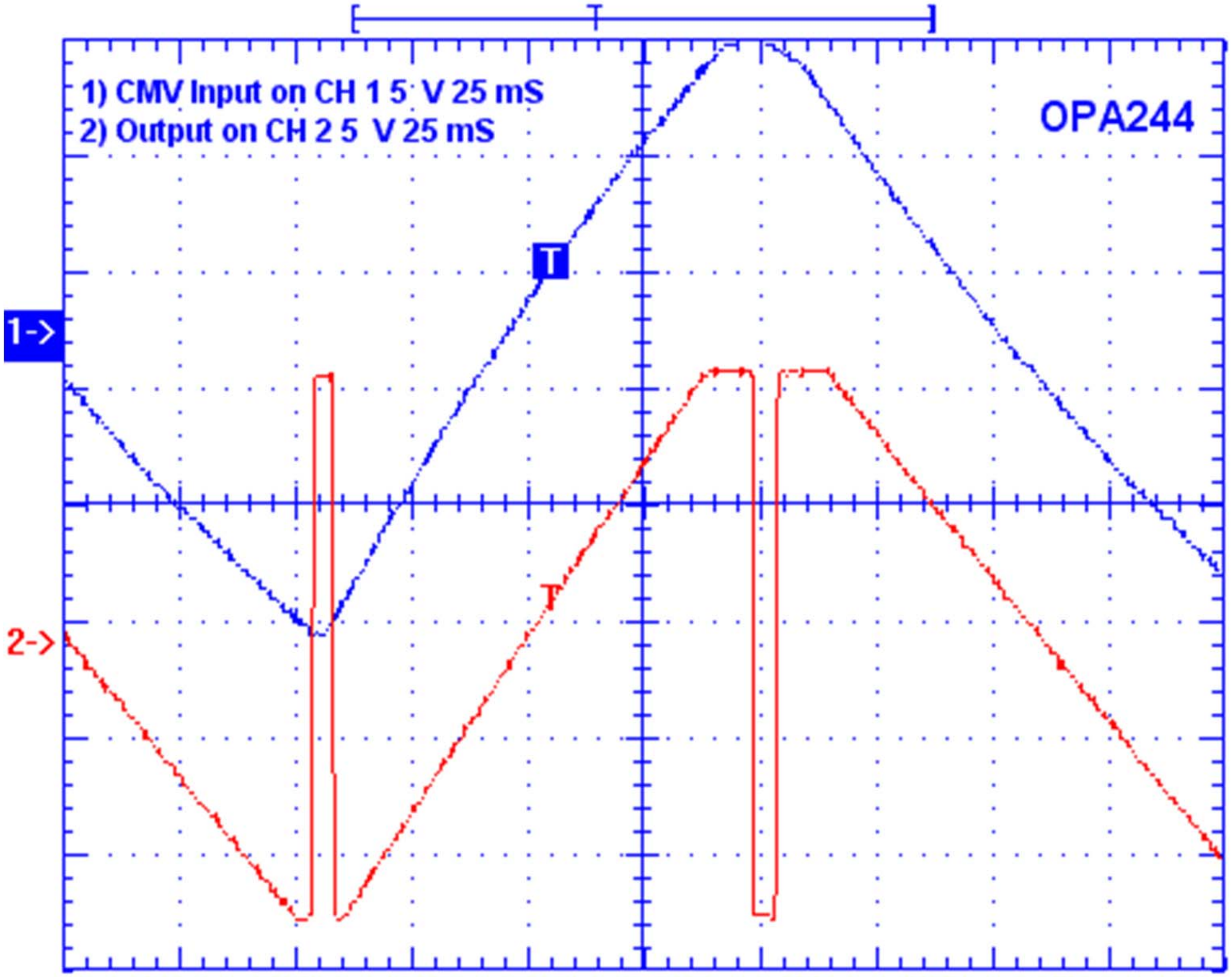
Figure 19. Equivalent Input Circuit

The typical input bias current of the OPA330 during normal operation is approximately 200pA. In over-driven conditions, the bias current can increase significantly (see Figure 17).The most common cause of an over-driven condition occurs when the op amp is outside of the linear range of operation. When the output of the op amp is driven to one of the supply rails the feedback loop requirements cannot be satisfied and a differential input voltage develops across the input pins. This differential input voltage results in activation of parasitic diodes inside the front end input chopping switches that combine with 10kΩ electromagnetic interference (EMI) filter resistors to create the equivalent circuit shown in Figure 19. Notice that the input bias current remains within specification within the linear region.

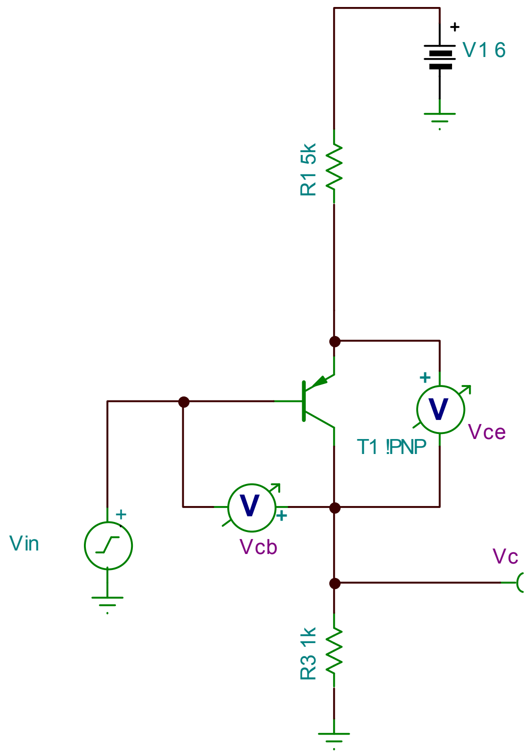
Section 2

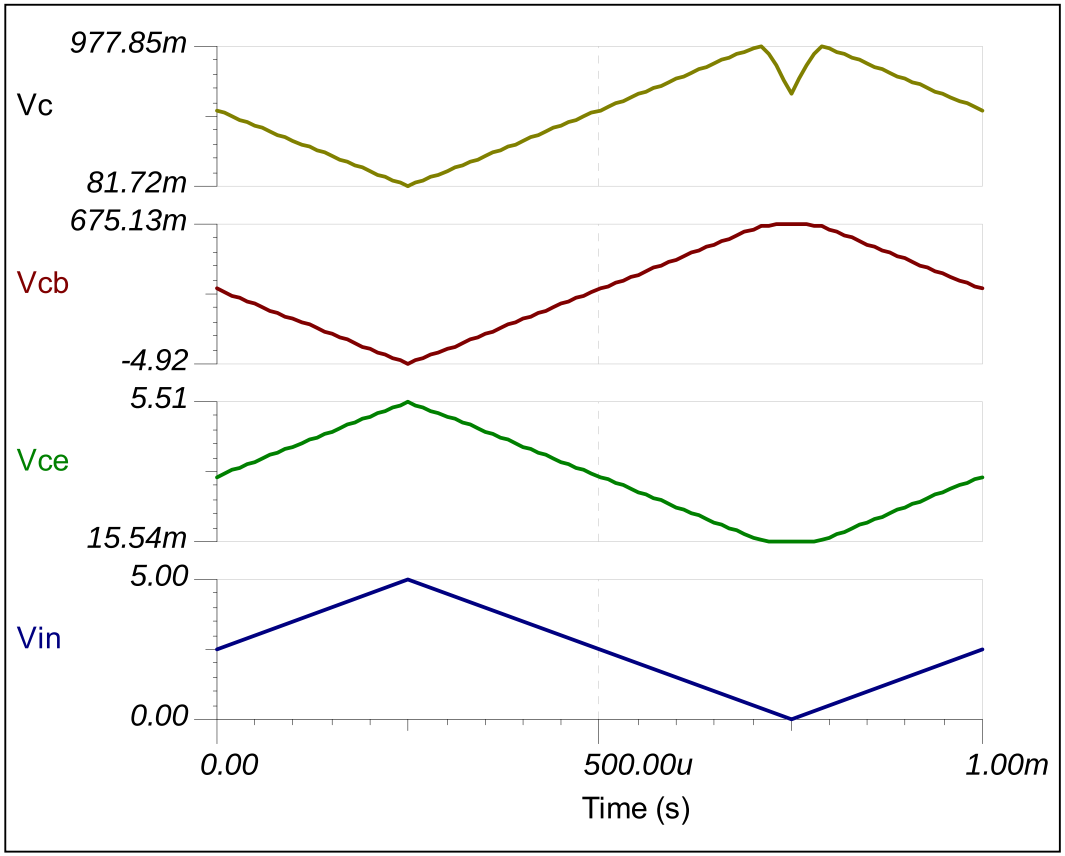
OP AMP OUTPUT PHASE INVERSION

Typical case of op amp phase inversion due to exceeding Vcm



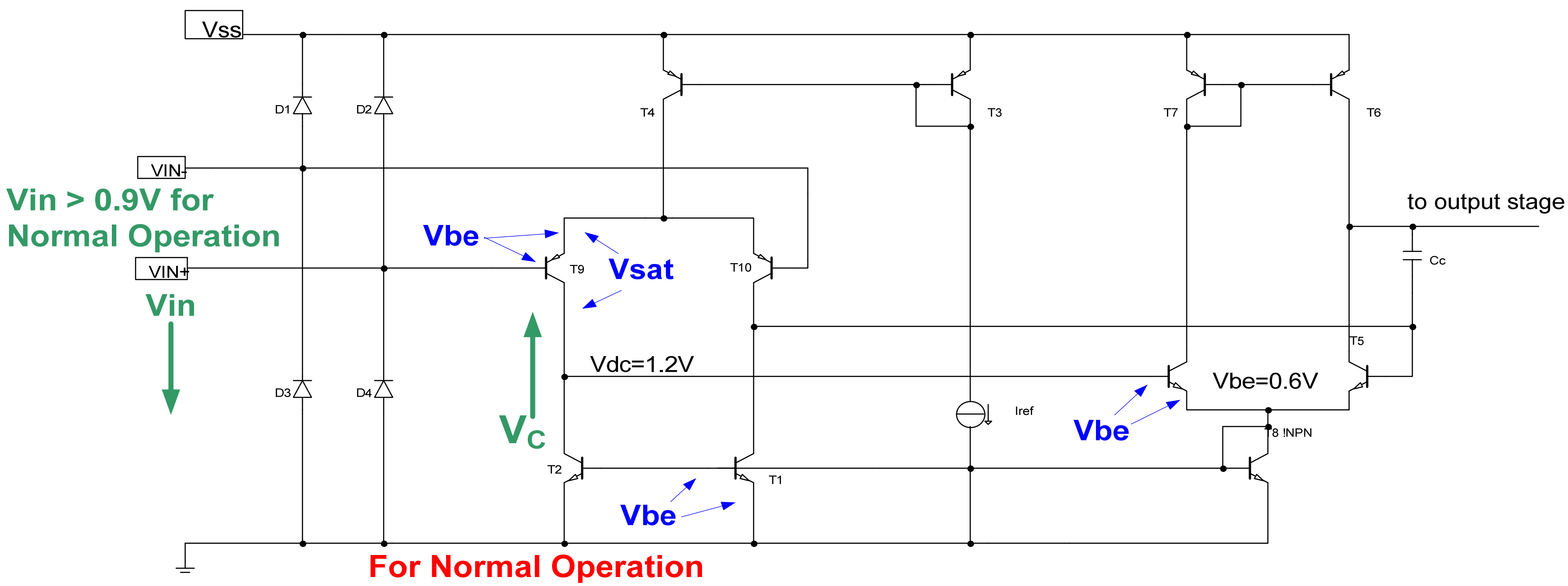
Phase inversion on a single transistor





PNP bipolar input op amp low-common-mode limitation

Normal operation – no phase inversion

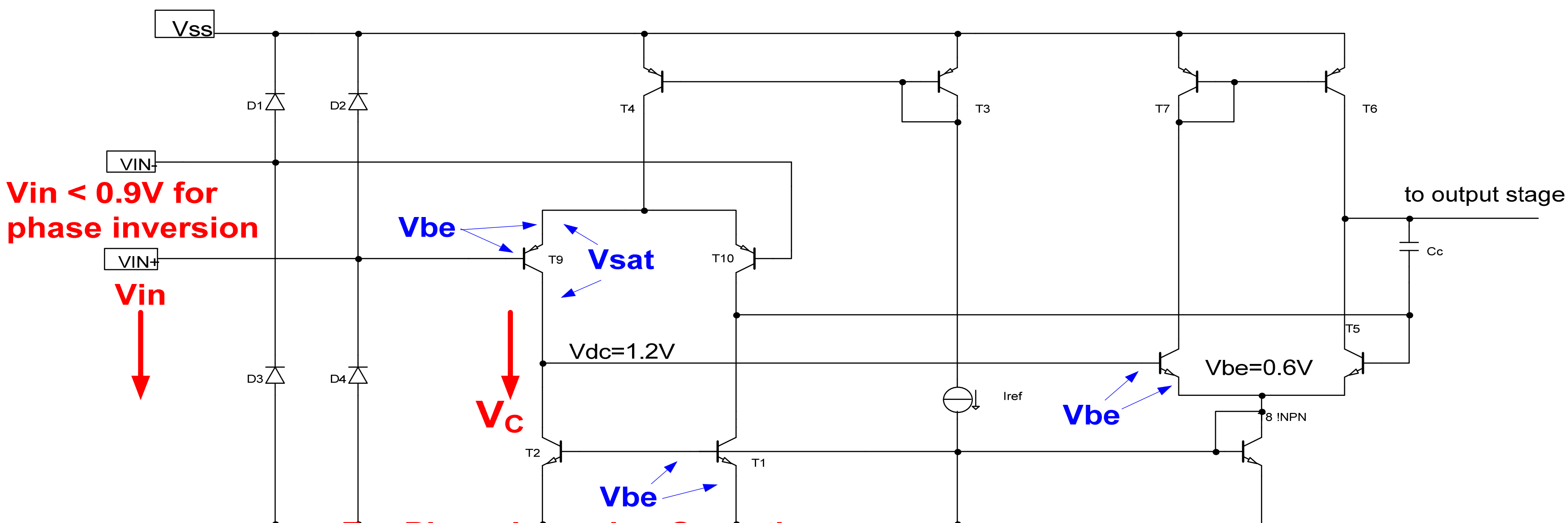


For Normal Operation
Vin decreases, Vc increases

Vin > -Vbe + Vsat + Vbe +Vbe
Vin > -.6V + (.3V+.6V+.6V)
Vin > 0.9V for normal operation
Vin < 0.9V for phase inversion

PNP bipolar input op amp low-common-mode limitation

Phase inversion issue!



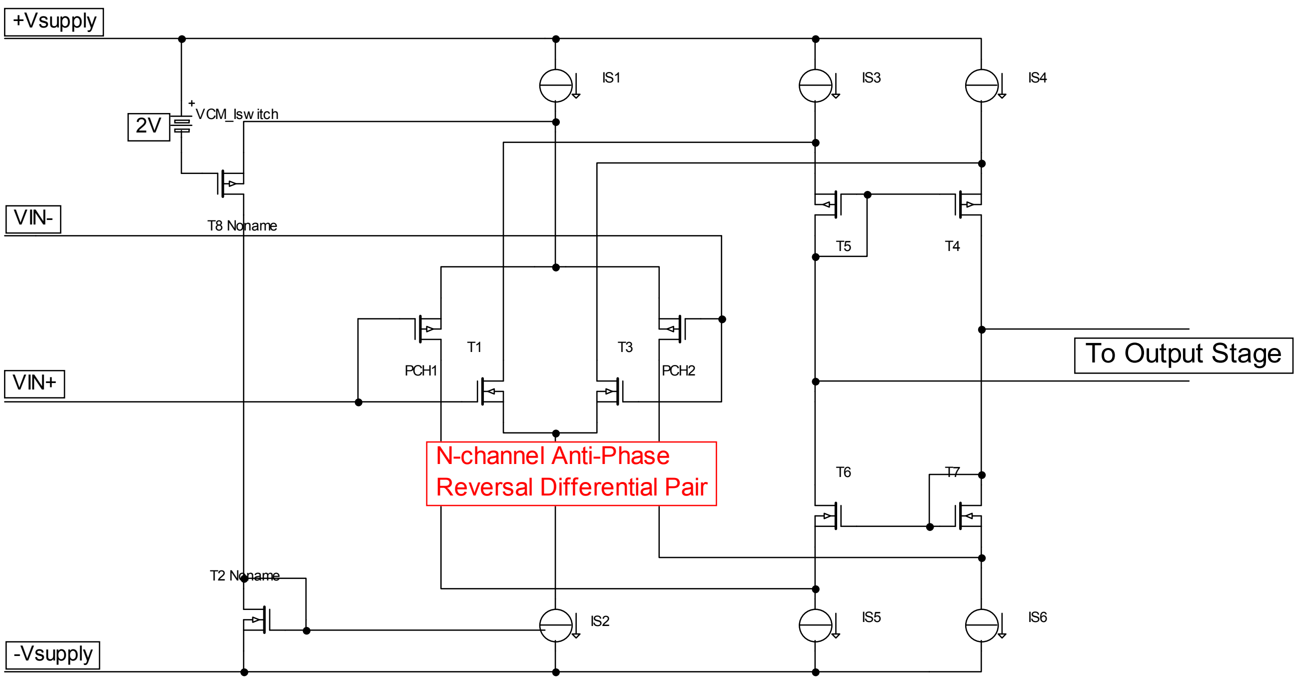
For Phase Inversion Operation

Decreasing Vin in saturation region causes Vc to become in phase (decreasing in this case). This happens because the emitter follows the base.

Vin > -Vbe + Vsat + Vbe +Vbe

Vin > -.6V + (.3V+.6V+.6V)

Example of IC circuit used to prevent a phase inversion



Summary of Output Phase Inversion

What causes a phase reversal?
Exceeding the input common-mode voltage range may cause a phase reversal.

How can it be prevented?
•Staying with op amp specified Vcm linear region
•Using op amp with a built-in anti-phase reversal circuitry
•Utilizing external circuitry to prevent a phase inversion

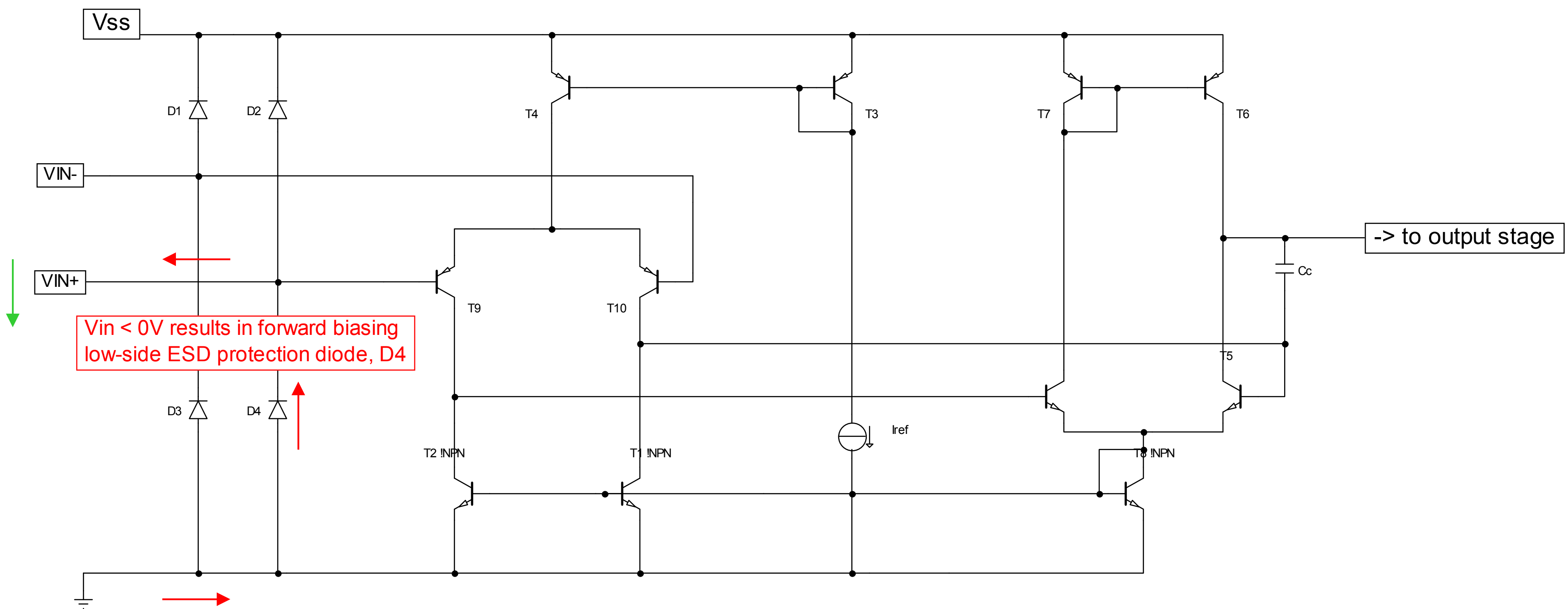
Is it process dependent?
•Some built-in anti-phase reversal circuitry might be process dependent depending on topology used
•Most modern op amps use a robust topologies assuring no phase reversal

How can a customer be confidant of no phase reversal?
(if it is not explicitly stated in the data sheet)
Apply a slow triangular waveform in a buffer configuration 1V beyond rails to test for phase inversion - you must limit the input current to less than 10mA to prevent damaging IC

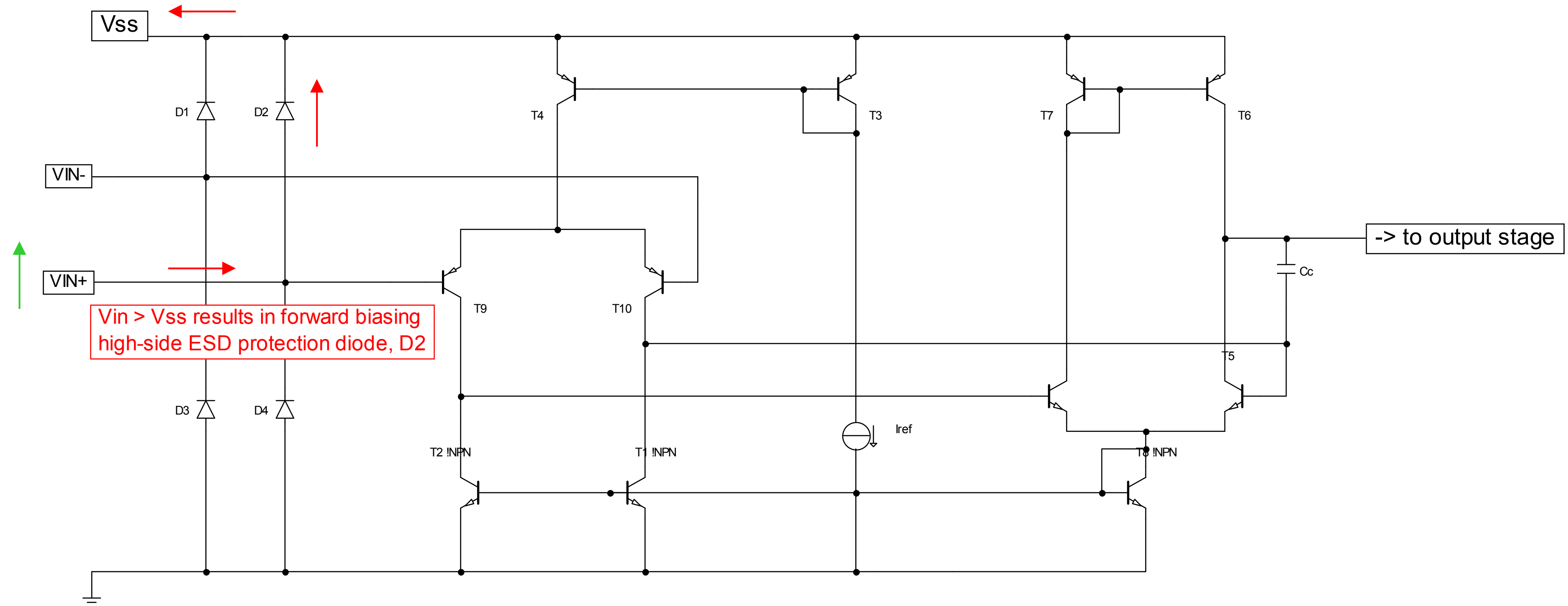
Section 3

OP AMP INPUT PROTECTION DIODES

Op amp input-common-mode below negative rail



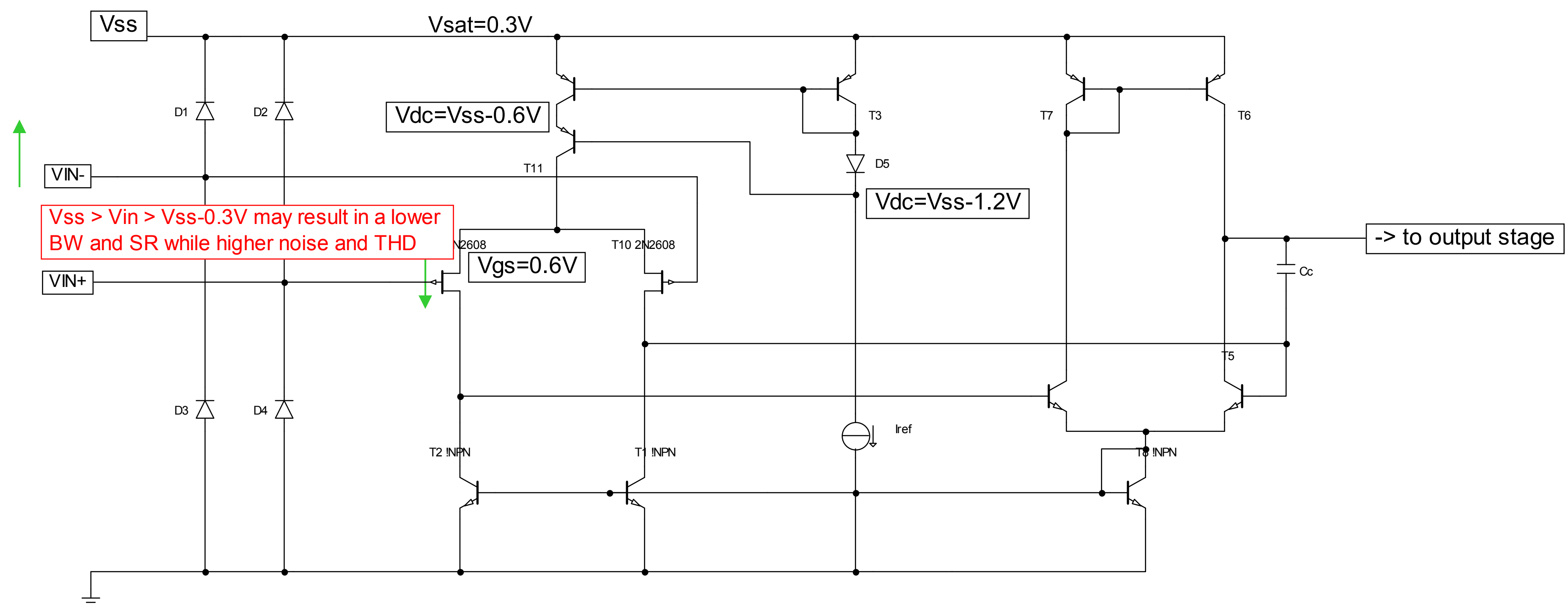
Op amp input-common-mode above positive rail



TEXAS INSTRUMENTS

JFET input op amp high-common-mode limitation

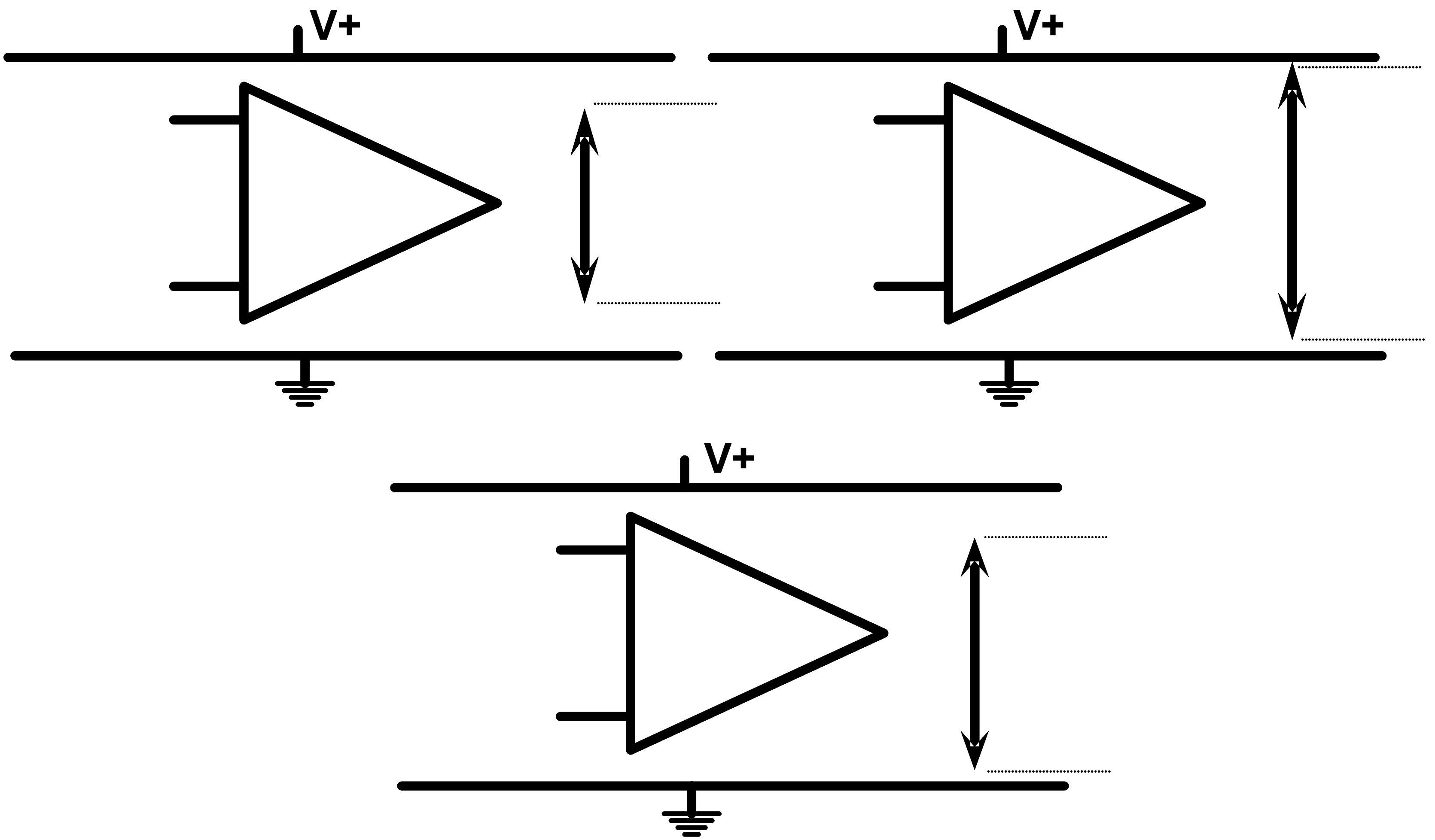
To positive rail looks like "dc rail to rail," to negative rail shows phase inversion



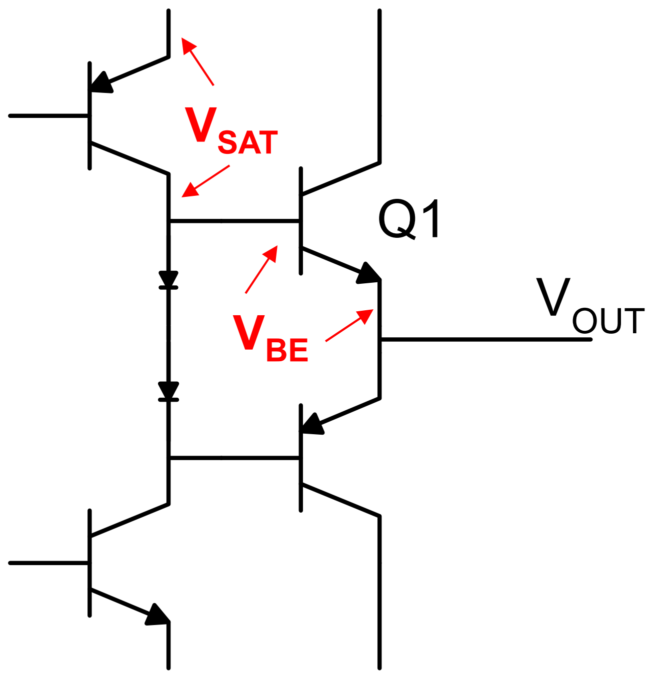
Section 4

OUTPUT STAGE CONSIDERATIONS

Real world outputs



Classic output stage

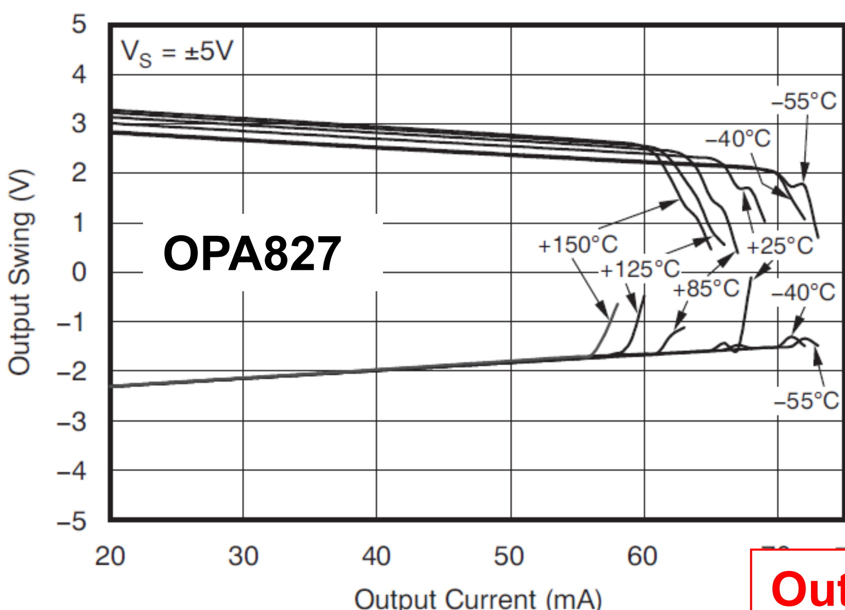


- Common-emitter output
- Current source driver
- Headroom set by VBE+VCESAT
- Unity Gain

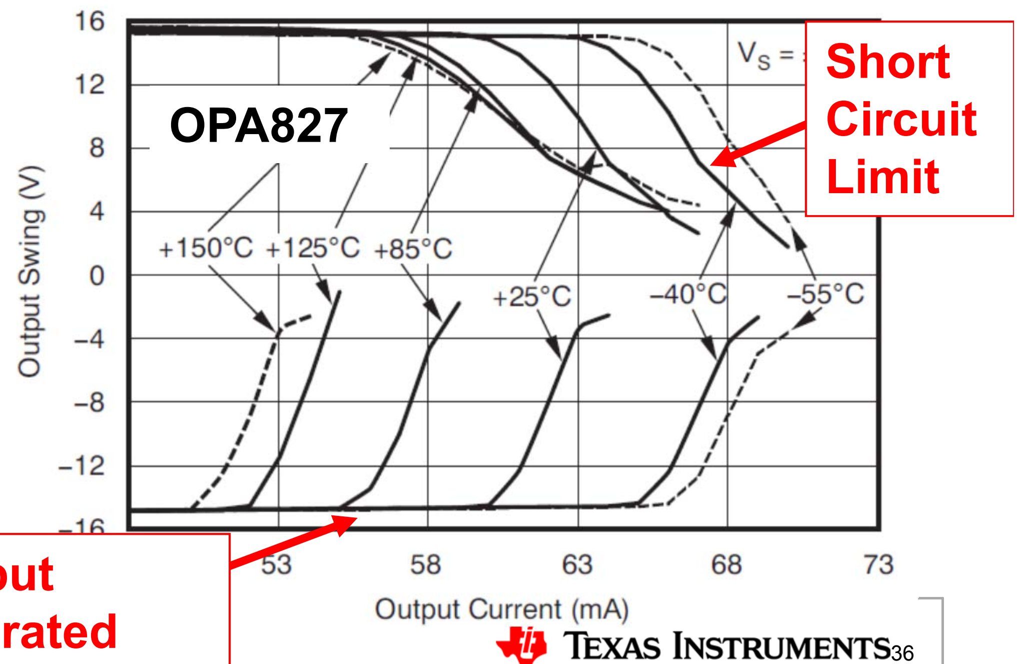
OPA827 – classic output

PARAMETER		CONDITIONS	STANDARD GRADE OPA827AI			UNIT
			MIN	TYP	MAX	
OUTPUT						
Voltage Output Swing		$R_L = 1k\Omega$, $A_{OL} > 120dB$	(V–)+3		(V+)–3	V
Over Temperature		$\mathbf{R_L = 1k\Omega}$, $\mathbf{A_{OL} > 114dB}$	**(V–)+3**		**(V+)–3**	**V**
Output Current	I_{OUT}	$\lvert V_S - V_{OUT} \rvert < 3V$		30		mA
Short-Circuit Current	I_{SC}			±65		mA

OUTPUT VOLTAGE SWING vs OUTPUT CURRENT



OUTPUT VOLTAGE SWING vs OUTPUT CURRENT



OPA827 – classic output

PARAMETER		CONDITIONS	STANDARD GRADE OPA827AI MIN	TYP	MAX	UNIT
OUTPUT						
Voltage Output Swing		$R_L = 1k\Omega$, $A_{OL} > 120dB$	(V–)+3		(V+)–3	V
Over Temperature		$R_L = 1k\Omega$, $A_{OL} > 114dB$	**(V–)+3**		**(V+)–3**	**V**
Output Current	I_{OUT}	$\lvert V_S - V_{OUT} \rvert < 3V$		30		mA
Short-Circuit Current	I_{SC}			±65		mA

The Table Output Swing is defined at:

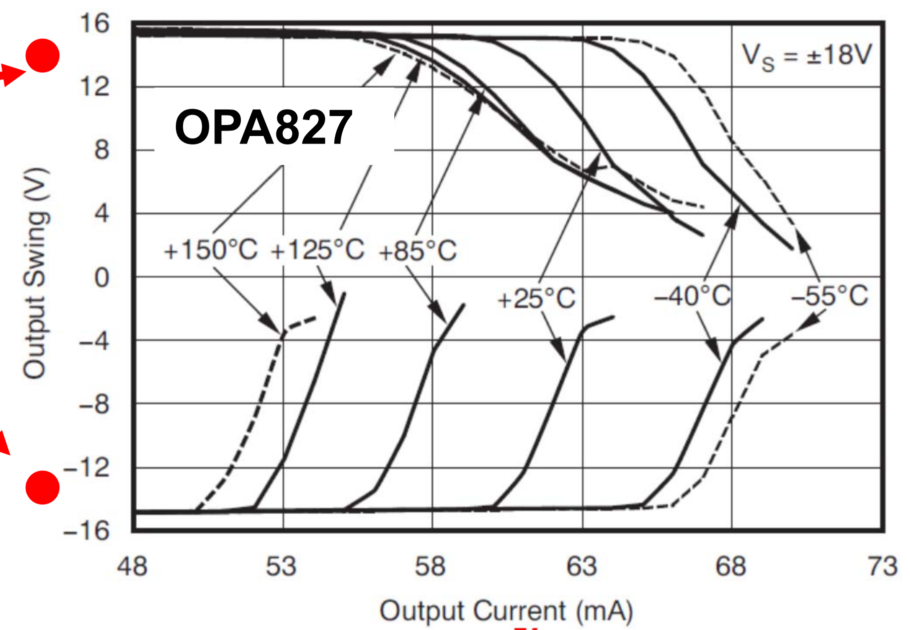
Vout swing = 18V – 3V = ±15V

Iout = 15V/1k = 15mA

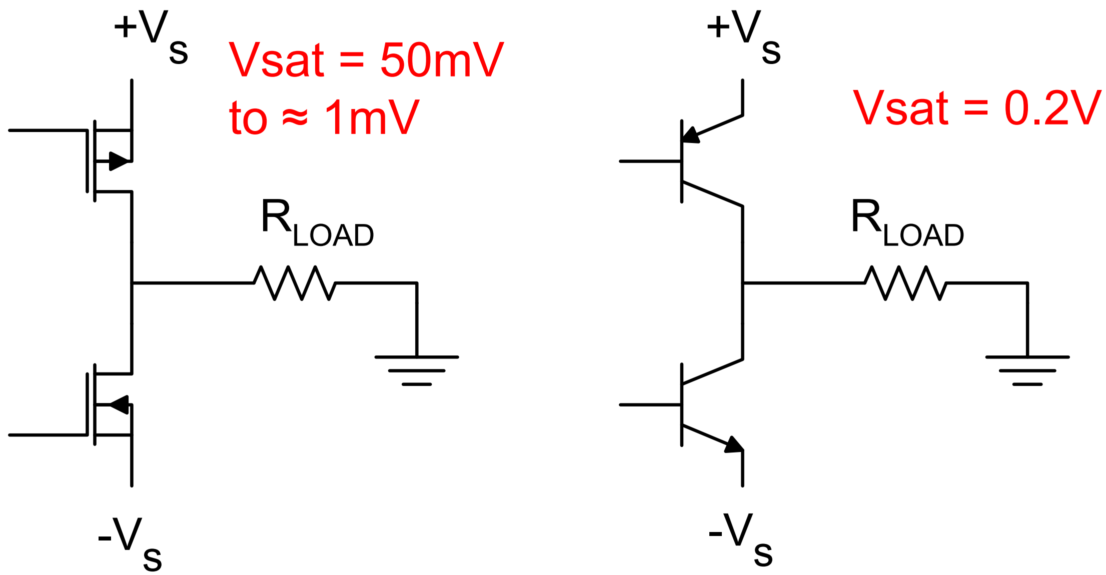
For Aol > 120dB

As you approach the limit or increase I_{LOAD}, Aol will decrease.

OUTPUT VOLTAGE SWING vs OUTPUT CURRENT

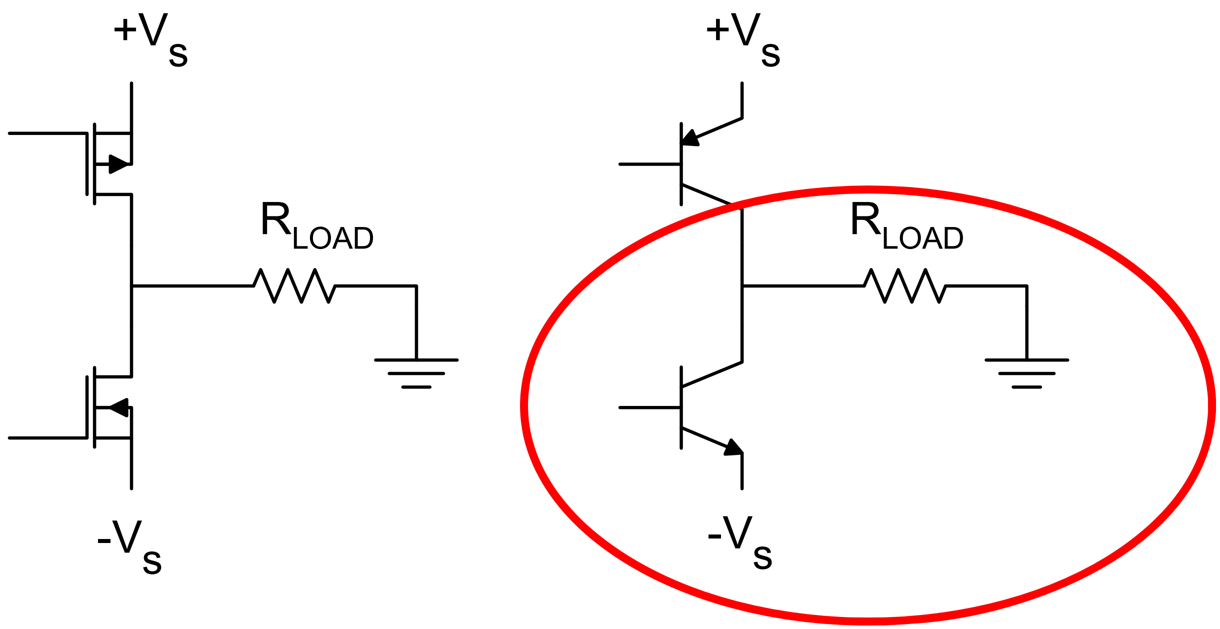


Rail-to-rail output stage



- Common Collector or Common Drain
- Headroom set by V_{DSsat} or V_{CEsat}
- On bipolar sat is approximately 0.2V
  - After sat Beta drops dramatically
- On FET sat is limited by output transistor scaling
  - Can achieve very low sat values (e.g. mV)

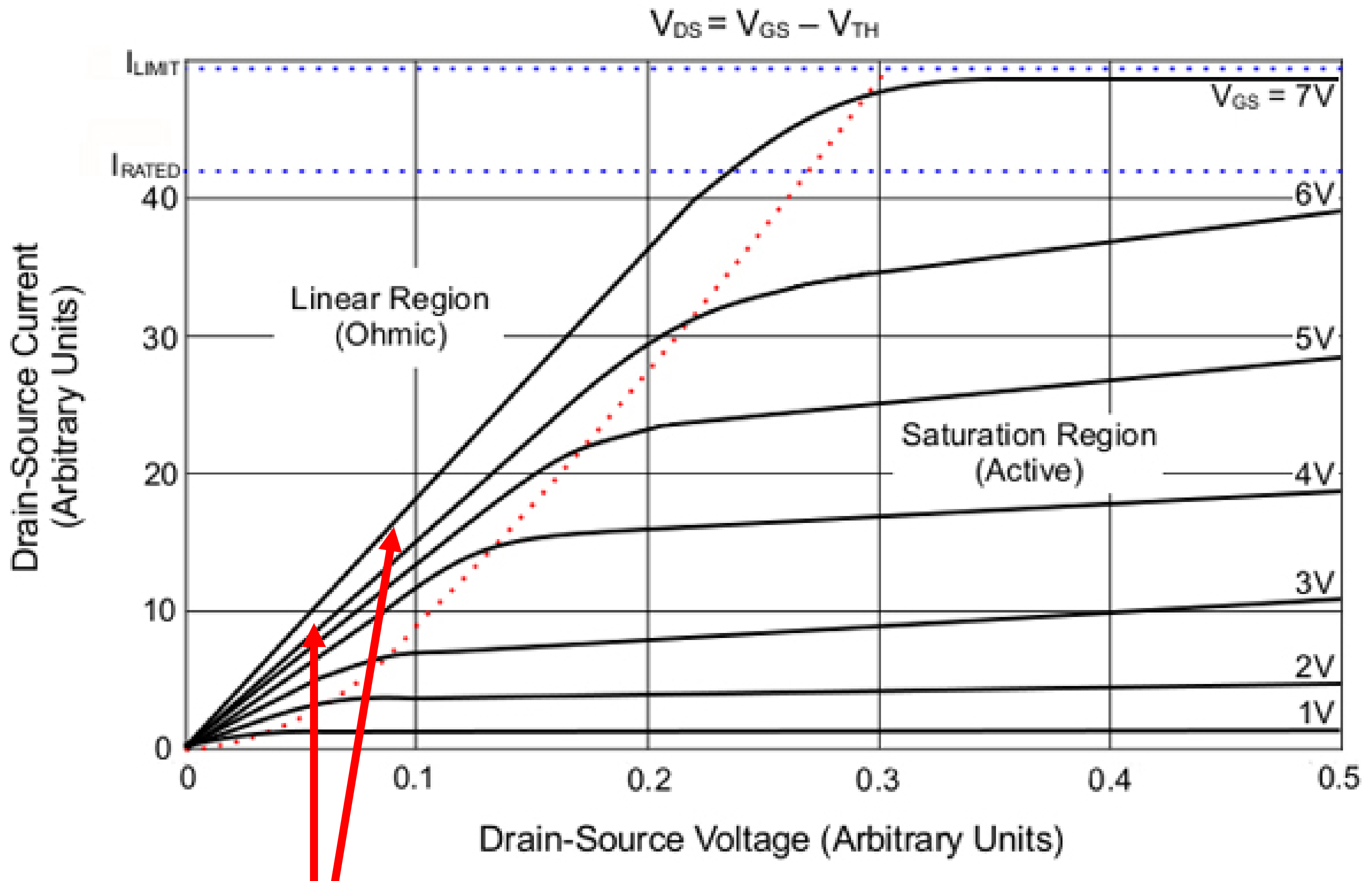
Rail-to-rail output stage



- Value of R_{LOAD} affects A_{OL} and Output Swing
  - the gain in the last stage is set by r_{out} / gm
  - r_{out} decreases with loading

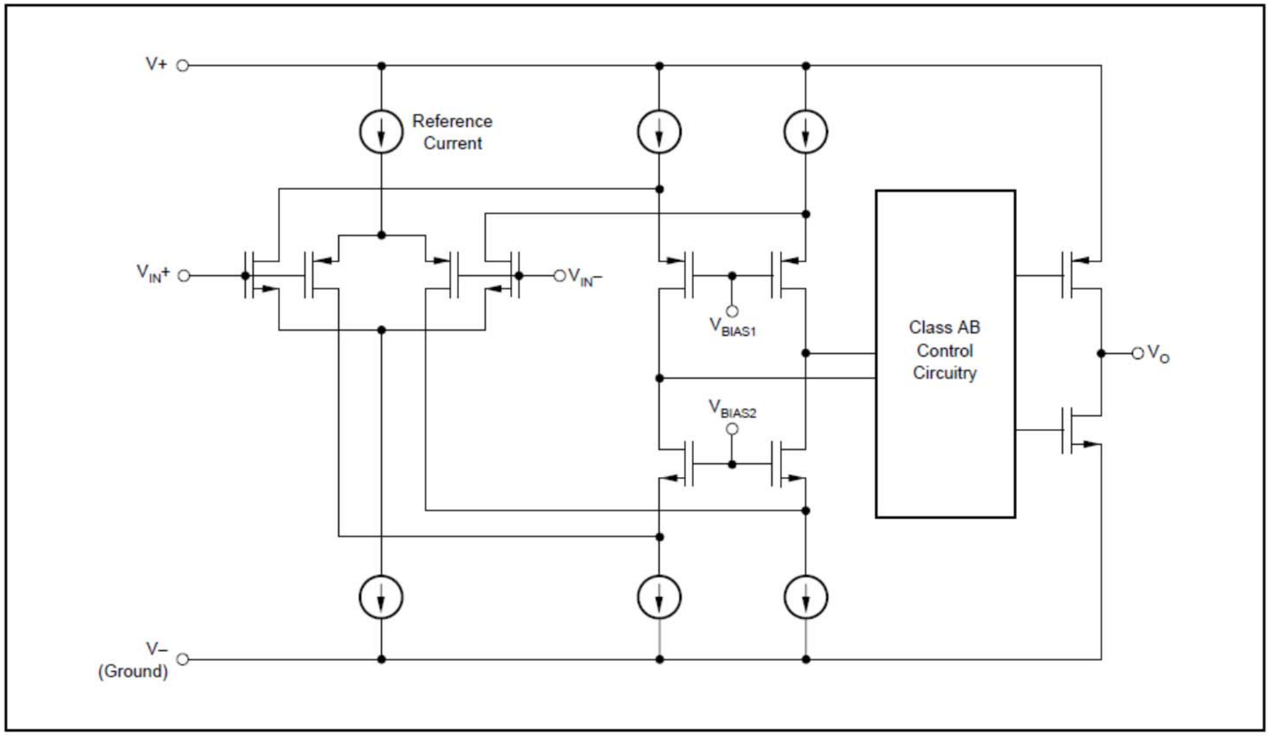
Why can't we get rail-to-rail on CMOS?

MOSFET characteristic curves



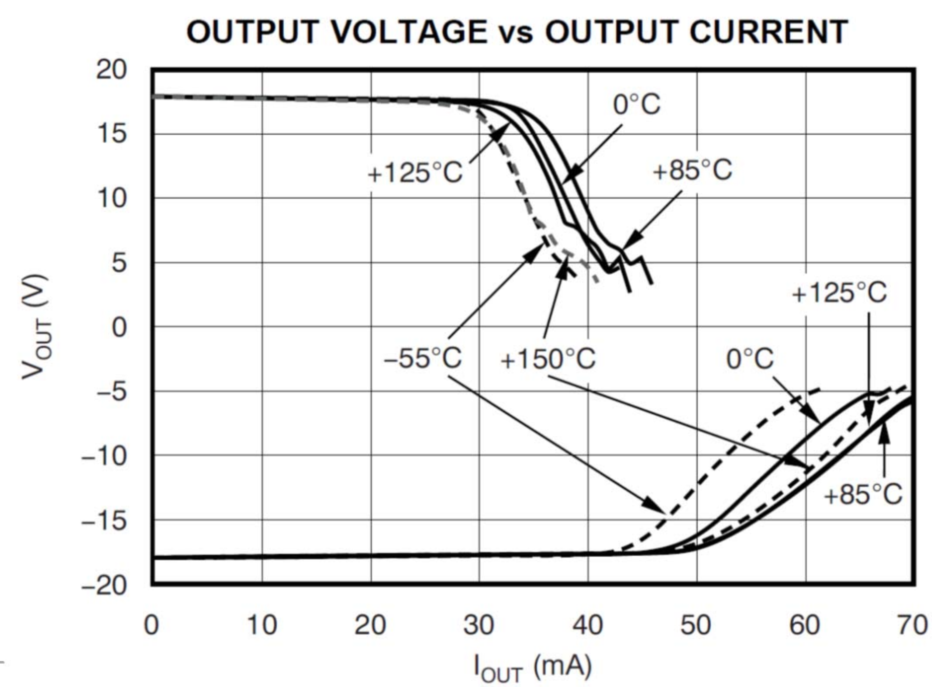
- Some minimum drain to source voltage is required.
- Increasing current requires more Vgs.

Typical rail-to-rail input/output topology



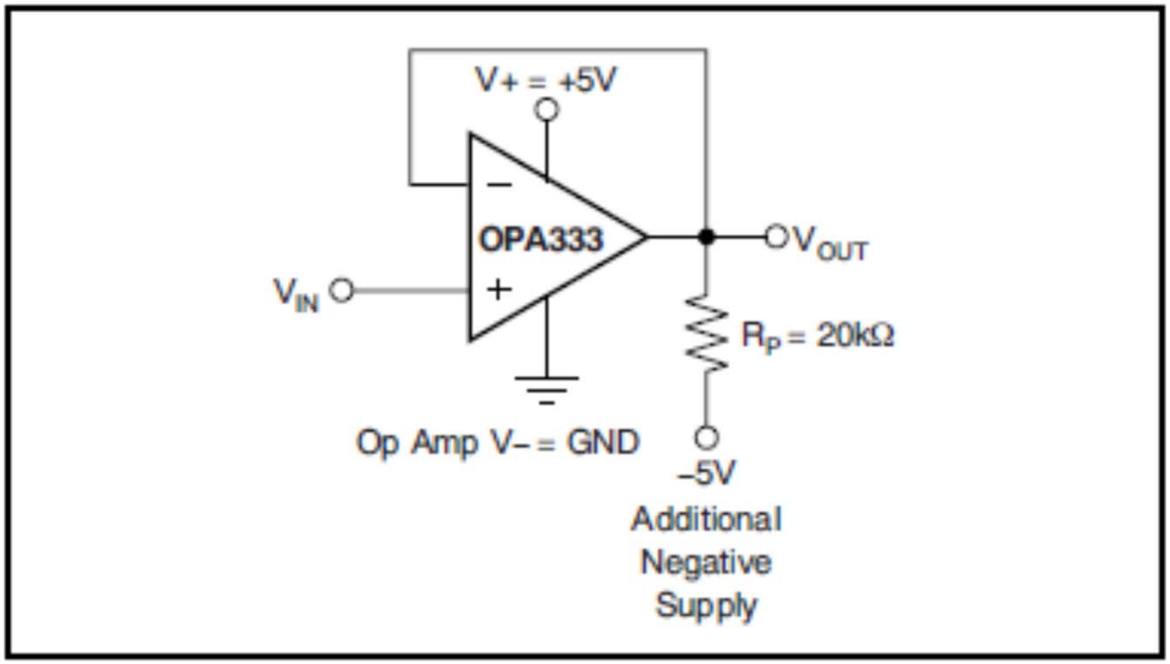
OPA211 – rail-to-rail out (bipolar)

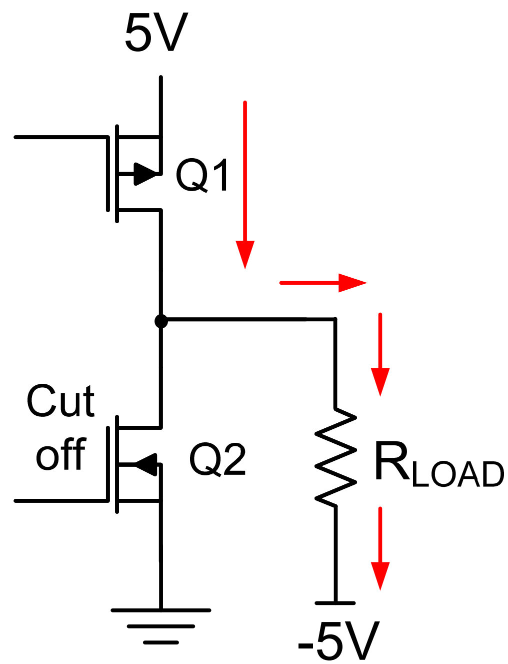
PARAMETER		CONDITIONS	Standard Grade OPA211AI, OPA2211AI			UNIT
			MIN	TYP	MAX	
OUTPUT						
Voltage Output	V_{OUT}	**R_L = 10kΩ, A_{OL} ≥ 114dB**	**(V–) + 0.2**		**(V+) – 0.2**	**V**
		R_L = 600Ω, A_{OL} ≥ 110dB	(V–) + 0.6		(V+) – 0.6	V
		I_O < 15mA, A_{OL} ≥ 110dB	**(V–) + 0.6**		**(V+) – 0.6**	**V**
Short-Circuit Current	I_{SC}			+30/–45		mA
Capacitive Load Drive	C_{LOAD}		See Typical Characteristics			pF



Loading limits output swing and reduces Aol.

Achieving output swing to the negative rail



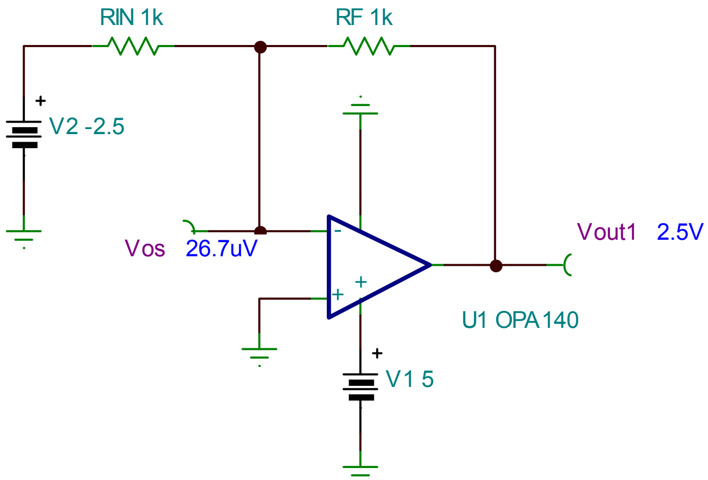


SS pull-down cheat sheet

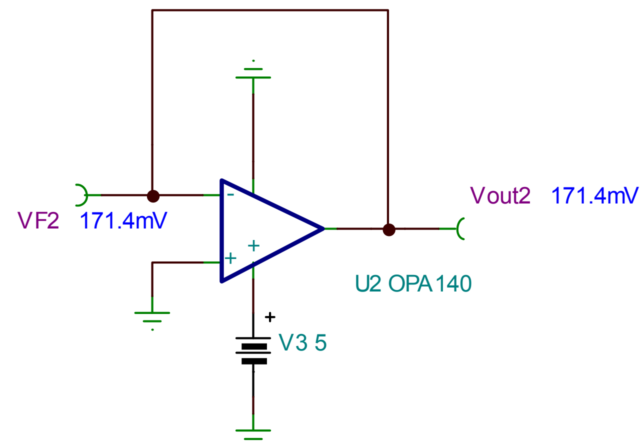
Part #	Resistor Value for -5V Supply
OPA335	40 kΩ
OPA340	7.5 kΩ
OPA343	7.5 kΩ
OPA348	250 kΩ
OPA350	2 kΩ
OPA353	2 kΩ
OPA333	20 kΩ

Selected to sink quiescent current in output stage. Approximately ½ Iq.

Common questions: Op amp output range consideration

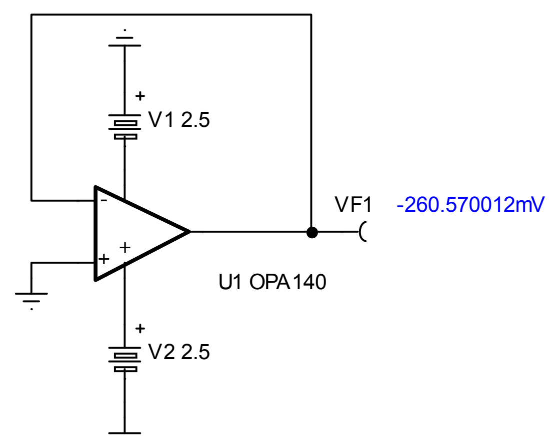


A Valid Op Amp Configuration
(Input and Output within the linear range)



An Invalid Op Amp Configuration
(Output outside of the linear range)

PARAMETER		CONDITIONS	OPA140, OPA2140, OPA4140 MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
Offset Voltage, RTI	V_{OS}	$V_S = \pm18V$		30	120	µV
INPUT VOLTAGE RANGE						
Common-Mode Voltage Range	V_{CM}		(V−) −0.1		(V+)−3.5	V
OUTPUT						
Voltage Output	V_O	$R_L = 10k\Omega$, $A_{OL} \geq 108dB$	(V−)+0.2		(V+)−0.2	V



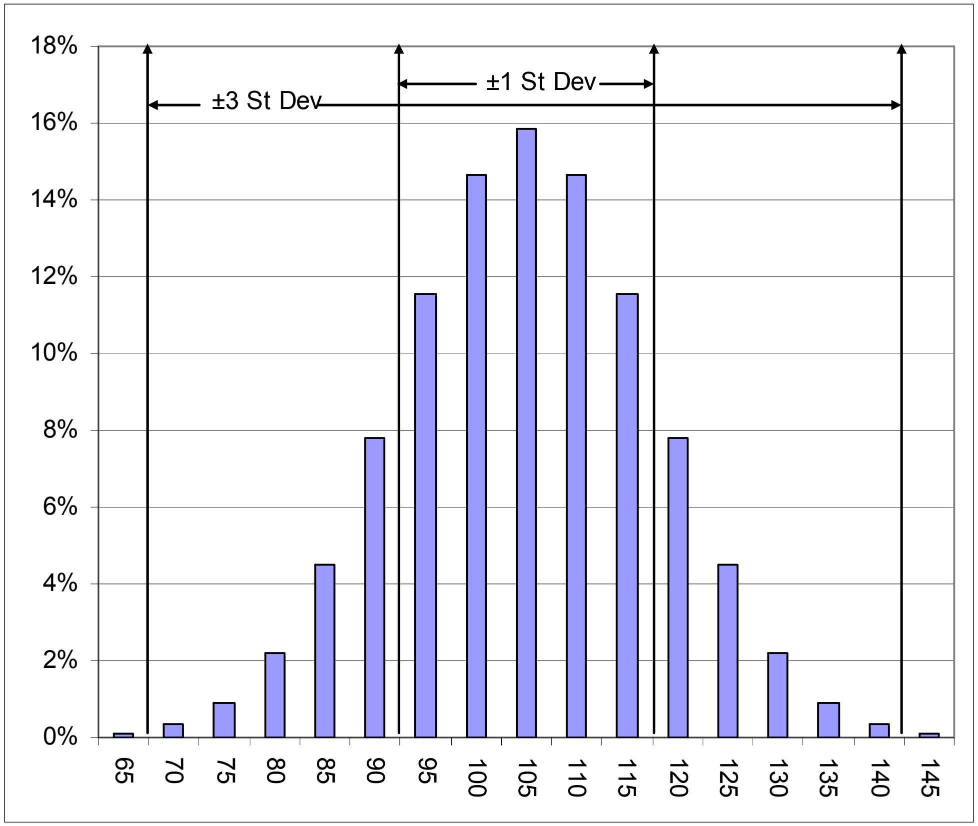
What causes the problem here?

Section 5

LONG-TERM STABILITY

Gaussian (or normal) distribution

n	$\operatorname{erf}\left(\frac{n}{\sqrt{2}}\right)$	i.e. 1 minus ...	or 1 in ...
1	0.682 689 492 137	0.317 310 507 863	3.151 487 187 53
2	0.954 499 736 104	0.045 500 263 896	21.977 894 5080
3	0.997 300 203 937	0.002 699 796 063	370.398 347 345
4	0.999 936 657 516	0.000 063 342 484	15,787.192 7673
5	0.999 999 426 697	0.000 000 573 303	1,744,277.893 62
6	0.999 999 998 027	0.000 000 001 973	506,797,345.897

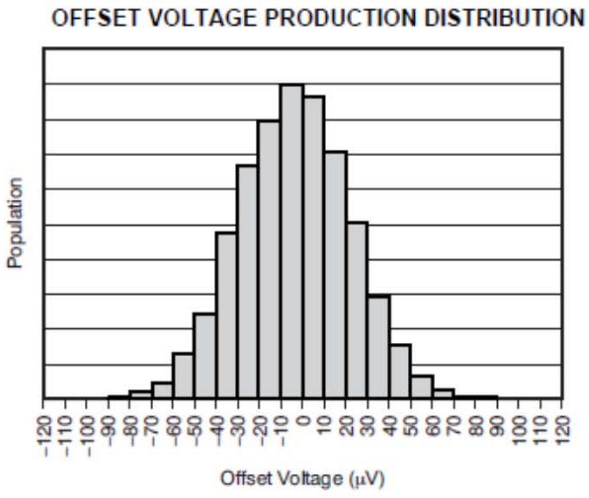


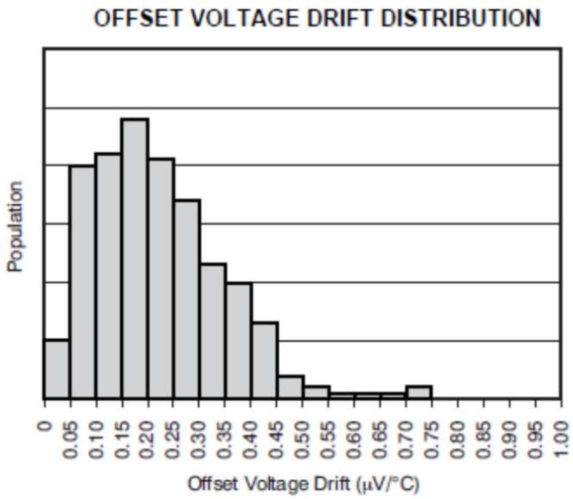
- 68% within ±1 standard deviation
- 99.7% within ±3 standard deviations

Understanding statistical distributions

Specs centered around a mean value

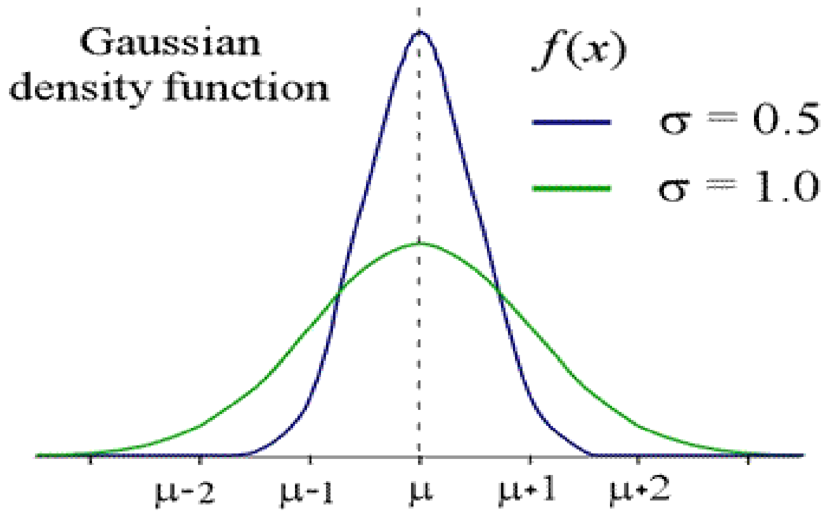
PARAMETER		CONDITIONS	OPA140, OPA2140, OPA4140			UNIT
			MIN	TYP	MAX	
OFFSET VOLTAGE						
Offset Voltage, RTI	V_{OS}	$V_S = \pm 18V$		30	120	μV
Over Temperature		**$V_S = \pm 18V$**			**220**	**μV**
Drift	**dV_{OS}/dT**	**$V_S = \pm 18V$**		**±0.35**	**1.0**	**μV/°C**





Long-term (10 year) shift for Gaussian distributions

Centered around a mean value

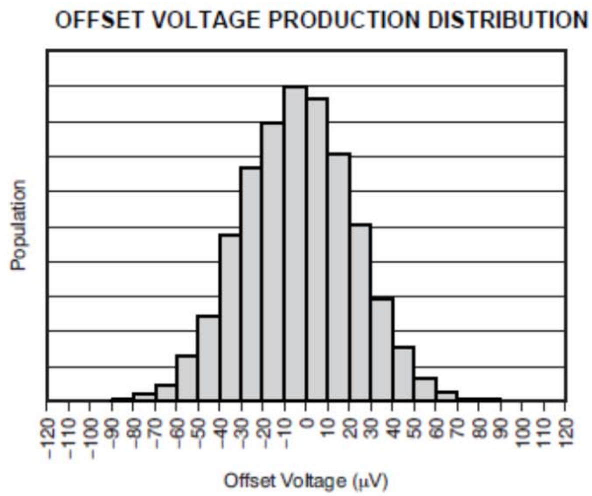


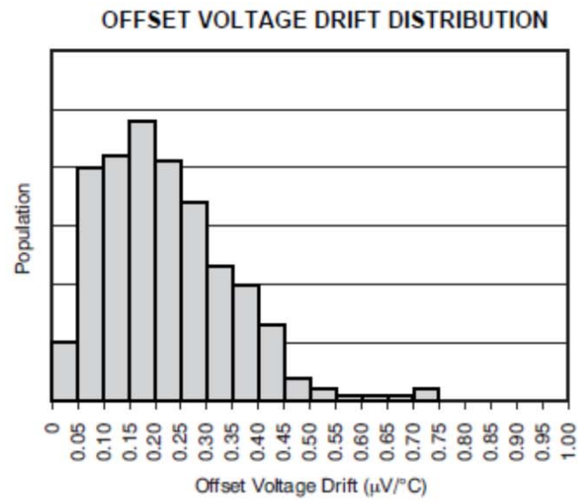
$$f(x) = \sqrt{\frac{1}{4\pi\sigma^2}}\, e^{-(x-\mu)^2/2\sigma^2}$$

Initial PDS Distribution (blue) vs Long-Term Parametric Shift (green)

For 10 year life of a product

Lifetime Vos and Vos temp drift shift





Max LT Vos = 240uV

Max LT Vos drift = 2.0uV/C

Lifetime max shift (10 year) = Max initial value

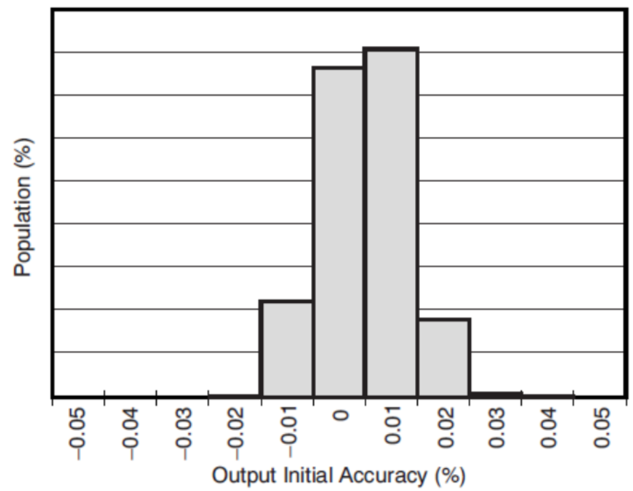
Long-term max spec = 2 * initial spec

Lifetime output voltage initial accuracy shift

Specs centered around a fixed value

PARAMETER		CONDITIONS	PER DEVICE MIN	TYP	MAX	UNIT
REF5020 (V_{OUT} = 2.048V)[1]						
OUTPUT VOLTAGE						
Output Voltage	V_{OUT}	2.7V < V_{IN} < 18V		2.048		V
Initial Accuracy: High-Grade			–0.05		0.05	%

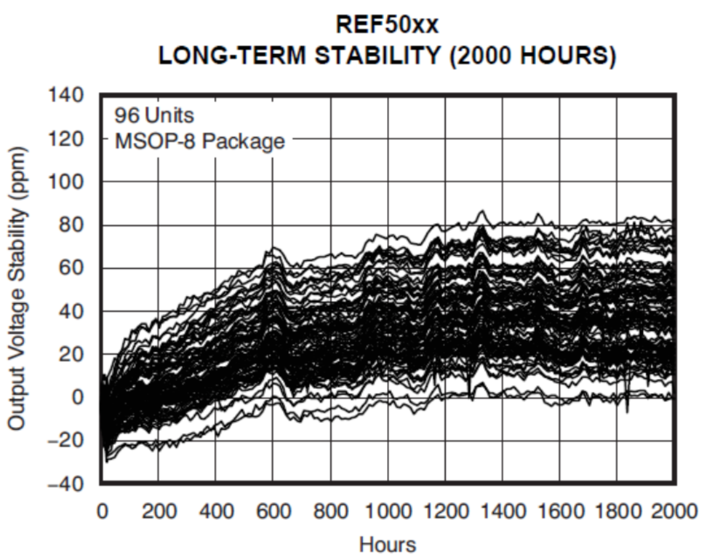
OUTPUT VOLTAGE INITIAL ACCURACY

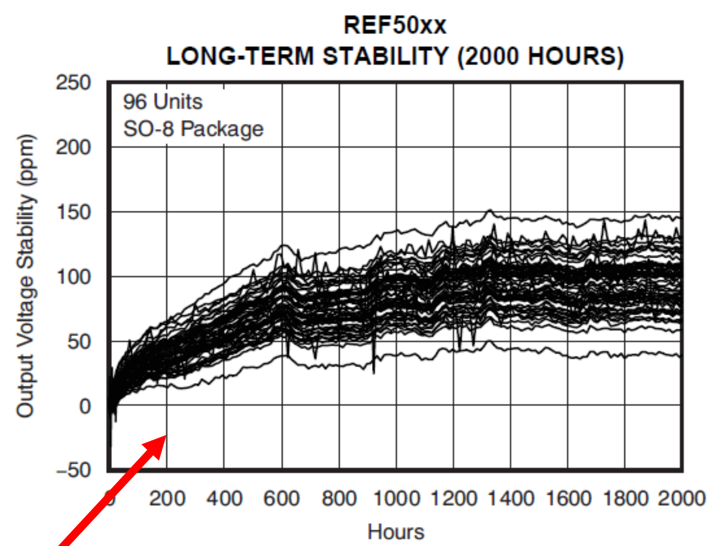


Max LT Vref = +/-0.1%

Long-term Vref shift

PARAMETER	CONDITIONS	REF50xx MIN	REF50xx TYP	REF50xx MAX	UNIT
LONG-TERM STABILITY					
MSOP-8	0 to 1000 hours		50		ppm/1000 hr
MSOP-8	1000 to 2000 hours		5		ppm/1000 hr
SO-8	0 to 1000 hours		90		ppm/1000 hr
SO-8	1000 to 2000 hours		10		ppm/1000 hr

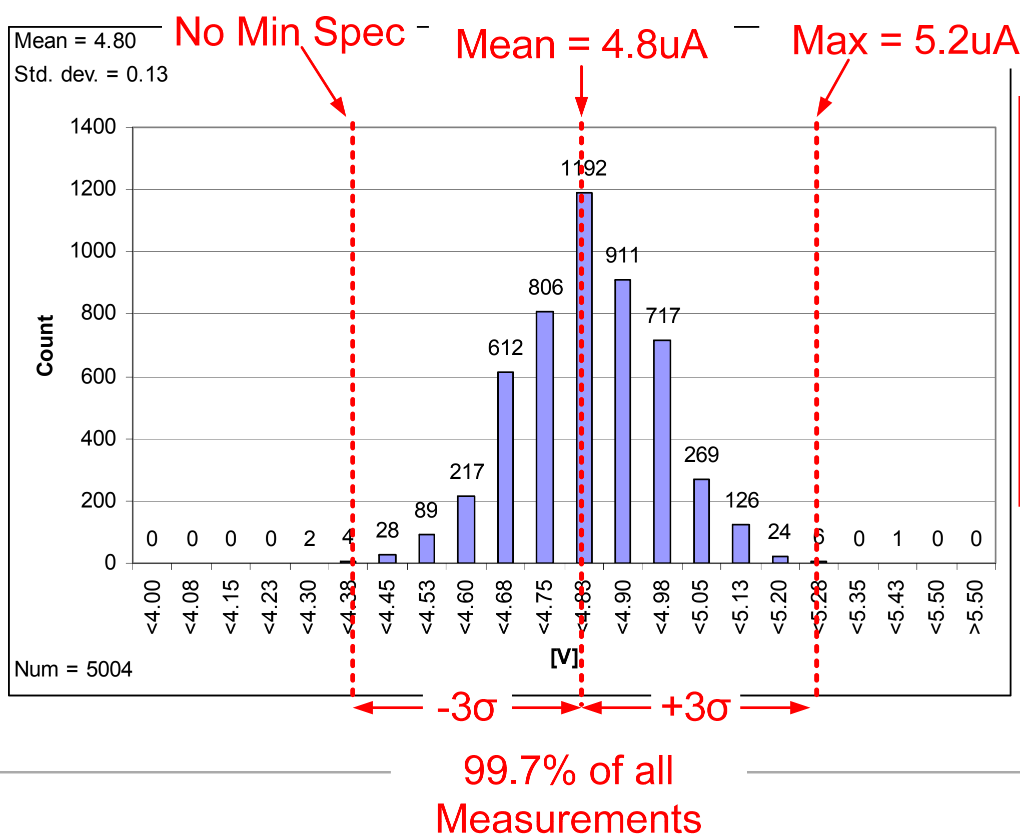




The initial shift (first few months) makes up the majority of change. Self curing of molding compound.

Single-ended limit

PARAMETER		CONDITIONS	STANDARD GRADE OPA827AI MIN	TYP	MAX
POWER SUPPLY					
Specified Voltage	V_S		±4		±18
Quiescent Current (per amplifier)	I_Q	I_{OUT} = 0A		4.8	5.2



A typical MIN and MAX range is at least +/-3σ:

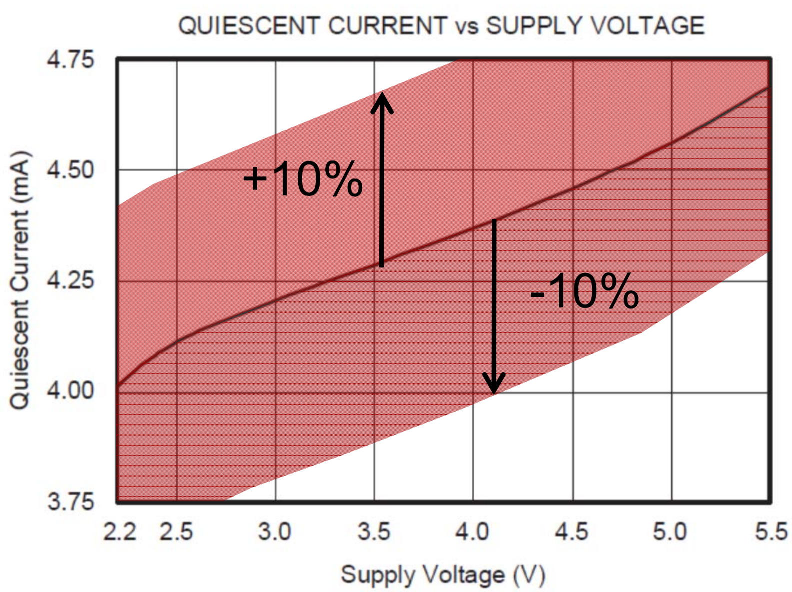
Mean = Typical

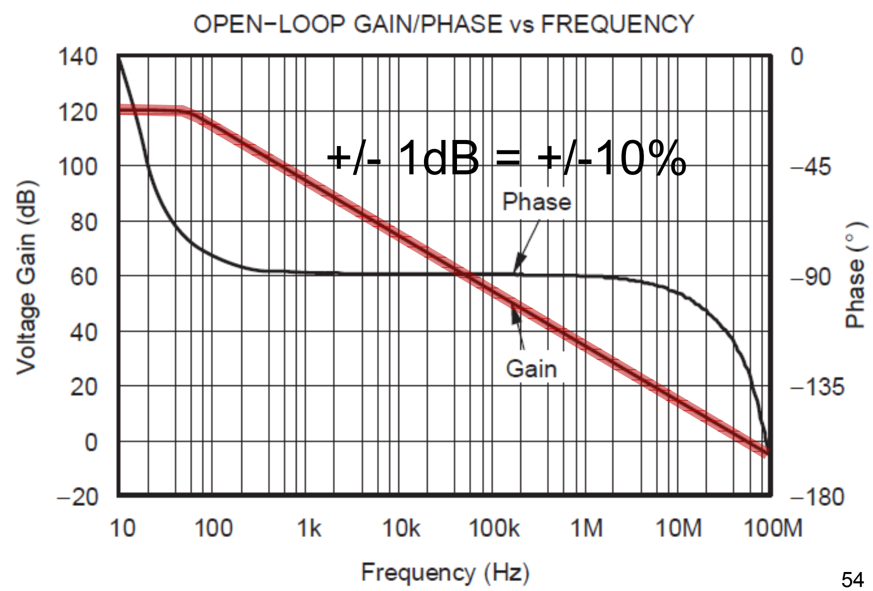
MAX = Mean + 3σ (or greater)

MIN = Mean - 3σ (or greater)

Long-term shift for single-ended specs

PARAMETER		TEST CONDITIONS	OPAx365 MIN	OPAx365 TYP	OPAx365 MAX	UNIT
Quiescent Current Per Amplifier	I_Q	$I_O = 0$		4.6	5	mA
over Temperature					**5**	**mA**
OPEN-LOOP GAIN						
Open-Loop Voltage Gain	**A_{OL}**	**$R_L = 10k\Omega$, $100mV < V_O < (V+) - 100mV$**	**100**	**120**		**dB**
		$R_L = 600\Omega$, $200mV < V_O < (V+) - 200mV$	100	120		dB
		$R_L = 600\Omega$, $200mV < V_O < (V+) - 200mV$	**94**			**dB**



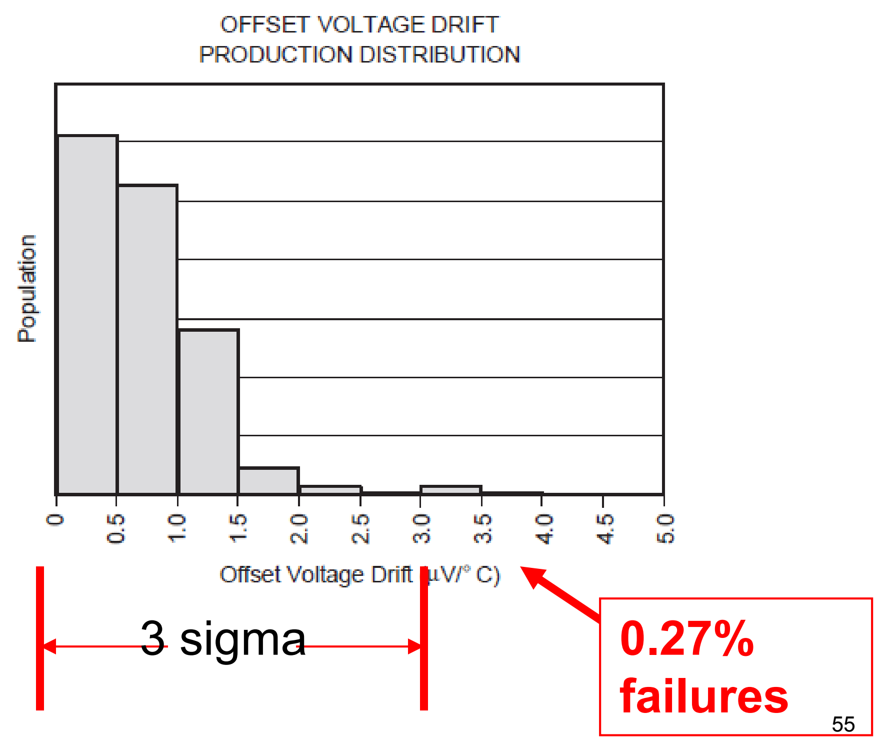


TEXAS INSTRUMENTS

Reading between the lines
Estimating max spec based on a typical value

PARAMETER		TEST CONDITIONS	OPAx365			UNIT
			MIN	TYP	MAX	
OFFSET VOLTAGE						
Input Offset Voltage	V_{OS}			100	200	μV
Drift	dV_{OS}/dT			**1**		**μV/°C**

Numb Standard Deviations	% chance of Pass	Percent Chance of Fail
1	68.2689491	31.73105087
2	95.449973	4.550027049
3	99.7300204	0.269979613
4	99.9936658	0.006334248
5	99.9999427	5.73303E-05
6	99.9999998	1.97318E-07



Lifetime shift rule summary

You may estimate the maximum expected parametric shift over any given period of time by using:

- **100% of the max (min) PDS guaranteed value in the case of specs centered around a mean value** (Vos, Vref, Vos Drift, etc).
- **10% of the max (min) guaranteed value for parameters specified as a fixed positive value** (IQ, AOL, PSRR, CMRR, etc).

and pro-rate them based on the expected ten-year life of the product.

You need to keep in mind that the long-term shift is not exactly a linear function of time - it is steeper (shifts faster) in the first year and slows down in the later years. It also usually excludes the first 30 days due to continuing self-curing of the molding compound used for packaging of IC.

Acknowledgments

Contributed to this presentation:

Art Kay & Todd Toporski

Appendix

APPENDIX

HTOL (high temperature operating life)

- HTOL is used to measure the constant failure rate region in the bottom of the bathtub curve as well as assess the wear-out phase of the curve for some use conditions.
- Smaller sample sizes than EFR but are run for a much longer duration
- Jedec and QSS default are Ta=125C for 1000 hours
- Q100 is 1000 hours at max temperature for the device's grade
- Most modern IC's undergo HTOL at Ta=150C for 300 hours
- But how much is this simulating in the field?

The Arrhenius equation

$$\text{Process rate} = Ae^{-(Ea/kT)}$$

A = A constant

Ea = Thermal activation energy in electron volts (eV)

k = Boltzman’s constant, 8.62×10^{-5} eV/K

T = Absolute temperature in degrees Kelvin (degrees C + 273.15)

Acceleration factors

Acceleration factors are the ratio of the process rate at two temperatures.

$$AF(T1 \text{ to } T2) = e^{(Ea/k)(1/T2\ -\ 1/T1)}$$

A = A constant (has canceled out of the formula)

Ea = Thermal activation energy in electron volts (eV)

k = Boltzman's constant, 8.62×10^{-5} eV/K

T = Absolute temperature in degrees Kelvin (degrees C + 273.15)

Acceleration factors examples

Calculate the thermal acceleration factor (AF) between the stress test temperature and the product use temperature:

T (life-test stress) =150C->423K

T (application) =65C->338K

Ea=0.7eV

$$AF(150 \text{ to } 65) = e^{(0.7eV/k)(1/328\ -\ 1/398)} = 125$$

This means every hour of stress at 150C is equivalent to 125 hours of use in the application at 65C.

Thus, for example, 300 hour life-test at 150C would cause similar shift as 37,500 hours (125*300hrs), or about 4 years, in the field at 65C.

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